

M5230L,FP

VARIABLE OUTPUT VOLTAGE REGULATOR (DUAL TRACKING TYPE)

DESCRIPTION

The M5230 is a semiconductor integrated circuit which is designed for variable output voltage regulator of dual tracking type.

It is housed in an 8-pin SIP and SOP. The output voltage can be adjusted over a wide range from $\pm 3 \sim \pm 30V$ by adjusting the value of the voltage setting external resistors. By adjusting the resistance of the external balance setting resistors the positive/negative output voltage ratio can also be set freely. Again by attaching power transistors high current gains can be achieved, making the device suitable for use in the power supplies of a wide variety of equipment.

FEATURES

- High input voltage $V_i = \pm 35V$
- Wide range of output voltage $V_o = \pm 3 \sim \pm 30V$
- Low output noise voltage $V_{NO} = 12 \mu V_{rms}(typ.)$
- Built-in current limiting and thermal shutdown circuit
- The output voltage rise time constant of the coefficients can be adjusted by the value of the external capacitor.
- Capability of operation control by the external control signal (Pin ⑧).

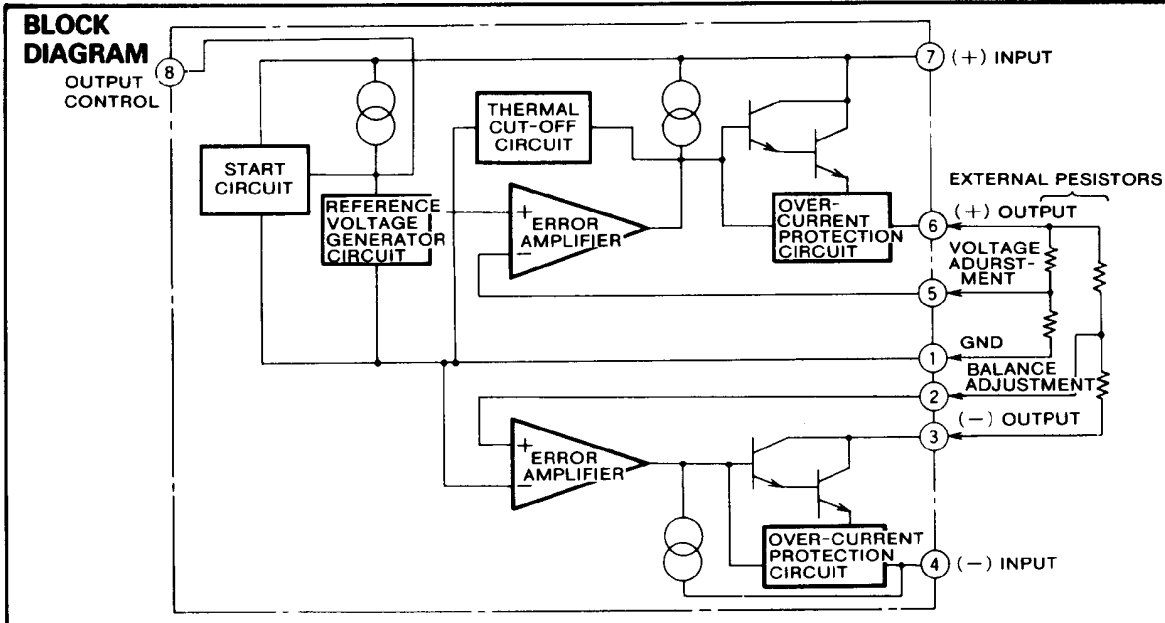
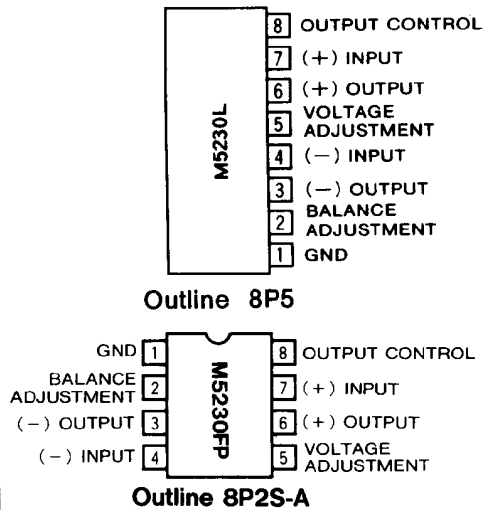
APPLICATION

Dual voltage power supplies for stereo preamplifiers, for the power supplies of other equipment, including operational amplifiers.

RECOMMENDED OPERATING CONDITIONS

- Supply voltage range $\pm 8 \sim \pm 35V$
- Rated supply voltage $\pm 20V$

PIN CONFIGURATION (TOP VIEW)



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ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

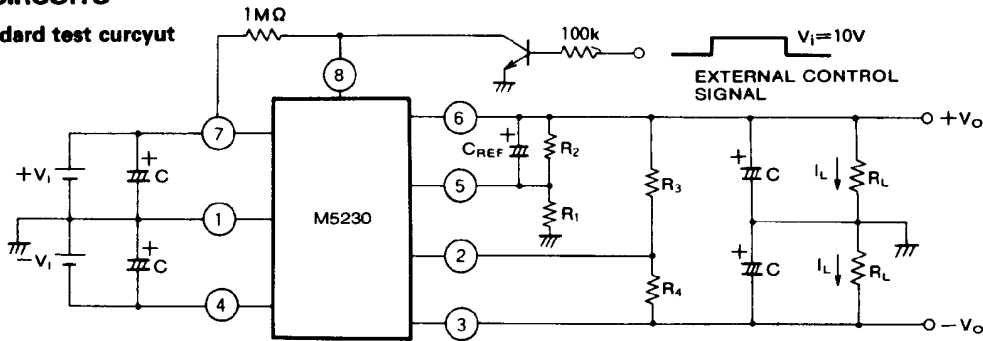
Symbol	Parameter	Ratings	Unit
V_i	Input voltage	± 35	V
I_L	Load current	± 30	mA
$V_i - V_o$	Input-output voltage difference	± 32	V
P_d	Power dissipation	800(L)/440(FP)	mW
T_{opr}	Ambient temperature	$-20 \sim +75$	$^\circ\text{C}$
T_{stg}	Storage temperature	$-55 \sim +125$	$^\circ\text{C}$

ELECTICAL CHARACTERISTICS (measurement circuit (a) is used with, $T_a=25^\circ\text{C}$, $V_i=\pm 20\text{V}$, $V_o=\pm 15\text{V}$, $I_L=10\text{mA}$, $C=10\mu\text{F}$, $C_{REF}=1\mu\text{F}$, $R_1=3.3\text{k}\Omega$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_i	Input voltage		± 8		± 35	V
V_o	Output voltage	$R_2 \approx 1.5 \sim 55\text{k}\Omega$	± 3		± 30	V
V_{REF}	Reference voltage	(between pin ⑤ and pin ①)	1.66	1.8	1.95	V
$V_i - V_o$	Minimum input-output voltage difference			2.5	3	V
$\Delta V_o \pm$	Dual voltage tracking				1	%
Reg_{in}	Input regulation	$V_i = \pm 18 \sim \pm 30\text{V}$		0.02	0.1	%/V
Reg_L	Load regulation	$I_L = 0 \sim 20\text{mA}$		0.02	0.1	%
I_B	Bias current	$I_L = 0$ (disregarding the current in resistors R_1, R_2, R_3, R_4)		1.3	3.0	mA
TC_{V_o}	Temperature coefficient of output voltage	$T_a = 0 \sim 75^\circ\text{C}$, $V_o = \pm 3 \sim \pm 30\text{V}$		0.01		%/C
RR	Ripple rejection	$f = 120\text{Hz}$ (measured with circuit (b))		68		dB
V_{NO}	Output noise voltage	$f = 20\text{Hz} \sim 100\text{kHz}$ (between the output terminal and ground)		12		μVrms
$V_{O(OFF)}$	Output cut-off voltage	$V_i = 10\text{V}$			± 0.1	V

TEST CIRCUITS

(a) Standard test circuit



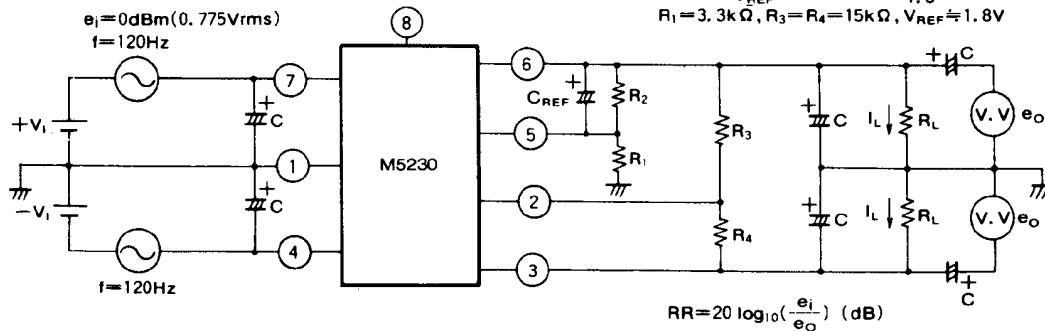
$$+V_o = V_{REF} \left(1 + \frac{R_2}{R_1}\right) \approx 1.8 \times \left(1 + \frac{R_2}{3.3}\right) \text{ (V)}$$

$$-V_o = +V_o \cdot \frac{R_4}{R_3} \text{ (V)}$$

$$R_2 = R_1 \left(\frac{+V_o}{V_{REF}} - 1\right) \approx 3.3 \times \left(\frac{+V_o}{1.8} - 1\right) \text{ (k}\Omega\text{)}$$

$$R_1 = 3.3\text{k}\Omega, R_3 = R_4 = 15\text{k}\Omega, V_{REF} \approx 1.8\text{V}$$

(b) Ripple rejection test circuit

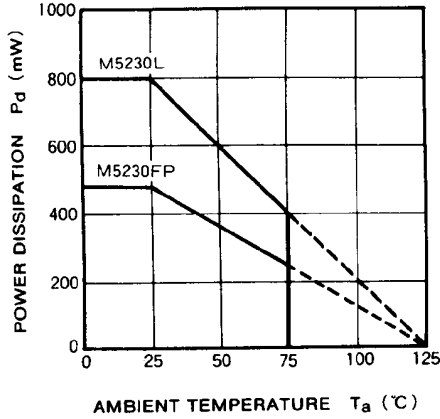


$$RR = 20 \log_{10} \left(\frac{-e_1}{e_o}\right) \text{ (dB)}$$

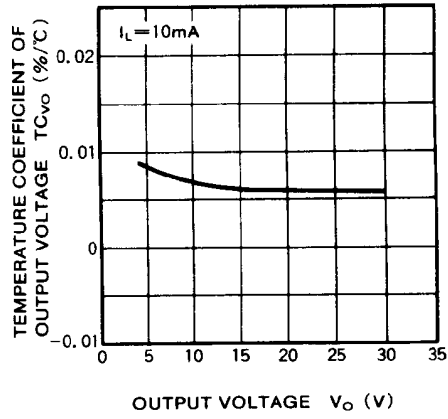
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TYPICAL CHARACTERISTICS

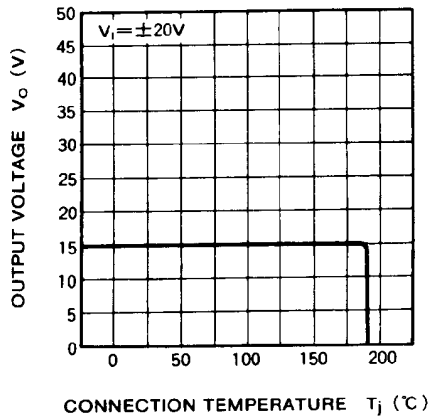
THERMAL DERATING (MAXIMUM RATING)



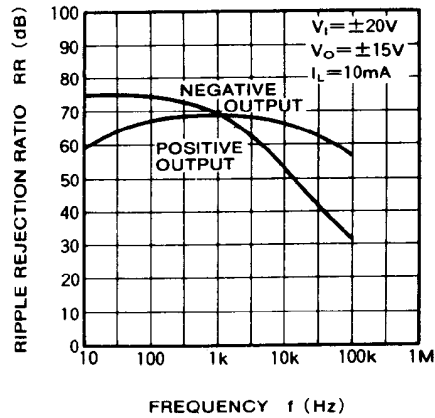
TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE VS. OUTPUT VOLTAGE CHARACTERISTICS



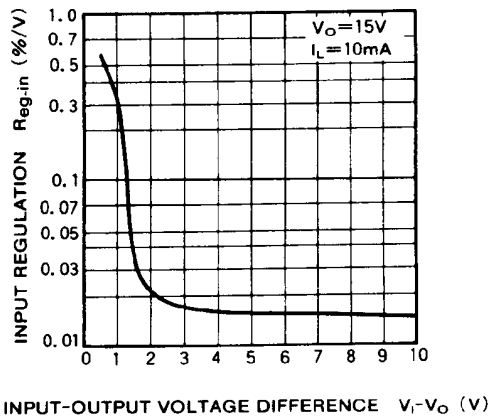
THERMAL CUTOFF



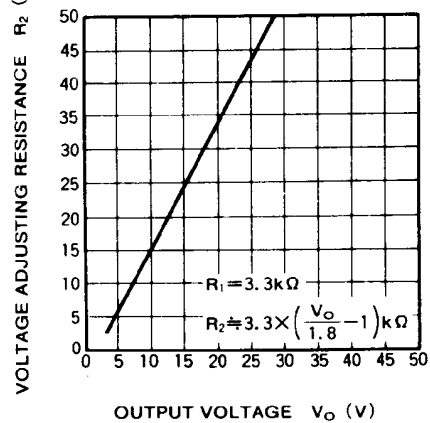
RIPPLE REJECTION



INPUT REGULATION VS. INPUT-OUTPUT VOLTAGE DIFFERENCE



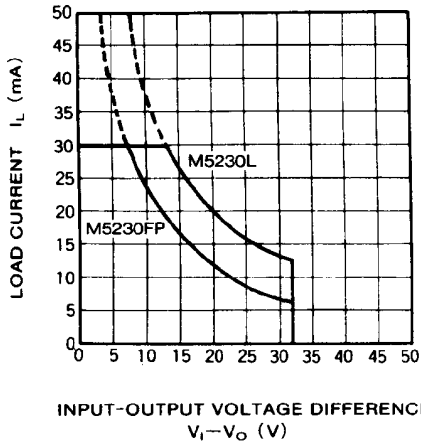
VOLTAGE ADJUSTMENT RESISTANCE VS. OUTPUT VOLTAGE



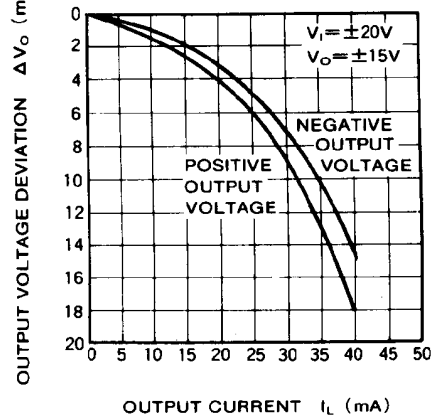
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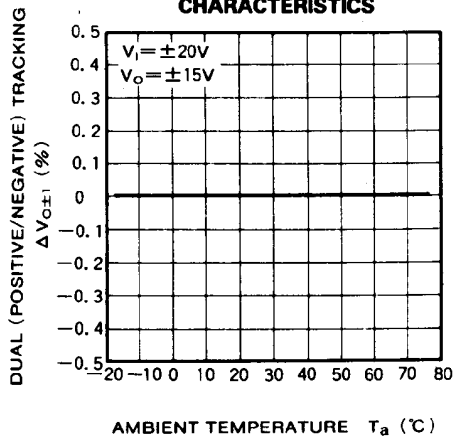
LOAD CURRENT VS. INPUT-OUTPUT VOLTAGE DIFFERENCE



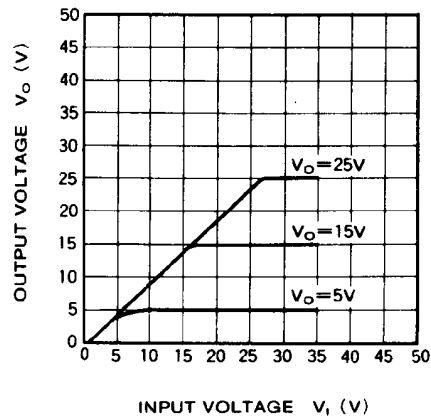
OUTPUT VOLTAGE REGULATION



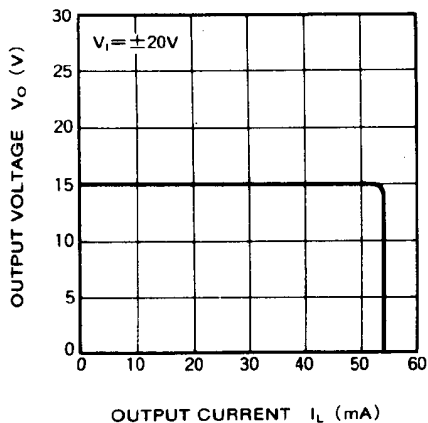
DUAL-TRACKING TEMPERATURE CHARACTERISTICS



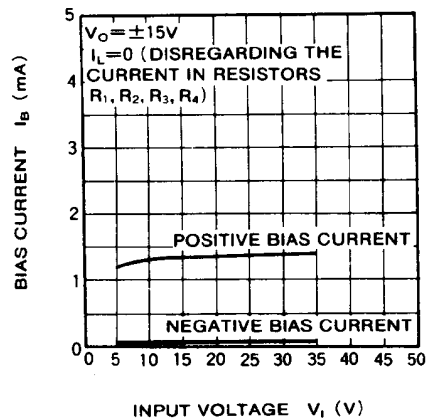
OUTPUT VOLTAGE CHARACTERISTICS



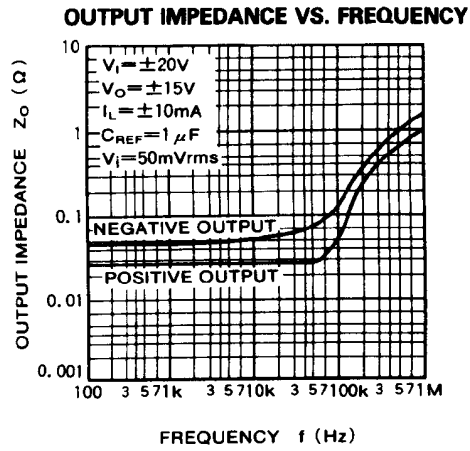
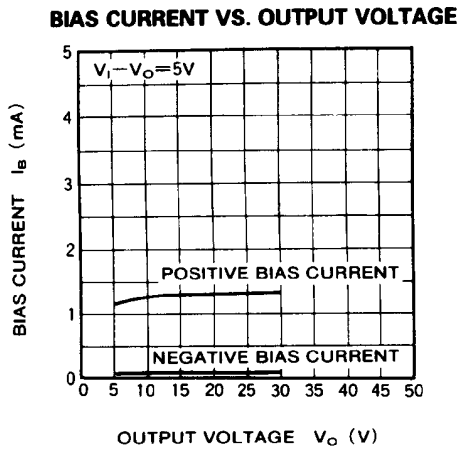
LOAD CHARACTERISTICS



BIAS CURRENT VS. INPUT VOLTAGE

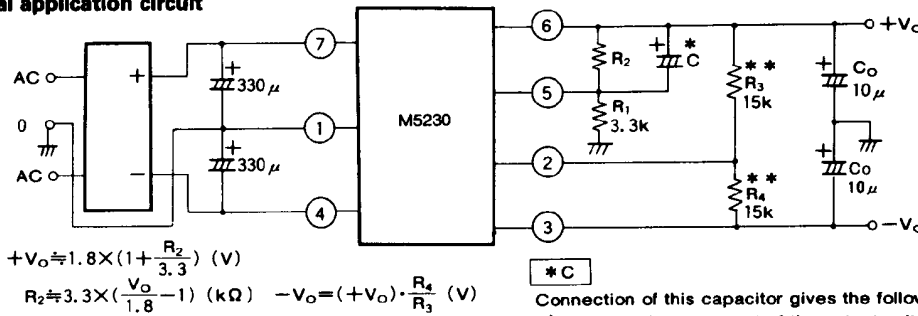


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APPLICATION EXAMPLES

(1) Typical application circuit



Note: When the input power supply lines become long, a 0.1 μF capacitor should be connected between input power supply pins ⑦ and ④ and ground.

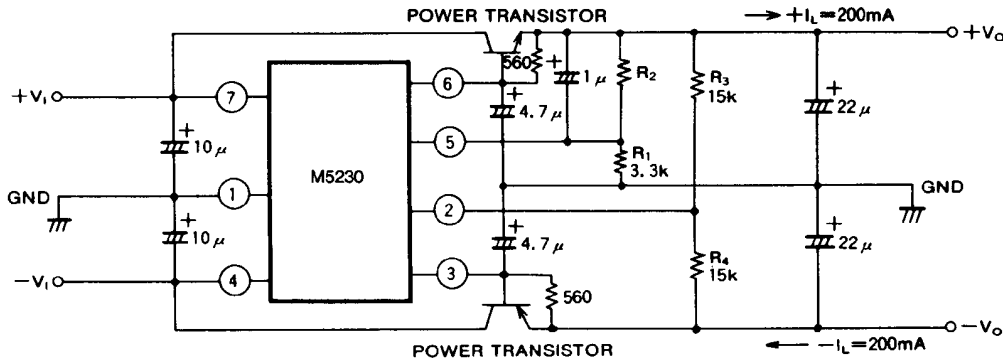
- * C
- Connection of this capacitor gives the following characteristics.
- 1) The rise time constant of the output voltage can be adjusted (slowed) (See Fig. 1)
 - 2) The ripple rejection ratio is improved.
 - 3) Noise output voltage is reduced.

** R_3, R_4

By changing the ratio of these two resistances the positive/negative voltage ratio can also be set freely. (See Fig. 2)

Unit Resistance : Ω
 Capacitance : F

(2) Typical application circuit with power transistors connected

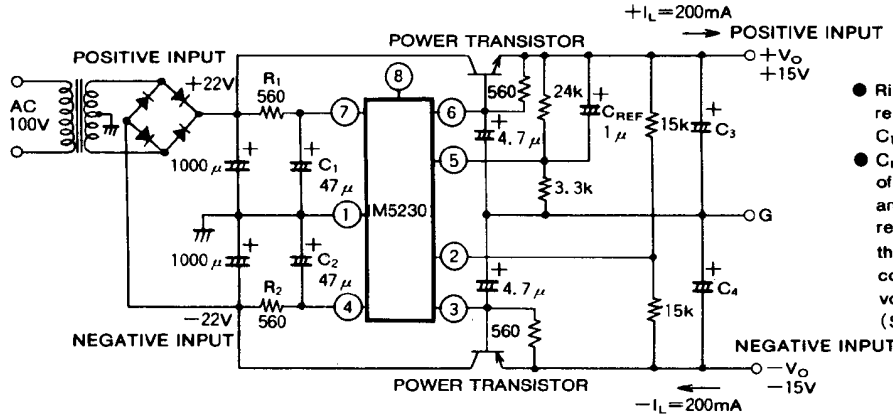


Unit Resistance : Ω
 Capacitance : F

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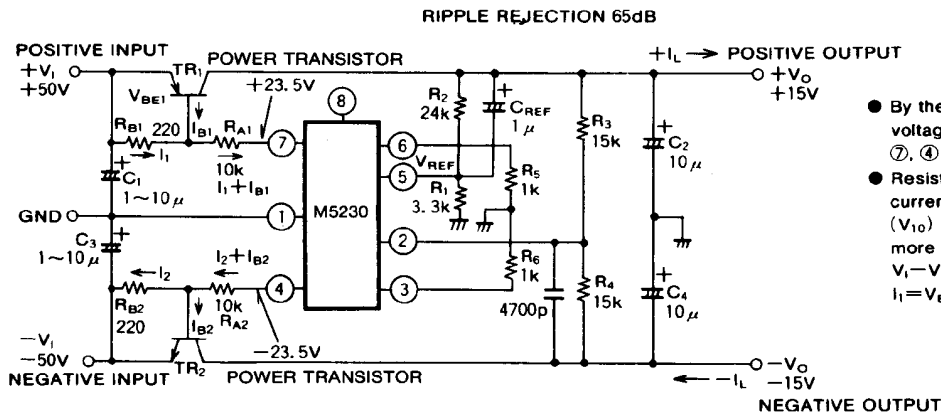
(3) High ripple rejection circuit (80dB)



- Ripple regained by the input resistance R_1 , (R_2), and capacitor C_1 , (C_2).
- C_{REF} can reduce noise to the 1/10 of that of 3 Terminal regulator IC, and also can improve the ripple rejection. In addition, by increasing the capacitance of the C_{REF} , the constant at set-up of the output voltage V_O can be adjusted. (Soft set-up enable).

Unit Resistance : Ω
Capacitance : F

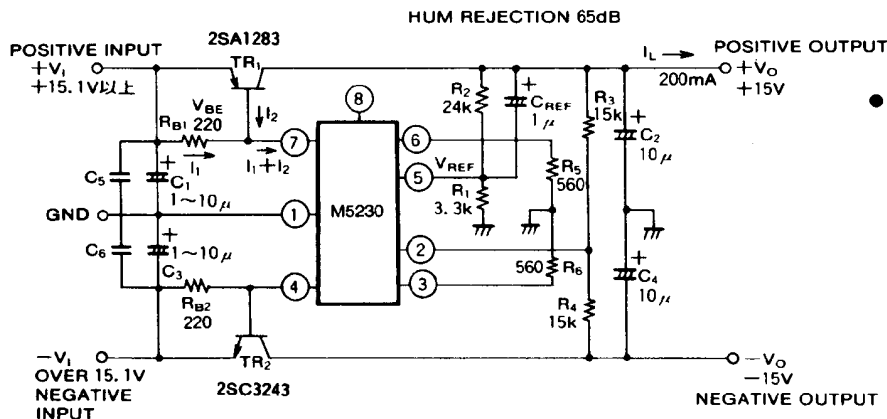
(4) High input voltage ($V_I = \pm 50V$)



- By the resistance R_{A1} , (R_{A2}), the voltage that will be supplied to pins ⑦, ④ can be lower.
- Resistances R_5 and R_6 are for load current limit. Keep the I/O voltage (V_{IO}) difference between ⑦-⑥ more than 6V.
 $V_I - V_{BE} - (I_1 + I_{B1} - I_B)R_5 > 3V$
 $I_1 = V_{BE}/R_{B1}$, $I_{B1} = I_L/h_{FE}$

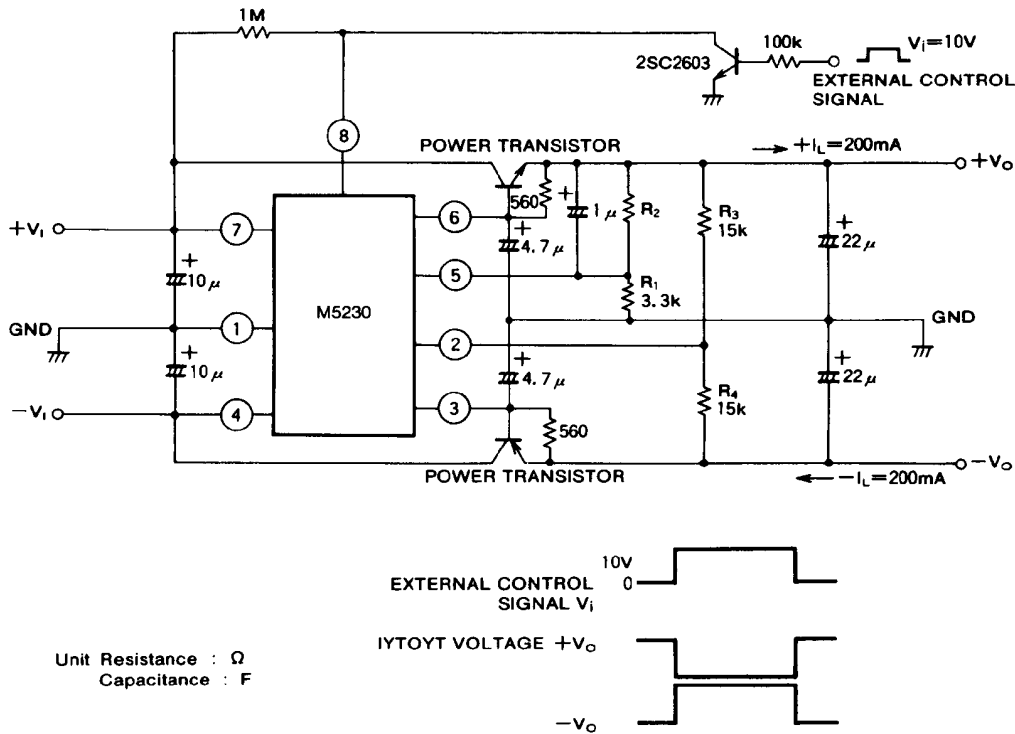
Unit Resistance : Ω
Capacitance : F

(5) Supper low dropout regulator circuit ($V_{IO} = 100mW$)



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(6) ON/OFF control of output voltage circuit



EXAMPLES OF THE CHARACTERISTICS ACHIEVED

Fig. 1 OUPUT VOLTAGE CHARACTERISTICS FOR EXTERNAL CAPACITORS (*C)

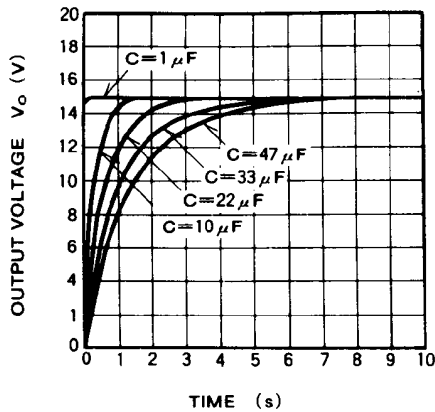


Fig. 2 OUTPUT VOLTAGE RATIO VS. BALNCE VOLTAGE ADJUSTING RESISTANCE CHARACTERISTICS

