

16 ardware Manu Rev.2.41

M16C/62P Group (M16C/62P, M16C/62PT)

Hardware Manual

RENESAS 16-BIT SINGLE-CHIP MICROCOMPUTER M16C FAMILY / M16C/60 SERIES

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How to Use This Manual

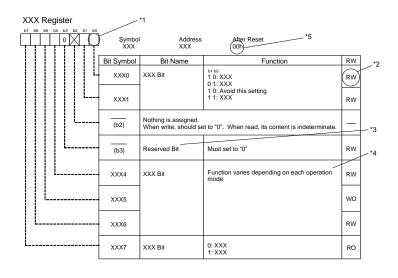
1. Introduction

This hardware manual provides detailed information on the M16C/62P Group (M16C/62P, M16C/62PT) of microcomputers.

Users are expected to have basic knowledge of electric circuits, logical circuits and microcomputers.

2. Register Diagram

The symbols, and descriptions, used for bit function in each register are shown below.



*1

Blank: Set to "0" or "1" according to the application

0: Set to "0"

1: Set to "1"

X: Nothing is assigned

*2

RW: Read and write

RO: Read only

WO: Write only

-: Nothing is assigned

*3

Reserved bit

Reserved bit. Set to specified value.

*4

•Nothing is assigned

Nothing is assigned to the bit concerned. As the bit may be use for future functions,

set to "0" when writing to this bit.

Do not set to this value

The operation is not guaranteed when a value is set.

•Function varies depending on mode of operation

Bit function varies depending on peripheral function mode.

Refer to respective register for each mode.

3. M16C Family Documents

The following documents were prepared for the M16C family. ⁽¹⁾

Document	Contents
Short Sheet	Hardware overview
Data Sheet	Hardware overview and electrical characteristics
Hardware Manual	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, timing charts)
Software Manual	Detailed description of assembly instructions and microcomputer performance of each instruction
Application Note	 Application examples of peripheral functions Sample programs Introduction to the basic functions in the M16C family Programming method with Assembly and C languages
RENESAS TECHNICAL UPDATE	Preliminary report about the specification of a product, a document, etc.

NOTES:

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0033h				0070h			+
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0035h				0072h	1		+
0036h				0072h	1		+
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0039h				0075h	1		+
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003Bh				0077h	1	ł	+
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003Dh				0079h			<u> </u>
003Eh				007Ah 007Bh	l		<u> </u>
003Fh				007Bh			+
NOTES:			<u> </u>	007Ch 007Dh			+
	lank columns are all reserved space. No	access is allow	ved	007Dh 007Eh			+
i. D	and soluting are an reserved space. NO	000000 15 all01	····			1	
				007Fh			

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			I
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036Fh	UART0 Special Mode Register	U0SMR U1SMR4	186 188
0370h	UART1 Special Mode Register 4	U1SMR4 U1SMR3	188 187
0371h 0372h	UART1 Special Mode Register 3	U1SMR3 U1SMR2	187
0372h 0373h	UART1 Special Mode Register 2 UART1 Special Mode Register	U1SMR2 U1SMR	187
0373h 0374h	UART1 Special Mode Register UART2 Special Mode Register 4	U1SMR U2SMR4	186
0374h 0375h	UART2 Special Mode Register 4	U2SMR4 U2SMR3	188
0375h 0376h	UART2 Special Mode Register 3	U2SMR3 U2SMR2	187
0376h	UART2 Special Mode Register 2	U2SMR2 U2SMR	187
0377h 0378h	UART2 Special Mode Register UART2 Transmit/Receive Mode Register	U2SMR U2MR	186
0378h 0379h	UART2 Iransmit/Receive Mode Register	U2IMR U2BRG	183
0379h 037Ah	UART2 Bit Rate Generator UART2 Transmit Buffer Register	U2BRG U2TB	182
037An 037Bh	CARTZ Hanshill Duiler Register	UZID	101
037Bh 037Ch	UART2 Transmit/Receive Control Register 0	U2C0	184
037Ch 037Dh	UART2 Transmit/Receive Control Register 0	U2C0	184
037Dh 037Eh	UART2 Transmit/Receive Control Register 1	U2C1 U2RB	185
037En 037Fh	UARTZ RECEIVE DUILEL REGISTEL	UZKD	101
037711	1	_1	1

NOTES: 1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Page
0380h	Count Start Flag	TABSR	141, 158
0381h	Clock Prescaler Reset Fag	CPSRF	143, 158
0382h	One-Shot Start Flag	ONSF	142
0383h	Trigger Select Register	TRGSR	142
0384h	Up-Down Flag	UDF	141
0385h	op boinn lag	05.	
0386h	Timer A0 Register	TA0	140
0387h	Timer no Register	1710	140
0388h	Timer A1 Register	TA1	140
0389h	Timer Att Register		140
038Ah	Timer A2 Register	TA2	140
038Bh	Timer / 2 Register		
038Ch	Timer A3 Register	TA3	140
038Dh			
038Eh	Timer A4 Register	TA4	140
038Fh	- Intel / Integrater		
0390h	Timer B0 Register	TB0	157
0391h	Timer Do Register	100	107
0392h	Timer B1 Register	TB1	157
0393h	Timer DT Register	101	107
0393h	Timer B2 Register	TB2	157
0395h		102	101
0396h	Timer A0 Mode Register	TAOMR	140
0397h	Timer A1 Mode Register	TAIMR	140
0398h	Timer A2 Mode Register	TA2MR	140
0399h	Timer A3 Mode Register	TA3MR	140
0399h	Timer A4 Mode Register	TA4MR	140
039An 039Bh	Timer B0 Mode Register	TBOMR	140
039Ch	Timer B1 Mode Register	TB1MR	157
039Dh	Timer B2 Mode Register	TB2MR	157
039Eh	Timer B2 Special Mode Register	TB2SC	170
039Fh		10200	170
03A0h	UART0 Transmit/Receive Mode Register	UOMR	183
03A0h	UARTO Bit Rate Generator	U0BRG	182
03A2h	UART0 Transmit Buffer Register	UOTB	181
03A3h	CARTO Hanamit Duner Register	0015	101
03A3h	UART0 Transmit/Receive Control Register 0	U0C0	184
03A5h	UART0 Transmit/Receive Control Register 0	U0C1	185
03A6h	UARTO Receive Buffer Register	UORB	181
03A7h	Britte Receive Builer Register	COND	101
03A8h	UART1 Transmit/Receive Mode Register	U1MR	183
03A9h	UART1 Bit Rate Generator	U1BRG	182
03AAh	UART1 Transmit Buffer Register	U1TB	181
03ABh		onb	101
03ACh	UART1 Transmit/Receive Control Register 0	U1C0	184
03ADh	UART1 Transmit/Receive Control Register 0	U1C1	185
03AEh	UART1 Receive Buffer Register	U1RB	181
03AFh		00	
03B0h	UART Transmit/Receive Control Register 2	UCON	186
03B1h			
03B2h			
03B3h			-
03B4h			
03B5h			
03B6h			+
03B7h			
03B8h	DMA0 Request Factor Select Register	DM0SL	128
03B9h		DINIOCL	120
03BAh	DMA1 Request Factor Select Register	DM1SL	129
03BAh 03BBh		DIVIDE	123
03BCh	CRC Data Register	CRCD	253
03BDh		GROD	200
03BDh 03BEh	CRC Input Register	CRCIN	253
03BEh 03BFh		GROIN	200
030-11	l		1

			_
Address	Register	Symbol	Page
03C0h 03C1h	A/D Register 0	AD0	237
03C2h	A/D Register 1	AD1	237
03C3h	, vo rogotor i	,	20.
03C4h	A/D Register 2	AD2	237
03C5h	-		
03C6h	A/D Register 3	AD3	237
03C7h			
03C8h	A/D Register 4	AD4	237
03C9h			
03CAh	A/D Register 5	AD5	237
03CBh	A/D De sister C	ADC	007
03CCh 03CDh	A/D Register 6	AD6	237
03CEh	A/D Register 7	AD7	237
03CFh	A/D Register /	ADI	231
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	236
03D5h	Ŭ Ŭ		
03D6h	A/D Control Register 0	ADCON0	235
03D7h	A/D Control Register 1	ADCON1	235
03D8h	D/A Register 0	DA0	252
03D9h			
03DAh	D/A Register 1	DA1	252
03DBh			
03DCh	D/A Control Register	DACON	252
03DDh			
03DEh	Port P14 Control Register	PC14	264
03DFh 03E0h	Pull-Up Control Register 3 Port P0 Register	PUR3 P0	264 263
03E0h 03E1h	Port P0 Register	P0 P1	263
03E2h	Port P0 Direction Register	PD0	263
03E2h	Port P1 Direction Register	PD0 PD1	262
03E4h	Port P2 Register	P2	262
03E5h	Port P3 Register	P3	263
03E6h	Port P2 Direction Register	PD2	262
03E7h	Port P3 Direction Register	PD3	262
03E8h	Port P4 Register	P4	263
03E9h	Port P5 Register	P5	263
03EAh	Port P4 Direction Register	PD4	262
03EBh	Port P5 Direction Register	PD5	262
03ECh	Port P6 Register	P6	263
03EDh	Port P7 Register	P7	263
03EEh	Port P6 Direction Register	PD6	262
03EFh	Port P7 Direction Register	PD7	262
03F0h	Port P8 Register	P8	263
03F1h	Port P9 Register	P9	263
03F2h	Port P8 Direction Register	PD8	262
03F3h	Port P9 Direction Register	PD9	262
03F4h 03F5h	Port P10 Register Port P11 Register	P10 P11	263 263
03F5h 03F6h	Port P10 Direction Register	PD10	263
03F6h	Port P11 Direction Register	PD10 PD11	262
03F8h	Port P12 Register	P12	262
03F9h	Port P13 Register	P13	263
03FAh	Port P12 Direction Register	PD12	262
03FBh	Port P13 Direction Register	PD13	262
03FCh	Pull-Up Control Register 0	PUR0	265
03FDh	Pull-Up Control Register 1	PUR1	265
03FEh	Pull-Up Control Register 2	PUR2	266
03FFh	Port Control Register	PCR	266
	·		

NOTES: 1. Blank columns are all reserved space. No access is allowed.

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M16C/62P Group (M16C/62P, M16C/62PT) SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

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1.2 Performance Outline

Table 1.1 to 1.3 list Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version).

	Item	Performance
		M16C/62P
CPU	Number of Basic Instructions	91 instructions
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion
		function)
	Memory Capacity	See Table 1.4 to 1.5 Product List
Peripheral	Port	Input/Output : 113 pins, Input : 1 pin
Function	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit
	Serial Interface	3 channels Clock synchronous, UART, I ² C bus ⁽¹⁾ , IEBus ⁽²⁾ 2 channels Clock synchronous
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels
	D/A Converter	8 bits x 2 channels
	DMAC	2 channels
	CRC Calculation Circuit	CCITT-CRC
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources Priority level: 7 levels
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detectio function
	Voltage Detection Circuit	Available (option ⁽⁴⁾)
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7µA (VCC1=VCC2=3V, stop mode)
Flash memory	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V
version	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) ⁽³⁾
Operating Ambie	nt Temperature	-20 to 85°C, -40 to 85°C ⁽³⁾
Package		128-pin plastic mold LQFP

Table 1.1	Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version)
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NOTES:

- 1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
- 2. IEBus is a registered trademark of NEC Electronics Corporation.

3. See **Table 1.8 Product Code** for the program and erase endurance, and operating ambient temperature. In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.

4. All options are on request basis.

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	Item	Performance				
		M16C/62P	M16C/62PT ⁽⁴⁾			
CPU	Number of Basic Instructions	91 instructions				
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)			
	Operating Mode	Single-chip, memory expansion and microprocessor mode	Single-chip			
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)	1 Mbyte			
	Memory Capacity	See Table 1.4 to 1.7 Product Lis	st			
Peripheral	Port	Input/Output : 87 pins, Input : 1 pin				
Function	Multifunction Timer	Timer A : 16 bits x 5 channels, Time Three phase motor control circuit	r B : 16 bits x 6 channels,			
	Serial Interface	3 channels Clock synchronous, UART, I ² C bu 2 channels Clock synchronous	us ⁽¹⁾ , IEBus ⁽²⁾			
	A/D Converter	10-bit A/D converter: 1 circuit, 26 ch	annels			
	D/A Converter	8 bits x 2 channels				
	DMAC	2 channels				
	CRC Calculation Circuit	CCITT-CRC				
	Watchdog Timer	15 bits x 1 channel (with prescaler)				
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels				
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.				
	Oscillation Stop Detection Function	Stop detection of main clock oscillati	ion, re-oscillation detection function			
	Voltage Detection Circuit		Absent			
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz)	VCC1=VCC2=4.0 to 5.5V (f(BCLK=24MHz)			
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8μA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=VCC2=3V, stop mode)	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 2.0μA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode) 0.8μA (VCC1=VCC2=5V, stop mode)			
Flash memory	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V	5.0±0.5 V			
version	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area with / 10,000 times (block A, block 1) ⁽³⁾	out block A and block 1)			
Operating Ambient Temperature		-20 to 85°C, T version : -40 to 85°C -40 to 85°C (3) V version : -40 to 125°C				
Package		100-pin plastic mold QFP, LQFP				

Table 1.2 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(100-pin version)

NOTES:

- 1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
- 2. IEBus is a registered trademark of NEC Electronics Corporation.
- 3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
 - In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
- 4. Use the M16C/62PT on VCC1=VCC2
- 5. All options are on request basis.

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	Item	Performance				
		M16C/62P	M16C/62PT ⁽⁴⁾			
CPU	Number of Basic Instructions	91 instructions				
	Minimum Instruction	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V			
	Execution Time	100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)				
	Operating Mode	Single-chip mode				
	Address Space	1 Mbyte				
	Memory Capacity	See Table 1.4 to 1.7 Product List	st			
Peripheral	Port	Input/Output : 70 pins, Input : 1 pin				
Function	Multifunction Timer	Timer A : 16 bits x 5 channels (Time Timer B : 16 bits x 6 channels (Time				
	Serial Interface	 2 channels Clock synchronous, UART, I²C bu 1 channel Clock synchronous, I²C bus⁽¹⁾, IE 2 channels Clock synchronous (1 channel is compared to the synchronous) 	Bus ⁽²⁾			
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels				
	D/A Converter	8 bits x 2 channels				
	DMAC	2 channels				
	CRC Calculation Circuit	CCITT-CRC				
	Watchdog Timer	15 bits x 1 channel (with prescaler)				
	Interrupt	Internal: 29 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels				
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.				
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function				
	Voltage Detection Circuit		Absent			
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, (f(BCLK=10MHz)	VCC1=4.0 to 5.5V, (f(BCLK=24MHz)			
	Power Consumption	14 mA (VCC1=5V, f(BCLK)=24MHz) 8 mA (VCC1=3V, f(BCLK)=10MHz) 1.8μA (VCC1=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=3V, stop mode)	14 mA (VCC1=5V, f(BCLK)=24MHz) 2.0μA (VCC1=5V, f(XCIN)=32kHz, wait mode) 0.8μA (VCC1=5V, stop mode)			
Flash memory	Program/Erase Supply Voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5V			
version	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area with / 10,000 times (block A, block 1) ⁽³⁾	out block A and block 1)			
Operating Amb	ient Temperature	-20 to 85°C, -40 to 85°C ⁽³⁾	T version : -40 to 85°C V version : -40 to 125°C			
Package		80-pin plastic mold QFP				

Table 1.3 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(80-pin version)

NOTES:

- 1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
- 2. IEBus is a registered trademark of NEC Electronics Corporation.
- 3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
- In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
- 4. All options are on request basis.

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1.3 Block Diagram

Figure 1.1 is a M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram, Figure 1.2 is a M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram.

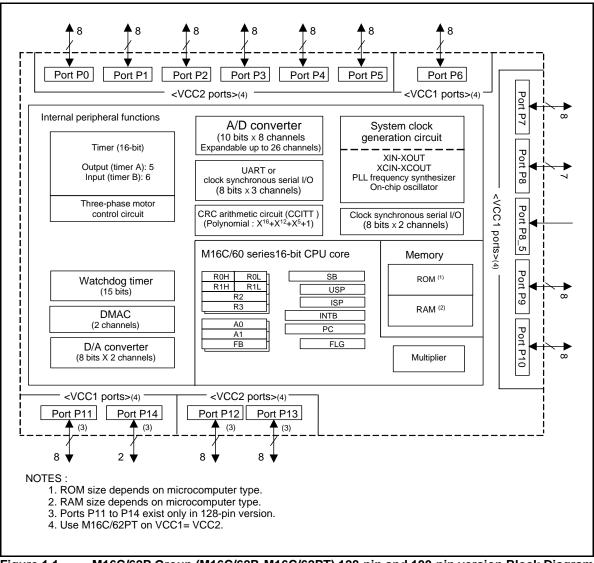


Figure 1.1 M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram

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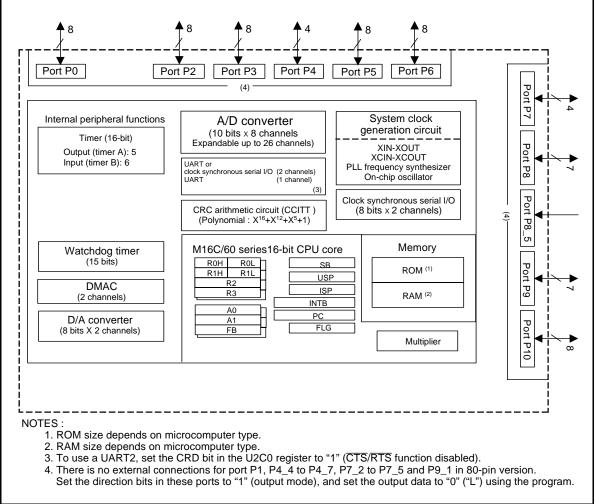


Figure 1.2 M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram



1.4 Product List

Table 1.4 to 1.7 list the product list, Figure 1.3 shows the Type No., Memory Size, and Package, Table 1.8 lists the Product Code of Flash Memory version and ROMless version for M16C/62P, and Table 1.9 lists the Product Code of Flash Memory version for M16C/62PT. Figure 1.4 shows the Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View), and Figure 1.5 shows the Marking Diagram of Flash Memory version for M16C/62PT (Top View) at the time of ROM order.

	(1) (11100/021)			A3 01 Dec. 2003
Type No.	ROM Capacity	RAM Capacity	Package Type (1)	Remarks
M30622M6P-XXXFP	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version
M30622M6P-XXXGP			PLQP0100KB-A	-
M30622M8P-XXXFP	64 Kbytes	4 Kbytes	PRQP0100JB-A	-
M30622M8P-XXXGP			PLQP0100KB-A	-
M30623M8P-XXXGP			PRQP0080JA-A	
M30622MAP-XXXFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	
M30622MAP-XXXGP			PLQP0100KB-A	
M30623MAP-XXXGP			PRQP0080JA-A	
M30620MCP-XXXFP	128 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620MCP-XXXGP			PLQP0100KB-A	
M30621MCP-XXXGP			PRQP0080JA-A	
M30622MEP-XXXFP	192 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MEP-XXXGP			PLQP0100KB-A	
M30623MEP-XXXGP			PLQP0128KB-A	
M30622MGP-XXXFP	256 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MGP-XXXGP			PLQP0100KB-A	
M30623MGP-XXXGP			PLQP0128KB-A	
M30624MGP-XXXFP		20 Kbytes	PRQP0100JB-A	
M30624MGP-XXXGP			PLQP0100KB-A	
M30625MGP-XXXGP			PLQP0128KB-A	
M30622MWP-XXXFP	320 Kbytes	16 Kbytes	PRQP0100JB-A	
M30622MWP-XXXGP			PLQP0100KB-A	
M30623MWP-XXXGP			PLQP0128KB-A	
M30624MWP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MWP-XXXGP			PLQP0100KB-A	
M30625MWP-XXXGP	7		PLQP0128KB-A	
M30626MWP-XXXFP	7	31 Kbytes	PRQP0100JB-A	
M30626MWP-XXXGP			PLQP0100KB-A]

Table 1.4Product List (1) (M16C/62P)

As of Dec. 2005

M30627MWP-XXXGP (D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.

PLQP0128KB-A : 128P6Q-A, PRQP0100JB-A : 100P6S-A, PLQP0100KB-A : 100P6Q-A, PRQP0080JA-A : 80P6S-A



PLQP0128KB-A

1.	Overview	

Type No.	ROM Capacity	RAM Capacity	Package Type (1)	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MHP-XXXGP			PLQP0100KB-A	
M30625MHP-XXXGP			PLQP0128KB-A	
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D) 512 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626MJP-XXXGP (D)		PLQP0100KB-A	
M30627MJP-XXXGP (D	,		PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	Flash memory
M30622F8PGP			PLQP0100KB-A	version ⁽²⁾
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	
M3062LFGPFP ⁽³⁾ (D) 256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	
M3062LFGPGP ⁽³⁾ (D)		PLQP0100KB-A	
M30625FGPGP	-		PLQP0128KB-A	-
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	-
M30626FHPGP			PLQP0100KB-A	
M30627FHPGP			PLQP0128KB-A	
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FJPGP			PLQP0100KB-A	
M30627FJPGP			PLQP0128KB-A	
M30622SPFP	-	4 Kbytes	PRQP0100JB-A	ROM-less version
M30622SPGP	\neg		PLQP0100KB-A	1
M30620SPFP		10 Kbytes	PRQP0100JB-A	1
M30620SPGP			PLQP0100KB-A	
M30624SPFP (C) –	20 Kbytes	PRQP0100JB-A	1
M30624SPGP (D)		PLQP0100KB-A	1
M30626SPFP (C)	31 Kbytes	PRQP0100JB-A	
M30626SPGP (D)		PLQP0100KB-A	

Table 1.5 Product List (2) (M16C/62P)

As of Dec. 2005

(D): Under development

NOTES:

- The old package type numbers of each package type are as follows. PLQP0128KB-A : 128P6Q-A, PRQP0100JB-A : 100P6S-A, PLQP0100KB-A : 100P6Q-A, PRQP0080JA-A : 80P6S-A
- 2. In the flash memory version, there is 4K bytes area (block A).
- Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

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As of Dec. 2005

Type No.		ROM Capacity	RAM Capacity	Package Type (1)	Re	marks
M3062CM6T-XXXFP	(D)	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM	T Version
M3062CM6T-XXXGP	(D)			PLQP0100KB-A	version	(High reliability
M3062EM6T-XXXGP	(P)			PRQP0080JA-A		85°C version)
M3062CM8T-XXXFP	(D)	64 Kbytes	4 Kbytes	PRQP0100JB-A		
M3062CM8T-XXXGP	(D)			PLQP0100KB-A		
M3062EM8T-XXXGP	(P)			PRQP0080JA-A		
M3062CMAT-XXXFP	(D)	96 Kbytes	5 Kbytes	PRQP0100JB-A		
M3062CMAT-XXXGP	(D)			PLQP0100KB-A		
M3062EMAT-XXXGP	(P)			PRQP0080JA-A		
M3062AMCT-XXXFP	(D)	128 Kbytes	10 Kbytes	PRQP0100JB-A		
M3062AMCT-XXXGP	(D)			PLQP0100KB-A		
M3062BMCT-XXXGP	(P)			PRQP0080JA-A		
M3062CF8TFP	(D)	64 K+4 Kbytes	4 Kbytes	PRQP0100JB-A	Flash	
M3062CF8TGP				PLQP0100KB-A	memory	
M3062AFCTFP	(D)	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	version ⁽²⁾	
M3062AFCTGP	(D)			PLQP0100KB-A		
M3062BFCTGP	(P)]		PRQP0080JA-A	1	
M3062JFHTFP	(D)	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	1	
M3062JFHTGP	(D)]		PLQP0100KB-A		

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Table 1.6 Product List (3) (T version (M16C/62PT))

(D): Under development

(P): Under planning

NOTES:

- The old package type numbers of each package type are as follows. PRQP0100JB-A : 100P6S-A, PLQP0100KB-A : 100P6Q-A, PRQP0080JA-A : 80P6S-A
- 2. In the flash memory version, there is 4K bytes area (block A).

As of Dec. 2005

-		1	-	1	1	
Type No.		ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Re	emarks
M3062CM6V-XXXFP	(P)	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM	V Version
M3062CM6V-XXXGP	(P)			PLQP0100KB-A	version	(High reliability
M3062EM6V-XXXGP	(P)			PRQP0080JA-A		125°C version)
M3062CM8V-XXXFP	(P)	64 Kbytes	4 Kbytes	PRQP0100JB-A		
M3062CM8V-XXXGP	(P)			PLQP0100KB-A		
M3062EM8V-XXXGP	(P)			PRQP0080JA-A		
M3062CMAV-XXXFP	(P)	96 Kbytes	5 Kbytes	PRQP0100JB-A		
M3062CMAV-XXXGP	(P)	1		PLQP0100KB-A	1	
M3062EMAV-XXXGP	(P)			PRQP0080JA-A		
M3062AMCV-XXXFP	(D)	128 Kbytes	10 Kbytes	PRQP0100JB-A		
M3062AMCV-XXXGP	(D)			PLQP0100KB-A		
M3062BMCV-XXXGP	(P)			PRQP0080JA-A		
M3062AFCVFP	(D)	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	Flash	
M3062AFCVGP	(D)	1		PLQP0100KB-A	memory	
M3062BFCVGP	(P)	1		PRQP0080JA-A	version ⁽²⁾	
M3062JFHVFP	(P)	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	1	
M3062JFHVGP	(P)	1		PLQP0100KB-A	1	

Table 1.7 Product List (4) (V version (M16C/62PT))

(D): Under development

(P): Under planning

NOTES:

1. The old package type numbers of each package type are as follows.

PLQP0128KB-A : 128P6Q-A, PRQP0100JB-A : 100P6S-A, PLQP0100KB-A : 100P6Q-A, PRQP0080JA-A : 80P6S-A

2. In the flash memory version, there is 4K bytes area (block A).

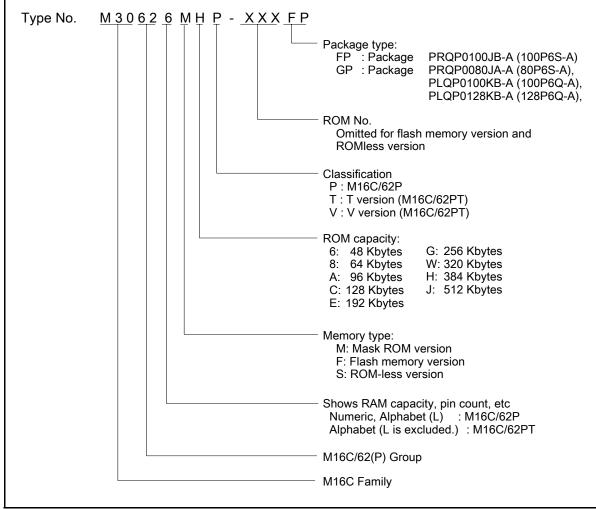
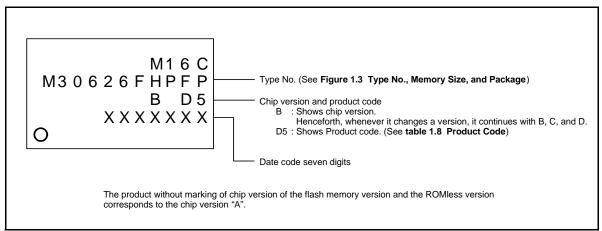


Figure 1.3 Type No., Memory Size, and Package

	Product	Deelvere	Interna (User ROM Area Bloc	Without Block A,	Interna (Block A,	Operating Ambient	
	Code	Package	Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	Temperature
Flash memory	D3	Lead-	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
Version	D5	included					-20°C to 85°C
	D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	D9					-20°C to 85°C	-20°C to 85°C
	U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	U5						-20°C to 85°C
	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	U9					-20°C to 85°C	-20°C to 85°C
ROM-less	D3	Lead-	-	-	-	-	-40°C to 85°C
version	D5	included					-20°C to 85°C
	U3	Lead-free	-	-	-	-	-40°C to 85°C
	U5						-20°C to 85°C

	Table 1.8	Product Code of Flash Memory	version and ROMIess version for M16C/62P
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Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View)

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		Product		Product Package -		(User R	al ROM OM Area ck A, Block 1)	Intern (Block A	Operating Ambient	
		Code	Fackage	Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	Temperature		
Flash	T Version	В	Lead-	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C		
memory	V Version		included					-40°C to 125°C		
Version	T Version	B7		1,000		10,000	-40°C to 85°C	-40°C to 85°C		
	V Version						-40°C to 125°C	-40°C to 125°C		
	T Version	U	Lead-free	100		100	0°C to 60°C	-40°C to 85°C		
	V Version							-40°C to 125°C		
	T Version	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C		
	V Version						-40°C to 125°C	-40°C to 125°C		

Table 1.9 Product Code of Flash Memory version for M16C/62PT

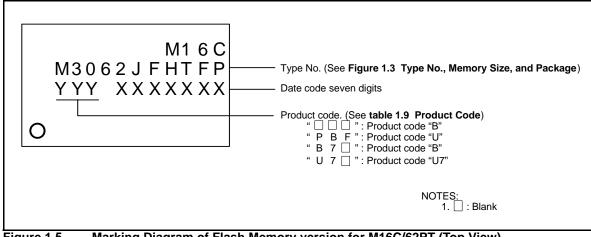


Figure 1.5 Marking Diagram of Flash Memory version for M16C/62PT (Top View)

1.5 Pin Configuration

Figures 1.6 to 1.9 show the Pin Configuration (Top View).

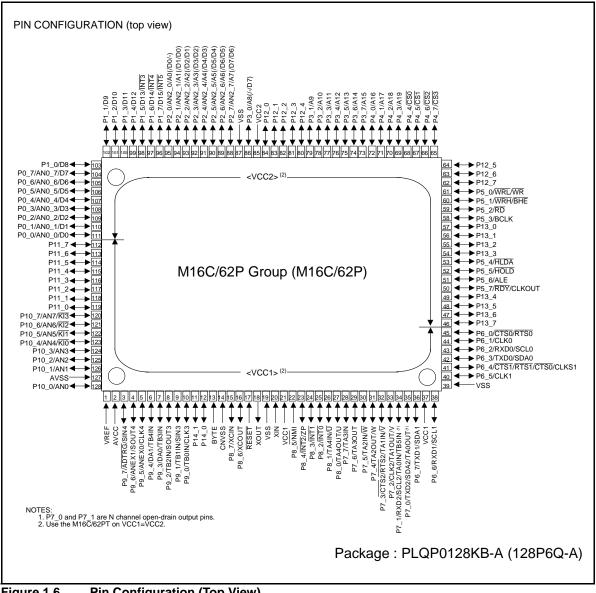


Figure 1.6 Pin Configuration (Top View)

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Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pi
1	VREF						
2	AVCC						
3		P9_7			SIN4	ADTRG	
4		P9_6			SOUT4	ANEX1	
5		P9_5			CLK4	ANEX0	
6		P9_4		TB4IN		DA1	
7		P9_3		TB3IN		DA0	
8		P9_2		TB2IN	SOUT3		
9		P9_1		TB1IN	SIN3		
10		P9_0		TB0IN	CLK3		
11		P14_1					
12		P14_0					
13	BYTE						
14	CNVSS						
15	XCIN	P8_7					
16	XCOUT	P8_6	ļ				
17	RESET						
18	XOUT						
19	VSS						
20	XIN						
21	VCC1						
22		P8_5	NMI				
23		P8_4	INT2	ZP			
24		P8_3	INT1				
25		P8_2	INT0				
26		P8_1		TA4IN/U			
20		P8_0		TA4IN/U TA4OUT/U			
28		P7_7		TA3IN			
20		P7_6		TASIN			
30				TA2IN/W			
		P7_5					
31		P7_4		TA2OUT/W			
32		P7_3		TA1IN/V	CTS2/RTS2		
33		P7_2		TA1OUT/V	CLK2		
34		P7_1		TA0IN/TB5IN	RXD2/SCL2		
35		P7_0		TA0OUT	TXD2/SDA2 TXD1/SDA1		
36 37	VCC1	P6_7					
		P6 6	+			+	+
38 39	VSS	P6_6	+		RXD1/SCL1	+	+
40	100	P6_5			CLK1		
40					CTS1/RTS1/CTS0/CLKS1		
41		P6_4 P6_3			TXD0/SDA0		
42		P6_3 P6_2	+		RXD0/SCL0	+	+
43		P6_2 P6_1	+		CLK0	+	+
44					CTS0/RTS0		
		P6_0			U130/K130		
46		P13_7					
47		P13_6					
48		P13_5					
49	+	P13_4 P5_7		1			RDY/CLKOUT

Table 1.10 Pin Characteristics for 128-Pin Package (1)

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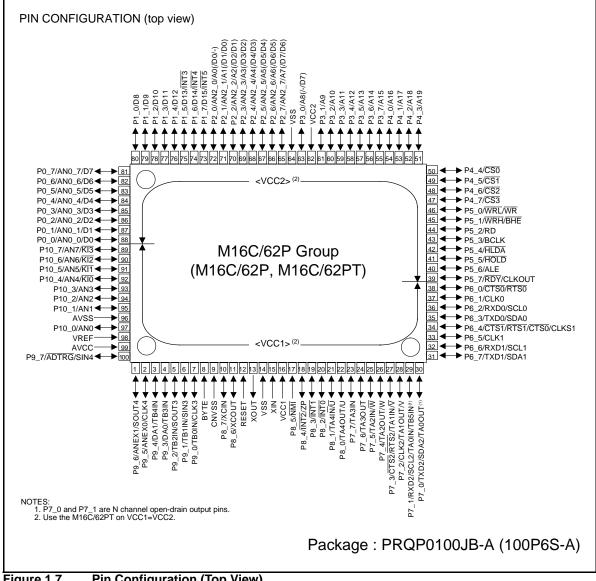
Pin No.	Control Pin		Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control P
51		P5_6					ALE
52		P5_5					HOLD
53		P5_4					HLDA
54		P13_3					
55		P13_2					
56		 P13_1					
57		 P13_0					
58		P5_3					BCLK
59		P5_2					RD
60		P5_1					WRH/BHE
61		1					WRL/WR
62		P5_0 P12_7					WRL/WR
63		P12_7 P12_6					
64		P12_0					
			+	<u> </u>			000
65		P4_7					CS3
66		P4_6					CS2
67		P4_5					CS1
68		P4_4					CS0
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8(/-/D7)
87	VSS						
88		P2_7	-			AN2_7	A7(/D7/D6)
89		P2_6	-			AN2_6	A6(/D6/D5)
90	<u> </u>	P2_5				AN2_5	A5(/D5/D4)
91		P2_4				AN2_4	A4(/D4/D3)
92		P2_3				AN2_3	A3(/D3/D2)
93 94		P2_2 P2_1		<u> </u>		AN2_2 AN2_1	A2(/D2/D1) A1(/D1/D0)
94 95		P2_1 P2_0	+	<u> </u>		AN2_1 AN2_0	A0(/D0/-)
			INITE				
96		P1_7	INT5				D15
97		P1_6	INT4				D14
98		P1_5	INT3				D13
99		P1_4					D12
100		P1_3					D11

Table 1.11 Pin Characteristics for 128-Pin Package (2)

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Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
101		P1_2					D10
102		P1_1					D9
103		P1_0					D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	KI3			AN7	
121		P10_6	KI2			AN6	
122		P10_5	KI1			AN5	
123		P10_4	KIO			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	

 Table 1.12
 Pin Characteristics for 128-Pin Package (3)



Pin Configuration (Top View) Figure 1.7

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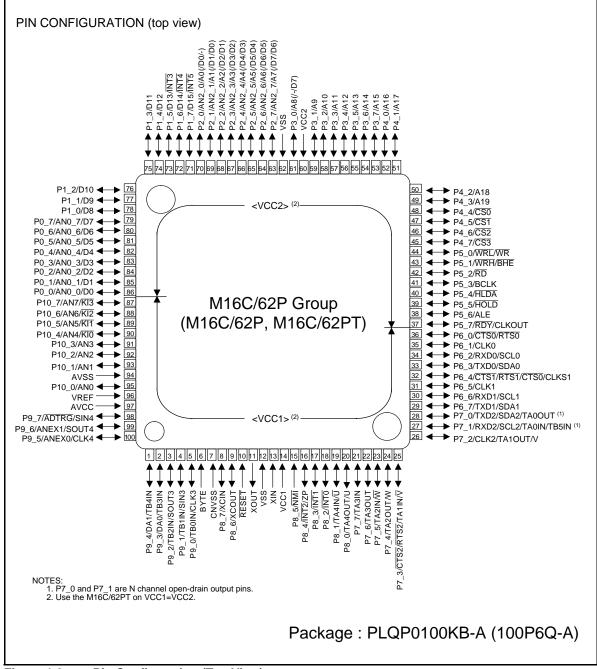


Figure 1.8 Pin Configuration (Top View)

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Pin FP	No. GP	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
1	99		P9_6			SOUT4	ANEX1	
2	100		_ P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN		DA1	
4	2		P9_3		TB3IN		DA0	
5	3		P9_2		TB2IN	SOUT3		
6	4		P9_1		TB1IN	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10		XCIN	P8_7					
11		XCOUT	P8_6					
12		RESET						
13		XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	NMI				
18	16		P8_4	INT2	ZP			
19	17		P8_3	INT1				
20	18		_ P8_2	INTO				
21	19		P8_1		TA4IN/U			
22	20		P8_0		TA4IIV/U TA4OUT/U			
23	20		P7_7		TA3IN			
24	22		P7_6		TA3OUT			
25	23		P7_5		TA2IN/W			
26	24		P7_4		TA2IN/W TA2OUT/W			
27	25		P7_3		TA1IN/V	CTS2/RTS2		
28	26		P7_3 P7_2		TATIN/V TATOUT/V	CLK2		
20	20		P7_1		TA0IN/TB5IN	RXD2/SCL2		
30	28		P7_0		TAOIN/TBSIN	TXD2/SDA2		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		 P6_4			CTS1/RTS1/CTS0/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0	1	1
37	35		P6_1			CLK0		+
38	36		P6_0			CTS0/RTS0		
39	37					0130/1130	+	
			P5_7					RDY/CLKOUT
40	38		P5_6				-	ALE
41	39		P5_5					HOLD
42	40		P5_4					HLAD
43	41		P5_3					BCLK
44	42		P5_2					RD
45	43		P5_1					WRH/BHE
46	44		P5_0					WRL/WR
47	45		P4_7					CS3
48	46		P4_6					CS2
40	40						+	
			P4_5					CS1
50	48		P4_4					CS0

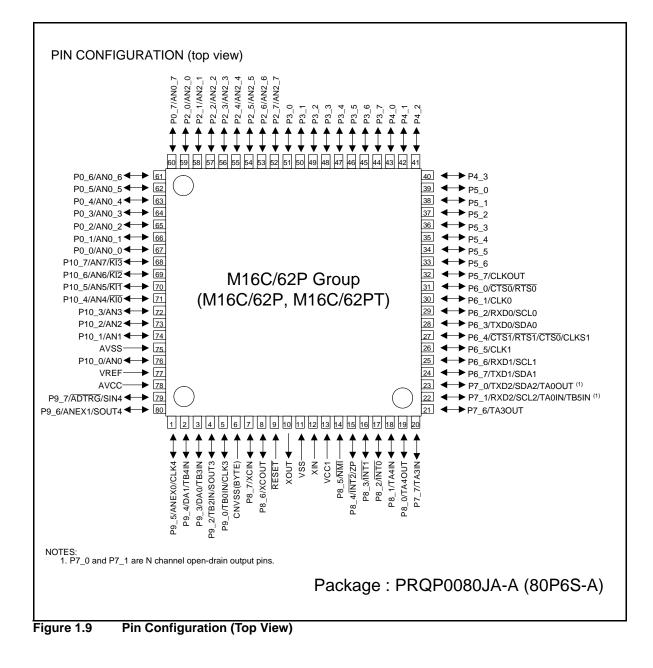
Table 1.13 Pin Characteristics for 100-Pin Package (1)

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Pin	No.	1				1		1
FP	GP	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51	49		P4_3					A19
52	50		_ P4_2					A18
53	51		P4_1					A17
54	52		 P4_0					A16
55	53		_ P3_7					A15
56	54		_ P3_6					A14
57	55		P3_5					A13
58	56		 P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8(/-/D7)
64	62	VSS						
65	63		P2_7				AN2_7	A7(/D7/D6)
66	64		P2_6				AN2_6	A6(/D6/D5)
67	65		P2_5				AN2_5	A5(/D5/D4)
68	66		P2_4				AN2_4	A4(/D4/D3)
69	67		P2_3				AN2_3	A3(/D3/D2)
70	68		P2_2				AN2_2	A2(/D2/D1)
71 72	69 70		P2_1 P2_0				AN2_1 AN2_0	A1(/D1/D0) A0(/D0/-)
73							AIN2_0	
	71		P1_7	INT5				D15
74	72		P1_6	INT4				D14
75	73		P1_5	INT3				D13
76	74		P1_4					D12
77	75		P1_3					D11
78	76		P1_2					D10
79	77		P1_1					D9
80	78		P1_0					D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	KI3			AN7	
90	88		P10_6	KI2			AN6	
91	89		P10_5	KI1			AN5	
92	90		P10_4	KI0			AN4	1
93	91		P10_3	-			AN3	
94	92		P10_2				AN2	1
95	93		 P10_1				AN1	1
96	94	AVSS						1
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						1
100	98		P9_7			SIN4	ADTRG	1
			1.9_1				AUING	I

Table 1.14 Pin Characteristics for 100-Pin Package (2)

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Pin No.	Control Pin		Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pir
1		P9_5			CLK4	ANEX0	
2		P9_4		TB4IN		DA1	
3		P9_3		TB3IN		DA0	
4		P9_2		TB2IN	SOUT3		
5		P9_0		TB0IN	CLK3		
6	CNVSS (BYTE)						
7	XCIN	P8_7					
8	XCOUT	P8_6					
9	RESET	_					
10	XOUT						
11	VSS						
12	XIN						
13	VCC1						
14		P8_5	NMI				
15		P8_4	INT2	ZP			
16		P8_3	INT1	21			
17							
		P8_2	INT0				
18		P8_1		TA4IN			
19		P8_0		TA4OUT			
20		P7_7		TA3IN			
21		P7_6		TA3OUT			
22		P7_1		TA0IN/TB5IN	RXD2/SCL2		
23		P7_0		TA0OUT	TXD2/SDA2		
24		P6_7			TXD1/SDA1		
25		P6_6			RXD1/SCL1		
26		P6_5			CLK1		
27		P6_4			CTS1/RTS1/CTS0/CLKS1		
28		P6_3			TXD0/SDA0		
29 30		P6_2 P6_1			RXD0/SCL0 CLK0		
				-			
31		P6_0			CTS0/RTS0		
32		P5_7					CLKOUT
33		P5_6					
34		P5_5					
35		P5_4					
36		P5_3					
37		P5_2					
38		P5_1		1	İ.	1	1
39		P5_0				1	1
40		P4_3		1		1	1
41							
		P4_2				<u> </u>	+
42		P4_1	-				
43		P4_0				 	
44		P3_7					ļ
45		P3_6					
46		P3_5					
47		P3_4	1			1	1
48		P3_3	1	1		1	1
		P3_2					
49							

Pin Characteristics for 80-Pin Package (1) Table 1.15

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Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51	P	3_0					
52	P2	2_7				AN2_7	
53	P2	2_6				AN2_6	
54	Pź	2_5				AN2_5	
55	P2	2_4				AN2_4	
56	P2	2_3				AN2_3	
57	P2	2_2				AN2_2	
58	Pź	2_1				AN2_1	
59	Pź	2_0				AN2_0	
60		0_7				AN0_7	
61		0_6				AN0_6	
62		0_5				AN0_5	
63		0_4				AN0_4	
64		0_3				AN0_3	
65		0_2				AN0_2	
66		0_1				AN0_1	
67		0_0				AN0_0	
68	P	10_7	KI3			AN7	
69	P	10_6	KI2			AN6	
70	P	10_5	KI1			AN5	
71	P	10_4	KI0			AN4	
72		10_3				AN3	
73	P	10_2				AN2	
74	P	10_1				AN1	
75	AVSS						
76	P	10_0				AN0	
77	VREF						
78	AVCC						
79	P	9_7			SIN4	ADTRG	
80	P	9_6			SOUT4	ANEX1	

 Table 1.16
 Pin Characteristics for 80-Pin Package (2)

1.6 Pin Description

	•	•	•	
Signal Name	Pin Name	I/O Type	Power Supply ⁽³⁾	Description
Power supply input	VCC1,VCC2 VSS	Ι	_	Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC1 \ge VCC2. ^(1, 2)
Analog power supply input	AVCC AVSS	I	VCC1	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	RESET	I	VCC1	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS	Ι	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode.
External data bus width select input	BYTE	Ι	VCC1	Switches the data bus in external memory space. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one. Connect this pin to VSS when an single-chip mode.
Bus control pins ⁽⁴⁾	D0 to D7	I/O	VCC2	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
	D8 to D15	I/O	VCC2	Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus.
	A0 to A19	0	VCC2	Output address bits (A0 to A19).
	A0/D0 to A7/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A0 to A7) by timesharing when external 8-bit data bus are set as the multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A1 to A8) by timesharing when external 16-bit data bus are set as the multiplexed bus.
	CS0 to CS3	0	VCC2	Output $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ signals. $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ are chip-select signals to specify an external space.
	WRL/WR WRH/BHE RD	0	VCC2	Output WRL, WRH, (WR, BHE), RD signals. WRL and WRH or BHE and WR can be switched by program. • WRL, WRH and RD are selected The WRL signal becomes "L" by writing data to an even address in an external memory space. The WRH signal becomes "L" by writing data to an odd address in an external memory space. The RD pin signal becomes "L" by reading data in an external memory space. • WR, BHE and RD are selected The WR signal becomes "L" by reading data in an external memory space. • WR, BHE and RD are selected The RD pin signal becomes "L" by writing data in an external memory space. • WR, BHE and RD are selected The RD signal becomes "L" by reading data in an external memory space. The RD signal becomes "L" by reading data in an external memory space. The BHE signal becomes "L" by accessing an odd address. Select WR, BHE and RD for an external 8-bit data bus.
	ALE	0	VCC2	ALE is a signal to latch the address.
	HOLD	Ι	VCC2	While the HOLD pin is held "L", the microcomputer is placed in a hold state.
	HLDA	0	VCC2	In a hold state, HLDA outputs a "L" signal.
	RDY	Ι	VCC2	While applying a "L" signal to the RDY pin, the microcomputer is placed in a wait state.

Table 1.17	Pin Description	(100-pin and	128-pin Version) (1)
		1.00 p aa	

I : Input O : Output I/O : Input and output

Power Supply : Power supplies which relate to the external bus pins are separated as VCC2, thus they can be interfaced using the different voltage as VCC1.

NOTES:

- 1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
- 2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 and VCC2 pins. Also the apply condition is that VCC1 = VCC2.
- 3. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
- 4. Bus control pins in M16C/62PT cannot be used.

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	-	-	-	
Signal Name	Pin Name	I/O Type	Power Supply ⁽¹⁾	Description
Main clock input	XIN	1	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT ⁽³⁾ . To use
Main clock output	XOUT	0	VCC1	the external clock, input the clock from XIN and leave XOUT open.
Sub clock input		I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal
Sub clock output	XCOUT	0	VCC1	oscillator between XCIN and XCOUT ⁽³⁾ . To use the external clock, input the clock from XCIN and leave XCOUT open.
BCLK output ⁽²⁾	BCLK	0	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	0	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
INT interrupt	INT0 to INT2	I	VCC1	Input pins for the INT interrupt.
input	NT3 to INT5	I	VCC2	
NMI interrupt input	NMI	I	VCC1	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.
Key input interrupt input	KI0 to KI3	-	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	These are timer A0 to timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TA0IN to TA4IN	—	VCC1	These are timer A0 to timer A4 input pins.
	ZP	-	VCC1	Input pin for the Z-phase.
Timer B	TB0IN to TB5IN	-	VCC1	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, <u>Ū,</u> V, ⊽, W, ₩	0	VCC1	These are Three-phase motor control output pins.
Serial interface	CTS0 CTS2	I	VCC1	These are send control input pins.
	RTS0 RTS2	0	VCC1	These are receive control output pins.
	CLK0 to CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	ļ	VCC1	These are serial data input pins.
	SIN3, SIN4		VCC1	These are serial data input pins.
	TXD0 to TXD2	0	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	0	VCC1	These are serial data output pins.
	CLKS1	0	VCC1	This is output pin for transfer clock output from multiple pins function.
I ² C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

 Table 1.18
 Pin Description (100-pin and 128-pin Version) (2)

NOTES:

- 1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
- 2. This pin function in M16C/62PT cannot be used.
- 3. Ask the oscillator maker the oscillation characteristic.

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			i .	
Signal Name	Pin Name	I/O	Power	Description
		Туре	Supply ⁽¹⁾	
Reference	VREF	I	VCC1	Applies the reference voltage for the A/D converter and D/A
voltage input				converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A/D converter.
	ADTRG	I	VCC1	This is an A/D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	0	VCC1	This is the output pin for the D/A converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7 ⁽²⁾ , P13_0 to P13_7 ⁽²⁾	1/0	VCC2	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7 ⁽²⁾	1/0	VCC1	8-bit I/O ports having equivalent functions to P0. (however, output of P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7, P14_0, P14_1 ⁽²⁾	I/O	VCC1	I/O ports having equivalent functions to P0.
Input port	P8_5	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

 Table 1.19
 Pin Description (100-pin and 128-pin Version) (3)

NOTES:

1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.

2. Ports P11 to P14 in M16C/62P (100-pin version) and M16C/62PT (100-pin version) cannot be used.

Signal Name	Pin Name	1/0	Power	Description
-		Туре	Supply	
Power supply input	VCC1, VSS	I	-	Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. $^{(1, 2)}$
Analog power supply input	AVCC AVSS	-	VCC1	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	RESET	—	VCC1	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS (BYTE)	Η	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. As for the BYTE pin of the 80-pin versions, pull-up processing is performed within the microcomputer.
Main clock input	XIN	Ι	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT ⁽³⁾ . To use
Main clock output	XOUT	0	VCC1	the external clock, input the clock from XIN and leave XOUT open.
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal
Sub clock output	XCOUT	0	VCC1	oscillator between XCIN and XCOUT ⁽³⁾ . To use the external clock, input the clock from XCIN and leave XCOUT open.
Clock output	CLKOUT	0	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
INT interrupt input	INT0 to INT2	I	VCC1	Input pins for the INT interrupt.
NMI interrupt input	NMI	I	VCC1	Input pin for the $\overline{\rm NMI}$ interrupt.
Key input interrupt input	KI0 to KI3	Ι	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT, TA3OUT, TA4OUT	I/O	VCC1	These are Timer A0, Timer A3 and Timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TAOIN, TA3IN, TA4IN	Ι	VCC1	These are Timer A0, Timer A3 and Timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	These are Timer B0, Timer B2 to Timer B5 input pins.
Serial interface	CTS0 to CTS1	Ι	VCC1	These are send control input pins.
	RTS0 to RTS1	0	VCC1	These are receive control output pins.
	CLK0, CLK1, CLK3, CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	-	VCC1	These are serial data input pins.
	SIN4	Ι	VCC1	This is serial data input pin.
	TXD0 to TXD2	0	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	0	VCC1	These are serial data output pins.
	CLKS1	0	VCC1	This is output pin for transfer clock output from multiple pins function.
I ² C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

Table 1.20Pin Description (80-pin Version) (1) (1)

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.

2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 pin.

3. Ask the oscillator maker the oscillation characteristic.

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Signal Name	Pin Name	I/O Type	Power Supply ⁽¹⁾	Description
Reference voltage input	VREF	Ι	VCC1	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	Ι	VCC1	Analog input pins for the A/D converter.
	ADTRG	Ι	VCC1	This is an A/D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1		VCC1	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	0	VCC1	This is the output pin for the D/A converter.
I/O port ⁽¹⁾	P0_0 to P0_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_7, P6_0 to P6_7, P10_0 to P10_7	I/O	VCC1	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7	I/O	VCC1	I/O ports having equivalent functions to P0.
	P4_0 to P4_3, P7_0, P7_1, P7_6, P7_7	I/O	VCC1	I/O ports having equivalent functions to P0. (however, output of P7_0 and P7_1 for the N-channel open drain output.)
Input port	P8_5	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

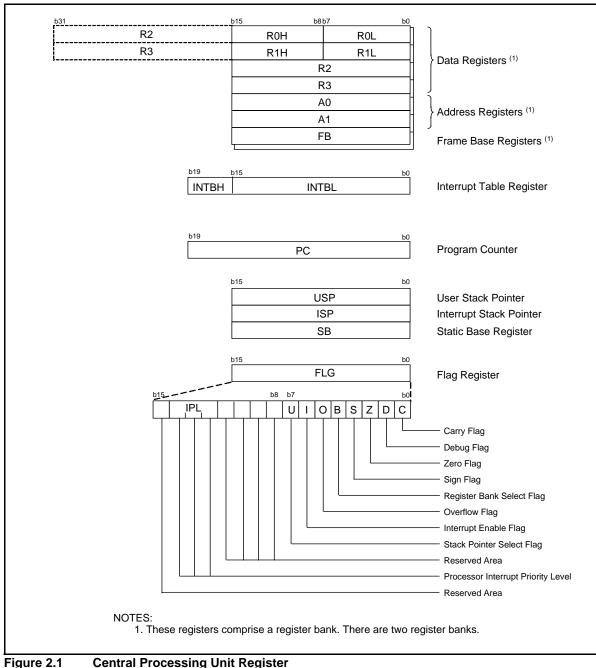
 Table 1.21
 Pin Description (80-pin Version) (2)

NOTES:

1. There is no external connections for port P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version. Set the direction bits in these ports to "1" (output mode), and set the output data to "0" ("L") using the program.

2. **Central Processing Unit (CPU)**

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

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2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits. Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a Memory Map of the M16C/62P group. The address space extends the 1M bytes from address 00000h to FFFFFh.

The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

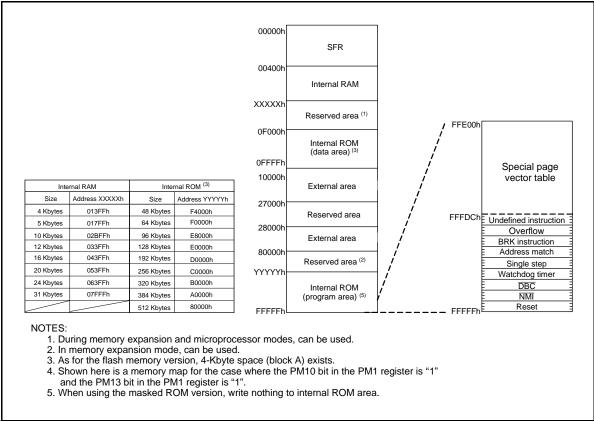
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 10-Kbyte internal RAM is allocated to the addresses from 00400h to 02BFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

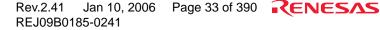
The SRF is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the M16C/60 and M16C/20 Series Software Manual.

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users. Use M16C/62P (80-pin version) and M16C/62PT in single-chip mode. The memory expansion and microprocessor modes cannot be used







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Special Function Register (SFR) 4.

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.6 list the SFR information.

Table 4.1 SFR Information (1) ⁽¹⁾

Address	Register	Symbol	After Reset
0000h	Register	Symbol	Allel Resel
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 ⁽²⁾	PMO	00000000b(CNVSS pin is "L") 00000011b(CNVSS pin is "H")
0005h	Processor Mode Register 1	PM1	00001000b
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	0010000b
0008h	Chip Select Control Register (6)	CSR	0000001b
0009h	Address Match Interrupt Enable Register	AIER	XXXXXX00b
000Ah	Protect Register	PRCR	XX000000b
000Bh	Data Bank Register (6)	DBR	00h
000Ch	Oscillation Stop Detection Register ⁽³⁾	CM2	0X00000b
000Dh		OINE	0/000000
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XXXXXXb (4)
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h	Voltage Detection Register 1 ^(5, 6)	VCR1	00001000b
0013h	Voltage Detection Register 2 ^(5, 6)	VCR2	00h
	Chip Select Expansion Control Register ⁽⁶⁾		00h
001Bh		CSE	
001Ch	PLL Control Register 0	PLC0	0001X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XXX00000b
001Fh	Low Voltage Detection Interrupt Register ⁽⁶⁾	D4INT	00h
0020h	DMA0 Source Pointer	SAR0	XXh
0021h			XXh
0022h			XXh
0023h			
0024h	DMA0 Destination Pointer	DAR0	XXh
0025h			XXh
0026h			XXh
0020h			7011
	DMAQ Transfer Counter	TODA	VVL
0028h	DMA0 Transfer Counter	TCR0	XXh
0029h			XXh
002Ah			
002Bh			
002Ch	DMA0 Control Register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h	DMA1 Source Pointer	SAR1	XXh
0031h			XXh
0032h			XXh
0033h			
0033h	DMA1 Destination Pointer	DAR1	XXh
0034n 0035h		DANT	XXh
0036h			XXh
0037h			
0038h	DMA1 Transfer Counter	TCR1	XXh
0039h			XXh
003Ah			
003Bh			
003Ch	DMA1 Control Register	DM1CON	00000X00b
003Dh	-	ł	
003Eh			
003Fh			

NOTES:

NOTES:

 The blank areas are reserved and cannot be accessed by users.
 The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
 The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
 The WDC5 bit is "0" (cold start) immediately after power-on. I t can only be set to "1" in a program.
 This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
 This register in M16C/62PT cannot be used.
 X : Nothing is mapped to this bit

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0040h Description 0041h INT3 Interrupt Control Register XXXXX000b 0043h INT3 Interrupt Control Register TBSIC XXXXX000b 0044h Timer B5 Interrupt Control Register TBSIC XXXXX00b 0044h Timer B5 Interrupt Control Register TBSIC XXXXX00b 0044h Timer B5 Interrupt Control Register TBSIC XXXXX00b 0044h SICA Interrupt Control Register SIC, INTSIC XXXXX00b 0044h SICA Interrupt Control Register SIC, INTSIC XXXXX00b 0044h XXXXX00b SICA Interrupt Control Register SIC XXXXX00b 0044h XXXXX00b SICA Interrupt Control Register SIC XXXXX00b 0044h XXXXX00b Control Register SICC XXXXX00b 0044h VART2 Transmit Interrupt Control Register SICC XXXXX00b 0055h UART2 Reserve Interrupt Control Register SICC XXXXX00b 0056h UART3 Reserve Interrupt Control Register SICC XXXXX00b 0056h UART3 Transmit Interrup	Address	Register	Symbol	After Reset
0041h INT3 Interrupt Control Register INT3IC XXXXX00b 0043h INT3 Interrupt Control Register INT3IC XXXXX00b 0044h Timer B5 Interrupt Control Register TBIC XXXXX00b 0044h Timer B5 Interrupt Control Register TBIC XXXXX00b 0044h Timer B5 Interrupt Control Register, INT5 Interrupt Control Register TBIC XXXXX00b 0048h SIGD Interrupt Control Register, INT5 Interrupt Control Register SIGI, INT4IC XXXXX00b 0048h SIGD Interrupt Control Register, INT6 Interrupt Control Register DMIC XXXXX00b 0048h DMAID Interrupt Control Register DMIC XXXXX00b 0047b DMAIT Interrupt Control Register DMIC XXXX00b 0047b DMAIT Interrupt Control Register DMIC XXXX00b 0047b A/D Conversion Interrupt Control Register DMIC XXXX00b 0047b A/D Conversion Interrupt Control Register S21C XXXX00b 0047b A/D Conversion Interrupt Control Register S21C XXXX00b 00580h Timer A/D Interrupt Control Register		l	Gymbol	
0943/h INT 3 Interrupt Control Register INT 31C XXXXXX00b 0944/h INT 3 Interrupt Control Register THSIC XXXXX00b 0044/h Timer B5 Interrupt Control Register THSIC XXXXX00b 0044/h Timer B5 Interrupt Control Register THSIC XXXXX00b 0044/h Timer B5 Interrupt Control Register SIC, INTSIC XXXXX00b 0044/h SICA Interrupt Control Register SIC, INTSIC XXXXX00b 0044/h SICA Interrupt Control Register SIC, INTSIC XXXXX00b 0044/h DMARD Interrupt Control Register DMARD XXXXX00b 0044/h DMARD Interrupt Control Register SDIC XXXXX00b 0044/h DMARD Interrupt Control Register SDIC XXXXX00b 00550 <td></td> <td></td> <td></td> <td></td>				
0044bn INT3 Interrupt Control Register INT3 IC XX00X000b 0044bn Timer B5 Interrupt Control Register TBSIC XXXXX006b 0044bn Timer B5 Interrupt Control Register TBSIC XXXXX006b 0044bn Timer B5 Interrupt Control Register TBSIC, U1BCNIC XXXXX006b 0044bn Timer B5 Interrupt Control Register SIC, INTSIC XX00X00b 0044bn SIC3 Interrupt Control Register SIC, INTSIC XX00X00b 0044bn MAND Interrupt Control Register DMIIC XXXXX00b 0044bn MART 2 bas Collision Register SIRIC XXXXX00b 0045bn UART2 bas collision Register SIRIC XXXXX00b 0055bn <				
0044h INT3 Interrupt Control Register INT3IC XXXX000b 0045h Timer B5 Interrupt Control Register TBUS Control Register XXXX000b 0046h Timer B5 Interrupt Control Register, UNRT IBUS Collision Detection Interrupt Control Register TBUC, UBECNIC XXXXX000b 0048h SIGA Interrupt Control Register, INT5 Interrupt Control Register SIG, INT4IC XXXX000b 0048h SIGA Interrupt Control Register, INT5 Interrupt Control Register SIG, INT4IC XXXXX00b 0048h DIAMI Interrupt Control Register DIMIC XXXXX00b 0048h DIAMI Interrupt Control Register DIMIC XXXXX00b 0041h AAD Conversion Interrupt Control Register DIMIC XXXXX00b 0041h AAD Conversion Interrupt Control Register SITIC XXXXX00b 0041h AAD Conversion Interrupt Control Register SITIC XXXXX00b 0051h LARTO Transmit Interrupt Control Register SITIC XXXXX00b 0051h LARTO Transmit Interrupt Control Register SITIC XXXXX00b 0055h Timer A0 Interrupt Control Register TAIC XXXXX00b				
0048h Timer B5 Interrupt Control Register TBSIC XXXXX000b 0048h Timer B5 Interrupt Control Register TB4IC, U1BCNIC XXXXX000b 0047h Timer B5 Interrupt Control Register, UNRT BUS Collision Detection Interrupt Control Register SIC, UNBCNIC XXXXX000b 0048h SIC/04 Interrupt Control Register, INT4 Interrupt Control Register SIC, INT4IC XXXXX00b 0048h SIC/03 Interrupt Control Register DM0IC XXXXX00b 0048h UARVI Interrupt Control Register DM0IC XXXXX00b 0048h UARVI Interrupt Control Register DM0IC XXXXX00b 0048h UARVI Interrupt Control Register DM0IC XXXXX00b 0047h UARVI Transmit Interrupt Control Register DM0IC XXXXX00b 0058h UARVI Transmit Interrupt Control Register SVIIC XXXXX00b 0058h UARVI Transmit Interrupt Control Register SVIIC XXXXX00b 0058h UARVI Transmit Interrupt Control Register TAIC XXXXX00b 0058h Timer A1 Interrupt Control Register TAIC XXXXX00b 0058h Time		INT3 Interrupt Control Register	INT3IC	XX00X000b
0046h Timer P4 Interrupt Control Register, INTS Interrupt Control Register TEAIC, UTBCNIC XXXXX000b 0047h Timer P3 Interrupt Control Register, INTS Interrupt Control Register SIG:, INT4IC XX00X000b 0048h SI/O-4 Interrupt Control Register, INTS Interrupt Control Register SIG:, INT4IC XX00X000b 0048h DIANT Interrupt Control Register, INTS Interrupt Control Register BCNIC XXXXX000b 0048h DIANT Interrupt Control Register DMIC XXXXX000b 0048h DIANT Interrupt Control Register DMIC XXXXX000b 0047h MART Interrupt Control Register DMIC XXXXX00b 0048h DMART Interrupt Control Register DMIC XXXXX00b 0047h DART Interrupt Control Register ADIC XXXXX00b 0047h DART I transmit Interrupt Control Register SIRC XXXXX00b 0047h UART I transmit Interrupt Control Register SIRC XXXXX00b 0058h Timer AD Interrupt Control Register SIRC XXXXX00b 0058h Timer AD Interrupt Control Register TAIC XXXXX00b 0058h </td <td></td> <td></td> <td></td> <td></td>				
11mmer B3 Interrupt Control Register, UARTO BUS Collision Detection Interrupt Control Register TB31C, UDBCNIC XXXXX000b 0049h SI/C3 Interrupt Control Register, INT4 Interrupt Control Register S3/C, INT4IC XX00X00b 0049h SI/C3 Interrupt Control Register, INT4 Interrupt Control Register BCNIC XXXXX000b 0044h UART2 Bus Collision Detection Interrupt Control Register DMIC XXXXX00b 0044b MART Interrupt Control Register DMIC XXXXX00b 0044b KAP Interrupt Control Register DMIC XXXXX00b 0044b KAP Interrupt Control Register DMIC XXXXX00b 0044b KAP Conversion Interrupt Control Register SZIIC XXXXX00b 0044b VART2 Transmit Interrupt Control Register SZIIC XXXXX00b 0054b UART1 Transmit Interrupt Control Register STIIC XXXXX00b 0054b UART1 Transmit Interrupt Control Register STIC XXXXX00b 0055h Umer An Interrupt Control Register TAIC XXXX00b 0056h Timer An Interrupt Control Register TAIC XXXXX00b 0056h				
0048h SUC4 Interrupt Control Register, INT5 Interrupt Control Register S4IC; INT3IC XX00X000b 0044h UART 2 bus; Collision Detection Interrupt Control Register BCNIC XXXXX000b 0044b UART 2 bus; Collision Detection Interrupt Control Register DMOIC XXXXX000b 0044b MAN 1 Interrupt Control Register DMOIC XXXXX000b 0044b MAN 1 Interrupt Control Register DMIC XXXXX000b 0044b MAN 1 Interrupt Control Register DMIC XXXXX000b 0044b MAT 1 famory 1 Control Register Conversion Interrupt Control Register ADIC XXXXX00b 0044b ADIC Conversion Interrupt Control Register SDIC XXXXX00b XXXXX00b 0055h UART 1 maxmit Interrupt Control Register SDIC XXXXX00b XXXXX00b 0055h UART 1 maxmit Interrupt Control Register SORC XXXXX00b XXXXX00b 0055h UART 1 maxmit Interrupt Control Register TAIC XXXXX00b XXXXX00b 0055h Timer AD Interrupt Control Register TAIC XXXXX00b XXXXX00b XXXXX00b XXXXX00b				
004Ab UX03 Interrupt Control Register S3(C, INT4I XX00X000b 004Ab UX12 Bus Collision Detection Interrupt Control Register DMIC XXXXX000b 004Ab DMA1 Interrupt Control Register DMIC XXXXX00b 004Ab MA1 Interrupt Control Register DMIC XXXXX00b 004Ab MA1 Interrupt Control Register ADIC XXXXX00b 004Ab MAY Conversion Interrupt Control Register SZIC XXXXX00b 004Ab UX4712 Transmit Interrupt Control Register SZIC XXXXX00b 005Ab UX4712 Receive Interrupt Control Register SUIC XXXXX00b 005Ab UX4717 Receive Interrupt Control Register SUIC XXXXX00b 005Ab UX4717 Receive Interrupt Control Register STIC XXXXX00b 005Ab UX4717 Receive Interrupt Control Register TAIC XXXXX00b 005Ab UX471 Receive Interrupt Control Register TAIC XXXXX00b 005Ab UX471 Receive Interrupt Control Register TAIC XXXXX00b 005Ab Timer Ab Interrupt Control Register TAIC XXXXX00b				
004Ah UAR 12 Bus Collision Detection Interrupt Control Register BCNIC XXXXX000b 004Bh DMAT Interrupt Control Register DMIC XXXXX00b 004Dh MAT Interrupt Control Register DMIC XXXXX00b 004Dh Kay Input Interrupt Control Register KUPIC XXXXX00b 004Dh Kay Input Interrupt Control Register SZIIC XXXXX00b 004Fh ADIC Conversion Interrupt Control Register SZIIC XXXXX00b 005bh UART2 Transmit Interrupt Control Register SZIIC XXXXX00b 005bh UART0 Reserve Interrupt Control Register SORIC XXXXX00b 005bh UART1 Transmit Interrupt Control Register TAIC XXXXX00b 005bh UART1 Reserve Interrupt Control Register TAIC XXXXX00b 005bh Timer AD Interrupt Control Register TAIC XXXXX00b	0049h			
004Bh DMA0 Interrupt Control Register DMIIC XXXXX000b 004Ch DMAI Interrupt Control Register DMIIC XXXXX000b 004Dh Kay Input Interrupt Control Register ADIC XXXXX000b 004Eh AD Conversion Interrupt Control Register S211C XXXXX000b 0045h UART 2 Transmit Interrupt Control Register S211C XXXXX000b 0055h UART 2 Transmit Interrupt Control Register S011C XXXXX000b 0055h UART 1 Receive Interrupt Control Register S011C XXXXX000b 0055h UART 1 Receive Interrupt Control Register S111C XXXXX000b 0055h UIRT 1 Receive Interrupt Control Register TA11C XXXX000b 0055h Timer AD Interrupt Control Register TA11C XXXX000b				
004Ch DMA1 Interrupt Control Register DMIC XXXX000b 004Dh K&UPIC XXXX000b XXXX000b 004Eh AD Conversion Interrupt Control Register ADIC XXXX000b 004Fh AD Conversion Interrupt Control Register S211C XXXX000b 005h UAR12 Reserve Interrupt Control Register S211C XXXX000b 005h UAR17 Reserve Interrupt Control Register S011C XXXX000b 005h UAR10 Reserve Interrupt Control Register S011C XXXX000b 0055h UAR11 Reserve Interrupt Control Register S111C XXXX000b 0055h UAR11 Reserve Interrupt Control Register TA01C XXXX000b 0055h Timer AD Interrupt Control Register TA01C XXXX000b 0055h Timer AD Interrupt Control Register TA11C XXXX000b 0055h Timer AD Interrupt Control Register TA21C XXXX000b 0055h Timer AD Interrupt Control Register TA21C XXXX000b 0055h Timer AD Interrupt Control Register TA21C XXXX000b 0055h </td <td>004Bh</td> <td></td> <td></td> <td></td>	004Bh			
004Dh Key Input Interrupt Control Register ADIC XXXXX000b 004Eh ADIC XXXXX000b 004Eh ADIC XXXXX000b 004Fh UART 2 Receive Interrupt Control Register S2RIC XXXXX000b 005bh UART 2 Receive Interrupt Control Register S0RIC XXXX000b 005bh UART 0 Transmit Interrupt Control Register S0RIC XXXX000b 005bh UART 1 Receive Interrupt Control Register S1RIC XXXX000b 005bh UART 1 Receive Interrupt Control Register S1RIC XXXX000b 005bh Timer AD Interrupt Control Register TA1IC XXXX000b 005bh Timer AD Interrupt Control Register TA2IC XXXX000b 005bh Timer AD Interrupt Control Register TA3IC XXXX000b 005bh Timer AD Interrupt Control Register TB1IC XXXX000b 005bh Timer AD Interrupt Control Register TA3IC XXXX000b 005bh Timer AD Interrupt Control Register TB1IC XXXX000b 005bh Timer BD Interrupt Control Register TB1I	004Ch		DM1IC	XXXXX000b
004Fh UAR12 Transmit Interrupt Control Register S2RIC XXXXX000b 0055h UAR12 Receive Interrupt Control Register S0RIC XXXXX000b 0055h UAR10 Transmit Interrupt Control Register S0RIC XXXXX000b 0055h UAR11 Transmit Interrupt Control Register S1RIC XXXXX000b 0055h UAR11 Transmit Interrupt Control Register S1RIC XXXXX000b 0055h UMR11 Receive Interrupt Control Register TA0IC XXXXX000b 0056h Timer A0 Interrupt Control Register TA0IC XXXXX000b 0056h Timer A1 Interrupt Control Register TA1IC XXXXX000b 0056h Timer A2 Interrupt Control Register TA2IC XXXXX000b 0056h Timer A1 Interrupt Control Register TA3IC XXXXX000b 0056h Timer A2 Interrupt Control Register TB1IC XXXXX000b 0056h Timer A1 Interrupt Control Register TB1IC XXXXX000b 0056h Timer B1 Interrupt Control Register TB1IC XXXXX000b 0056h Timer B1 Interrupt Control Register TB1IC XXXXX	004Dh		KUPIC	XXXXX000b
0050h UART2 Receive Interrupt Control Register SQRC XXXXX000b 0051h UART0 Transmit Interrupt Control Register SQRC XXXXX000b 0053h UART0 Transmit Interrupt Control Register STRC XXXXX000b 0053h UART1 Receive Interrupt Control Register STRC XXXXX000b 0053h UART1 Receive Interrupt Control Register TAIC XXXXX000b 0056h Timer AD Interrupt Control Register TAIC XXXXX000b 0056h Timer AD Interrupt Control Register TAIC XXXXX000b 0056h Timer AJ Interrupt Control Register TBIC XXXXX000b 0056h Timer BD Interrupt Control Register TBIC XXXXX000b 0056h Timer BD Interrupt Control Register INTIC XX0XX000b 0056h Interrupt Control Register INTIC XX0XX000b	004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
0051h UARTO Transmit Interrupt Control Register SOTIC XXXXX000b 0055h UARTO To Receive Interrupt Control Register SORIC XXXXX000b 0055h UARTI Transmit Interrupt Control Register STRIC XXXXX000b 0055h UARTI Transmit Interrupt Control Register TAIIC XXXXX000b 0055h Timer AD Interrupt Control Register TAIIC XXXXX000b 0055h Timer AJ Interrupt Control Register TAIIC XXXXX000b 0056h Timer AJ Interrupt Control Register TAIIC XXXX000b 0056h Timer BJ Interrupt Control Register TBIIC XXXX000b 0056h Timer BJ Interrupt Control Register TBIC XXXX000b 0056h Timer BJ Interrupt Control Register TBIC XXXX000b 0056h Interrupt Control Register TBIC XXXX000b <	004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0053h UARTO Receive Interrupt Control Register SORIC XXXX000b 0053h UART1 Transmit Interrupt Control Register STRIC XXXX000b 0055h UART1 Receive Interrupt Control Register TARIC XXXX000b 0055h Timer AD Interrupt Control Register TARIC XXXX000b 0055h Timer AI Interrupt Control Register TARIC XXXX000b 0056h Timer BD Interrupt Control Register TBRIC XXXX000b 0056h Timer BD Interrupt Control Register TBRIC XXXX000b 0056h Timer BD Interrupt Control Register TBRIC XXXX000b 0056h Intro Interrupt Control Register NTOIC XX0X000b 0056h Introl Interrupt Control Register INTIC X00X000b 0056h Introl Interrupt Control Register INTIC X00X000b <t< td=""><td>0050h</td><td>UART2 Receive Interrupt Control Register</td><td>S2RIC</td><td>XXXXX000b</td></t<>	0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0055h UART1 Transmit Interrupt Control Register STRIC XXXXX000b 0055h UART1 Traceswit Interrupt Control Register TA0IC XXXXX000b 0055h Timer AI Interrupt Control Register TA0IC XXXXX000b 0056h Timer AI Interrupt Control Register TA2IC XXXXX000b 0057h Timer A2 Interrupt Control Register TA3IC XXXX000b 0058h Timer A2 Interrupt Control Register TA3IC XXXX000b 0058h Timer A3 Interrupt Control Register TB0IC XXXX000b 0058h Timer B1 Interrupt Control Register TB1IC XXXX000b 0058h Timer B1 Interrupt Control Register TB1IC XXXX000b 0056h Timer B1 Interrupt Control Register TB1IC XXXX000b 0056h Timer B1 Interrupt Control Register INT0IC XX00X00b 0056h Interrupt Control Register INT0IC XX00X00b 0056h Interrupt Control Register INT0IC X00X000b 0066h Interrupt Control Register INT0IC X00X000b 0066h	0051h	UART0 Transmit Interrupt Control Register	SOTIC	XXXXX000b
0054h UART1 Receive Interupt Control Register STRIC XXXX000b 0055h Timer A0 Interupt Control Register TAIIC XXXX000b 0056h Timer A1 Interupt Control Register TAIIC XXXX000b 0057h Timer A1 Interupt Control Register TAIIC XXXX000b 0058h Timer A3 Interupt Control Register TAIIC XXXX000b 0058h Timer A3 Interupt Control Register TAIIC XXXX000b 0058h Timer A3 Interupt Control Register TBIIC XXXX000b 0058h Timer B0 Interupt Control Register TBIIC XXXX000b 0058h Timer B2 Interupt Control Register TBIIC XXXX000b 0058h Timer B2 Interupt Control Register INTIIC XX0X000b 0058h INT2 Interupt Control Register INTIIC X00X000b 0058h INT2 Interupt Control Register INTIC X00X000b 0058h INT2 Interupt Control Register INTIC X00X000b 0068h Interupt Control Register INTIC X00X000b 0068h Interupt Con	0052h	UART0 Receive Interrupt Control Register	SORIC	XXXXX000b
0055h Timer A0 Interrupt Control Register TAUC XXXXX000b 0056h Timer A1 Interrupt Control Register TAUC XXXXX000b 0057h Timer A2 Interrupt Control Register TA2C XXXXX000b 0058h Timer A2 Interrupt Control Register TA3IC XXXXX000b 0058h Timer A3 Interrupt Control Register TA3IC XXXXX00b 0058h Timer B1 Interrupt Control Register TB1IC XXXXX00b 0058h Timer B1 Interrupt Control Register TB1IC XXXXX00b 0056h Timer B1 Interrupt Control Register INT1IC XX00x00b 0056h Timer B1 Interrupt Control Register INT1IC XX00x00b 0056h INT1 Interrupt Control Register INT1IC XX00x00b 0056h INT1 Interrupt Control Register INT1IC XX00x00b 0066h INT2 Interrupt Control Register INT1IC XX00x00b 0066h INT2 Interrupt Control Register INT1IC XX00x00b 0066h INT2 Interrupt Control Register INT2 Interrupt Control Register INT1INT1	0053h			
0056h Timer A1 Interrupt Control Register TA1IC XXXXX000b 0057h Timer A2 Interrupt Control Register TA2IC XXXXX00b 0058h Timer A3 Interrupt Control Register TA3IC XXXXX00b 0058h Timer A4 Interrupt Control Register TA4IC XXXXX00b 0058h Timer A4 Interrupt Control Register TB0IC XXXXX00b 0058h Timer B0 Interrupt Control Register TB1IC XXXXX00b 0055h Timer B2 Interrupt Control Register TB1IC XXXXX00b 0055h INT0 Interrupt Control Register INT1IC XX00x00b 0055h INT1 Interrupt Control Register INT1IC XX00x00b 0056h INT2 Interrupt Control Register INT1IC XX00x00b 0056h INT2 Interrupt Control Register INT1IC XX00x00b 0066h INT2 Interrupt Control Register INT2IC XX00x00b 0066h INT2 Interrupt Control Register INT2IC XX00x00b 0066h INT2 Interrupt Control Register INT2IC XX00x00b 0066h INT2	0054h	UART1 Receive Interrupt Control Register		
0057h Timer A2 Interrupt Control Register TA2IC XXXXX000b 0058h Timer A3 Interrupt Control Register TA4IC XXXXX00b 0059h Timer A4 Interrupt Control Register TA4IC XXXXX00b 0058h Timer B0 Interrupt Control Register TB0IC XXXXX00b 0058h Timer B1 Interrupt Control Register TB1IC XXXXX00b 0055h Timer B1 Interrupt Control Register INT0 C XX00x00b 0055h INT1 Interrupt Control Register INT10 C XX00x00b 0055h INT1 Interrupt Control Register INT10 C XX00x00b 0055h INT1 Interrupt Control Register INT10 C XX00x00b 0056h INT2 Interrupt Control Register INT10 C XX00x00b 0067h INT2 Interrupt Control Register INT10 C XX00x00b 0067h INT2 Interrupt Control Register INT10 C XX00x00b 0067h INT2 Interrupt Control Register INT10 C XX00x00b 0062h INT2 Interrupt Control Register INT10 C XX00x00b 0062h <t< td=""><td>0055h</td><td></td><td></td><td></td></t<>	0055h			
1mer A3 Interrupt Control Register TA3C XXXXX000b 0059h Timer A4 Interrupt Control Register TA4IC XXXXX000b 0059h Timer B0 Interrupt Control Register TB1C XXXXX000b 0050h Timer B0 Interrupt Control Register TB2IC XXXXX000b 0050h Timer B1 Interrupt Control Register TB2IC XXXXX000b 0050h INT0 Interrupt Control Register TB1C XXXXX00b 0050h INT1 Interrupt Control Register INT2IC XXXX000b 0051h INT1 Interrupt Control Register INT2IC XX0000b 0052h INT2 Interrupt Control Register INT2IC XX0000b 0053h INT2 Interrupt Control Register INT2IC XX0000b 0064h INT2 Interrupt Control Register INT2IC XX0000b 0065h INT2 Interrupt Control Register	0056h			
Differ Timer AI Interrupt Control Register TAIC XXXXX00b 005Ah Timer B0 Interrupt Control Register TB0C XXXXX00b 005Bh Timer B1 Interrupt Control Register TB1C XXXXX00b 005Ch Timer B1 Interrupt Control Register INT0IC XXXX000b 005Ch Timer B1 Interrupt Control Register INT0IC XXX000b 005Ch INT1 Interrupt Control Register INT1C XX0000b 005Fh INT2 Interrupt Control Register INT1C XX0000b 005Fh INT2 Interrupt Control Register INT1C XX0000b 0066h INT2 Interrupt Control Register INT1C XX0000b 0066h INT2 Interrupt Control Register INT1C XX0000b 0066h INT2 Interrupt Control Registe	0057h		-	
005Ah Timer B0 Interrupt Control Register TB0IC XXXXX000b 005Bh Timer B1 Interrupt Control Register TB1IC XXXXX000b 005Ch Timer B2 Interrupt Control Register TB2IC XXXXX000b 005Bh INT0 Interrupt Control Register INT0IC XX0X000b 005Fh INT1 Interrupt Control Register INT1IC XX0X000b 005Fh INT1 Interrupt Control Register INT2IC XX00X00b 0067h INT2 Interrupt Control Register INT2IC XX00X00b 0067h INT2 Interrupt Control Register INT2IC XX00X00b 0067h INT2 Interrupt Control Register INT2IC XX00X00b 0068h INT2IC INT2IC XX00X00b 0068h INT2IC INT2IC INT2IC 0068h INT2IC INT2IC INT2IC </td <td></td> <td></td> <td></td> <td></td>				
11mer B1 Interrupt Control Register TB1C XXXX000b 005Ch Timer B2 Interrupt Control Register TB2IC XXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Fh INT1 Interrupt Control Register INT1IC XX00X000b 005Fh INT1 Interrupt Control Register INT1IC XX00X000b 005Fh INT2 Interrupt Control Register INT2IC X00X000b 0060h 0062h 0063h 0065h 0065h				
1mmer B2 Interrupt Control Register TB2IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X00b 005Fh INT1 Interrupt Control Register INT1IC XX00X00b 005Fh INT1 Interrupt Control Register INT1IC XX00X00b 005Fh INT2 Interrupt Control Register INT2IC XX00X00b 0060h INT2 Interrupt Control Register INT2IC XX00X00b 0061h INT2IC XX00X00b INT2IC XX00X00b 0061h INT2IC XX00X00b INT2IC <				
NTO Interrupt Control Register INTOIC XX00X000b 005Fh INT1 Interrupt Control Register INT1IC XX00X000b 0060h INT2 Interrupt Control Register INT2IC XX00X000b 0060h INT2 Interrupt Control Register INT2IC XX00X00b 0061h INT2 Interrupt Control Register INT2IC XX00X00b 0062h INT2 Interrupt Control Register INT2IC XX00X00b 0063h INT2 Interrupt Control Register INT2 Interrupt Control Register Interrupt Control Register 0064h Interrupt Control Register Interrupt Control Register Interrupt Control Register 0065h Interrupt Control Register Interrupt Control Register Interrupt Control Register 0066h Interrupt Control Register Interrupt Control Register Interrupt Control Register 0066h Interrupt Control Register In				
INT1 Interrupt Control Register INT1IC XX00X000b 005Fh INT2 Interrupt Control Register INT2IC XX00X000b 0060h INT2 XX00X000b INT2IC XX00X000b 0061h INT2 INT2IC XX00X000b 0061h INT2 INT2IC XX00X000b 0061h INT2 INT2IC XX00X000b 0063h INT2 INT2IC INT2IC 0063h INT2 INT2IC INT2IC 0063h INT2 INT2IC INT2IC 0063h INT2 INT2IC INT2IC 0065h INT2 INT2IC INT2IC 0065h INT2 INT2IC INT2IC 0066h INT2 INT2IC INT2IC 0067h INT2 INT2IC INT2IC INT2IC 0066h INT2 INT2IC INT2IC INT2IC 0066h INT2 INT2IC INT2IC INT2IC 0066h INT2 INT2IC INT2IC				
005Fh INT2 Interrupt Control Register INT2IC XX00X00b 0060h				
0000h				
0061h Image: Constraint of the second s		IN12 Interrupt Control Register	INT2IC	XX00X000b
0062h 0063h 0064h 0065h 0066h 0067h 0068h 0078h				
0063h 0064h 0066h 0066h 0067h 0068h 0067h 0068h 0068h 0068h 0068h 0068h				
0064hIntersectionIntersection0065hIntersectionIntersection0067hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0068hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hIntersectionIntersection0078hI				
0065h				
0066h				
0067h 0068h 0069h 006Ah 006Bh 006Ch 006Dh 006Eh 006Eh 006Fh 007h 007h 007th <				
0068h 0069h 006Ah 006Bh 006Ch 006Eh 006Fh 006Fh 006Fh 006Fh 007h 007h <td></td> <td></td> <td></td> <td></td>				
0069h 006Ah 006Bh 006Ch 006Eh 006Fh 006Fh 006Th 006Th 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0078h				
006Ah 006Bh 006Ch 006Dh 006Eh 006Fh 0070h 0071h 0072h 0073h 0073h 0073h 0075h 0076h 0075h 0076h 0077h 0078h 0078h 0078h 0078h 007Bh 007Ch 007Eh				
006Bh 006Ch 006Dh 006Eh 006Fh 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0078h 0070h <td></td> <td></td> <td></td> <td></td>				
006Ch 006Dh 006Eh 006Fh 0070h 0071h 0072h 0073h 0074h 0074h 0074h 0074h 0074h 0074h 0074h 0074h 0074h 0075h 0076h 0078h 0078h 0078h 0078h 0078h 0078h 0070h				
006Dh 006Eh 006Fh 0070h 0071h 0072h 0073h 0073h 0073h 0073h 0073h 0074h 0075h 0076h 0077h 0078h 0078h 0078h 0078h 0078h 0078h 0078h 0078h 0070h 0070h 007Dh			+	+
006Eh 006Fh 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0077h 0076h 0077h 0078h 0079h 0078h 0078h 0078h 0078h 0078h 0077h 0078h 0077h 0078h 0079h 0072h 0075h 0072h 0075h 007Dh 007Eh				
006Fh 0070h 0071h 0072h 0073h 0074h 0075h 0075h 0076h 0077h 0078h 0077h 0078h 0078h 0078h 0078h 0070h 0072h	006Eh			1
0070h	006Fh		1	1
0071h 0072h 0073h 0074h 0075h 0076h 0077h 0078h 0077h 0078h 0078h 0078h 0078h 0078h 0078h 0078h 0078h 007Bh 007Dh 007Dh 007Eh	0070h		1	1
0072h	0071h		1	1
0074h	0072h			1
0075h	0073h			1
0076h 0077h 0078h 0079h 007Ah 007Ah 007Bh 007Ch 007Ch 007Ch 007Ch 007Ch 007Ch 007Eh	0074h			1
0077h	0075h		1	
0078h	0076h		1	
0079h 007Ah	0077h			
007Ah 007Bh 007Bh 007Ch 007Dh 007Dh 007Eh	0078h			
007Bh 007Ch 007Dh 007Ch 007Dh 007Ch 007Ch 007Dh 007Ch	0079h			
007Ch 007Dh 007Eh 007Eh	007Ah			
007Dh 007Eh 007Eh	007Bh			
007Eh	007Ch			
007Fh				
	007Fh			

Table 4.2	SFR Information	(2) ⁽¹⁾
Table 4.2	SFR Information	(2) (1)

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

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X : Nothing is mapped to this bit

REJ09B0185-0241

Address	Register	Symbol	After Reset
0080h	····g.····		
0081h			
0082h			
0083h			
0083h			
0085h			
0086h			
0087h			
to			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h			
01B4h	Flash Identification Register (2)	FIDR	XXXXXX00b
01B5h	Flash Memory Control Register 1 (2)	FMR1	0X00XX0Xb
01B6h			
01B7h	Flash Memory Control Register 0 ⁽²⁾	FMR0	0000001b
01B8h	Address Match Interrupt Register 2	RMAD2	00h
01B9h	· ~		00h
01BAh			XXh
01BBh	Address Match Interrupt Enable Register 2	AIER2	XXXXXX00b
01BCh	Address Match Interrupt Register 3	RMAD3	00h
01BDh			00h
01BEh			XXh
01C0h			2211
to			
024Fh			
024FN 0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral Clock Select Register	PCLKR	00000011b
025Fh			
0260h			
to			1
032Fh			1
0330h			1
0331h			
0332h			1
0333h			l
0334h			l
0335h		+	
0335h 0336h		+	
0337h			
0338h			
0339h			
033Ah			ļ
033Bh			
033Ch			
033Dh			
033Eh			
033Fh			
	•		•

Table 4.3 SFR Information (3) (1)

NOTES:

The blank areas are reserved and cannot be accessed by users.
 This register is included in the flash memory version.

X : Nothing is mapped to this bit

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After De

Address	Register	Symbol	After Reset
0340h	Timer B3, 4, 5 Count Start Flag	TBSR	000XXXXXb
0341h			
0342h	Timer A1-1 Register	TA11	XXh
0343h			XXh
0344h	Timer A2-1 Register	TA21	XXh
	Timer Az-T Register	TAZT	
0345h			XXh
0346h	Timer A4-1 Register	TA41	XXh
0347h			XXh
0348h	Three-Phase PWM Control Register 0	INVC0	00h
0349h	Three-Phase PWM Control Register 1	INVC1	00h
034Ah	Three-Phase Output Buffer Register 0	IDB0	00h
034Bh	Three-Phase Output Buffer Register 1	IDB1	00h
034Ch	Dead Time Timer	DTT	XXh
034Dh		ICTB2	XXh
	Timer B2 Interrupt Occurrence Frequency Set Counter	IC I BZ	~~!!
034Eh			
034Fh			
0350h	Timer B3 Register	TB3	XXh
0351h			XXh
0352h	Timer B4 Register	TB4	XXh
0353h			XXh
0354h	Timer B5 Register	TB5	XXh
0355h			XXh
			~~!!
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh	Timer B3 Mode Register	TB3MR	00XX0000b
035Ch	Timer B4 Mode Register	TB4MR	00XX0000b
035Dh	Timer B5 Mode Register	TB5MR	00XX0000b
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0361h			
0362h	SI/O3 Control Register	S3C	0100000b
0363h	SI/O3 Bit Rate Generator	S3BRG	XXh
0364h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0365h	5		
0366h	SI/O4 Control Register	S4C	0100000b
0367h	SI/O4 Bit Rate Generator	S4BRG	XXh
0368h	SI/O4 DIL IVALE GENERALDI	34BI(0	2211
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UARTO Special Mode Register 2	U0SMR2	X000000b
036Fh	UARTO Special Mode Register	U0SMR	X000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0370h	UART1 Special Mode Register 3	U1SMR3	
			000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X000000b
0373h	UART1 Special Mode Register	U1SMR	X000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
		U LA BLUE A	X000000b
0376h	UART2 Special Mode Register 2	U2SMR2	70000000
	UART2 Special Mode Register 2 UART2 Special Mode Register		
0377h	UART2 Special Mode Register	U2SMR	X000000b
0377h 0378h	UART2 Special Mode Register UART2 Transmit/Receive Mode Register	U2SMR U2MR	X000000b 00h
0377h 0378h 0379h	UART2 Special Mode Register UART2 Transmit/Receive Mode Register UART2 Bit Rate Generator	U2SMR U2MR U2BRG	X0000000b 00h XXh
0377h 0378h 0379h 037Ah	UART2 Special Mode Register UART2 Transmit/Receive Mode Register	U2SMR U2MR	X0000000b 00h XXh XXh
0377h 0378h 0379h 037Ah 037Bh	UART2 Special Mode Register UART2 Transmit/Receive Mode Register UART2 Bit Rate Generator UART2 Transmit Buffer Register	U2SMR U2MR U2BRG U2TB	X0000000b 00h XXh XXh XXh XXh XXh
0377h 0378h 0379h 037Ah 037Bh 037Ch	UART2 Special Mode Register UART2 Transmit/Receive Mode Register UART2 Bit Rate Generator UART2 Transmit Buffer Register UART2 Transmit/Receive Control Register 0	U2SMR U2MR U2BRG U2TB U2C0	X0000000b 00h XXh XXh XXh XXh 00001000b
0377h 0378h 0379h 037Ah 037Bh	UART2 Special Mode Register UART2 Transmit/Receive Mode Register UART2 Bit Rate Generator UART2 Transmit Buffer Register	U2SMR U2MR U2BRG U2TB	X0000000b 00h XXh XXh XXh XXh XXh
0377h 0378h 0379h 037Ah 037Bh 037Ch	UART2 Special Mode Register UART2 Transmit/Receive Mode Register UART2 Bit Rate Generator UART2 Transmit Buffer Register UART2 Transmit/Receive Control Register 0	U2SMR U2MR U2BRG U2TB U2C0	X0000000b 00h XXh XXh XXh XXh 00001000b

Table 4.4SFR Information (4) (1)

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

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Address		Symbol	After Reset
0380h	Count Start Flag	TABSR	00h
0381h	Clock Prescaler Reset Fag	CPSRF	0XXXXXXb
0382h	One-Shot Start Flag	ONSF	00h
0383h	Trigger Select Register	TRGSR	00h
0384h	Up-Down Flag	UDF	00h ⁽²⁾
0385h		051	CON CONTRACT
0386h	Timer A0 Register	TAO	XXh
0387h	Timer Au Register	140	
	Times A4 Deviator	T 6.4	XXh
0388h	Timer A1 Register	TA1	XXh
0389h			XXh
038Ah	Timer A2 Register	TA2	XXh
038Bh			XXh
038Ch	Timer A3 Register	TA3	XXh
038Dh	-		XXh
038Eh	Timer A4 Register	TA4	XXh
038Fh	- °		XXh
0390h	Timer B0 Register	TB0	XXh
0391h		180	XXh
0392h	Timor P1 Pogistor	TB1	XXh
	Timer B1 Register	IDI	
0393h	Times Do Devictor	750	XXh
0394h	Timer B2 Register	TB2	XXh
0395h			XXh
0396h	Timer A0 Mode Register	TAOMR	00h
0397h	Timer A1 Mode Register	TA1MR	00h
0398h	Timer A2 Mode Register	TA2MR	00h
0399h	Timer A3 Mode Register	TA3MR	00h
039Ah	Timer A4 Mode Register	TA4MR	00h
039Bh	Timer B0 Mode Register	TBOMR	00XX0000b
039Ch	9	TB1MR	00XX0000b
	Timer B1 Mode Register		
039Dh	Timer B2 Mode Register	TB2MR	00XX0000b
039Eh	Timer B2 Special Mode Register	TB2SC	XXXXXX00b
039Fh			
03A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
03A1h	UART0 Bit Rate Generator	U0BRG	XXh
03A2h	UART0 Transmit Buffer Register	U0TB	XXh
03A3h	, i i i i i i i i i i i i i i i i i i i		XXh
03A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
03A5h	UART0 Transmit/Receive Control Register 1	U0C1	00XX0010b
03A6h	UARTO Receive Buffer Register	UORB	XXh
03A01	OARTO Receive Buller Register	OURB	XXh
03A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
03A9h	UART1 Bit Rate Generator	U1BRG	XXh
03AAh	UART1 Transmit Buffer Register	U1TB	XXh
03ABh			XXh
03ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
03ADh	UART1 Transmit/Receive Control Register 1	U1C1	00XX0010b
03AEh	UART1 Receive Buffer Register	U1RB	XXh
03AFh		0.1.2	XXh
03B0h	LIAPT Transmit/Pagaina Control Pagistor 2	UCON	X000000b
03B0h	UART Transmit/Receive Control Register 2		20000000
03B2h			
03B3h			
03B3h			
03B4h			
03B4h 03B5h 03B6h			
03B4h 03B5h 03B6h 03B7h	DMA0 Request Eactor Select Register	DMOSI	00b
03B4h 03B5h 03B6h 03B7h 03B8h	DMA0 Request Factor Select Register	DM0SL	00h
03B4h 03B5h 03B6h 03B7h 03B8h 03B9h			
03B4h 03B5h 03B6h 03B7h 03B8h 03B9h 03BAh	DMA0 Request Factor Select Register DMA1 Request Factor Select Register	DM0SL DM1SL	00h 00h
03B4h 03B5h 03B6h 03B7h 03B8h 03B9h 03BAh 03BBh	DMA1 Request Factor Select Register	DM1SL	00h
03B4h 03B5h 03B6h 03B7h 03B8h 03B9h 03BAh 03BBh 03BCh			00h XXh
03B4h 03B5h 03B6h 03B7h 03B8h 03B9h 03BAh 03BBh	DMA1 Request Factor Select Register	DM1SL	00h
03B4h 03B5h 03B6h 03B7h 03B8h 03B9h 03BAh 03BBh 03BCh	DMA1 Request Factor Select Register	DM1SL	00h XXh

Table 4.5 SFR Information (5) ⁽¹⁾

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. Bit 5 in the Up-down flag is "0" by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

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Address		Symbol	After Reset
03C0h	A/D Register 0	AD0	XXh
03C1h			XXh
)3C2h	A/D Register 1	AD1	XXh
)3C3h			XXh
)3C4h	A/D Register 2	AD2	XXh
)3C5h			XXh
)3C6h	A/D Register 3	AD3	XXh
)3C7h			XXh
)3C8h	A/D Register 4	AD4	XXh
)3C9h			XXh
)3CAh	A/D Register 5	AD5	XXh
)3CBh			XXh
)3CCh	A/D Register 6	AD6	XXh
)3CDh			XXh
)3CEh	A/D Register 7	AD7	XXh
)3CFh			XXh
)3D0h			
3D1h			
3D2h			
)3D3h			
3D4h	A/D Control Register 2	ADCON2	00h
3D5h			
)3D6h	A/D Control Register 0	ADCON0	00000XXXb
03D7h	A/D Control Register 1	ADCON1	00000000000000000000000000000000000000
03D8h	D/A Register 0	DAO	00h
03D9h	DIA Register 0	BAO	0011
D3D9h D3DAh	D/A Register 1	DA1	00h
D3DBh	DIA Register 1	DAT	0011
03DCh	D/A Control Register	DACON	00h
)3DDh	D/A Control Register	DACON	001
	Port P14 Control Register ⁽³⁾	PC14	YYOOYYYYk
D3DEh		PUR3	XX00XXXXb 00h
03DFh	Pull-Up Control Register 3 ⁽³⁾		
D3E0h	Port P0 Register	PO	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
)3EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
)3EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
)3F1h	Port P9 Register	P9	XXh
)3F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register ⁽³⁾	P11	XXh
3F6h	Port P10 Direction Register	PD10	00h
3F7h	Port P11 Direction Register ⁽³⁾	PD11	00h
)3F8h	Port P12 Register ⁽³⁾	P12	XXh
3F9h	Port P13 Register ⁽³⁾	P13	XXh
03FAh	Port P12 Direction Register ⁽³⁾	PD12	00h
03FBh	Port P13 Direction Register ⁽³⁾	PD12	00h
03FCh	Pull-Up Control Register 0	PUR0	00h
03FDh	Pull-Up Control Register 1	PUR1	0000000b (2)
			00000000 (2) 00000010b (2)
03FEh	Pull-Up Control Register 2	PUR2	000000100 (=)

SFR Information (6) ⁽¹⁾ Table 4.6

NOTES:

The blank areas are reserved and cannot be accessed by users.
 At hardware reset 1 or hardware reset 2, the register is as follows:

 "00000000b" where "L" is inputted to the CNVSS pin
 "00000010b" where "H" is inputted to the CNVSS pin

At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:

• "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).

• "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).

3. These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).

X : Nothing is mapped to this bit

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5. Reset

Hardware reset 1, brown-out detection reset (hardware reset 2), software reset, watchdog timer reset and oscillation stop detection reset are available to reset the microcomputer.

5.1 Hardware Reset 1

The microcomputer resets pins, the CPU and SFR by setting the $\overline{\text{RESET}}$ pin. If the supply voltage meets the recommended operating conditions, the microcomputer resets all pins when an "L" signal is applied to the $\overline{\text{RESET}}$ pin (see **Table 5.1 Pin Status When RESET Pin Level is "L**"). The oscillation circuit is also reset and the main clock starts oscillation. The microcomputer resets the CPU and SFR when the signal applied to the $\overline{\text{RESET}}$ pin changes low ("L") to high ("H"). The microcomputer executes the program in an address indicated by the reset vector. The internal RAM is not reset. When an "L" signal is applied to the $\overline{\text{RESET}}$ pin while writing data to the internal RAM, the internal RAM is in an indeterminate state.

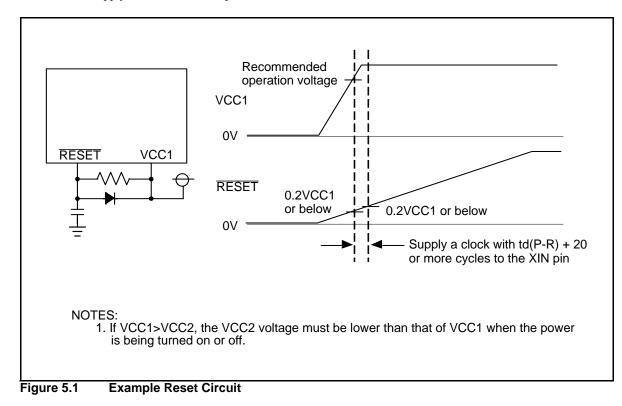
Figure 5.1 shows an Example Reset Circuit. Figure 5.2 shows a Reset Sequence. Table 5.1 lists Pin Status When RESET Pin Level is "L". Figure 5.3 shows CPU Register Status After Reset. Refer to 4. Special Function Register (SFR) for SFR states after reset.

5.1.1 Reset on a Stable Supply Voltage

- (1) Apply "L" to the $\overline{\text{RESET}}$ pin
- (2) Apply 20 or more clock cycles to the XIN pin
- (3) Apply an "H" signal to the $\overline{\text{RESET}}$ pin

5.1.2 Power-on Reset

- (1) Apply "L" to the $\overline{\text{RESET}}$ pin
- (2) Raise the supply voltage to the recommended operating level
- (3) Insert td(P-R) ms as wait time for the internal voltage to stabilize
- (4) Apply 20 or more clock cycles to the XIN pin
- (5) Apply "H" to the $\overline{\text{RESET}}$ pin



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(IN td(P-R) 20 cycles are needed	1 100000000000000000000000000000000000	10000000C
Microprocessor mode BYTE = H		
RESET	BCLK 28cycles	
BCLK	\	Content of reșet vector
Address	C	FFFFCh / FFFFDh / FFFFEh /
RD		
WR		
CSO		
Microprocessor mode BYTE = L		Content of reset vector
Address	C	FFFFCh / FFFFEh / /
RD		
WR		
CS0		
Single chip mode	F	FFFCh Content of reset vector
Address		✓ FFFFEh / / / / / / / / / / / / / / / / / / /

Figure 5.2 Reset Sequence

Pin Name		Status	
	CNVSS = VSS	CNVSS =	= VCC1 ⁽¹⁾
	CNV35 = V35	BYTE = VSS	BYTE = VCC1
P0	Input port	Data input	Data input
P1	Input port	Data input	Input port
P2, P3, P4_0 to P4_3	Input port	Address output (underfined)	Address output (underfined)
P4_4	Input port	CS0 output ("H" is output)	CS0 output ("H" is output)
P4_5 to P4_7	Input port	Input port (Pulled high)	Input port (Pulled high)
P5_0	Input port	WR output ("H" is output)	WR output ("H" is output)
P5_1	Input port	BHE output (undefined)	BHE output (undefined)
P5_2	Input port	RD output ("H" is output)	RD output ("H" is output)
P5_3	Input port	BCLK output	BCLK output
P5_4	Input port	HLDA output (The output value	HLDA output (The output value
		depends on the input to the HOLD pin)	depends on the input to the HOLD pin)
P5_5	Input port	HOLD input	HOLD input
P5_6	Input port	ALE output ("L" is output)	ALE output ("L" is output)
P5_7	Input port	RDY input	RDY input
P6, P7, P8_0 to P8_4, P8_6, P8_7, P9, P10	Input port	Input port	Input port
P11, P12, P13, P14_0, P14_1 ⁽²⁾	Input port	Input port	Input port

Table 5.1 Pin Status When RESET Pin Level is "L"

NOTES:

1. Shown here is the valid pin state when the internal power supply voltage has stabilized after power on.

When CNVSS = VCC1, the pin state is indeterminate until the internal power supply voltage stabilizes.

2. P11, P12, P13, P14_0, P14_1 pins exist in 128-pin version.

5.2 Brown-out Detection Reset (Hardware Reset 2)

The microcomputer resets pins, the CPU or SFR by setting the built-in voltage detect circuit. The voltage detect circuit monitors the voltage applied to the VCC1 pin.

When the VC26 bit in the VCR2 register is set to "1" (reset level detect circuit enabled), the microcomputer resets pins, the CPU and SFR as soon as the voltage that is applied to the VCC1 pin drops to Vdet3 or below. The microcomputer resets pins and it is in a reset state when the voltage that is applied to the VCC1 pin is Vdet3 or below. The microcomputer resets pins, CPU and SFR with Vdet3r or above and it executes the program from the address determined by the reset vector. The microcomputer executes the program after detecting Vdet3r and waiting td(S-R) ms. The same pins and registers are reset by the hardware reset 1 and brown-out detection reset (hardware reset 2), and are also placed in the same reset state.

The microcomputer cannot exit stop mode by the brown-out detection reset (hardware reset 2).

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5.3 Software Reset

The microcomputer resets pins, the CPU and SFR when the PM03 bit in the PM0 register is set to "1" (microcomputer reset). Then the microcomputer executes the program in an address determined by the reset vector. Set the PM03 bit to "1" while the main clock is selected as the CPU clock and the main clock oscillation is stable. In the software reset, the microcomputer does not reset a part of the SFR. Refer to **4. Special Function Register (SFR)** for details.

Processor mode remains unchanged since the PM01 to PM00 bits in the PM0 register are not reset.

5.4 Watchdog Timer Reset

The microcomputer resets pins, the CPU and SFR when the CM06 bit in the CM0 register is set to "1" (reset) and the watchdog timer underflows. Then the microcomputer executes the program in an address determined by the reset vector.

In the watchdog timer reset, the microcomputer does not reset a part of the SFR. Refer to **4. Special Function Register** (**SFR**) for details. Processor mode remains unchanged since the PM01 to PM00 bits in the PM0 register are not reset.

5.5 Oscillation Stop Detection Reset

The microcomputer resets and stops pins, the CPU and SFR when the CM27 bit in the CM2 register is 0, if it detects main clock oscillation circuit stop. Refer to **10.6 Oscillation Stop and Re-oscillation Detect Function** for details.

In the oscillation stop detection reset, the microcomputer does not reset a part of the SFR. Refer to **4. Special Function Register (SFR)** for details. Processor mode remains unchanged since the PM01 to PM00 bits in the PM0 register are not reset.

5.6 Internal Space

Figure 5.3 shows CPU Register Status After Reset. Refer to **4. Special Function Register (SFR)** for SFR states after reset.

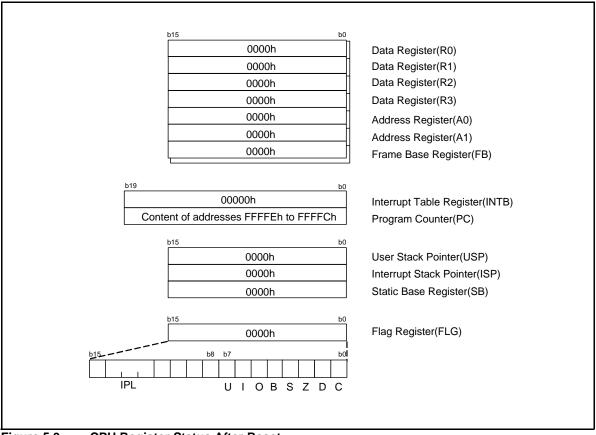


Figure 5.3 CPU Register Status After Reset

6. Voltage Detection Circuit

Note

The M16C/62PT do not use the voltage detection circuit.

However, the cold start-up/warm start-up determine function is available.

The voltage detection circuit consists of the reset level detection circuit and the low voltage detection circuit. The reset level detection circuit monitors the voltage applied to the VCC1 pin. The microcomputer is reset if the reset level detection circuit detects VCC1 is Vdet3 or below. This circuit is disabled when the microcomputer is in stop mode.

The voltage detection circuit also monitors the voltage applied to the VCC1 pin. The low voltage detection signal is generated when the low voltage detection circuit detects VCC1 is above or below Vdet4. This signal generates the low voltage detection interrupt. The VC13 bit in the VCR1 register determines whether VCC1 is above or below Vdet4. The voltage detection circuit is available when VCC1=5.0V.

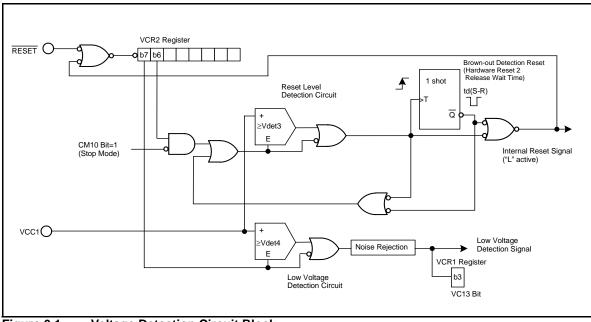
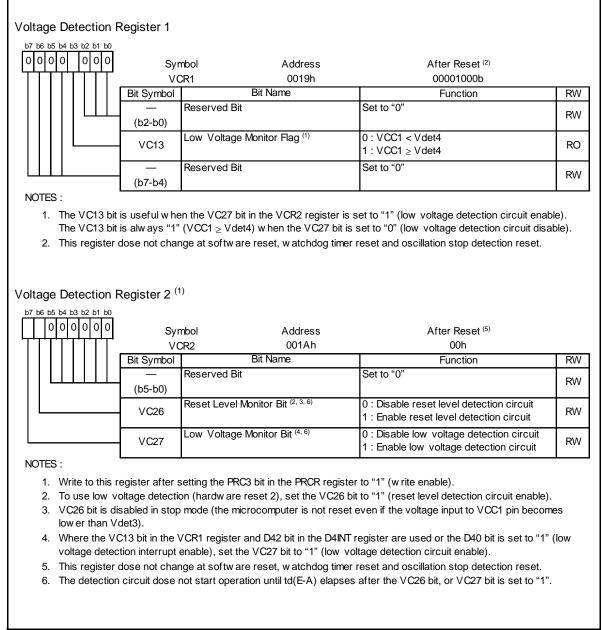
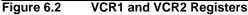


Figure 6.1 shows a Voltage Detection Circuit Block.

Figure 6.1 Voltage Detection Circuit Block





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	Symbol	Address	After Reset	
	D4INT	001Fh	00h	
	Bit Symbol	Bit Name	Function	RW
	D40	Low Voltage Detection Interrupt Enable Bit ⁽⁵⁾	0 : Disable 1 : Enable	RW
	D41	STOP Mode Deactivation Control Bit ⁽⁴⁾	 0 : Disable (do not use the Low voltage detection interrupt to get out of stop mode) 1 : Enable (use the low voltage detection interrupt to get out of stop mode) 	RW
	D42	Voltage Change Detection Flag ⁽²⁾	0 : Not detected 1 : Vdet4 passing detection	RW ⁽³⁾
	D43	WDT Overflow Detect Flag	0 : Not detected 1 : Detected	RW (3)
	DF0	Sampling Clock Select Bit	b5 b4 0 0 : CPU clock divided by 8	RW
	DF1		0 1 : CPU clock divided by 16 1 0 : CPU clock divided by 32 1 1 : CPU clock divided by 64	RW
	 (b7-b6)	Nothing is assigned. When w rite, s When read, their contents are "0".	et to "0".	-

set to "0" (low voltage detection circuit disabled), the D42 bit is set to "0" (Not detect).

3. This bit is set to "0" by writing a "0" in a program. (Writing a "1" has no effect.)

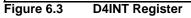
4. If the low voltage detection interrupt needs to be used to get out of stop mode again after once used for that purpose, reset the D41 bit by writing a "0" and then a "1".

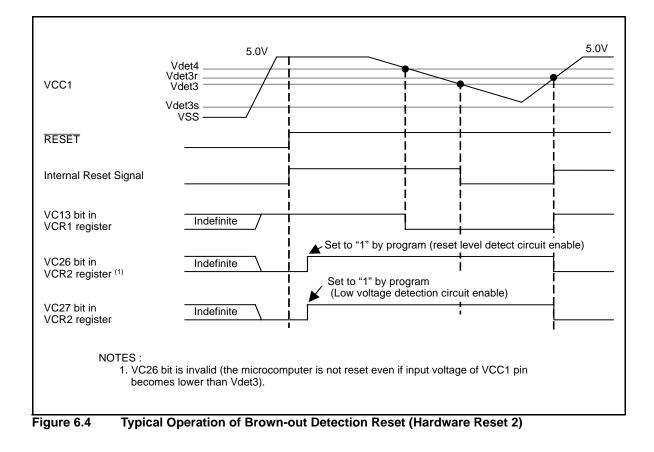
5. The D40 bit is effective when the VC27 bit = 1. To set the D40 bit to "1", set bits in the following order.

(a) Set the VC27 bit to "1".

(b) Wait for td(E-A) until the detection circuit is actuated.

- (c) Wait for the sampling time. (See Table 6.2 Sampling Period.)
- (d) Set the D40 bit to "1".





6.1 Low Voltage Detection Interrupt

If the D40 bit in the D4INT register is set to "1" (low voltage detection interrupt enabled), the low voltage detection interrupt request is generated when the voltage applied to the VCC1 pin is above or below Vdet4.

The low voltage detection interrupt shares the same interrupt vector with the watchdog timer interrupt and oscillation stop, re-oscillation detection interrupt.

Set the D41 bit in the D4INT register to "1" (enabled) to use the low voltage detection interrupt to exit stop mode. The D42 bit in the D4INT register is set to "1" as soon as the voltage applied to the VCC1 pin reaches Vdet4 due to the voltage rise and voltage drop. When the D42 bit changes "0" to "1", the low voltage detection interrupt request is generated. Set the D42 bit to "0" by program. However, when the D41 bit is set to "1" and the microcomputer is in stop mode, the low voltage detection interrupt request is generated regardless of the D42 bit state if the voltage applied to the VCC1 pin is detected to be above Vdet4. The microcomputer then exits stop mode.

 Table 6.1 shows Low Voltage Detection Interrupt Request Generation Conditions.

The DF1 to DF0 bits in the D4INT register determine the sampling period that detects the voltage applied to the VCC1 pin reaches Vdet4. Table 6.2 shows the Sampling Periods.

 Table 6.1
 Low Voltage Detection Interrupt Request Generation Conditions

Operating Mode	VC27 Bit	D40 Bit	D41 Bit	D42 Bit	CM02 Bit	VC13 Bit
Normal Operating				0 to 1		0 to 1 ⁽³⁾
Mode ⁽¹⁾			_	0.01	—	1 to 0 ⁽³⁾
	1	1		0 to 1	0	0 to 1 ⁽³⁾
Wait Mode (2)	I	I	_	0.01	0	1 to 0 ⁽³⁾
			1	-	1	0 to 1
Stop Mode ⁽²⁾			I	_	0	0 to 1

– : "0"or "1"

- 1. The status except the wait mode and stop mode is handled as the normal mode. (Refer to **10. Clock Generation Circuit**)
- 2. Refer to 6.2 Limitations on Exiting Stop Mode, 6.3 Limitations on Exiting Wait Mode.
- 3. An interrupt request for voltage reduction is generated a sampling time after the value of the VC13 bit has changed.

See the Figure 6.6 Low Voltage Detection Interrupt Generation Circuit Operation Example for details.

Table 6.2Sampling Periods

CPU Clock		Sampling	Clock (µs)	
(D4INT clock)	DF1 to DF0=00	DF1 to DF0=01	DF1 to DF0=10	DF1 to DF0=11
(MHz)	(CPU clock divided by 8)	(CPU clock divided by 16)	(CPU clock divided by 32)	(CPU clock divided by 64)
16	3.0	6.0	12.0	24.0

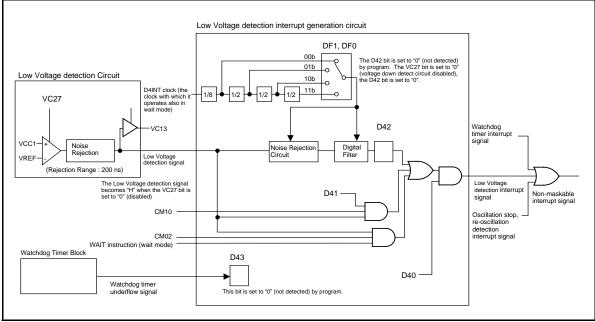
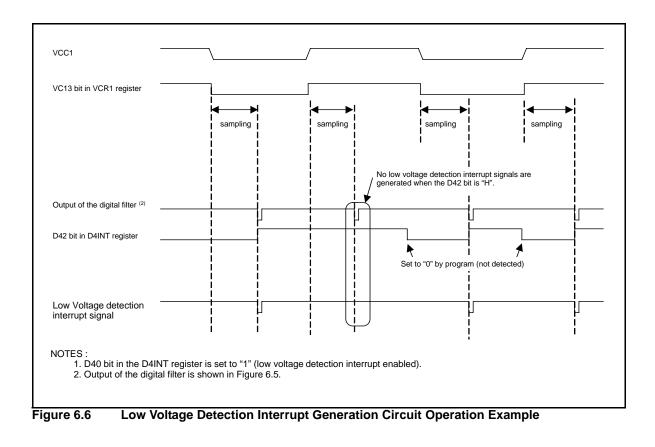


Figure 6.5 Low Voltage detection Interrupt Generation Block



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6.2 Limitations on Exiting Stop Mode

The low voltage detection interrupt is immediately generated and the microcomputer exits stop mode if the CM10 bit in the CM1 register is set to "1" under the conditions below.

- the VC27 bit in the VCR2 register is set to "1" (low voltage detection circuit enabled),
- the D40 bit in the D4INT register is set to "1" (low voltage detection interrupt enabled),
- the D41 bit in the D4INT register is set to "1" (low voltage detection interrupt is used to exit stop mode), and
- the voltage applied to the VCC1 pin is higher than Vdet4 (the VC13 bit in the VCR1 register is "1")

If the microcomputer is set to enter stop mode when the voltage applied to the VCC1 pin drops below Vdet4 and to exit stop mode when the voltage applied rises to Vdet4 or above, set the CM10 bit to "1" when VC13 bit is "0" (VCC1 < Vdet4).

6.3 Limitations on Exiting Wait Mode

(VCC1 < Vdet4).

The low voltage detection interrupt is immediately generated and the microcomputer exits wait mode If WAIT instruction is executed under the conditions below.

- the CM02 bit in the CM0 register is set to "1" (stop peripheral function clock),
- the VC27 bit in the VCR2 register is set to "1" (low voltage detection circuit enabled),
- the D40 bit in the D4INT register is set to "1" (low voltage detection interrupt enabled),
- the D41 bit in the D4INT register is set to "1" (low voltage detection interrupt is used to exit wait mode), and

• the voltage applied to the VCC1 pin is higher than Vdet4 (the VC13 bit in the VCR1 register is "1") If the microcomputer is set to enter wait mode when the voltage applied to the VCC1 pin drops below Vdet4 and to exit wait mode when the voltage applied rises to Vdet4 or above, perform WAIT instruction when VC13 bit is "0"

6.4 Cold Start-up / Warm Start-up Determine Function

As for the cold start-up/warm start-up determine function, the WDC5 flag in the WDC register determines either cold start-up (reset process) when power-on or warm start-up (reset process) when reset signal is applied during the microcomputer running.

Default value of the WDC5 bit is "0" (cold start-up) when power-on. It is set to "1" (warm start-up) by writing desired values to the WDC register. The WDC bit is not reset, regardless of a software reset or a reset operation. Figure 6.7 shows Cold Start-up/Warm Start-up Determine Function Block Diagram. Figure 6.8 shows the Cold Start-up/Warm Start-up Determine Function Example. Figure 6.9 shows WDC Register.

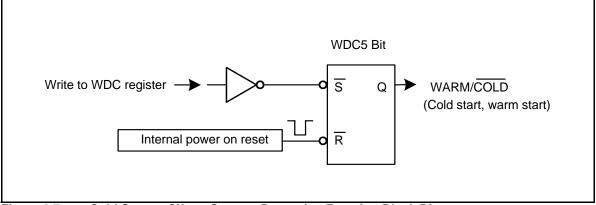
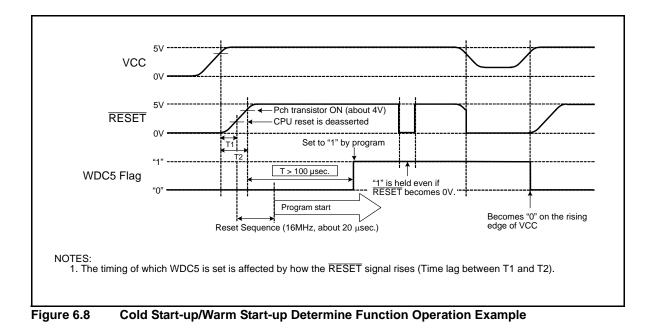


Figure 6.7 Cold Start-up/Warm Start-up Determine Function Block Diagram



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0	┰ <mark>┥┥┥┥</mark>	Symbol WDC	Address 000Fh	After Reset 00XXXXXXb ⁽²⁾	
		Bit Symbol	Bit Name	Function	R
		 (b4-b0)	High-order Bit of Watchdog Timer	+	R
		WDC5	Cold Start / Warm Start Discrimination Flag ^(1, 2)	0 : Cold Start 1 : Warm Start	R
		(b6)	Reserved Bit	Set to "0"	R
		WDC7	Prescaler Select Bit	0 : Divided by 16 1 : Divided by 128	R

Figure 6.9 WDC Register

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7. Processor Mode

Note

The M16C/62P (80-pin version) and M16C/62PT do not use memory expansion mode, and microprocessor mode.

7.1 Types of Processor Mode

Three processor modes are available to choose from: single-chip mode, memory expansion mode, and microprocessor mode. Table 7.1 shows the Features of Processor Modes.

Processor Modes	Access Space	Pins which are Assigned I/O Ports
Single-Chip Mode	SFR, Internal RAM, Internal ROM	All pins are I/O ports or peripheral function I/O pins
Memory Expansion Mode	SFR, Internal RAM, Internal ROM, External Area ⁽¹⁾	Some pins serve as bus control pins ⁽¹⁾
Microprocessor Mode	SFR, Internal RAM, External Area (1)	Some pins serve as bus control pins ⁽¹⁾

Table 7.1 Features of Processor Modes

NOTES:

1. Refer to 8. Bus.

7.2 Setting Processor Modes

Processor mode is set by using the CNVSS pin and the PM01 to PM00 bits in the PM0 register. Table 7.2 shows the Processor Mode After Hardware Reset. Table 7.3 shows the PM01 to PM00 Bits Set Values and Processor Modes.

Table 7.2Processor Mode After Hardware Reset	Table 7.2	Processor	Mode Af	ter Hardware F	Reset
--	-----------	-----------	---------	----------------	-------

CNVSS Pin Input Level	Processor Modes
VSS	Single-Chip Mode
VCC1 ^(1, 2)	Microprocessor Mode

NOTES:

- If the microcomputer is reset in hardware by applying VCC1 to the CNVSS pin (hardware reset 1 or brown-out detection reset (hardware reset 2)), the internal ROM cannot be accessed regardless of PM10 to PM00 bits.
- 2. The multiplexed bus cannot be assigned to the entire \overline{CS} space.

PM01 to PM00 Bits	Processor Modes
00b	Single-Chip Mode
01b	Memory Expansion Mode
10b	Do not set
11b	Microprocessor Mode

Table 7.3 PM01 to PM00 Bits Set Values and Processor Modes

Rewriting the PM01 to PM00 bits places the microcomputer in the corresponding processor mode regardless of whether the input level on the CNVSS pin is "H" or "L". Note, however, that the PM01 to PM00 bits cannot be rewritten to "01b" (memory expansion mode) or "11b" (microprocessor mode) at the same time the PM07 to PM02 bits are rewritten. Note also that these bits cannot be rewritten to enter microprocessor mode in the internal ROM, nor can they be rewritten to exit microprocessor mode in areas overlapping the internal ROM.

If the microcomputer is reset in hardware by applying VCC1 to the CNVSS pin (hardware reset 1 or brown-out detection reset (hardware reset 2)), the internal ROM cannot be accessed regardless of PM01 to PM00 bits. Figures 7.1 and 7.2 show the PM0 Register and PM1 Register. Figure 7.3 show the Memory Map in Single Chip

Mode.

b7 b6	ib5 b/	4 b3 b2	b1 b0	1			
				Symbol	Address	After Reset	
П		TT	ΤT	PM0	0004h	00000000b (CNVSS pin = L)	
						00000011b (CNVSS pin = H)	
				Bit Symbol	Bit Name	Function	RW
				PM00	Processor Mode Bit ⁽⁴⁾	^{b1 b0} 0 0 : Single-chip mode	RW
				- PM01		0 1 : Memory expansion mode 1 0 : Do not set 1 1 : Microprocessor mode	RW
				- PM02	R/W Mode Select Bit (2)	0 : RD, BHE, WR 1 : RD, WRH, WRL	RW
		L		- PM03	Softw are Reset Bit	Setting this bit to "1" resets the microcomputer. When read, its content is "0".	RW
				- PM04	Multiplexed Bus Space Select Bit ⁽²⁾	^{b5 b4} 0 0 : Multiplexed bus is unused (Separate bus in the entire CS space) 0 1 : Allocated to CS2 space	RW
	L			- PM05		1 0 : Allocated to CS1 space 1 1 : Allocated to the entire CS space ⁽³⁾	RW
l				PM06	Port P4_0 to P4_3 Function Select Bit ⁽²⁾	0 : Address output 1 : Port function (Address is not output)	RW
				PM07	BCLK Output Disable Bit ⁽²⁾	0 : BCLK is output 1 : BCLK is not output (Pin is left high-impedance)	RW

1. Write to this register after setting the PRC1 bit in the PRCR register to "1" (write enable).

 Effective when the PM01 to PM00 bits are set to "01b" (memory expansion mode) or "11b" (microprocessor mode).
 To set the PM01 to PM00 bits are "01b" and the PM05 to PM04 bits are "11b" (multiplexed bus assigned to the entire CS space), apply an "H" signal to the BYTE pin (external data bus is 8 bits wide). While the CNVSS pin is held "H" (= VCC1), do not rew rite the PM05 to PM04 bits to "11b" after reset. If the PM05 to PM04 bits are set to "11b" during memory expansion mode, P3_1 to P3_7 and P4_0 to P4_3 become VO ports, in w hich case the accessible area for each CS is 256 bytes.

4. The PM01 to PM00 bits do not change at softw are reset, w atchdog timer reset and oscillation stop detection reset.

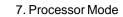
Figure 7.1 PM0 Register

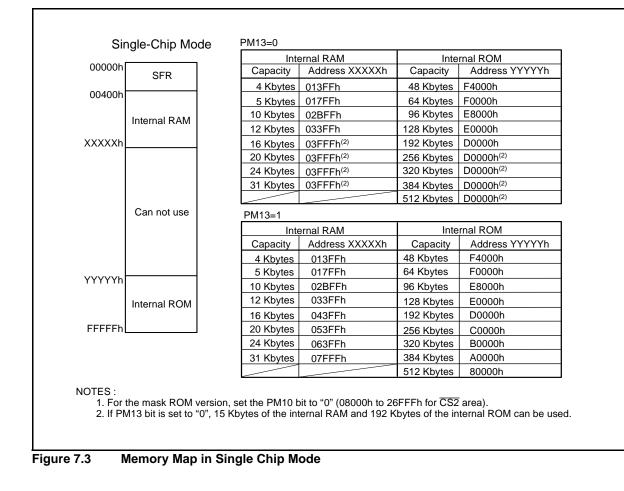
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b7 b6 b5	5 b4 b3 l	b2 b1 b0				
0			Symbol	Address	After Reset	
TTT	ΤT	TTT	PM1	0005h	0X001000b	
			Bit Symbol	Bit Name	Function	RW
		L	PM10	CS2 Area Sw itch Bit (Data Block Enable Bit) ⁽²⁾	0 : 08000h to 26FFFh (Block A disable) 1 : 10000h to 26FFFh (Block A enable)	RW
			PM11	Port P3_7 to P3_4 Function Select Bit ⁽³⁾	0 : Address output 1 : Port function	RW
			- PM12	Watchdog Timer Function Select Bit	0 : Watchdog timer interrupt 1 : Watchdog timer reset ⁽⁴⁾	RW
	L		- PM13	Internal Reserved Area Expansion Bit ⁽⁶⁾	(NOTE 7)	RW
			- PM14	Memory Area Expansion Bit ⁽³⁾	^{b5 b4} 0 0 : 1-Mbyte mode (Do not expand) 0 1 : Do not set	RW
			- PM15		1 0 : Do not set 1 1 : 4-Mbyte mode	RW
			(b6)	Reserved Bit	Set to "0".	RW
			()			
	S :		- PM17	Wait Bit ⁽⁵⁾	0 : No w ait state 1 : With w ait state (1 w ait)	RW
1. 2. 3. 4. 5.	Write Set the enable In add rew rise Effect mode PM12 Wher interr Wher (with The F	he PM dition, dition, ite mo ctive w e). 2 bit is n PM17 n al RO n PM17 n w ait s PM13 b	PM17 PM17 D bit to "0" for disabled. Whe the PM10 bit is de). hen the PM01 set to "1" by w 7 bit is set to "7 M. 7 bit is set to "7 state). bit is automatic	r setting the PRC1 bit in the PRCR regis Mask ROM version. For flash memory en the PM10 bit is set to "1", 0F000h to automatically set to "1" while the FMF to PM00 bits are set to "01b" (memory v riting a "1" in a program (w riting a "0" 1" (w ith w ait state), one w ait state is i 1" and accesses an external area, set ally set to "1" w hen the FMR01 bit in th	1 : With w ait state (1 w ait) ter to "1" (w rite enable). y version, the PM10 bit controls w hether Blk OFFFFh can be used as internal ROM area. R01 bit in the FMR0 register is set to "1" (CPU expansion mode) or "11b" (microprocesso has no effect). nserted w hen accessing the internal RAM, the CSiW bit in the CSR register (i=0 to 3) to be FMR0 register is "1" (CPU rew rite mode).	Dock A i
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1. 2. 3. 4. 5. 6. 7. Ac	Write Set th enabl In add rew ri Effec mode PM12 Wher interr (with The F The a cccess	he PM ⁴ bled or dition, rite mod ctive w e). 2 bit is n PM17 n w ait PM13 b access s Area	PM17 PM17 PM17 I0 bit to "0" for disabled. Whe the PM10 bit is de). hen the PM01 set to "1" by w 7 bit is set to "7 M. 7 bit is set to "7 state). bit is automatic s area is chang	r setting the PRC1 bit in the PRCR regis Mask ROM version. For flash memory on the PM10 bit is set to "1", 0F000h to automatically set to "1" while the FMF to PM00 bits are set to "01b" (memory vriting a "1" in a program (writing a "0" 1" (with w ait state), one w ait state is i 1" and accesses an external area, set ally set to "1" when the FMR01 bit in th ged by the PM13 bit as listed in the tab	1 : With w ait state (1 w ait) ter to "1" (w rite enable). y version, the PM10 bit controls w hether Bla OFFFFh can be used as internal ROM area. R01 bit in the FMR0 register is set to "1" (CPU expansion mode) or "11b" (microprocesso has no effect). nserted w hen accessing the internal RAM, the CSiW bit in the CSR register (i=0 to 3) to he FMR0 register is "1" (CPU rew rite mode). le below .	Dock A i
1. 2. 3. 4. 5. 6. 7. Ac	Write Set the enable In addorew rite Effect mode PM12 Wher interr Wher (with The F The a	he PM ¹ led or dition, ctive w e). 2 bit is n PM17 n v ait s PM13 b access s Area RAM	PM17 PM17 PM17 IO bit to "0" for disabled. Whe the PM10 bit is de). hen the PM01 set to "1" by w 7 bit is set to "7 bit is set to "7 state). bit is automatic s area is chang I Up to Addres	r setting the PRC1 bit in the PRCR regis Mask ROM version. For flash memory en the PM10 bit is set to "1", 0F000h to automatically set to "1" while the FMF to PM00 bits are set to "01b" (memory virting a "1" in a program (writing a "0" 1" (with wait state), one wait state is in 1" and accesses an external area, set ally set to "1" when the FMR01 bit in the ged by the PM13 bit as listed in the tab PM13=0	1 : With w ait state (1 w ait) ter to "1" (w rite enable). y version, the PM10 bit controls w hether Blk OFFFFh can be used as internal ROM area. R01 bit in the FMR0 register is set to "1" (CPU expansion mode) or "11b" (microprocesso has no effect). nserted w hen accessing the internal RAM, the CSiW bit in the CSR register (i=0 to 3) to the FMR0 register is "1" (CPU rew rite mode). le below. PM13=1	Dock A i



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8. Bus

Note

The M16C/62P (80-pin version) and M16C/62PT do not use bus control pins.

During memory expansion or microprocessor mode, some pins serve as the bus control pins to perform data input/ output to and from external devices. These bus control pins include A0 to A19, D0 to D15, $\overline{CS0}$ to $\overline{CS3}$, \overline{RD} , $\overline{WRL}/\overline{WR}$, $\overline{WRH}/\overline{BHE}$, ALE, \overline{RDY} , \overline{HOLD} , \overline{HLDA} and BCLK.

8.1 Bus Mode

The bus mode, either multiplexed or separate, can be selected using the PM05 to PM04 bits in the PM0 register. Table 8.1 shows the Difference Between a Separate Bus and Multiplexed Bus.

8.1.1 Separate Bus

In this bus mode, data and address are separate.

8.1.2 Multiplexed Bus

In this bus mode, data and address are multiplexed.

8.1.2.1 When the input level on BYTE pin is high (8-bit data bus)

D0 to D7 and A0 to A7 are multiplexed.

8.1.2.2 When the input level on BYTE pin is low (16-bit data bus)

D0 to D7 and A1 to A8 are multiplexed. D8 to D15 are not multiplexed. Do not use D8 to D15. External devices connecting to a multiplexed bus are allocated to only the even addresses of the microcomputer. Odd addresses cannot be accessed.

Pin Name ⁽¹⁾	Separate Bus	Multipl	ex Bus	
Fin Name (*)	Separate Dus	BYTE = H	BYTE = L	
P0_0 to P0_7/D0 to D7	D0 to D7	(NOTE 2)	(NOTE 2)	
P1_0 to P1_7/D8 to D15	D8 to D15	I/O Port P1_0 to P1_7	(NOTE 2)	
P2_0/A0 (/D0/-)	A0 X	X A0 X D0 X	X A0 X	
P2_1 to P2_7/A1 to A7 (/D1 to D7/D0 to D6)	A1 to A7	A1 to A7 D1 to D7	A1 to A7 D0 to D6	
P3_0/A8 (/-/D7)	X A8 X	X A8 X	A8 D7	

NOTES:

- 1. See **Table 8.6 Pin Functions for Each Processor Mode** for bus control signals other than the above. Setting Processor Modes.
- It changes with a setup of PM05 to PM04, and area to access.
 See Table 8.6 Pin Functions for Each Processor Mode for details.

8.2 Bus Control

The following describes the signals needed for accessing external devices and the functionality of software wait.

8.2.1 Address Bus

The address bus consists of 20 lines, A0 to A19. The address bus width can be chosen to be 12, 16 or 20 bits by using the PM06 bit in the PM0 register and the PM11 bit in the PM1 register. Table 8.2 shows the PM06 and PM11 Bits Set Value and Address Bus Width.

Set Value (1)	Pin Function	Address Bus Width		
PM11=1	P3_4 to P3_7	12 bits		
PM06=1	P4_0 to P4_3			
PM11=0	A12 to A15	16 bits		
PM06=1	P4_0 to P4_3			
PM11=0	A12 to A15	20 bits		
PM06=0	A16 to A19			

Table 8.2 PM06 and PM11 Bits Set Value and Address Bus Width

NOTES:

1. No values other than those shown above can be set.

When processor mode is changed from single-chip mode to memory extension mode, the address bus is indeterminate until any external area is accessed.

8.2.2 Data Bus

When input on the BYTE pin is high (data bus is 8 bits wide), 8 lines D0 to D7 comprise the data bus; when input on the BYTE pin is low(data bus is 16 bits wide), 16 lines D0 to D15 comprise the data bus. Do not change the input level on the BYTE pin while in operation.

8.2.3 Chip Select Signal

The chip select (hereafter referred to as the \overline{CSi}) signals are output from the \overline{CSi} (i = 0 to 3) pins. These pins can be chosen to function as I/O ports or as \overline{CS} by using the CSi bit in the CSR register. Figure 8.1 shows the CSR Register.

During 1-Mbyte mode, the external area can be separated into up to 4 by the $\overline{\text{CSi}}$ signal which is output from the $\overline{\text{CSi}}$ pin. During 4-Mbyte mode, $\overline{\text{CSi}}$ signal or bank number is output from the $\overline{\text{CSi}}$ pin. Refer to **9. Memory Space Expansion Function**. Figure 8.2 shows the Example of Address Bus and $\overline{\text{CSi}}$ Signal Output in 1-Mbyte mode.

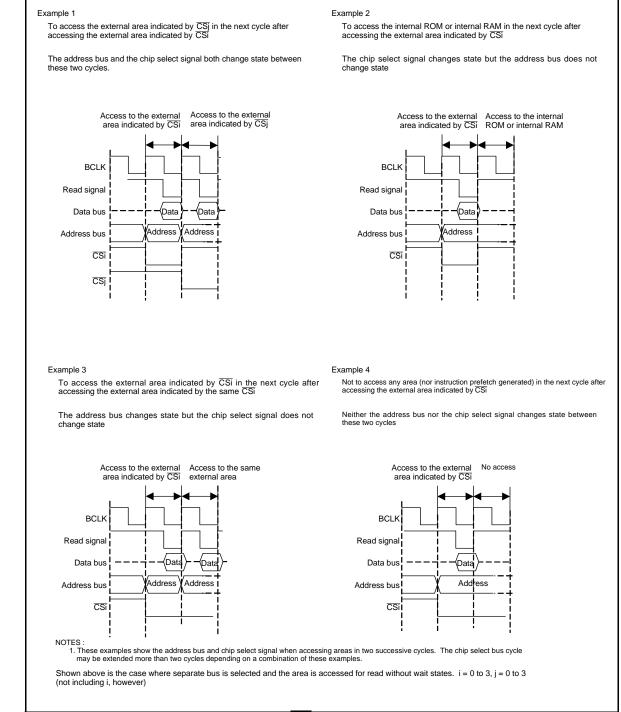
		Sy	mbol	Address	After Reset	
			SR	0008h	0000001b	
		Bit Symbol	E	Bit Name	Function	RV
	CS0 CS1	CS0	CS0 Output Ena	ble Bit	0 : Chip select output disabled (functions as I/O port)	RV
		CS1	CS1 Output Ena	ble Bit	1 : Chip select output enabled	RV
		CS2	CS2 Output Ena	ble Bit		RV
		CS3	CS3 Output Ena	ble Bit		RV
		CS0W	CS0 Wait Bit		0 : With w ait state 1 : Without w ait state ^(1, 2, 3)	RV
		CS1W	CS1 Wait Bit			RV
L		CS2W	CS2 Wait Bit			RV
		CS3W	CS3 Wait Bit			RV

2. If the PM17 bit in the PM1 register is set to "1" (with wait state), set the CSiW bit to "0" (with wait state).

3. When the CSiW bit = 0 (with wait state), the number of wait states can be selected using the CSE1W to CSE0W bits in the CSE register.

Figure 8.1 CSR Register

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Example of Address Bus and CSi Signal Output in 1-Mbyte mode

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8.2.4 Read and Write Signals

When the data bus is 16 bits wide, the read and write signals can be chosen to be a combination of $\overline{\text{RD}}$, $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ or a combination of $\overline{\text{RD}}$, $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ by using the PM02 bit in the PM0 register. When the data bus is 8 bits wide, use a combination of $\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{BHE}}$.

Table 8.3 shows the Operation of $\overline{\text{RD}}$, $\overline{\text{WRL}}$, and $\overline{\text{WRH}}$ Signals. Table 8.4 shows the Operation of $\overline{\text{RD}}$, $\overline{\text{WRL}}$, and $\overline{\text{BHE}}$ Signals.

Table 8.3 Operation of RD, WRL and WRH Signals

Data Bus Width	RD	WRL	WRH	Status of External Data Bus
16-bit	L	Н	Н	Read data
(BYTE pin input = L)	Н	L	Н	Write 1 byte of data to an even address
	Н	Н	L	Write 1 byte of data to an odd address
	Н	L	L	Write data to both even and odd addresses

Table 8.4 C	Operation	of RD,	WRL a	and BHE	Signals

Data Bus Width	RD	WRL	BHE	A0	Status of External Data Bus
16-bit	Н	L	L	Н	Write 1 byte of data to an odd address
(BYTE pin input = L)	L	Н	L	Н	Read 1 byte of data from an odd address
	Н	L	Н	L	Write 1 byte of data to an even address
	L	Н	Н	L	Read 1 byte of data from an even address
	Н	L	L	L	Write data to both even and odd addresses
	L	Н	L	L	Read data from both even and odd addresses
8-bit	Н	L	Not used	H or L	Write 1 byte of data
(BYTE pin input = H)	L	Н	Not used	H or L	Read 1 byte of data

8.2.5 ALE Signal

The ALE signal latches the address when accessing the multiplex bus space. Latch the address when the ALE signal falls.

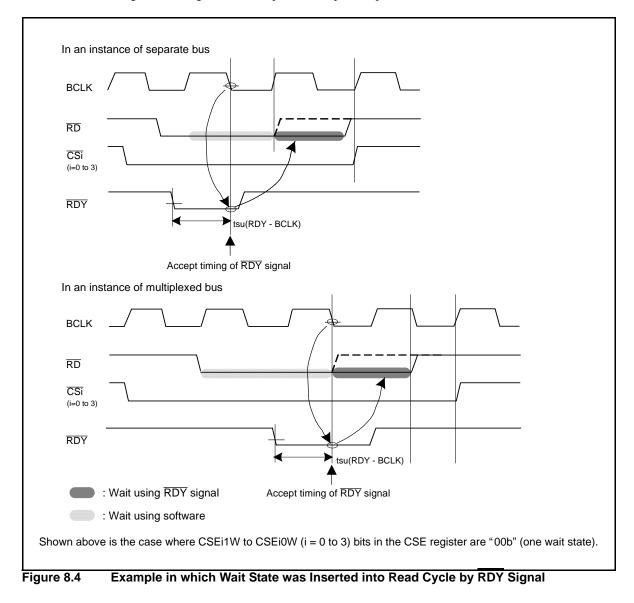
When BYTE Pin Input = H	When BYTE Pin Input = L
ALE _	ALE
A0/D0 to A7/D7 Address Data	A0 Address
A8 to A19 Address (1)	A1/D0 to A8/D7 Address Data
	A9 to A19 Address
NOTES : 1. If the entire $\overline{\text{CS}}$ space is assigned a multiplexed I	bus, these pins function as I/O ports.
Figure 8.3 ALE Signal, Address Bus, Dat	a Bus

8.2.6 RDY Signal

This signal is provided for accessing external devices which need to be accessed at low speed. If input on the $\overline{\text{RDY}}$ pin is asserted low at the last falling edge of BCLK of the bus cycle, one wait state is inserted in the bus cycle. While in a wait state, the following signals retain the state in which they were when the $\overline{\text{RDY}}$ signal was acknowledged.

A0 to A19, D0 to D15, CS0 to CS3, RD, WRL, WRH, WR, BHE, ALE, HLDA

Then, when the input on the $\overline{\text{RDY}}$ pin is detected high at the falling edge of BCLK, the remaining bus cycle is executed. Figure 8.4 shows Example in which the Wait State was Inserted into Read Cycle by $\overline{\text{RDY}}$ Signal. To use the $\overline{\text{RDY}}$ signal, set the corresponding bit (CS3W to CS0W bits) in the CSR register to "0" (with wait state). When not using the $\overline{\text{RDY}}$ signal, the $\overline{\text{RDY}}$ pin must be pulled-up.



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8.2.7 HOLD Signal

This signal is used to transfer control of the bus from the CPU or DMAC to an external circuit. When the input on $\overline{\text{HOLD}}$ pin is pulled low, the microcomputer is placed in a hold state after the bus access then in process finishes. The microcomputer remains in the hold state while the $\overline{\text{HOLD}}$ pin is held low, during which time the $\overline{\text{HLDA}}$ pin outputs a low-level signal.

Table 8.5 shows the Microcomputer Status in Hold State.

Bus-using priorities are given to $\overline{\text{HOLD}}$, DMAC, and CPU in order of decreasing precedence. However, if the CPU is accessing an odd address in word units, the DMAC cannot gain control of the bus during two separate accesses.

HOLD > DMAC > CPU

Figure 8.5 Bus-Using Priorities

Item		Status
		Sidius
BCLK		Output
A0 to A19, D0 to D15, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ WR, BHE	, RD, WRL, WRH,	High-impedance
I/O ports	P0, P1, P3, P4 ⁽²⁾	High-impedance
	P6 to P14 ⁽¹⁾	Maintains status when HOLD signal is received
HLDA		Output "L"
Internal Peripheral Circuits		ON (but watchdog timer stops) ⁽³⁾
ALE Signal		Undefined

Table 8.5 Microcomputer Status in Hold State

NOTES:

- 1. P11 to P14 are included in the 128-pin version.
- 2. When I/O port function is selected.
- 3. The watchdog timer dose not stop when the PM22 bit in the PM2 register is set to "1" (the count source for the watchdog timer is the on-chip oscillator clock).

8.2.8 8.2.8 BCLK Output

If the PM07 bit in the PM0 register is set to "0" (output enable), a clock with the same frequency as that of the CPU clock is output as BCLK from the BCLK pin. Refer to **10.2 CPU Clock and Peripheral Function Clock**.

Process	sor Mode	Mer	Memory Expansion Mode					
PM05 to PM04 bits		00b(separate bus) bits		othe <u>rs ar</u> e for se 10b(CS1 is for i	01b(CS2 is for multiplexed bus and others are for separate bus) 10b(CS1 is for multiplexed bus and others are for separate bus)			
Data Bus Width BYTE Pin		8 bits "H"	16 bits "L"	8 bits "H"	16 bits "L"	8 bits "H"		
P0_0 to P0	_7	D0 to D7	D0 to D7	D0 to D7 ⁽⁴⁾	D0 to D7 ⁽⁴⁾	I/O ports		
P1_0 to P1	_7	I/O ports	D8 to D15	I/O ports	D8 to D15 ⁽⁴⁾	I/O ports		
P2_0		A0	A0	A0/D0 (2)	A0	A0/D0		
P2_1 to P2	_7	A1 to A7	A1 to A7	A1 to A7 /D1 to D7 ⁽²⁾	A1 to A7 /D0 to D6 ⁽²⁾	A1 to A7 /D1 to D7		
P3_0		A8	A8	A8	A8/D7 ⁽²⁾	A8		
P3_1 to P3		A9 to A11	÷	•	·	I/O ports		
P3_4 to	PM11=0	A12 to A15				I/O ports		
P3_7	PM11=1	I/O ports	I/O ports					
P4_0 to	PM06=0	A16 to A19	I/O ports					
P4_3	PM06=1	I/O ports	I/O ports					
P4_4	CS0=0	I/O ports						
	CS0=1	CS0						
P4_5	CS1=0	I/O ports						
	CS1=1	CS1						
P4_6	CS2=0	I/O ports						
	CS2=1	CS2						
P4_7	CS3=0	I/O ports						
	CS3=1	CS3						
P5_0	PM02=0	WR						
	PM02=1	_ (3)	WRL	_ (3)	WRL	_ (3)		
P5_1	PM02=0	BHE	I	1		1		
	PM02=1	_ (3)	WRH	_ (3)	WRH	_ (3)		
P5_2		RD	I	I	I	I		
P5_3		BCLK						
 P5_4		HLDA						
 P5_5		HOLD						
 P5_6		ALE						
P5_7		RDY						

Pin Functions for Each Processor Mode Table 8.6

I/O ports : Function as I/O ports or peripheral function I/O pins. NOTES:

- 1. To set the PM01 to PM00 bits are set to "01b" and the PM05 to PM04 bits are set to "11b" (multiplexed bus assigned to the entire CS space), apply "H" to the BYTE pin (external data bus 8 bits wide). While the CNVSS pin is held "H" (= VCC1), do not rewrite the PM05 to PM04 bits to "11b" after reset. If the PM05 to PM04 bits are set to "11b" during memory expansion mode, P3_1 to P3_7 and P4_0 to P4_3 become I/O ports, in which case the accessible area for each \overline{CS} is 256 bytes.
- 2. In separate bus mode, these pins serve as the address bus.

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- 3. If the data bus is 8 bits wide, make sure the PM02 bit is set to "0" (RD, BHE, WR).
- 4. When accessing the area that uses a multiplexed bus, these pins output an indeterminate value during a write.

8. Bus

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8.2.9 External Bus Status When Internal Area Accessed

Table 8.7 shows the External Bus Status When Internal Area Accessed.

Table 8.7 External Bus Status When Internal Area Accessed

lte	em	SFR Accessed	Internal ROM, RAM Accessed
A0 to A19		Address output	Maintain status before accessed address of external area or SFR
D0 to D15 When Read When Write		High-impedance	High-impedance
		Output data	Undefined
RD, WR, WRL	, WRH	RD, WR, WRL, WRH output	Output "H"
BHE		BHE output	Maintain status before accessed status of external area or SFR
CS0 to CS3		Output "H"	Output "H"
ALE		Output "L"	Output "L"

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8.2.10 Software Wait

Software wait states can be inserted by using the PM17 bit in the PM1 register, the CS0W to CS3W bits in the CSR register, and the CSE register. The SFR area is unaffected by these control bits. This area is always accessed in 2 BCLK or 3 BCLK cycles as determined by the PM20 bit in the PM2 register. See **Table 8.8 Bit and Bus Cycle Related to Software Wait** for details.

To use the $\overline{\text{RDY}}$ signal, set the corresponding CS3W to CS0W bit to "0" (with wait state). Figure 8.6 shows the CSE Register. Table 8.8 shows the Bit and Bus Cycle Related to Software Wait. Figure 8.7 and 8.8 show the Typical Bus Timings Using Software Wait.

Ш		Symbol CSE	Address 001Bh	After Reset 00h	
	Bit Symb		Bit Name	Function	RW
	CSE00V	CS0 Wait Evr	pansion Bit ⁽¹⁾	^{b1 b0} 0 0 : 1 w ait	RW
	CSE01V	v		0 1 : 2 w aits 1 0 : 3 w aits 1 1 : Do not set	RW
	CSE10V	V CS1 Wait Exp	pansion Bit ⁽¹⁾	b3 b2 0 0 : 1 w ait	RW
	CSE11V	v		0 1 : 2 w aits 1 0 : 3 w aits 1 1 : Do not set	RW
	CSE20V	V CS2 Wait Exp	pansion Bit ⁽¹⁾	^{b5 b4} 0 0 : 1 w ait	RW
	CSE21V	v		0 1 : 2 w aits 1 0 : 3 w aits 1 1 : Do not set	RW
L	CSE30V	V CS3 Wait Exp	pansion Bit ⁽¹⁾	^{b7 b6} 0 0 : 1 w ait 0 1 : 2 w aits	RW
	CSE31V	v		1 0 : 2 w aits 1 0 : 3 w aits 1 1 : Do not set	RW

 Set the CSiW bit (i = 0 to 3) in the CSR register to "0" (with w ait state) before w riting to the CSE1W to CSE0W bits. If the CSiW bit needs to be set to "1" (w ithout w ait state), set the CSE1W to CSE10W bits to "00b" before setting it.

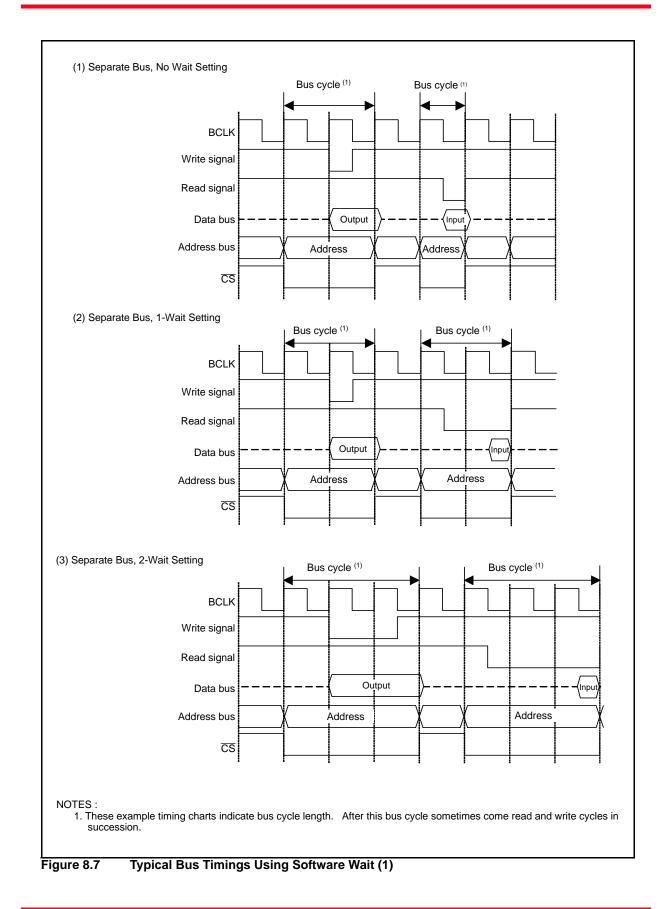
Figure 8.6 CSE Register

1							
Area	Bus Mode	PM2 Register PM20 Bit	PM1 Register PM17 Bit ⁽⁵⁾	CSR Register CS3W Bit ⁽¹⁾ CS2W Bit ⁽¹⁾ CS1W Bit ⁽¹⁾ CS0W Bit ⁽¹⁾	CSE Register CSE31W to CSE30W Bit CSE21W to CSE20W Bit CSE11W to CSE10W Bit CSE01W to CSE00W Bit	Software Wait	Bus Cycle
SFR	-	1	-	-	-	-	2 BCLK cycles (3)
	_	0	-	-	-	-	3 BCLK cycles (3)
Internal	-	-	0	-	-	No wait	1 BCLK cycle (4)
RAM, ROM	-	-	1	_	-	1 wait	2 BCLK cycles
	Separate Bus	_	0	1	00b	No wait	1 BCLK cycle (read) 2 BCLK cycles (write)
		-	-	0	00b	1 wait	2 BCLK cycle (4)
		-	-	0	01b	2 waits	3 BCLK cycles
		-	-	0	10b	3 waits	4 BCLK cycle
		-	1	0	00b	1 wait	2 BCLK cycle
	Multiplexed	-	-	0	00b	1 wait	3 BCLK cycles
E	Bus ⁽²⁾	-	-	0	01b	2 waits	3 BCLK cycles
		-	-	0	10b	3 waits	4 BCLK cycles
		-	1	0	00b	1 wait	3 BCLK cycles

 Table 8.8
 Bit and Bus Cycle Related to Software Wait

NOTES:

- 1. To use the \overline{RDY} signal, set this bit to "0".
- 2. To access in multiplexed bus mode, set the corresponding bit of CS0W to CS3W to "0" (with wait state).
- 3. When the selected CPU clock source is the PLL clock, the number of wait cycles can be altered by the PM20 bit in the PM2 register. When using a 16 MHz or higher PLL clock, be sure to set the PM20 bit to "0" (2 wait cycles).
- 4. After reset, the PM17 bit is set to "0" (without wait state), all of the CS0W to CS3W bits are set to "0" (with wait state), and the CSE register is set to "00h" (one wait state for CS0 to CS3). Therefore, the internal RAM and internal ROM are accessed with no wait states, and all external areas are accessed with one wait state.
- 5. When PM17 bit is set to "1" and accesses an external area, set the CSiW (i=0 to 3) bits to "0" (with wait state).



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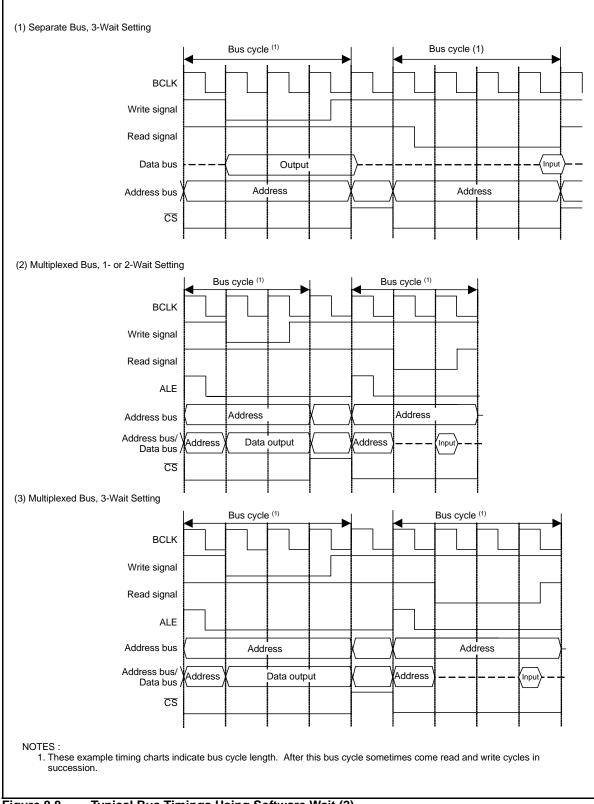


Figure 8.8 Typical Bus Timings Using Software Wait (2)

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9. Memory Space Expansion Function

Note

The M16C/62P (80-pin version) and M16C/62PT do not use the memory space expansion function.

The following describes a memory space extension function.

During memory expansion or microprocessor mode, the memory space expansion function allows the access space to be expanded using the appropriate register bits.

Table 9.1 shows The Way of Setting Memory Space Expansion Function, Memory Space.

Table 9.1 The Way of Setting Memory Space	Expansion Function, Memory Space
---	----------------------------------

Memory Space Expansion Function	How to Set (PM15 to PM14)	Memory Space
1-Mbyte Mode	00b	1 Mbyte (no expansion)
4-Mbyte Mode	11b	4 Mbytes

9.1 1-Mbyte Mode

In this mode, the memory space is 1 Mbytes. In 1-Mbyte mode, the external area to be accessed is specified using the \overline{CSi} (i = 0 to 3) signals (hereafter referred to as the \overline{CSi} area). Figures 9.2 to 9.3 show the Memory Mapping and \overline{CS} Area in 1-Mbyte mode.

9.2 4-Mbyte Mode

In this mode, the memory space is 4 Mbytes. Figure 9.1 shows the DBR Register. The BSR2 to BSR0 bits in the DBR register select a bank number which is to be accessed to read or write data. Setting the OFS bit to "1" (with offset) allows the accessed address to be offset by 40000h.

In 4-Mbyte mode, the \overline{CSi} (i=0 to 3) pin functions differently for each area to be accessed.

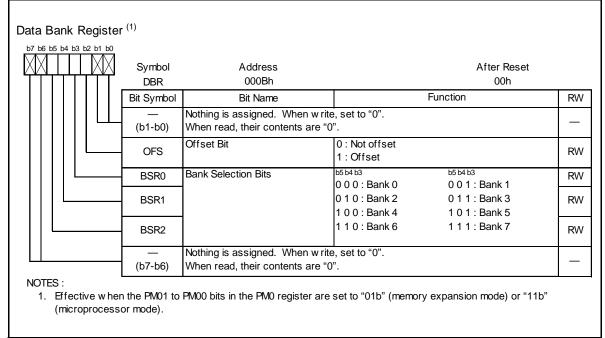
9.2.1 9.2.1 Addresses 04000h to 3FFFFh, C0000h to FFFFFh

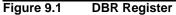
• The CSi signal is output from the $\overline{\text{CSi}}$ pin (same operation as 1-Mbyte mode. However, the last address of $\overline{\text{CS1}}$ area is 3FFFFh).

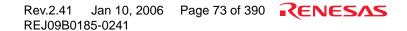
9.2.2 9.2.2 Addresses 40000h to BFFFFh

- The $\overline{\text{CS0}}$ pin outputs "L"
- The $\overline{\text{CS1}}$ to $\overline{\text{CS3}}$ pins output the value of setting as the BSR2 to BSR0 bits (bank number)

Figures 9.4 to 9.5 show the Memory Mapping and \overline{CS} Area in 4-Mbyte mode. Note that banks 0 to 6 are data-only areas. Locate the program in bank 7 or the \overline{CSi} area.







00000h	SFR			SFR				
00400h	Internal RA	м	Inter	nal RAM				
XXXXXh	Reserved ar	ea – – – – –		rved area				
04000h			_		CS3 (16	- Khytes)		
08000h	Reserved, external	area ⁽²⁾	- Reserved e	external area ⁽²⁾	· · · · · · · · · · · · · · · · · · ·	<u>/</u> //10=0: 124 Kb	utos)	
10000h		<u>aica</u>				(PM10=0: 124 Rb)		
27000h	Reserved ar	ea	Rese	rved area	. y_ y_			
28000h	mhanhandandan.hanhanhandan.h				CS1 (32	Kbytes)		
30000h	External are	 ea	Exte	rnal area		_	pansion mode:640 Kbytes)	
D0000h	Reserved area				*		node:832 Kbytes)	
YYYYYh FFFFFh	Internal RO	м			.	-	ioue.osz kuytes)	
PM13=0								
	Internal RAM		rnal ROM			1	al Area	
	ity Address XXXXXh	Capacity	Address YYYYYh	CS	-	CS1	CS2	CS3
Capaci	ny in the	,						04000h to
4 Kby	/tes 013FFh	48 Kbytes		Memory expan		28000h to	When PM10=0	
4 Kby 5 Kby	vtes 013FFh vtes 017FFh	48 Kbytes 64 Kbytes	F0000h	30000h to ĊFF	FFh	28000h to 2FFFFh	08000h to 26FFFh	07FFFh
4 Kby 5 Kby 10 Kby	rtes 013FFh rtes 017FFh rtes 02BFFh	48 Kbytes 64 Kbytes 96 Kbytes	F0000h E8000h		FFh r mode			
4 Kby 5 Kby 10 Kby 12 Kby	rtes 013FFh rtes 017FFh rtes 02BFFh rtes 033FFh	48 Kbytes 64 Kbytes 96 Kbytes 128 Kbytes	F0000h E8000h E0000h	30000h to ĊFF Microprocesso	FFh r mode		08000h to 26FFFh When PM10=1	
4 Kby 5 Kby 10 Kby 12 Kby 16 Kby	rtes 013FFh rtes 017FFh rtes 02BFFh	48 Kbytes 64 Kbytes 96 Kbytes	F0000h E8000h E0000h D0000h	30000h to ĊFF Microprocesso	FFh r mode		08000h to 26FFFh When PM10=1	
4 Kby 5 Kby 10 Kby 12 Kby 16 Kby 20 Kby	vtes 013FFh vtes 017FFh vtes 02BFFh vtes 033FFh vtes 03FFFh ⁽¹⁾ vtes 03FFFh ⁽¹⁾	48 Kbytes 64 Kbytes 96 Kbytes 128 Kbytes 192 Kbytes	F0000h E8000h E0000h D0000h D0000h ⁽¹⁾	30000h to ĊFF Microprocesso	FFh r mode		08000h to 26FFFh When PM10=1	
4 Kby 5 Kby 10 Kby 12 Kby 16 Kby 20 Kby 24 Kby	Arrow O13FFh vtes 013FFh vtes 017FFh vtes 02BFFh vtes 033FFh vtes 03FFh ⁽¹⁾	48 Kbytes 64 Kbytes 96 Kbytes 128 Kbytes 192 Kbytes 256 Kbytes	F0000h E8000h E0000h D0000h D0000h ⁽¹⁾	30000h to ĊFF Microprocesso	FFh r mode		08000h to 26FFFh When PM10=1	

Figure 9.2 Memory Mapping and CS Area in 1-Mbyte mode (PM13=0)

0000h	SFR		s	SFR				
0400h (XXXh	Internal RAM		Interr	Internal RAM				
			Reser	rved area				
8000h	Reserved, external	l area ⁽¹⁾	Reserved, e	xternal area ⁽¹⁾		_ M10=0: 124 Kb	ytes)	
0000h				CS2 (PM10=1: 92 Kbytes)				
7000h	necented area		Reser	Reserved area				
8000h					CS1 (32	- 2 Kbytes)		
0000h	External are				·- ††	-		
			Exter	rnal area	$\overline{\text{CS0}}$ (Memory expansion mode : 320 Kbytes)			
			Exici	lidi arca			xparision mode . 520 raya	55)
0000h					±_	-		
000011	Reserved ar	rea						
YYYh				CS0 (Microprocessor mode : 832 Kbytes)				
FFFh	Internal RO	M			Ļ			
					¥	-		
/13=1		la ta	- DOM	1		5 dama dama		
Capacity	Internal RAM	Inte Capacity	rnal ROM		External area			CS3
4 Kbyt	,	48 Kbytes	F4000h	Memory expan	-	28000h to	When PM10=0	No area
5 Kbyt		64 Kbytes	F0000h	30000h to 7FF		2FFFFh	08000h to 26FFFh	i to alca
10 Kbyt		96 Kbytes	E8000h	Microprocesso	or mode		When PM10=1	
12 Kbyt		128 Kbytes	E0000h	30000h to FFF	FFh		10000h to 26FFFh	
16 Kbyt	es 043FFh	192 Kbytes	D0000h]				
20 Kbyt	es 053FFh	256 Kbytes	C0000h					
24 Kbyt	es 063FFh	320 Kbytes	B0000h					
31 Kbyt	es 07FFh	384 Kbytes	A0000h					
_		512 Kbytes	80000h					

Figure 9.3 Memory Mapping and CS Area in 1-Mbyte mode (PM13=1)

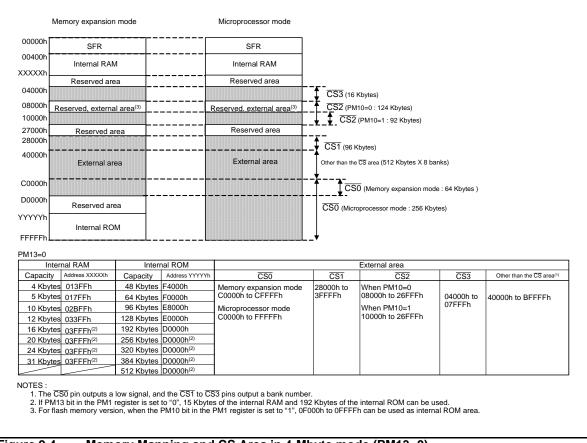


Figure 9.4 Memory Mapping and CS Area in 4-Mbyte mode (PM13=0)

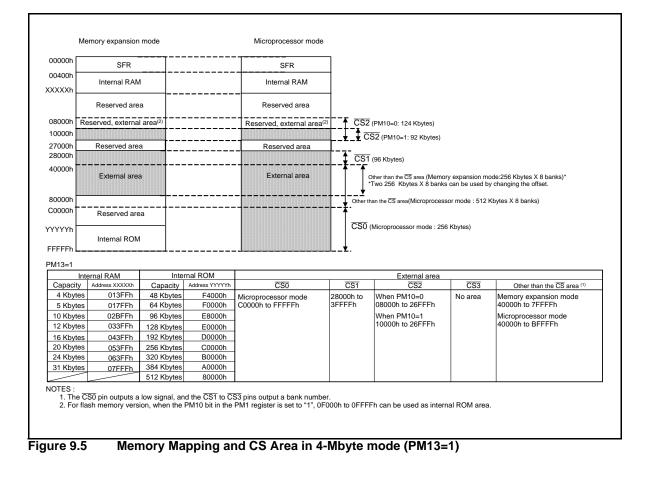


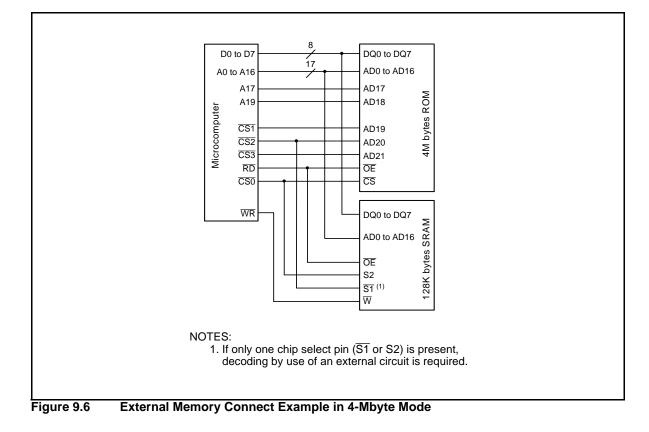
Figure 9.6 shows the External Memory Connect Example in 4-Mbyte Mode.

In this example, the \overline{CS} pin of 4-Mbyte ROM is connected to the $\overline{CS0}$ pin of microcomputer. The 4 Mbyte ROM address input AD21, AD20 and AD19 pins are connected to the $\overline{CS3}$, $\overline{CS2}$ and $\overline{CS1}$ pins of microcomputer, respectively. The address input AD18 pin is connected to the A19 pin of microcomputer. Figures Figure 9.7 to 9.9 show the Relationship of Addresses Between the 4-Mbyte ROM and the Microcomputer for the Case of a Connection Example in Figure 9.6.

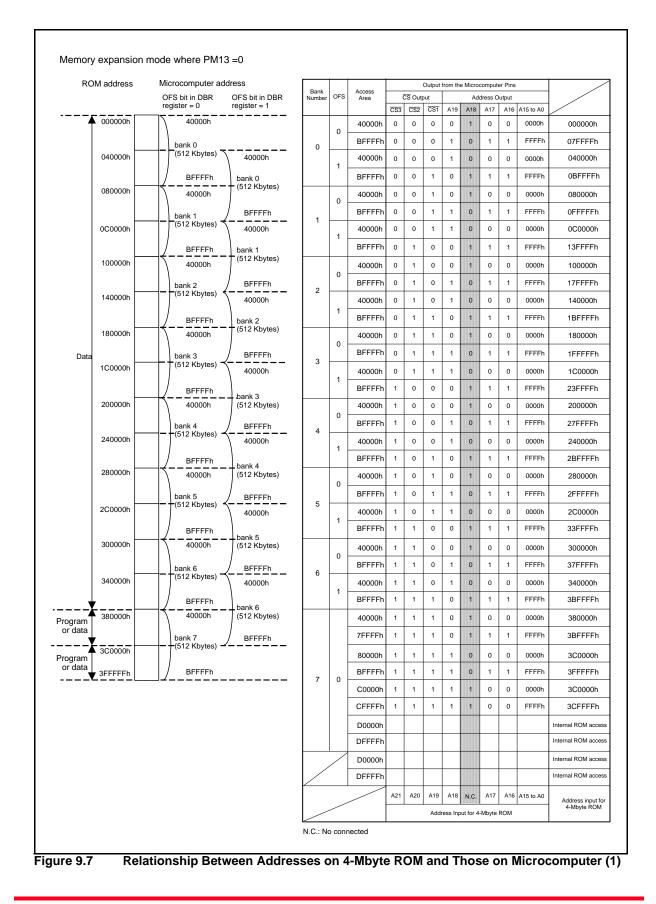
In microprocessor mode, or in memory expansion mode where the PM13 bit in the PM1 register is "0", banks are located every 512 Kbytes. Setting the OFS bit in the DBR register to "1" (offset) allows the accessed address to be offset by 40000h, so that even the data overlapping a bank boundary can be accessed in succession.

In memory expansion mode where the PM13 bit is "1," each 512-Kbyte bank can be accessed in 256 Kbyte units by switching them over with the OFS bit.

Because the SRAM can be accessed on condition that the chip select signals S2 = H and S1 = L, $\overline{CS0}$ and $\overline{CS2}$ can be connected to S2 and $\overline{S1}$, respectively. If the SRAM does not have the input pins to accept "H" active and "L" active chip select signals($\overline{S1}$, S2), $\overline{CS0}$ and $\overline{CS2}$ should be decoded external to the chip.



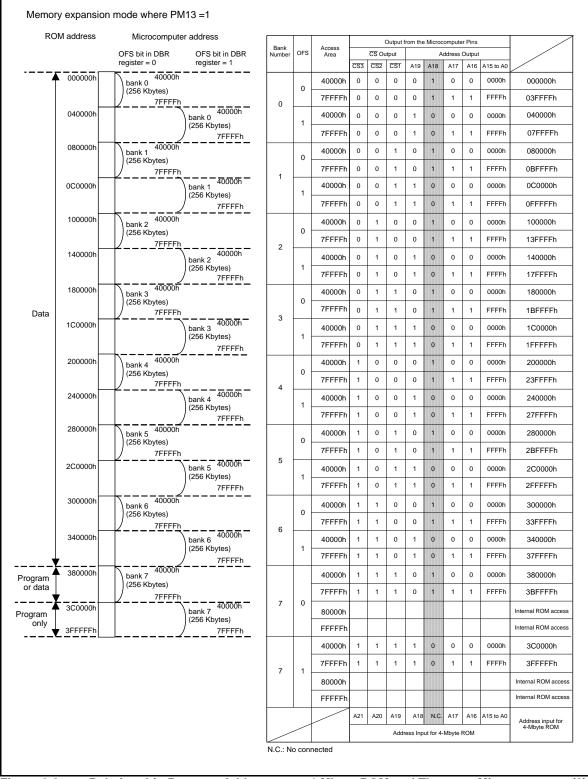
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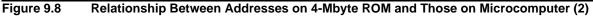


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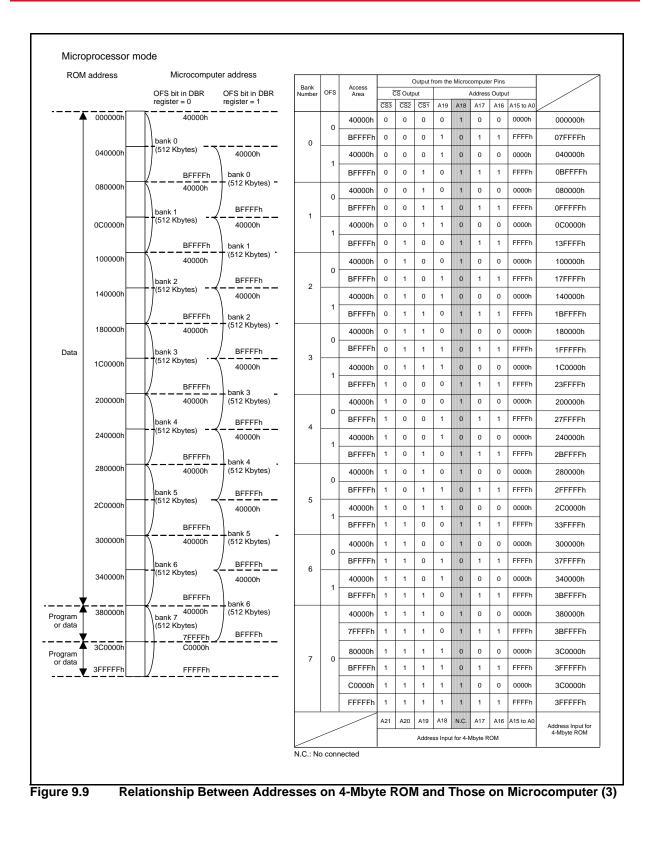




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10. Clock Generation Circuit

10.1 Types of the Clock Generation Circuit

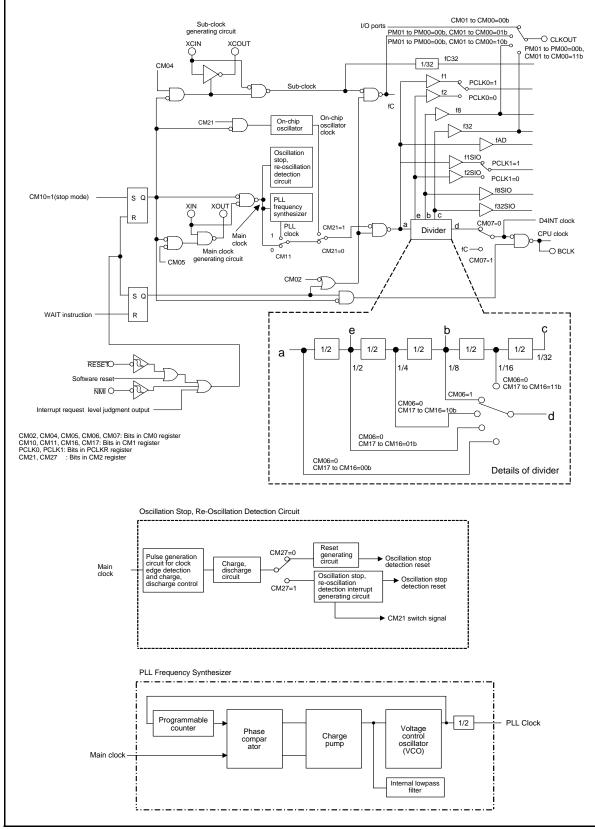
4 circuits are incorporated to generate the system clock signal :

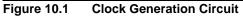
- Main clock oscillation circuit
- Sub clock oscillation circuit
- On-chip oscillator
- PLL frequency synthesizer

Table 10.1 lists the Clock Generation Circuit Specifications. Figure 10.1 shows the Clock Generation Circuit. Figures 10.2 to 10.6 show the clock-related registers.

Item	Main Clock Oscillation Circuit	Sub Clock Oscillation Circuit	On-chip oscillator	PLL frequency synthesizer
Use of Clock	CPU clock source Peripheral function clock source	CPU clock source Timer A, B's clock source	 CPU clock source Peripheral function clock source CPU and peripheral function clock sources when the main clock stops oscillating 	CPU clock source Peripheral function clock source
Clock Frequency	0 to 16 MHz	32.768 kHz	About 1 MHz	10 to 24MHz
Usable Oscillator	Ceramic oscillator Crystal oscillator	 Crystal oscillator 	-	-
Pins to Connect Oscillator	XIN, XOUT	XCIN, XCOUT	-	-
Oscillation Stop, Restart Function	Presence	Presence	Presence	Presence
Oscillator Status After Reset	Oscillating	Stopped	Stopped	Stopped
Other	Externally derived clo	ck can be input	-	_

Table 10.1 Clock Generation Circuit Specifications





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7 b6 b5 b4	4 b3 b2 b1 b0				
		Symbol	Address	After Reset	
		CM0	0006h	01001000b	
		Bit Symbol	Bit Name	Function	RW
		CM00	Clock Output Function Select Bit	b1 b0 0 0 : VO port P5_7	RW
		CM01	(Valid only in single-chip mode)	0 1 : Output fC 1 0 : Output f8 1 1 : Output f32	RW
		- CM02	WAIT Mode Peripheral Function Clock Stop Bit ⁽¹⁰⁾	 0 : Peripheral function clock does not stop in w ait mode 1 : Peripheral function clock stops in w ait mode⁽⁸⁾ 	RW
		CM03	XCIN-XCOUT Drive Capacity Select Bit ⁽²⁾	0 : LOW 1 : HIGH	RW
L		CM04	Port XC Select Bit ⁽²⁾	0 : VO ports P8_6, P8_7 1 : XCIN-XCOUT oscillation function ⁽⁹⁾	RW
╎╎└		CM05	Main Clock Stop Bit (3, 10, 12, 13)	0 : On 1 : Off ^(4, 5)	RW
		CM06	Main Clock Division Select Bit 0 ^(7, 13, 14)	0 : CM16 and CM17 enabled 1 : Division-by-8 mode	RW
		CM07	System Clock Select Bit (6, 10, 11, 12)	0 : Main clock, PLL clock, or on-chip oscillator clock 1 : Sub clock	RW

- 1. Rew rite this register after setting the PRC0 bit in the PRCR register to "1" (write enable).
- 2. The CM03 bit is set to "1" (high) while the CM04 bit is set to "0" (I/O port) or when entering stop mode.

3. This bit is provided to stop the main clock when the low power consumption mode or on-chip oscillator low power dissipation mode is selected. This bit cannot be used for detection as to whether the main clock stops or not. To stop the main clock, set bits as follow s:

- (a) Set the CM07 bit to "1" (sub clock selected) or the CM21 bit in the CM2 register to "1" (On-chip oscillator selected)
 - with the sub-clock stably oscillates.
- (b) Set the CM20 bit in the CM2 register to "0" (Oscillation stop, re-oscillation detection function disabled).
- (c) Set the CM05 bit to "1" (Stop).
- 4. During external clock input, Set the CM05 bit to "0" (oscillate).
- 5. When CM05 bit is set to "1", the XOUT pin is held "H". Because the internal feedback resistor remains connected, the XIN pin is pulled "H" to the same level as XOUT via the feedback resistor.
- 6. After setting the CM04 bit to "1" (XCIN-XCOUT oscillator function), wait until the sub-clock oscillates stably before switching the CM07 bit from "0" to "1" (sub-clock).
- 7. When entering stop mode from high-speed or middle-speed mode, on-chip oscillator mode or on-chip oscillator low pow er mode, the CM06 bit is set to "1" (divide-by-8 mode).
- 8. The fC32 clock does not stop. In low-speed mode or low pow er consumption mode, do not set this bit to "1" (peripheral clock stops in wait mode).
- 9. To use a sub-clock, set this bit to "1". Also make sure ports P8 6 and P8 7 are directed for input, with no pull-ups.
- 10. When the PM21 bit in the PM2 register is set to "1" (disable clock modification), this bit remains unchanged even if w riting to the CM02, CM05, and CM07 bits.
- 11. When setting the PM21 bit to "1", set the CM07 bit to "0" (main clock) before setting the PM21 bit to "1".
- 12. To use the main clock as the clock source for the CPU clock, set bits as follow s.
 - (a) Set the CM05 bit to "0" (oscillate).
 - (b) Wait the main clock oscillation stabilizes.
 - (c) Set the CM11, CM21 and CM07 bits to "0".
- 13. When the CM21 bit is set to "0" (on-chip oscillator stops) and the CM05 bit is set to "1" (main clock stops), the CM06 bit is fixed to "1" (divide-by-8 mode) and the CM15 bit is fixed to "1" (drive capacity High).
- 14. To return from on-chip oscillator mode to high-speed or middle-speed mode, set the CM06 and CM15 bits to "1".

Figure 10.2 **CM0** Register

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	Symbol CM1	Address 0007h	After Reset 00100000b	
	Bit Symbol	Bit Name	Function	RW
	CM10	All Clock Stop Control Bit ^(4, 6)	0 : Clock on 1 : All clocks off (stop mode)	RW
	CM11	System Clock Select Bit 1 (6, 7)	0 : Main clock 1 : PLL clock ⁽⁵⁾	RW
	 (b4-b2)	Reserved Bit	Set to "0"	RW
	CM15	XIN-XOUT Drive Capacity Select Bit ⁽²⁾	0 : LOW 1 : HIGH	RW
	CM16	Main Clock Division Select Bit 1 ⁽³⁾	^{b7 b6} 0 0 : No division mode	RW
	CM17		0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
NOTES : 1 Rew rite this re	Lengister after s	etting the PRC0 bit in the PRCR registe	er to "1" (write enable)	
	0	0 0	e, or the CM05 bit is set to "1" (main clock	stops) in

XCIN and XCOUT pins are in high-impedance state. When the CM11 bit is set to "1" (PLL clock), or the CM20 bit in the CM2 register is set to "1" (oscillation stop, re-oscillation detection function enabled), do not set the CM10 bit to "1".

- 5. After setting the PLC07 bit in the PLC0 register to "1" (PLL operation), w ait tsu (PLL) elapses before setting the CM11 bit to "1" (PLL clock).
- When the PM21 bit in the PM2 register is set to "1" (disable clock modification), this bit remains unchanged even if writing to the CM10, CM11 bits.

When the PM22 bit in the PM2 register is set to "1" (on-chip oscillator clock is selected as watchdog timer count source), this bit remains unchanged even if writing to the CM10 bit.

7. This bit is valid when the CM07 bit is set to "0" and the CM21 bit is set to "0".



X 0 0 	Symbol CM2	Address 000Ch	After Reset 0X00000b (11)	
	Bit Symbol	Bit Name	Function	RW
	CM20	Oscillation Stop, Re-Oscillation Detection Enable Bit ^(7, 9, 10,11)	 0: Oscillation stop, re-oscillation detection function disabled 1: Oscillation stop, re-oscillation detection function enabled 	RW
	CM21	System Clock Select Bit 2 (2, 3, 6, 8, 11, 12)	0: Main clock or PLL clock 1: On-chip oscillator clock (On-chip oscillator oscillates)	RW
	CM22	Oscillation Stop, Re-Oscillation Detection Flag ⁽⁴⁾	0: Main clock stops, re-oscillation not detected 1: Main clock stops, re-oscillation detected	RW
	 CM23	XIN Monitor Flag ⁽⁵⁾	0: Main clock oscillates 1: Main clock stops	RO
	 (b5-b4)	Reserved Bit	Set to "0"	RW
	(b6)	Nothing is assigned. When w When read, its content is "0".	rite, set to "0".	_
	CM27	Operation Select Bit (w hen an oscillation stop, re-oscillation is detected) ⁽¹¹⁾	0: Oscillation stop detection reset 1: Oscillation stop, re-oscillation detection interrupt	RW

NOTES :

1. Rew rite this register after setting the PRC0 bit in the PRCR register to "1" (w rite enable).

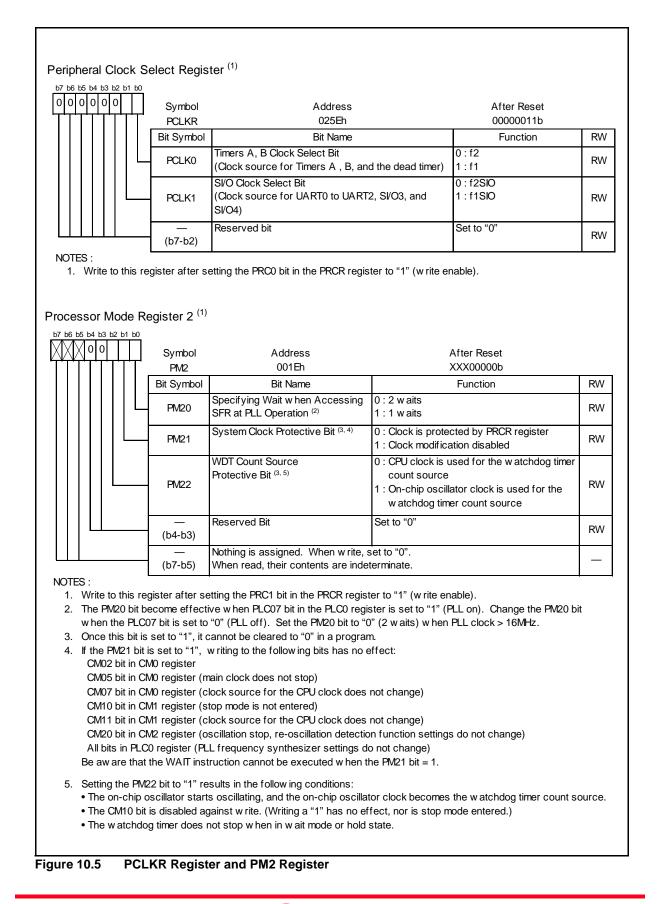
- 2. When the CM20 bit is set to "1" (oscillation stop, re-oscillation detection function enabled), the CM27 bit is set to "1" (oscillation stop, re-oscillation detection interrupt), and the CPU clock source is the main clock, the CM21 bit is set to "1" (on-chip oscillator clock) if the main clock stop is detected.
- 3. If the CM20 bit is set to "1" and the CM23 bit is set to "1" (main clock stops), do not set the CM21 bit to "0".
- 4. This bit is set to "1" when the main clock stop is detected and the main clock re-oscillation is detected. When this flag changes state from "0" to "1", an oscillation stop or a re-oscillation detection interrupt is generated. Use this bit in an interrupt routine to determine the factors of interrupts betw een the oscillation stop and re-oscillation detection interrupt and the watchdog timer interrupt. This bit is set to "0" by writing "0" in a program. (This bit remains unchanged even if writing "1". Nor is it set to "0" when an oscillation stop or a re-oscillation detection interrupt request is acknow ledged.)

When the CM22 bit is set to "1" and an oscillation stop or a re-oscillation is detected, an oscillation stop or a re-oscillation detection interrupt is not generated.

- 5. Determine the main clock status by reading the CM23 bit several times in an oscillation stop or a re-oscillation detection interrupt routine
- 6. This bit is valid when the CM07 bit in the CM0 register is set to "0".
- 7. When the PM21 bit in the PM2 register is set to "1" (disable clock modification), this bit remains unchanged even if w riting to the CM20 bit.
- 8. Where the CM20 bit is set to "1" (oscillation stop, re-oscillation detection function enabled), the CM27 bit is "1" (oscillation stop, re-oscillation detection interrupt), and the CM11 bit is set to "1" (PLL clock is selected as the CPU clock source), the CM21 bit remains unchanged even if a main clock stop is detected. When the CM22 bit is set to "0" under these conditions, an oscillation stop, a re-oscillation detection interrupt request is generated at main clock stop detection. Set the CM21 bit to "1" (on-chip oscillator clock) in the interrupt routine.
- Set the CM20 bit to "0" (disabled) before entering stop mode. Exit stop mode before setting the CM20 bit back to "1" (enabled).
- 10. Set the CM20 bit in the CM2 register to "0" (disabled) before setting the CM05 bit in the CM0 register to "1" (main clock stops).
- 11. The CM20, CM21 and CM27 bits remain unchanged at the oscillation stop detection reset.
- 12. When the CM21 bit is set to "0" (on-chip oscillator stops) and the CM05 bit is set to "1" (main clock stops), the CM06 bit is fixed to "1" (divide-by-8 mode) and the CM15 bit is fixed to "1" (drive capacity High).

Figure 10.4 CM2 Register

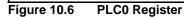
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b7 b6 b5 b4 b3 b2 b1 b0				
001	Symbol	Address	After Reset	
	PLC0	001Ch	0001X010b	
	Bit Symbol	Bit Name	Function	RW
	PLC00	PLL Multiplying Factor Select Bit ⁽³⁾	^{b2 b1 b0} 0 0 0 : Do not set 0 0 1 : Multiply by 2	RW
	PLC01		0 1 0 : Multiply by 4 0 1 1 : Multiply by 6 1 0 0 : Multiply by 8	RW
	PLC02		101: 110: 111: 111:	RW
	_	Nothing is assigned. When wri	te, set to "0".	
	(b3)	When read, its content is indete	erminate.	_
	(b4)	Reserved Bit	Set to "1"	RW
	 (b6-b5)	Reserved Bit	Set to "0"	RW
	PLC07	Operation Enable Bit ⁽⁴⁾	0: PLL Off 1: PLL On	RW

NOTES :

- 1. Write to this register after setting the PRC0 bit in the PRCR register to "1" (write enable).
- 2. When the PM21 bit in the PM2 register is "1" (clock modification disable), writing to this register has no effect.
- 3. These three bits can only be modified when the PLC07 bit = 0 (PLL turned off). The value once w ritten to this bit cannot be modified.
- 4. Before setting this bit to "1", set the CM07 bit in the CM0 register to "0" (main clock), set the CM17 to CM16 bits in the CM1 register to "00b" (main clock undivided mode), and set the CM06 bit in the CM0 register to "0" (CM16 and CM17 bits enable).



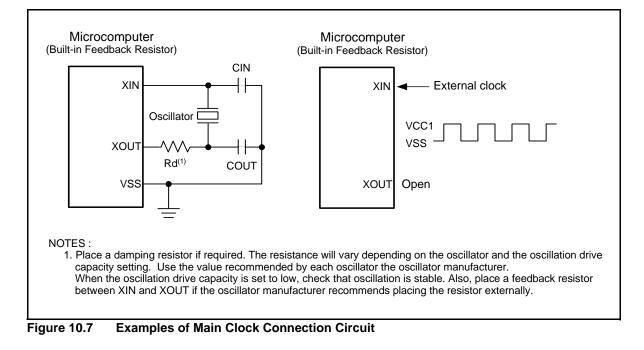
The following describes the clocks generated by the clock generation circuit.

10.1.1 Main Clock

This clock is used as the clock source for the CPU and peripheral function clocks. This clock is used as the clock source for the CPU and peripheral function clocks. The main clock oscillator circuit is configured by connecting a resonator between the XIN and XOUT pins. The main clock oscillator circuit contains a feedback resistor, which is disconnected from the oscillator circuit during stop mode in order to reduce the amount of power consumed in the chip. The main clock oscillator circuit may also be configured by feeding an externally generated clock to the XIN pin. Figure 10.7 shows the Examples of Main Clock Connection Circuit. After reset, the main clock divided by 8 is selected for the CPU clock.

The power consumption in the chip can be reduced by setting the CM05 bit in the CM0 register to "1" (main clock oscillator circuit turned off) after switching the clock source for the CPU clock to a sub clock or on-chip oscillator clock. In this case, XOUT goes "H". Furthermore, because the internal feedback resistor remains on, XIN is pulled "H" to XOUT via the feedback resistor. Note that if an externally generated clock is fed into the XIN pin, the main clock cannot be turned off by setting the CM05 bit to "1," unless the sub clock is chosen as a CPU clock. If necessary, use an external circuit to turn off the clock.

During stop mode, all clocks including the main clock are turned off. Refer to 10.4 Power Control.



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10.1.2 Sub Clock

The sub clock is generated by the sub clock oscillation circuit. This clock is used as the clock source for the CPU clock, as well as the timer A and timer B count sources. In addition, an fc clock with the same frequency as that of the sub clock can be output from the CLKOUT pin.

The sub clock oscillator circuit is configured by connecting a crystal resonator between the XCIN and XCOUT pins. The sub clock oscillator circuit contains a feedback resistor, which is disconnected from the oscillator circuit during stop mode in order to reduce the amount of power consumed in the chip. The sub clock oscillator circuit may also be configured by feeding an externally generated clock to the XCIN pin.

Figure 10.8 shows the Examples of Sub Clock Connection Circuit.

After reset, the sub clock is turned off. At this time, the feedback resistor is disconnected from the oscillator circuit.

To use the sub clock for the CPU clock, set the CM07 bit in the CM0 register to "1" (sub clock) after the sub clock becomes oscillating stably.

During stop mode, all clocks including the sub clock are turned off. Refer to 10.4 Power Control.

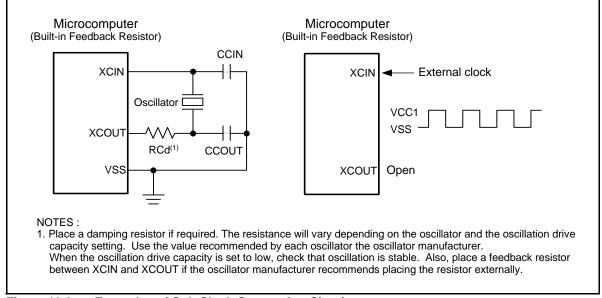


Figure 10.8 Examples of Sub Clock Connection Circuit

10.1.3 On-chip Oscillator Clock

This clock, approximately 1MHz, is supplied by a on-chip oscillator. This clock is used as the clock source for the CPU and peripheral function clocks. In addition, if the PM22 bit in the PM2 register is "1" (on-chip oscillator clock for the watchdog timer count source), this clock is used as the count source for the watchdog timer (Refer to **13.1 Count source protective mode**).

After reset, the on-chip oscillator is turned off. It is turned on by setting the CM21 bit in the CM2 register to "1" (on-chip oscillator clock), and is used as the clock source for the CPU and peripheral function clocks, in place of the main clock. If the main clock stops oscillating when the CM20 bit in the CM2 register is "1" (oscillation stop, re-oscillation detection function enabled) and the CM27 bit is "1" (oscillation stop, re-oscillation detection function automatically starts operating, supplying the necessary clock for the microcomputer.

10.1.4 PLL Clock

The PLL clock is generated PLL frequency synthesizer. This clock is used as the clock source for the CPU and peripheral function clocks. After reset, the PLL clock is turned off. The PLL frequency synthesizer is activated by setting the PLC07 bit to "1" (PLL operation). When the PLL clock is used as the clock source for the CPU clock, wait tsu(PLL) for the PLL clock to be stable, and then set the CM11 bit in the CM1 register to "1".

Before entering wait mode or stop mode, be sure to set the CM11 bit to "0" (CPU clock source is the main clock). Furthermore, before entering stop mode, be sure to set the PLC07 bit in the PLC0 register to "0" (PLL stops). Figure 10.9 shows the Procedure to Use PLL Clock as CPU Clock Source.

The PLL clock frequency is determined by the equation below. When the PLL clock frequency is 16 MHz or more, set the PM20 bit in the PM2 register to "0" (2 waits).

PLL clock frequency=f(XIN) X (multiplying factor set by the PLC02 to PLC00 bits in the PLC0 register (However, 10 MHz PLL clock frequency 24 MHz)

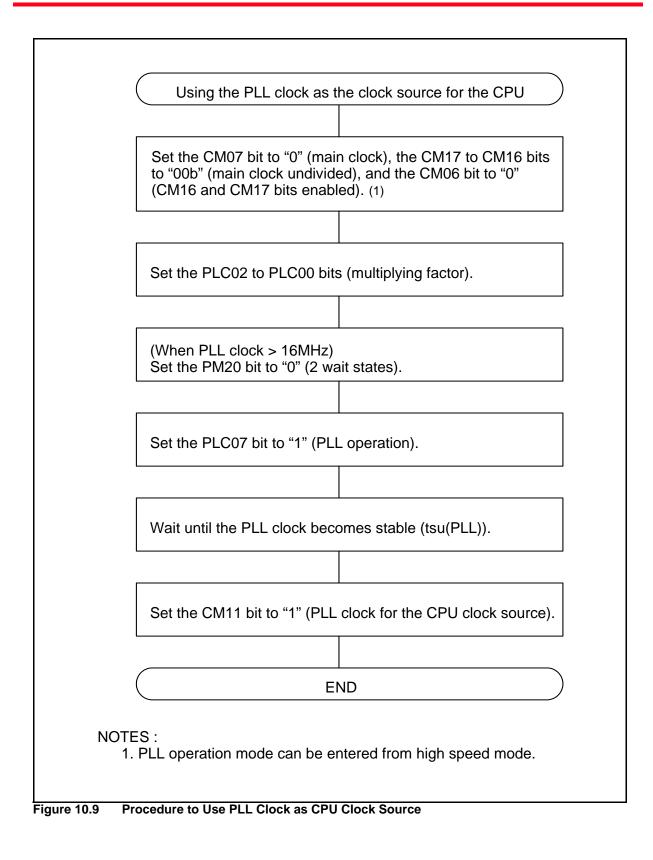
The PLC02 to PLC00 bits can be set only once after reset. Table 10.2 shows the Example for Setting PLL Clock Frequencies.

XIN (MHz)	PLC02	PLC01	PLC00	Multiplying Factor	PLL Clock (MHz) ⁽¹⁾	
10	0	0	1	2		
5	0	1	0	4	20	
3.33	0	1	1	6	20	
2.5	1	0	0	8		
12	0	0	1	2		
6	0	1	0	4	24	
4	0	1	1	6	24	
3	1	0	0	8		

Table 10.2 Example for Setting PLL Clock Frequencies

NOTES:

1. $10MHz \le PLL$ clock frequency $\le 24MHz$.



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10.2 CPU Clock and Peripheral Function Clock

Two type clocks: CPU clock to operate the CPU and peripheral function clocks to operate the peripheral functions.

10.2.1 CPU Clock and BCLK

These are operating clocks for the CPU and watchdog timer.

The clock source for the CPU clock can be chosen to be the main clock, sub clock, on-chip oscillator clock or the PLL clock.

If the main clock or on-chip oscillator clock is selected as the clock source for the CPU clock, the selected clock source can be divided by 1 (undivided), 2, 4, 8 or 16 to produce the CPU clock. Use the CM06 bit in CM0 register and the CM17 to CM16 bits in the CM1 register to select the divide-by-n value.

When the PLL clock is selected as the clock source for the CPU clock, the CM06 bit should be set to "0" and the CM17 to CM16 bits to "00b" (undivided).

After reset, the main clock divided by 8 provides the CPU clock.

During memory expansion or microprocessor mode, a BCLK signal with the same frequency as the CPU clock can be output from the BCLK pin by setting the PM07 bit in the PM0 register to "0" (output enabled).

Note that when entering stop mode from high or middle speed mode, on-chip oscillator mode or on-chip oscillator low power dissipation mode, or when the CM05 bit in the CM0 register is set to "1" (main clock turned off) in low-speed mode, the CM06 bit in the CM0 register is set to "1" (divide-by-8 mode).

10.2.2 Peripheral Function Clock (f1, f2, f8, f32, f1SIO, f2SIO, f8SIO, f32SIO, fAD, fC32)

These are operating clocks for the peripheral functions.

Of these, fi (i = 1, 2, 8, 32) and fiSIO are derived from the main clock, PLL clock or on-chip oscillator clock by dividing them by i. The clock fi is used for timers A and B, and fiSIO is used for serial I/O. The f8 and f32 clocks can be output from the CLKOUT pin.

The fAD clock is produced from the main clock, PLL clock or on-chip oscillator clock, and is used for the A/D converter.

When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to "1" (peripheral function clock turned off during wait mode), or when the microcomputer is in low power dissipation mode, the fi, fiSIO and fAD clocks are turned off.

The fC32 clock is produced from the sub clock, and is used for timers A and B. This clock can be used when the sub clock is on.

10.3 Clock Output Function

During single-chip mode, the f8, f32 or fC clock can be output from the CLKOUT pin. Use the CM01 to CM00 bits in the CM0 register to select.

10.4 Power Control

Normal operating mode, wait mode and stop mode are provided as the power consumption control. All mode states, except wait mode and stop mode, are called normal operating mode in this document.

10.4.1 Normal Operating Mode

Normal operating mode is further classified into seven modes.

In normal operating mode, because the CPU clock and the peripheral function clocks both are on, the CPU and the peripheral functions are operating. Power control is exercised by controlling the CPU clock frequency. The higher the CPU clock frequency, the greater the processing capability. The lower the CPU clock frequency, the smaller the power consumption in the chip. If the unnecessary oscillator circuits are turned off, the power consumption is further reduced.

Before the clock sources for the CPU clock can be switched over, the new clock source to which switched must be oscillating stably. If the new clock source is the main clock, sub clock or PLL clock, allow a sufficient wait time in a program until it becomes oscillating stably.

Note that operating modes cannot be changed directly from low speed or low power dissipation mode to onchip oscillator or on-chip oscillator low power dissipation mode. Nor can operating modes be changed directly from on-chip oscillator or on-chip oscillator low power dissipation mode to low speed or low power dissipation mode. Where the CPU clock source is changed from the on-chip oscillator to the main clock, change the operating mode to the medium speed mode (divided by 8 mode) after the clock was divided by 8 (the CM06 bit in the CM0 register was set to "1") in the on-chip oscillator mode.

10.4.1.1 High-speed Mode

The main clock divided by 1 provides the CPU clock. If the sub clock is on, fC32 can be used as the count source for Timers A and B.

10.4.1.2 PLL Operating Mode

The main clock multiplied by 2, 4, 6 or 8 provides the PLL clock, and this PLL clock serves as the CPU clock. If the sub clock is on, fC32 can be used as the count source for Timers A and B. PLL operating mode can be entered from high speed mode. If PLL operating mode is to be changed to wait or stop mode, first go to high speed mode before changing.

10.4.1.3 Medium-Speed Mode

The main clock divided by 2, 4, 8 or 16 provides the CPU clock. If the sub clock is on, fC32 can be used as the count source for Timers A and B.

10.4.1.4 Low-Speed Mode

The sub clock provides the CPU clock. The main clock is used as the clock source for the peripheral function clock when the CM21 bit in the CM2 register is set to "0" (on-chip oscillator turned off), and the on-chip oscillator clock is used when the CM21 bit is set to "1" (on-chip oscillator oscillating). The fC32 clock can be used as the count source for Timers A and B.

10.4.1.5 Low Power Dissipation Mode

In this mode, the main clock is turned off after being placed in low speed mode. The sub clock provides the CPU clock. The fC32 clock can be used as the count source for Timers A and B.

Simultaneously when this mode is selected, the CM06 bit becomes "1" (divided by 8 mode). In the low power dissipation mode, do not change the CM06 bit. Consequently, the medium speed (divided by 8) mode is to be selected when the main clock is operated next

10.4.1.6 On-chip Oscillator Mode

The on-chip oscillator clock divided by 1 (undivided), 2, 4, 8 or 16 provides the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. If the sub clock is on, fC32 can be used as the count source for Timers A and B. When the operating mode is returned to the high and medium speed modes, set the CM06 bit in the CM0 register to "1" (divided by 8 mode).

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10.4.1.7 On-chip Oscillator Low Power Dissipation Mode

The main clock is turned off after being placed in on-chip oscillator mode. The CPU clock can be selected as in the on-chip oscillator mode. The on-chip oscillator clock is the clock source for the peripheral function clocks. If the sub clock is on, fC32 can be used as the count source for Timers A and B.

Modes		CM2 Register	CM1	Register		CM0 R	egister	
		CM21	CM11	CM17, CM16	CM07	CM06	CM05	CM04
PLL Operating	Mode	0	1	00b	0	0	0	_
High-Speed M	ode	0	0	00b	0	0	0	-
Medium-	divided by 2	0	0	01b	0	0	0	-
Speed Mode	divided by 4	0	0	10b	0	0	0	_
	divided by 8	0	0	-	0	1	0	-
	divided by 16	0	0	11b	0	0	0	-
Low-Speed M	ode	-	0	-	1	-	0	1
Low Power Dis	ssipation Mode	0	0	-	1	1(1)	1(1)	1
On-chip	divided by 1	1	0	00b	0	0	0	-
Oscillator	divided by 2	1	0	01b	0	0	0	-
Mode	divided by 4	1	0	10b	0	0	0	-
	divided by 8	1	0	-	0	1	0	-
	divided by 16	1	0	11b	0	0	0	-
On-chip Oscill Dissipation Mo	ator Low Power	1	0	(NOTE 2)	0	(NOTE 2)	1	_

Table 10.3	Setting Clock Related Bit and Modes
------------	-------------------------------------

NOTES:

-: "0" or "1"

- 1. When the CM05 bit is set to "1" (main clock turned off) in low-speed mode, the mode goes to low power dissipation mode and CM06 bit is set to "1" (divided by 8 mode) simultaneously.
- 2. The divide-by-n value can be selected the same way as in on-chip oscillator mode.

10.4.2 Wait Mode

In wait mode, the CPU clock is turned off, so are the CPU (because operated by the CPU clock) and the watchdog timer. However, if the PM22 bit in the PM2 register is "1" (on-chip oscillator clock for the watchdog timer count source), the watchdog timer remains active. Because the main clock, sub clock and on-chip oscillator clock all are on, the peripheral functions using these clocks keep operating.

10.4.2.1 Peripheral Function Clock Stop Function

If the CM02 bit in the CM0 register is "1" (peripheral function clocks turned off during wait mode), the f1, f2, f8, f32, f1SIO, f8SIO, f32SIO and fAD clocks are turned off when in wait mode, with the power consumption reduced that much. However, fC32 remains on.

10.4.2.2 Entering Wait Mode

The microcomputer is placed into wait mode by executing the WAIT instruction.

When the CM11 bit = 1 (CPU clock source is the PLL clock), be sure to clear the CM11 bit in the CM1 register to "0" (CPU clock source is the main clock) before going to wait mode. The power consumption of the chip can be reduced by clearing the PLC07 bit in the PLC0 register to "0" (PLL stops).

10.4.2.3 Pin Status During Wait Mode

Table 10.4 lists Pin Status During Wait Mode.

Pin		Memory Expansion Mode Microprocessor Mode	Single-Chip Mode	
A0 to A19, BHE	D0 to D15, $\overline{CS0}$ to $\overline{CS3}$,	Retains status before wait mode	Does not become a bus control pin	
RD, WR, W	/RL, WRH	"H"		
HLDA, BCI	_K	"H"		
ALE		"L"		
I/O ports		Retains status before wait mode	Retains status before wait mode	
CLKOUT	When fC selected	Does not become a CLKOUT pin	Does not stop	
	When f8, f32 selected		Does not stop when the CM02 bit is "0". When the CM02 bit is "1", the status immediately prior to entering wait mode is maintained.	

Table 10.4 Pin Status During Wait Mode

10.4.2.4 Exiting Wait Mode

The microcomputer is moved out of wait mode by a hardware reset, $\overline{\text{NMI}}$ interrupt, low voltage detection interrupt or peripheral function interrupt.

If the microcomputer is to be moved out of exit wait mode by a hardware reset, $\overline{\text{NMI}}$ interrupt or low voltage detection interrupt, set the peripheral function interrupt priority ILVL2 to ILVL0 bits to "000b" (interrupts disabled) before executing the WAIT instruction.

The peripheral function interrupts are affected by the CM02 bit. If CM02 bit is "0" (peripheral function clocks not turned off during wait mode), peripheral function interrupts can be used to exit wait mode. If CM02 bit is "1" (peripheral function clocks turned off during wait mode), the peripheral functions using the peripheral function clocks stop operating, so that only the peripheral functions clocked by external signals can be used to exit wait mode.

Interrupt	CM02=0	CM02=1
NMI Interrupt	Can be used	Can be used
Serial Interface Interrupt	Can be used when operating with internal or external clock	Can be used when operating with external clock
Key Input Interrupt	Can be used	Can be used
A/D Conversion Interrupt	Can be used in one-shot mode or single sweep mode	–(Do not use)
Timer A Interrupt Timer B Interrupt	Can be used in all modes	Can be used in event counter mode or when the count source is fC32
INT Interrupt	Can be used	Can be used
Low Voltage Detection Interrupt	Can be used	Can be used

Table 10.5 Interrupts to Exit Wait Mode and Use Conditions

Table 10.5 lists the Interrupts to Exit Wait Mode and Use Conditions.

If the microcomputer is to be moved out of wait mode by a peripheral function interrupt, set up the following before executing the WAIT instruction.

(1) Set the ILVL2 to ILVL0 bits in the interrupt control register, for peripheral function interrupts used to exit wait mode.

The ILVL2 to ILVL0 bits in all other interrupt control registers, for peripheral function interrupts not used to exit wait mode, are set to "000b" (interrupt disable).

- (2) Set the I flag to "1".
- (3) Start operating the peripheral functions used to exit wait mode. When the peripheral function interrupt is used, an interrupt routine is performed as soon as an interrupt request is acknowledged and the CPU clock is supplied again.

When the microcomputer exits wait mode by the peripheral function interrupt, the CPU clock is the same clock as the CPU clock executing the WAIT instruction.

10.4.3 Stop Mode

In stop mode, all oscillator circuits are turned off, so are the CPU clock and the peripheral function clocks. Therefore, the CPU and the peripheral functions clocked by these clocks stop operating. The least amount of power is consumed in this mode. If the voltage applied to VCC1 and VCC2 pins is VRAM or more, the internal RAM is retained. When applying 2.7 or less voltage to VCC1 and VCC2 pins, make sure VCC1 \geq VCC2 \geq VRAM.

However, the peripheral functions clocked by external signals keep operating. The following interrupts can be used to exit stop mode. Table 10.6 lists Interrupts to Stop Mode and Use Conditions

Interrupt	Condition
NMI Interrupt	Can be used
Key Input Interrupt	Can be used
INT Interrupt	Can be used
Timer A Interrupt Timer B Interrupt	Can be used (when counting external pulses in event counter mode)
Serial Interface Interrupt	Can be used (when external clock is selected)
Low Voltage Detection Interrupt	Can be used (Refer to 6.1 Low Voltage Detection Interrupt for an Operating Condition)

 Table 10.6
 Interrupts to Stop Mode and Use Conditions

10.4.3.1 Entering Stop Mode

The microcomputer is placed into stop mode by setting the CM10 bit in the CM1 register to "1" (all clocks turned off). At the same time, the CM06 bit in the CM0 register is set to "1" (divide-by-8 mode) and the CM15 bit in the CM1 register is set to "1" (main clock oscillator circuit drive capability high).

Before entering stop mode, set the CM20 bit in the CM2 register to "0" (oscillation stop, re-oscillation detection function disable).

Also, if the CM11 bit in the CM1 register is "1" (PLL clock for the CPU clock source), set the CM11 bit to "0" (main clock for the CPU clock source) and the PLC07 bit in the PLC0 register to "0" (PLL turned off) before entering stop mode.

10.4.3.2 Pin Status in Stop Mode

Table 10.7 lists Pin Status in Stop Mode.

	Pin	Memory Expansion Mode Microprocessor Mode	Single-Chip Mode
A0 to A19, D0 to D15, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, BHE		Retains status before stop mode	Does not become a bus control pin
RD, WR, W	RL, WRH	"H"	
HLDA, BCLK		"H"	
ALE		indeterminate	
I/O ports		Retains status before stop mode	Retains status before stop mode
CLKOUT	When fC selected	Does not become a CLKOUT pin	"Н"
	When f8, f32 selected		Retains status before stop mode

Table 10.7 F	Pin Status in	Stop Mode
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10.4.3.3 Exiting Stop Mode

Stop mode is exited by a hardware reset, $\overline{\text{NMI}}$ interrupt, low voltage detection interrupt or peripheral function interrupt.

When the hardware reset, $\overline{\text{NMI}}$ interrupt or low voltage detection interrupt is used to exit stop mode, set all ILVL2 to ILVL0 bits in the interrupt control registers for the peripheral function interrupt to "000b" (interrupt disabled) before setting the CM10 bit to "1".

When the peripheral function interrupt is used to exit stop mode, set the CM10 bit to "1" after the following settings are completed.

- Set the ILVL2 to ILVL0 bits in the interrupt control registers to decide the peripheral priority level of the peripheral function interrupt.
 Set the interrupt priority levels of the interrupts, not being used to exit stop mode, to "0" by setting the
 - all ILVL2 to ILVL0 bits to "000b".
- (2) Set the I flag to "1".
- (3) Start operation of peripheral function being used to exit wait mode.

When exiting stop mode by the peripheral function interrupt, the interrupt routine is performed when an interrupt request is generated and the CPU clock is supplied again.

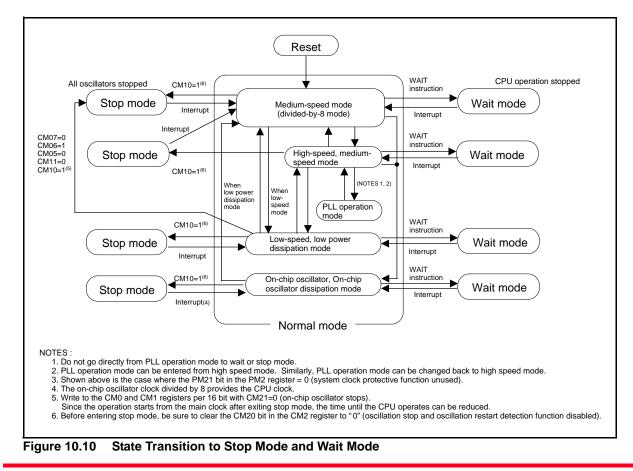
When stop mode is exited by the peripheral function interrupt or \overline{NMI} interrupt, the CPU clock source is as follows, in accordance with the CPU clock source setting before the microcomputer had entered stop mode.

- When the sub clock is the CPU clock before entering stop mode : Sub clock
- When the main clock is the CPU clock source before entering stop mode : Main clock divided by 8
- When the on-chip oscillator clock is the CPU clock source before entering stop mode

: On-chip oscillator clock divided by 8

Figure 10.10 shows the State Transition from Normal Operating Mode to Stop Mode and Wait Mode. Figure 10.11 shows the State Transition in Normal Operating Mode.

Table 10.8 shows a state transition matrix describing Allowed Transition and Setting. The vertical line shows current state and horizontal line shows state after transition.



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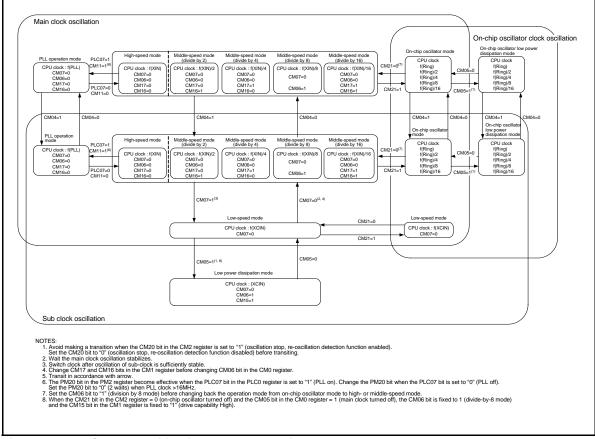


Figure 10.11 State Transition in Normal Operating Mode

		State After Transition							
		High-Speed Mode, Middle-Speed Mode	Low-Speed Mode ⁽²⁾	Low Power Dissipation Mode	PLL Operating Mode ⁽²⁾	On-chip Oscillator Mode	On-chip Oscillator Low Power Dissipation Mode	Stop Mode	Wait Mode
Current State	High-Speed Mode, Middle-Speed Mode	(NOTE 8)	(9) ^(NOTE 7)	-	(13) (NOTE 3)	(15)	-	(16) (NOTE 1)	(17)
	Low-Speed Mode ⁽²⁾	(8)		(11) (NOTE 1, 6)	-	-	-	(16) (NOTE 1)	(17)
	Low Power Dissipation Mode	-	(10)		-	-	-	(16) (NOTE 1)	(17)
	PLL Operating Mode ⁽²⁾	(12) ^(NOTE 3)	_	_		-	-	-	-
	On-chip Oscillator Mode	(14) ^(NOTE 4)	-	_	-	(NOTE 8)	(11) ^(NOTE 1)	(16) (NOTE 1)	(17)
	On-chip Oscillator Low Power Dissipation Mode	_	-	-	-	(10)	(NOTE 8)	(16) (NOTE 1)	(17)
	Stop Mode	(18) ^(NOTE 5)	(18)	(18)	-	(18) (NOTE 5)	(18) ^(NOTE 5)		_
	Wait Mode	(18)	(18)	(18)	-	(18)	(18)	-	

Allowed Transition and Setting⁽⁹⁾ Table 10.8

NOTES:

-: Cannot transit

1. Avoid making a transition when the CM20 bit is set in to "1" (oscillation stop, re-oscillation detection function enabled).

Set the CM20 bit to "0" (oscillation stop, re-oscillation detection function disabled) before transiting. 2. On-chip oscillator clock oscillates and stops in low-speed mode. In this mode, the on-chip oscillator can be used as peripheral function clock. Sub clock oscillates and stops in PLL operating mode. In this mode, sub clock can be used as peripheral function clock.

PLL operating mode can only be entered from and changed to high-speed mode.
 Set the CM06 bit to "1" (division by 8 mode) before transiting from on-chip oscillator mode to high- or middle-speed mode.

When exiting stop mode, the CM0S6 bit is set to "1" (division by 8 mode). 5.

6. If the CM05 bit set to "1" (main clock stop), then the CM06 bit is set to "1" (division by 8 mode).

7. A transition can be made only when sub clock is oscillating.

8. State transitions within the same mode (divide-by-n values changed or subclock oscillation turned on or off) are shown in the table below.

			Sub Clock Oscillating					Sub Clock Turned Off			
		No Division	Divided by 2	Divided by 4	Divided by 8	Divided by 16	No Division	Divided by 2	Divided by 4	Divided by 8	Divided by 16
	No Division		(4)	(5)	(7)	(6)	(1)	-	-	-	-
ъg	Divided by 2	(3)		(5)	(7)	(6)	-	(1)	-	-	-
Sub clock Oscillating	Divided by 4	(3)	(4)		(7)	(6)	-	-	(1)	-	-
Sul Osc	Divided by 8	(3)	(4)	(5)		(6)	-	-	-	(1)	-
	Divided by 16	(3)	(4)	(5)	(7)		-	-	-	-	(1)
	No Division	(2)	-	-	-	-		(4)	(5)	(7)	(6)
ЗĘ	Divided by 2	-	(2)	-	-	-	(3)		(5)	(7)	(6)
Sub clock Turned Off	Divided by 4	-	-	(2)	-	-	(3)	(4)		(7)	(6)
Sul Tun	Divided by 8	-	-	-	(2)	-	(3)	(4)	(5)		(6)
	Divided by 16	-	-	-	_	(2)	(3)	(4)	(5)	(7)	

9. (): setting method. See the following table.

	Setting	Operation		Setting	Operation
(1)	CM04 = 0	Sub clock turned off	(10)	CM05 = 0	Main clock oscillating
(2)	CM04 = 1	Sub clock oscillating	(11)	CM05 = 1	Main clock turned off
(3)	CM06 = 0, CM17 = 0, CM16 = 0	CPU clock no division mode	(12)	PLC07=0, CM11=0	Main clock selected
(4)	CM06 = 0, CM17 = 0, CM16 = 1	CPU clock division by 2 mode	(13)	PLC07=1, CM11=1	PLL clock selected
(5)	CM06 = 0, CM17 = 1, CM16 = 0	CPU clock division by 4 mode	(14)	CM21=0	Main clock or PLL clock selected
(6)	CM06 = 0, CM17 = 1, CM16 = 1	CPU clock division by 16 mode	(15)	CM21=1	On-chip oscillator clock selected
(7)	CM06 = 1	CPU clock division by 8 mode	(16)	CM10=1	Transition to stop mode
(8)	CM07 = 0	Main clock, PLL clock, or on-chip oscillator clock selected	(17)	Wait Instruction	Transition to wait mode
(9)	CM07 = 1	Sub clock selected	(18)	Hardware Interrupt	Exit stop mode or wait mode

: Bits in CM2 register

: Bits in PLC0 register

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CM20, CM21 PLC07

-: Cannot transit

10.5 System Clock Protection Function

The system clock protection function prohibits the CPU clock from changing clock sources when the main clock is selected the CPU clock source. This prevents the CPU clock from stopping should the program crash. This function is available when the main clock is selected as the CPU clock source.

When the PM21 bit in the PM2 register is set to "1" (clock change disabled), the following bits cannot be written to:

- The CM02 bit, CM05 bit and CM07 bit in the CM0 register
- The CM10 bit and CM11 bit in the CM1 register
- The CM20 bit in the CM2 register
- All bits in the PLC0 register

When using the system clock protection function, set the CM05 bit in the CM0 register to "0" (main clock oscillation) and CM07 bit to "0" (main clock as CPU clock source) and follow the procedure below.

- (1) Set the PRC1 bit in the PRCR register to "1" (write enable).
- (2) Set the PM21 bit in the PM2 register to "1" (protects the clock).
- (3) Set the PRC1 bit in the PRCR register to "0" (write disable).

When the PM21 bit is set to "1," do not execute the WAIT instruction.

10.6 Oscillation Stop and Re-oscillation Detect Function

The oscillation stop and re-oscillation detect function is such that main clock oscillation circuit stop and reoscillation are detected. At oscillation stop, re-oscillation detection, reset or oscillation stop, re-oscillation detection interrupt are generated. Which is to be generated can be selected using the CM27 bit in the CM2 register. The oscillation stop detection function can be enabled and disabled by the CM20 bit in the CM2 register. Table 10.9 lists a Specification Overview of Oscillation Stop and Re-Oscillation Detect Function.

 Table 10.9
 Specification Overview of Oscillation Stop and Re-Oscillation Detect Function

Item	Specification
Oscillation Stop Detectable Clock and Frequency Bandwidth	f(XIN)≥2 MHz
Enabling Condition for Oscillation Stop, Re-Oscillation Detection Function	Set CM20 bit to "1" (enable)
Operation at Oscillation Stop, Re-Oscillation Detection	 Reset occurs (when CM27 bit =0) Oscillation stop, re-oscillation detection interrupt generated (when CM27 bit =1)

10.6.1 Operation When CM27 bit = 0 (Oscillation Stop Detection Reset)

Where main clock stop is detected when the CM20 bit is "1" (oscillation stop, re-oscillation detection function enabled), the microcomputer is initialized, coming to a halt (oscillation stop reset; refer to **4. Special Function Register (SFR)**, **5. Reset**).

This status is reset with hardware reset 1 or hardware reset 2. Also, even when re-oscillation is detected, the microcomputer can be initialized and stopped; it is, however, necessary to avoid such usage (During main clock stop, do not set the CM20 bit to "1" and the CM27 bit to "0").

10.6.2 Operation When CM27 bit = 0 (Oscillation Stop and Re-oscillation Detect Interrupt)

Where the main clock corresponds to the CPU clock source and the CM20 bit is "1" (oscillation stop and reoscillation detect function enabled), the system is placed in the following state if the main clock comes to a halt:

- Oscillation stop and re-oscillation detect interrupt request occurs.
- The on-chip oscillator starts oscillation, and the on-chip oscillator clock becomes the clock source

for CPU clock and peripheral functions in place of the main clock.

- CM21 bit = 1 (on-chip oscillator clock for CPU clock source and clock source of peripheral function.)
- CM22 bit = 1 (main clock stop detected)
- CM23 bit = 1 (main clock stopped)

Where the PLL clock corresponds to the CPU clock source and the CM20 bit is "1," the system is placed in the following state if the main clock comes to a halt: Since the CM21 bit remains unchanged, set it to "1" (on-chip oscillator clock) inside the interrupt routine.

- Oscillation stop and re-oscillation detect interrupt request occurs.
- CM22 bit = 1 (main clock stop detected)
- CM23 bit = 1 (main clock stopped)
- CM21 bit remains unchanged

Where the CM20 bit is "1", the system is placed in the following state if the main clock re-oscillates from the stop condition:

- Oscillation stop and re-oscillation detect interrupt request occurs.
- CM22 bit = 1 (main clock re-oscillation detected)
- CM23 bit = 0 (main clock oscillation)
- CM21 bit remains unchanged

10.6.3 How to Use Oscillation Stop and Re-oscillation Detect Function

- The oscillation stop and re-oscillation detect interrupt shares the vector with the watchdog timer interrupt and low voltage detection interrupt. If the oscillation stop, re-oscillation detection and watchdog timer interrupts both are used, read the CM22 bit in an interrupt routine to determine which interrupt source is requesting the interrupt.
- Where the main clock re-oscillated after oscillation stop, the clock source for the CPU clock and peripheral functions must be switched to the main clock in the program. Figure 10.12 shows the Procedure to Switch Clock Source From On-chip Oscillator to Main Clock.
- Simultaneously with oscillation stop, re-oscillation detection interrupt occurrence, the CM22 bit becomes "1". When the CM22 bit is set at "1," oscillation stop, re-oscillation detection interrupt are disabled. By setting the CM22 bit to "0" in the program, oscillation stop, re-oscillation detection interrupt are enabled.
- If the main clock stops during low speed mode where the CM20 bit is "1", an oscillation stop, re-oscillation detection interrupt request is generated. At the same time, the on-chip oscillator starts oscillating. In this case, although the CPU clock is derived from the sub clock as it was before the interrupt occurred, the peripheral function clocks now are derived from the on-chip oscillator clock.
- To enter wait mode while using the oscillation stop, re-oscillation detection function, set the CM02 bit to "0" (peripheral function clocks not turned off during wait mode).
- Since the oscillation stop, re-oscillation detection function is provided in preparation for main clock stop due to external factors, set the CM20 bit to "0" (Oscillation stop, re-oscillation detection function disabled) where the main clock is stopped or oscillated in the program, that is where the stop mode is selected or the CM05 bit is altered.
- This function cannot be used if the main clock frequency is 2 MHz or less. In that case, set the CM20 bit to "0".

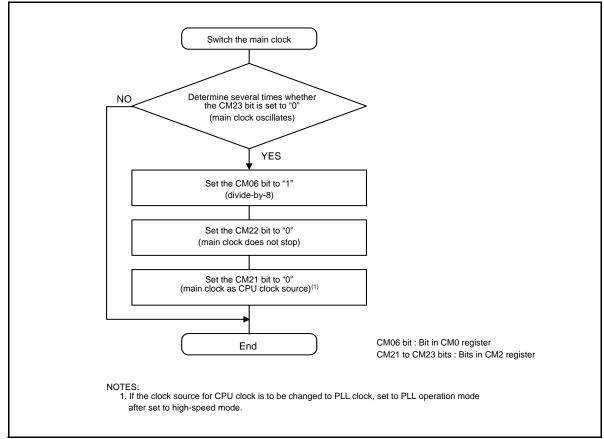


Figure 10.12 Procedure to Switch Clock Source From On-chip Oscillator to Main Clock

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11. Protection

Note

The M16C/62PT do not use the PRC3 bit in the PRCR register.

In the event that a program runs out of control, this function protects the important registers so that they will not be rewritten easily. Figure 11.1 shows the PRCR Register. The following lists the registers protected by the PRCR register.

- The PRC0 bit protects the CM0, CM1, CM2, PLC0 and PCLKR registers;
- The PRC1 bit protects the PM0, PM1, PM2, TB2SC, INVC0 and INVC1 registers;
- The PRC2 bit protects the PD9, S3C and S4C registers;
- The PRC3 bit protects the VCR2 and D4INT registers.

Set the PRC2 bit to "1" (write enabled) and then write to any address, and the PRC2 bit will be cleared to "0" (write protected). The registers protected by the PRC2 bit should be changed in the next instruction after setting the PRC2 bit to "1". Make sure no interrupts or DMA transfers will occur between the instruction in which the PRC2 bit is set to "1" and the next instruction. The PRC0, PRC1 and PRC3 bits are not automatically cleared to "0" by writing to any address. They can only be cleared in a program.

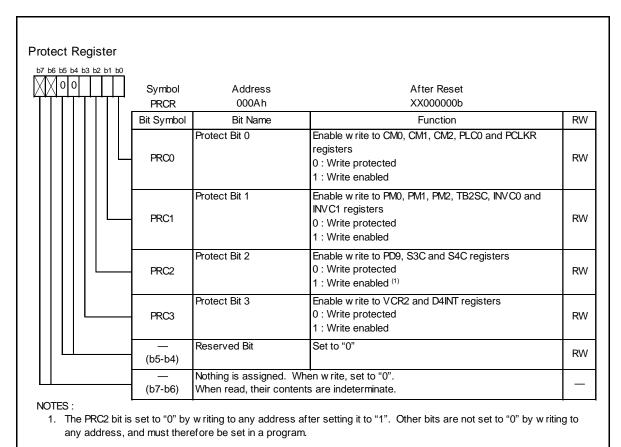


Figure 11.1 PRCR Register

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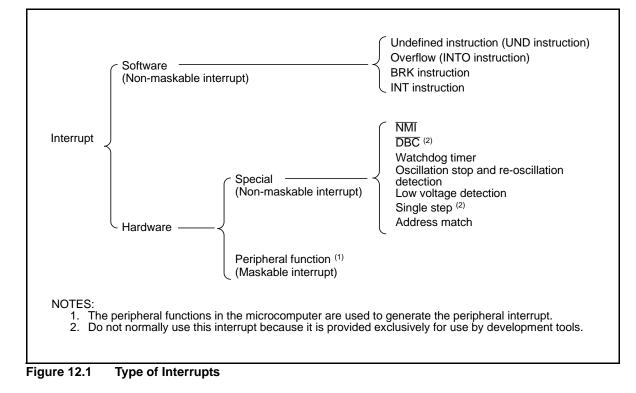
12. Interrupt

Note

The M16C/62P (80-pin version) do not use INT3 to INT5 interrupt of peripheral function. The M16C/62PT (100-pin version) do not use low voltage detection interrupt. The M16C/62PT (80-pin version) do not use low voltage detection interrupt and INT3 to INT5 interrupt of peripheral function.

12.1 Type of Interrupts

Figure 12.1 shows Type of Interrupts.



- Maskable Interrupt : An interrupt which can be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority **can be changed** by priority level.
- Non-Maskable Interrupt : An interrupt which cannot be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority **cannot be changed** by priority level.

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12.2 Software Interrupts

A software interrupt occurs when executing certain instructions. Software interrupts are non-maskable interrupts.

12.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt occurs when executing the UND instruction.

12.2.2 Overflow Interrupt

An overflow interrupt occurs when executing the INTO instruction with the O flag in the FLG register set to "1" (the operation resulted in an overflow). The following are instructions whose O flag changes by arithmetic: ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, SUB

12.2.3 BRK Interrupt

A BRK interrupt occurs when executing the BRK instruction.

12.2.4 INT Instruction Interrupt

An INT instruction interrupt occurs when executing the INT instruction. Software interrupt Nos. 0 to 63 can be specified for the INT instruction. Because software interrupt Nos. 4 to 31 are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.

In software interrupt Nos. 0 to 31, the U flag is saved to the stack during instruction execution and is cleared to "0" (ISP selected) before executing an interrupt sequence. The U flag is restored from the stack when returning from the interrupt routine. In software interrupt Nos. 32 to 63, the U flag does not change state during instruction execution, and the SP then selected is used.

12.3 Hardware Interrupts

Hardware interrupts are classified into two types - special interrupts and peripheral function interrupts.

12.3.1 Special Interrupts

Special interrupts are non-maskable interrupts.

12.3.1.1 NMI Interrupt

An <u>NMI</u> interrupt is generated when input on the <u>NMI</u> pin changes state from high to low. For details about the <u>NMI</u> interrupt, refer to the **12.7** <u>NMI</u> Interrupt.

12.3.1.2 DBC Interrupt

Do not normally use this interrupt because it is provided exclusively for use by development tools.

12.3.1.3 Watchdog Timer Interrupt

Generated by the watchdog timer. Once a watchdog timer interrupt is generated, be sure to initialize the watchdog timer. For details about the watchdog timer, refer to the **13. Watchdog Timer**.

12.3.1.4 Oscillation Stop and Re-oscillation Detection Interrupt

Generated by the oscillation stop and re-oscillation detection function. For details about the oscillation stop and re-oscillation detection function, refer to the **10. Clock Generation Circuit.**

12.3.1.5 12.3.1.5 Low Voltage Detection Interrupt

Generated by the voltage detection circuit. For details about the voltage detection circuit, refer to the **6. Voltage Detection Circuit**.

12.3.1.6 Single-Step Interrupt

Do not normally use this interrupt because it is provided exclusively for use by development tools.

12.3.1.7 Address Match Interrupt

An address match interrupt is generated immediately before executing the instruction at the address indicated by the RMAD0 to RMAD3 register that corresponds to one of the AIER0 or AIER1 bit in the AIER register or the AIER20 or AIER21 bit in the AIER2 register which is "1" (address match interrupt enabled). For details about the address match interrupt, refer to the **12.9 Address Match Interrupt**.

12.3.2 Peripheral Function Interrupts

The peripheral function interrupt occurs when a request from the peripheral functions in the microcomputer is acknowledged. The peripheral function interrupt is a maskable interrupt. See **Table 12.2 Relocatable Vector Tables** about how the peripheral function interrupt occurs. Refer to the descriptions of each function for details.

12.4 Interrupts and Interrupt Vector

One interrupt vector consists of 4 bytes. Set the start address of each interrupt routine in the respective interrupt vectors. When an interrupt request is accepted, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows the Interrupt Vector.

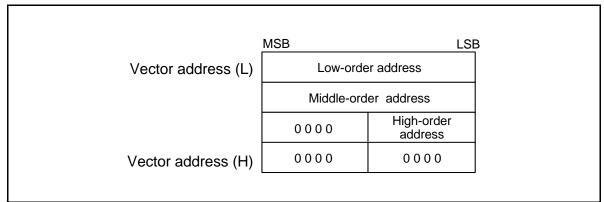


Figure 12.2 Interrupt Vector

12.4.1 Fixed Vector Tables

The fixed vector tables are allocated to the addresses from FFFDCh to FFFFFh. Table 12.1 lists the Fixed Vector Tables. In the flash memory version of microcomputer, the vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to the **22.2 Functions To Prevent Flash Memory from Rewriting**.

Interrupt Source	Vector Table Addresses Address (L) to Address (H)	Reference	
Undefined Instruction (UND instruction)	FFFDCh to FFFDFh	M16C/60, M16C/20 Series	
Overflow (INTO instruction)	FFFE0h to FFFE3h	software manual	
BRK Instruction ⁽²⁾	FFFE4h to FFFE7h		
Address Match	FFFE8h to FFFEBh	12.9 Address Match Interrupt	
Single Step ⁽¹⁾	FFFECh to FFFEFh		
Watchdog Timer, Oscillation Stop and Re-Oscillation Detection, Low Voltage Detection	FFFF0h to FFFF3h	 13. Watchdog Timer 10. Clock Generation Circuit 6. Voltage Detection Circuit 	
DBC ⁽¹⁾	FFFF4h to FFFF7h		
NMI	FFFF8h to FFFFBh	12.7 NMI interrupt	
Reset	FFFFCh to FFFFFh	5. Reset	

NOTES:

- 1. Do not normally use this interrupt because it is provided exclusively for use by development tools.
- 2. If the contents of address FFFE7h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.

12.4.2 Relocatable Vector Tables

The 256 bytes beginning with the start address set in the INTB register comprise a reloacatable vector table area. Table 12.2 lists the Relocatable Vector Tables. Setting an even address in the INTB register results in the interrupt sequence being executed faster than in the case of odd addresses.

Interrupt Source	Vector Address ⁽¹⁾ Address (L) to Address (H)	Software Interrupt Number	Reference
BRK Instruction ⁽⁵⁾	+0 to +3 (0000h to 0003h)	0	M16C/60, M16C/20
-(Reserved)		1 to 3	Series software manual
INT3	+16 to +19 (0010h to 0013h)	4	12.6 INT interrupt
Timer B5	+20 to +23 (0014h to 0017h)	5	15. Timers
Timer B4, UART1 Bus Collision Detect (4, 6)	+24 to +27 (0018h to 001Bh)	6	15. Timers
Timer B3, UART0 Bus Collision Detect (4, 6)	+28 to +31 (001Ch to 001Fh)	7	17. Serial Interface
SI/O4, INT5 (2)	+32 to +35 (0020h to 0023h)	8	12.6 INT interrupt
SI/O3, INT4 ⁽²⁾	+36 to +39 (0024h to 0027h)	9	17. Serial Interface
UART 2 Bus Collision Detection ⁽⁶⁾	+40 to +43 (0028h to 002Bh)	10	17. Serial Interface
DMA0	+44 to +47 (002Ch to 002Fh)	11	14. DMAC
DMA1	+48 to +51 (0030h to 0033h)	12	-
Key Input Interrupt	+52 to +55 (0034h to 0037h)	13	12.8 Key Input Interrupt
A/D	+56 to +59 (0038h to 003Bh)	14	18. A/D Converter
UART2 Transmit, NACK2 (3)	+60 to +63 (003Ch to 003Fh)	15	17. Serial Interface
UART2 Receive, ACK2 ⁽³⁾	+64 to +67 (0040h to 0043h)	16	
UART0 Transmit, NACK0 (3)	+68 to +71 (0044h to 0047h)	17	
UART0 Receive, ACK0 ⁽³⁾	+72 to +75 (0048h to 004Bh)	18	
UART1 Transmit, NACK1 (3)	+76 to +79 (004Ch to 004Fh)	19	
UART1 Receive, ACK1 ⁽³⁾	+80 to +83 (0050h to 0053h)	20	
Timer A0	+84 to +87 (0054h to 0057h)	21	15. Timers
Timer A1	+88 to +91 (0058h to 005Bh)	22	
Timer A2	+92 to +95 (005Ch to 005Fh)	23	
Timer A3	+96 to +99 (0060h to 0063h)	24	-
Timer A4	+100 to +103 (0064h to 0067h)	25	
Timer B0	+104 to +107 (0068h to 006Bh)	26	
Timer B1	+108 to +111 (006Ch to 006Fh)	27	
Timer B2	+112 to +115 (0070h to 0073h)	28	
INTO	+116 to +119 (0074h to 0077h)	29	12.6 INT interrupt
INT1	+120 to +123 (0078h to 007Bh)	30	
INT2	+124 to +127 (007Ch to 007Fh)	31	1
Software Interrupt (5)	+128 to +131 (0080h to 0083h)	32	M16C/60, M16C/20
	to	to	Series software manual
	+252 to +255 (00FCh to 00FFh)	63	

Table 12.2 Relocatable Vector Tables	Table 12.2	Relocatable	Vector	Tables
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NOTES:

- 2. Use the IFSR6 and IFSR7 bits in the IFSR register to select.
- 3. During I²C mode, NACK and ACK interrupts comprise the interrupt source.
- 4. Use the IFSR26 and IFSR27 bits in the IFSR2A register to select.
- 5. These interrupts cannot be disabled using the I flag.
- 6. Bus collision detection : During IE mode, this bus collision detection constitutes the factor of an interrupt.

During I²C mode, however, a start condition or a stop condition detection constitutes the factor of an interrupt.

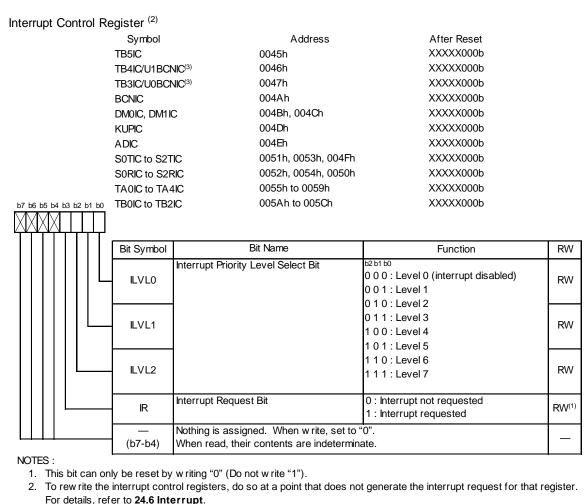
^{1.} Address relative to address in INTB.

12.5 **Interrupt Control**

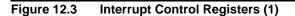
The following describes how to enable/disable the maskable interrupts, and how to set the priority in which order they are accepted. What is explained here does not apply to nonmaskable interrupts.

Use the I flag in the FLG register, IPL, and ILVL2 to ILVL0 bits in the each interrupt control register to enable/ disable the maskable interrupts. Whether an interrupt is requested is indicated by the IR bit in the each interrupt control register.

Figure 12.3 and Figure 12.4 show the Interrupt Control Registers.



3. Use the IFSR2A register to select.



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TT	52 b1 b0				
Ц		Symbol	Address	After Reset	
			0044h	XX00X000b	
		S4IC/INT5	-	XX00X000b	
		S3IC/INT4		XX00X000b	
		INTOIC to		XX00X000b	
		Bit Symbol	Bit Name	Function	RW
		ILVL0	Interrupt Priority Level Select Bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1	RW
		LVL1		0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5	RW
		LVL2		1 1 0 : Level 6 1 1 1 : Level 7	RW
		- IR	Interrupt Request Bit	0: Interrupt not requested 1: Interrupt requested	RW ⁽¹⁾
		POL	Polarity Select Bit	0 : Selects falling edge ^(3, 5) 1 : Selects rising edge	RW
		(b5)	Reserved Bit	Set to "0"	RW
		 (b7-b6)	Nothing is assigned. When w rite, a When read, their contents are inde		_

- 1. This bit can only be reset by writing "0" (Do not write "1").
- 2. To rew rite the interrupt control register, do so at a point that does not generate the interrupt request for that register. For details, refer to **24.6 Interrupt**.
- 3. If the IFSRi bit (i = 0 to 5) in the IFSR register are "1" (both edges), set the POL bit in the INTIC register to "0" (falling edge).
- 4. When the BYTE pin is low and the processor mode is memory expansion or microprocessor mode, set the LVL2 to ILVL0
- Set the POL bit in the S3IC or S4IC register to "0" (falling edge) when the IFSR6 bit in the IFSR register = 0 (SI/O3 selected) or IFSR7 bit = 0 (SI/O4 selected), respectively.

Figure 12.4 Interrupt Control Registers (2)

12.5.1 I Flag

The I flag enables or disables the maskable interrupt. Setting the I flag to "1" (= enabled) enables the maskable interrupt. Setting the I flag to "0" (= disabled) disables all maskable interrupts.

12.5.2 IR Bit

The IR bit is set to "1" (= interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted and the CPU branches to the corresponding interrupt vector, the IR bit is cleared to "0" (= interrupt not requested).

The IR bit can be cleared to "0" in a program. Note that do not write "1" to this bit.

12.5.3 ILVL2 to ILVL0 Bits and IPL

Interrupt priority levels can be set using the ILVL2 to ILVL0 bits.

Table 12.3 shows the Settings of Interrupt Priority Levels and Table 12.4 shows the Interrupt Priority Levels Enabled by IPL.

The following are conditions under which an interrupt is accepted:

- I flag = 1
- IR bit = 1
- interrupt priority level > IPL

The I flag, IR bit, ILVL2 to ILVL0 bits and IPL are independent of each other. In no case do they affect one another.

Table 12.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 Bits	Interrupt Priority Level	Priority Order
000b	Level 0 (interrupt disabled)	-
001b	Level 1	Low
010b	Level 2	
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	High

Table 12.4Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Levels
000b	Interrupt levels 1 and above are enabled
001b	Interrupt levels 2 and above are enabled
010b	Interrupt levels 3 and above are enabled
011b	Interrupt levels 4 and above are enabled
100b	Interrupt levels 5 and above are enabled
101b	Interrupt levels 6 and above are enabled
110b	Interrupt levels 7 and above are enabled
111b	All maskable interrupts are disabled

12.5.4 Interrupt Sequence

An interrupt sequence – what are performed over a period from the instant an interrupt is accepted to the instant the interrupt routine is executed – is described here.

If an interrupt occurs during execution of an instruction, the processor determines its priority when the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. If an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

The CPU behavior during the interrupt sequence is described below. Figure 12.5 shows Time Required for Executing Interrupt Sequence.

- (1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 000000h. Then, the IR bit applicable to the interrupt information is set to "0" (interrupt requested).
- (2) The FLG register, prior to an interrupt sequence, is saved to a temporary register ⁽¹⁾ within the CPU.
- (3) The I, D and U flags in the FLG register become as follows:
 - The I flag is set to "0" (interrupt disabled)
 - The D flag is set to "0" (single-step interrupt disabled)
 - The U flag is set to "0" (ISP selected)

However, the U flag does not change state if an INT instruction for software interrupt Nos. 32 to 63 is executed.

- (4) The temporary register ⁽¹⁾ within the CPU is saved to the stack.
- (5) The PC is saved to the stack.
- (6) The interrupt priority level of the acknowledged interrupt in IPL is set.
- (7) The start address of the relevant interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, an instruction is executed from the starting address of the interrupt routine.

NOTES:

1. Temporary register cannot be modified by users.

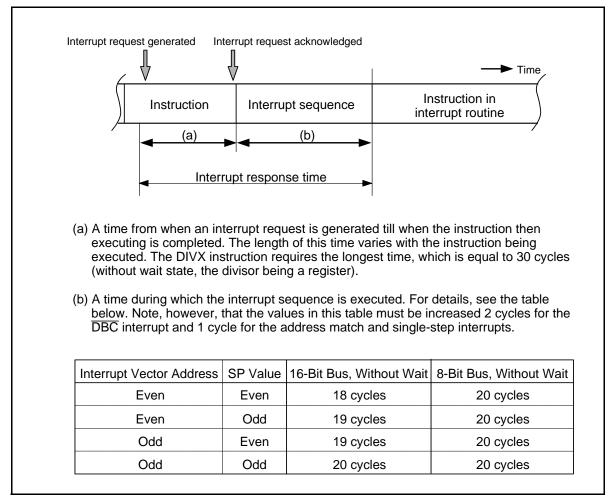
CPU clock	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
Address bus	Address Indeterminate ⁽¹⁾ SP-2 SP-4 vec vec+2 PC
Data bus	Interrupt Indeterminate ⁽¹⁾ SP-2 SP-4 vec vec+2 contents
RD	
WR ⁽²)
	S : The indeterminate state depends on the instruction queue buffer. A read cycle occurs when the instruction queue buffer is ready to accept instructions. The \overline{WR} signal timing shown here is for the case where the stack is located in the internal RAM.

Figure 12.5 Time Required for Executing Interrupt Sequence

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12.5.5 Interrupt Response Time

Figure 12.6 shows the Interrupt Response Time. The interrupt response or interrupt acknowledge time denotes a time from when an interrupt request is generated till when the first instruction in the interrupt routine is executed. Specifically, it consists of a time from when an interrupt request is generated till when the instruction then executing is completed ((a) on Figure 12.6) and a time during which the interrupt sequence is executed ((b) on Figure 12.6).





12.5.6 Variation of IPL when Interrupt Request is Accepted

When a maskable interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

When a software interrupt or special interrupt request is accepted, one of the interrupt priority levels listed in Table 12.5 is set in the IPL. Table 12.5 lists the IPL Level That is Set to IPL When a Software or Special Interrupt is Accepted.

Table 12.5 IPL Level That is Set to IPL When a Software or Special Interrupt is Accepted

Interrupt Sources	Level that is Set to IPL
Watchdog Timer, NMI, Oscillation Stop and Re-Oscillation Detection, Low Voltage Detection	7
Software, Address Match, DBC, Single-Step	Not changed

12.5.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved to the stack.

At this time, the 4 high-order bits of the PC and the 4 high-order (IPL) and 8 low-order bits in the FLG register, 16 bits in total, are saved to the stack first. Next, the 16 low-order bits of the PC are saved.

Figure 12.7 shows the Stack Status Before and After Acceptance of Interrupt Request.

The other necessary registers must be saved in a program at the beginning of the interrupt routine. Use the PUSHM instruction, and all registers except SP can be saved with a single instruction.

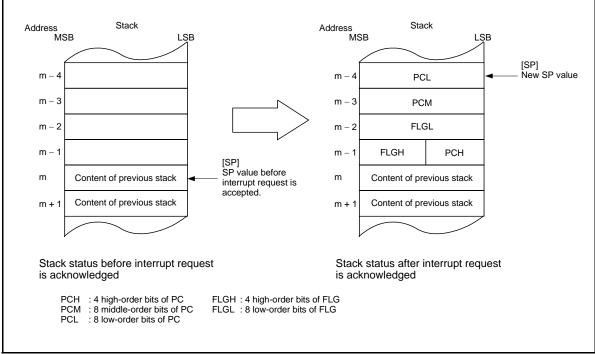


Figure 12.7 Stack Status Before and After Acceptance of Interrupt Request

The operation of saving registers carried out in the interrupt sequence is dependent on whether the SP $^{(1)}$, at the time of acceptance of an interrupt request, is even or odd. If the stack pointer $^{(1)}$ is even, the FLG register and the PC are saved,16 bits at a time. If odd, they are saved in two steps, 8 bits at a time. Figure 12.8 shows the Operation of Saving Register.

NOTES:

1. When any INT instruction in software numbers 32 to 63 has been executed, this is the SP indicated by the U flag. Otherwise, it is the ISP.

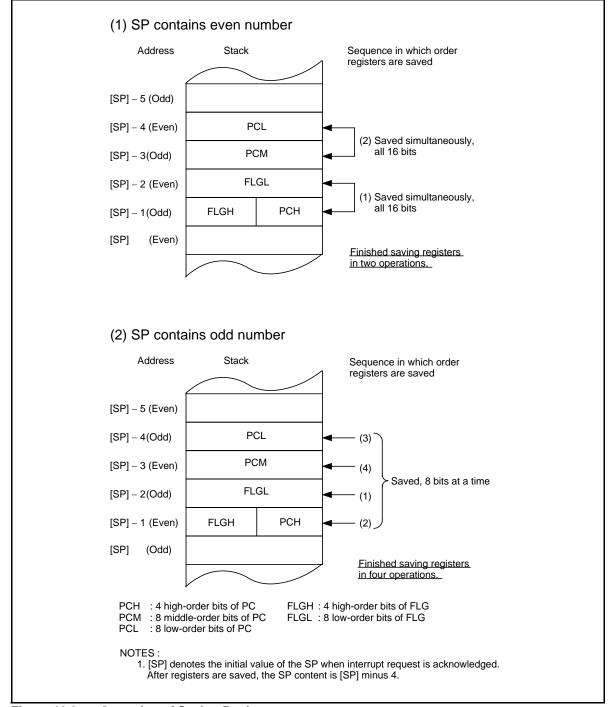


Figure 12.8 Operation of Saving Register

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12.5.8 Returning from an Interrupt Routine

The FLG register and PC in the state in which they were immediately before entering the interrupt sequence are restored from the stack by executing the REIT instruction at the end of the interrupt routine.

Thereafter the CPU returns to the program which was being executed before accepting the interrupt request. Return the other registers saved by a program within the interrupt routine using the POPM or similar instruction before executing the REIT instruction.

Register bank is switched back to the bank used prior to the interrupt sequence by the REIT instruction.

12.5.9 Interrupt Priority

If two or more interrupt requests are sampled at the same sampling points (a timing to detect whether an interrupt request is generated or not), the interrupt with the highest priority is acknowledged.

For maskable interrupts (peripheral functions interrupt), any desired priority level can be selected using the ILVL2 to ILVL0 bits. However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the highest priority interrupt accepted.

The watchdog timer and other special interrupts have their priority levels set in hardware. Figure 12.9 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, control branches invariably to the interrupt routine.

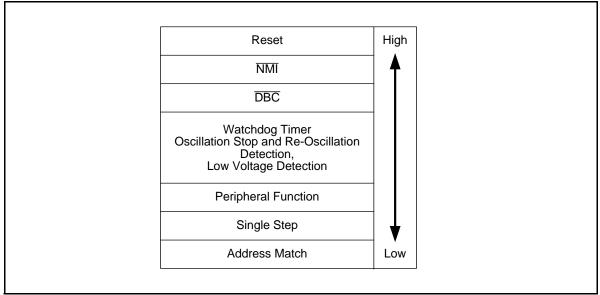


Figure 12.9 Hardware Interrupt Priority

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12.5.10 Interrupt Priority Level Select Circuit

The interrupt priority level select circuit selects the highest priority interrupt when two or more interrupt requests are sampled at the same sampling point.

Figure 12.10 shows the Interrupts Priority Select Circuit.

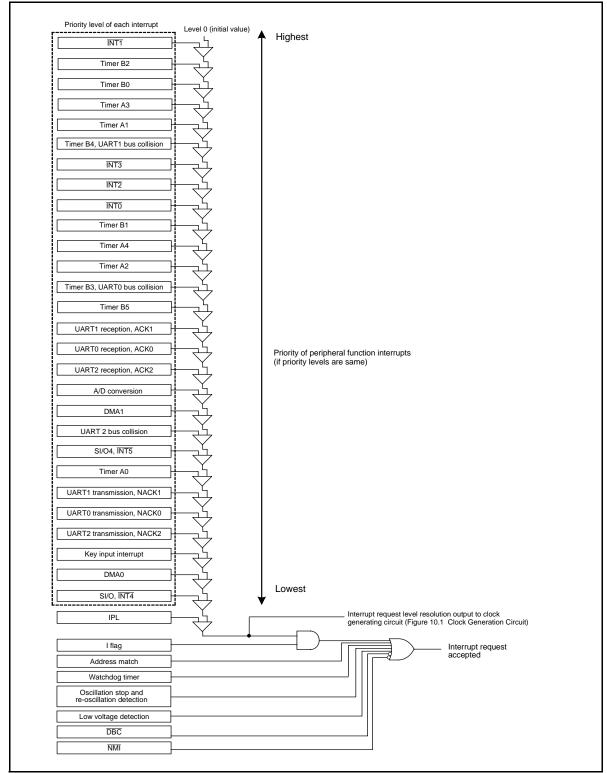


Figure 12.10 Interrupts Priority Select Circuit

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12.6 INT Interrupt

 $\overline{\text{INTi}}$ interrupt (i=0 to 5) is triggered by the edges of external inputs. The edge polarity is selected using the IFSRi bit in the IFSR register.

 $\overline{INT4}$ and $\overline{INT5}$ share the interrupt vector and interrupt control register with SI/O3 and SI/O4, respectively. To use the $\overline{INT4}$ interrupt, set the IFSR6 bit in the IFSR register to "1" (= $\overline{INT4}$). To use the $\overline{INT5}$ interrupt, set the IFSR7 bit in the IFSR register to "1" (= $\overline{INT5}$).

After modifying the IFSR6 or IFSR7 bit, clear the corresponding IR bit to "0" (= interrupt not requested) before enabling the interrupt.

Figure 12.11 shows the IFSR and IFSR2A Registers.

b7 b6 b5	5 b4 b3 l	b2 b1 b0				
			Symbol	Address	After Reset	
			IFSR	035Fh	00h	
			Bit Symbol	Bit Name	Function	RW
		L	IFSR0	INT0 Interrupt Polarity Switching Bit	0 : One edge 1 : Both edges ⁽¹⁾	RW
			IFSR1	INT1 Interrupt Polarity Switching Bit	0 : One edge 1 : Both edges ⁽¹⁾	RW
			IFSR2	INT2 Interrupt Polarity Switching Bit	0 : One edge 1 : Both edges ⁽¹⁾	RW
			IFSR3	INT3 Interrupt Polarity Switching Bit	0 : One edge 1 : Both edges ⁽¹⁾	RW
			IFSR4	INT4 Interrupt Polarity Switching Bit	0 : One edge 1 : Both edges ⁽¹⁾	RW
			IFSR5	INT5 Interrupt Polarity Switching Bit	0 : One edge 1 : Both edges ⁽¹⁾	RW
			IFSR6	Interrupt Request Factor Select Bit (2)	0 : SI/O3 ⁽³⁾ 1 : INT4	RW
			IFSR7	Interrupt Request Factor Select Bit (2)	0 : SI/O4 ⁽³⁾ 1 : INT5	RW

NOTES :

1. When setting this bit to "1" (= both edges), make sure the POL bit in the INT0IC to INT5IC register are set to "0" (= falling edge).

 During memory expansion and microprocessor modes, when the data bus is 16 bits wide (BYTE pin is "L"), set this bit to "0" (= SI/O3, SI/O4).

When setting this bit to "0" (= SI/O3, SI/O4), make sure the POL bit in the S3IC and S4IC registers are set to "0" (= falling edge).

Interrupt Factor Select Register 2

b7 b6 b5 b4 b3 b2 b1 b0	Symbol IFSR2A	Address 035Eh	After Reset 00XXXXXXb	
	Bit Symbol	Bit Name	Function	RW
	 (b5-b0)	Nothing is assigned. When w rite, set to "0". When read, their contents are indeterminate.		
	IFSR26	Interrupt Request Factor Select Bit ⁽¹⁾ 0 : Timer B3 1 : UART0 bus collision detection		
	IFSR27	Interrupt Request Factor Select Bit ⁽²⁾	0 : Timer B4 1 : UART1 bus collision detection	RW

NOTES :

1. Timer B3 and UART0 bus collision detection share the vector and interrupt control register. When using Timer B3 interrupt, clear the IFSR26 bit to "0" (Timer B3). When using UART0 bus collision detection, set the IFSR26 bit to "1".

 Timer B4 and UART1 bus collision detection share the vector and interrupt control register. When using Timer B4 interrupt, clear the IFSR27 bit to "0" (Timer B4). When using UART1 bus collision detection, set the IFSR27 bit to "1".

Figure 12.11 IFSR and IFSR2A Registers

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12.7 NMI Interrupt

An $\overline{\text{NMI}}$ interrupt is generated when input on the $\overline{\text{NMI}}$ pin changes state from high to low. The $\overline{\text{NMI}}$ interrupt is a non-maskable interrupt.

The input level of this $\overline{\text{NMI}}$ interrupt input pin can be read by accessing the P8_5 bit in the P8 register. This pin cannot be used as an input port.

12.8 Key Input Interrupt

Of P10_4 to P10_7, a key input interrupt is generated when input on any of the P10_4 to P10_7 pins which has had the PD10_4 to PD10_7 bits in the PD10 register set to "0" (= input) goes low. Key input interrupts can be used as a key-on wake up function, the function which gets the microcomputer out of wait or stop mode. However, if you intend to use the key input interrupt, do not use P10_4 to P10_7 as analog input ports. Figure 12.12 shows the block diagram of the Key Input Interrupt. Note, however, that while input on any pin which has had the PD10_4 to PD10_7 bits set to "0" (= input mode) is pulled low, inputs on all other pins of the port are not detected as interrupts.

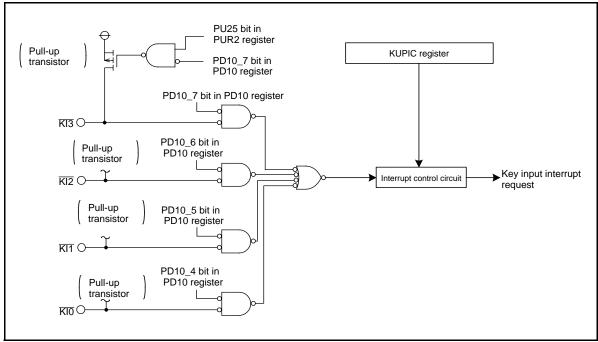


Figure 12.12 Key Input Interrupt

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12.9 Address Match Interrupt

An address match interrupt is generated immediately before executing the instruction at the address indicated by the RMADi register (i=0 to 3). Set the start address of any instruction in the RMADi register. Use the AIER0 and AIER1 bits in the AIER register and AIER20 and AIER21 bits in the AIER2 register to enable or disable the interrupt. Note that the address match interrupt is unaffected by the I flag and IPL. For address match interrupts, the value of the PC that is saved to the stack area varies depending on the instruction being executed (refer to **12.5.7 Saving Registers**).

(The value of the PC that is saved to the stack area is not the correct return address.) Therefore, follow one of the methods described below to return from the address match interrupt.

- Rewrite the content of the stack and then use the REIT instruction to return.
- Restore the stack to its previous state before the interrupt request was accepted by using the POP or similar other instruction and then use a jump instruction to return.

Table 12.6 shows the Value of the PC that is Saved to the Stack Area when an Address Match Interrupt Request is Accepted

Figure 12.13 shows the AIER, AIER2 and RMAD0 to RMAD3 Registers.

Table 12.6Value of the PC that is Saved to the Stack Area when an Address Match Interrupt
Request is Accepted

	Value of the PC that is saved to the stack area						
 16-bit op-cod 	16-bit op-code instruction						
 Instruction sh 	nown below amo	ong 8-bit oper	ation code instruct	tions		indicated by the	
ADD.B:S	#IMM8,dest	SUB.B:S	#IMM8,dest	AND.B:S	#IMM8,dest	RMADi register +2	
OR.B:S	#IMM8,dest	MOV.B:S	#IMM8,dest	STZ.B:S	#IMM8,dest		
STNZ.B:S	#IMM8,dest	STZX.B:S	#IMM81,#IMM82	2,dest			
CMP.B:S	#IMM8,dest	PUSHM	src	POPM dest			
JMPS	#IMM8	JSRS	#IMM8				
MOV.B:S	#IMM,dest (Ho	owever, dest=	A0 or A1)				
Instructions of	her than the abo	ove				The address indicated by the RMADi register +1	

Value of the PC that is saved to the stack area : Refer to 12.5.7 Saving Registers.

Table 12.7 Relationship Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt sources	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address Match Interrupt 0	AIER0	RMAD0
Address Match Interrupt 1	AIER1	RMAD1
Address Match Interrupt 2	AIER20	RMAD2
Address Match Interrupt 13	AIER21	RMAD3

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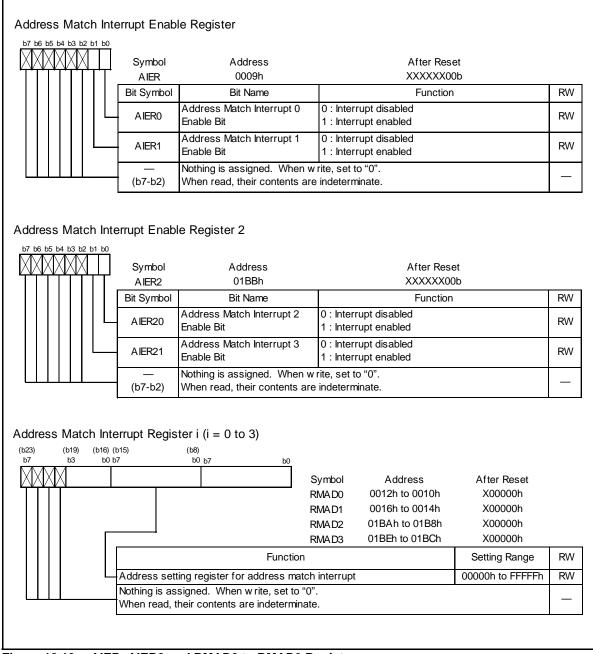


Figure 12.13 AIER, AIER2 and RMAD0 to RMAD3 Registers

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13. Watchdog Timer

The watchdog timer is the function of detecting when the program is out of control. Therefore, we recommend using the watchdog timer to improve reliability of a system. The watchdog timer contains a 15-bit counter which counts down the clock derived by dividing the CPU clock using the prescaler. Whether to generate a watchdog timer interrupt request or apply a watchdog timer reset as an operation to be performed when the watchdog timer underflows after reaching the terminal count can be selected using the PM12 bit of PM1 register. The PM12 bit can only be set to "1" (reset). Once this bit is set to "1," it cannot be set to "0" (watchdog timer interrupt) in a program. Refer to **5.4 Watchdog Timer Reset** for the details of watchdog timer reset.

When the main clock source is selected for CPU clock, on-chip oscillator clock, PLL clock, the divide-by-N value for the prescaler can be chosen to be 16 or 128. If a sub-clock is selected for CPU clock, the divide by-N value for the prescaler is always 2 no matter how the WDC7 bit is set. The period of watchdog timer can be calculated as given below. The period of watchdog timer is, however, subject to an error due to the prescaler.

With main clock chosen for CPU clock, on-chip oscillator clock, PLL clock

Watchdog timer period	=	Prescaler dividing (16 or 128) \times Watchdog timer count (32768)
watchuog tiller periou	_	CPU clock

With sub-clock chosen for CPU clock

Watchdog timer period = Prescaler dividing (2) × Watchdog timer count (32768) CPU clock

For example, when CPU clock = 16 MHz and the divide-by-N value for the prescaler= 16, the watchdog timer period is approx. 32.8 ms.

The watchdog timer is initialized by writing to the WDTS register. The prescaler is initialized after reset. Note that the watchdog timer and the prescaler both are inactive after reset, so that the watchdog timer is activated to start counting by writing to the WDTS register.

In stop mode, wait mode and hold state, the watchdog timer and prescaler are stopped. Counting is resumed from the held value when the modes or state are released.

Figure 13.1 shows the Watchdog Timer Block Diagram. Figure 13.2 shows the WDC and WDTS Register.

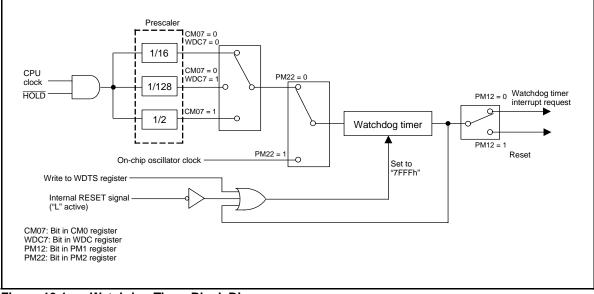


Figure 13.1 Watchdog Timer Block Diagram

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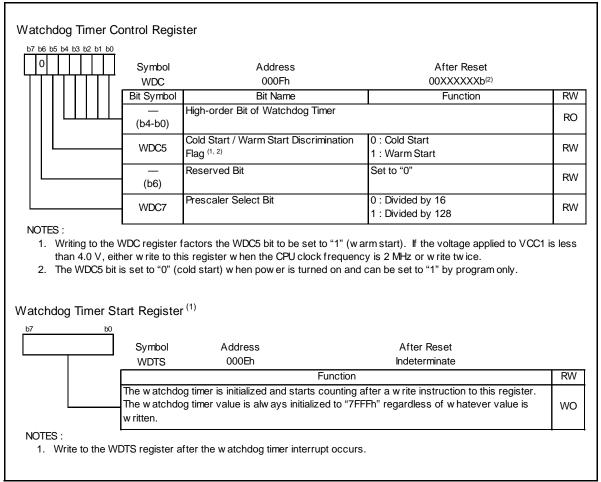


Figure 13.2 WDC and WDTS Register

13.1 Count source protective mode

In this mode, a on-chip oscillator clock is used for the watchdog timer count source. The watchdog timer can be kept being clocked even when CPU clock stops as a result of run-away.

Before this mode can be used, the following register settings are required:

- (1) Set the PRC1 bit in the PRCR register to "1" (enable writes to PM1 and PM2 registers).
- (2) Set the PM12 bit in the PM1 register to "1" (reset when the watchdog timer underflows).
- (3) Set the PM22 bit in the PM2 register to "1" (on-chip oscillator clock used for the watchdog timer count source).
- (4) Set the PRC1 bit in the PRCR register to "0" (disable writes to PM1 and PM2 registers).
- (5) Write to the WDTS register (watchdog timer starts counting).

Setting the PM22 bit in the PM register to "1" results in the following conditions.

• The on-chip oscillator starts oscillating, and the on-chip oscillator clock becomes the watchdog timer count source.

Watchdog timer period =

Watchdog timer count (32768) On-chip oscillator clock

- The CM10 bit in the CM1 register is disabled against write (Writing a "1" has no effect, nor is stop mode entered).
- The watchdog timer does not stop when in wait mode or hold state.

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14. DMAC

The DMAC (Direct Memory Access Controller) allows data to be transferred without the CPU intervention. Two DMAC channels are included. Each time a DMA request occurs, the DMAC transfers one (8 or 16-bit) data from the source address to the destination address. The DMAC uses the same data bus as used by the CPU. Because the DMAC has higher priority of bus control than the CPU and because it makes use of a cycle steal method, it can transfer one word (16 bits) or one byte (8 bits) of data within a very short time after a DMA request is generated. Figure 14.1 shows the DMAC Block Diagram. Table 14.1 lists the DMAC Specifications. Figures 14.2 to 14.4 shows the DMACrelated registers.

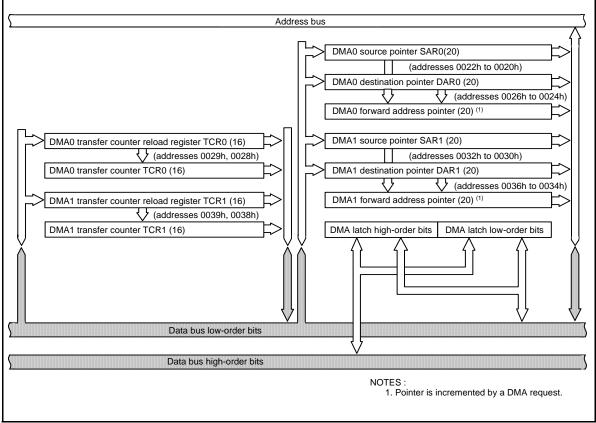


Figure 14.1 DMAC Block Diagram

A DMA request is generated by a write to the DSR bit in the DMiSL register (i = 0 to 1), as well as by an interrupt request which is generated by any function specified by the DMS and DSEL3 to DSEL0 bits in the DMiSL register. However, unlike in the case of interrupt requests, DMA requests are not affected by the I flag and the interrupt control register, so that even when interrupt requests are disabled and no interrupt request can be accepted, DMA requests are always accepted. Furthermore, because the DMAC does not affect interrupts, the IR bit in the interrupt control register does not change state due to a DMA transfer.

A data transfer is initiated each time a DMA request is generated when the DMAE bit in the DMiCON register = 1 (DMA enabled). However, if the cycle in which a DMA request is generated is faster than the DMA transfer cycle, the number of transfer requests generated and the number of times data is transferred may not match. Refer to **14.4 DMA Request** for details.

Item		Specification		
No. of Channels		2 (cycle steal method)		
Transfer Memory Space		 From any address in the 1-Mbyte space to a fixed address From a fixed address to any address in the 1-Mbyte space From a fixed address to a fixed address 		
Maximum No. of Bytes Transferred		128 Kbytes (with 16-bit transfers) or 64 Kbytes (with 8-bit transfers)		
DMA Request Factors ^(1, 2)		Falling edge of INT0 or INT1 Both edge of INT0 or INT1 Timer A0 to timer A4 interrupt requests Timer B0 to timer B5 interrupt requests UART0 transfer, UART0 reception interrupt requests UART1 transfer, UART1 reception interrupt requests UART2 transfer, UART2 reception interrupt requests SI/O3, SI/O4 interrupt requests A/D conversion interrupt requests Software triggers		
Channel Priority		DMA0 > DMA1 (DMA0 takes precedence)		
Transfer Unit		8 bits or 16 bits		
Transfer Address Direction		forward or fixed (The source and destination addresses cannot both be in the forward direction.)		
Transfer Mode	Single Transfer Repeat Transfer	Transfer is completed when the DMAi transfer counter (i = 0 to 1) underflows after reaching the terminal count. When the DMAi transfer counter underflows, it is reloaded with the value of the DMAi transfer counter reload register and a DMA transfer is		
		continued with it.		
DMA Interrupt Request Generation Timing		When the DMAi transfer counter underflowed		
DMA Start up		Data transfer is initiated each time a DMA request is generated when th DMAE bit in the DMAiCON register = 1 (enabled).		
DMA Shutdown	Single Transfer	 When the DMAE bit is set to "0" (disabled) After the DMAi transfer counter underflows 		
	Repeat Transfer	When the DMAE bit is set to "0" (disabled)		
Reload Timing for Forward Address Pointer and Transfer Counter		When a data transfer is started after setting the DMAE bit to "1" (enabled), the forward address pointer is reloaded with the value of the SARi or the DARi pointer whichever is specified to be in the forward direction and the DMAi transfer counter is reloaded with the value of the DMAi transfer counter reload register.		
DMA Transfer Cycles		Minimum 3 cycles between SFR and internal RAM		

NOTES:

- 1. DMA transfer is not effective to any interrupt. DMA transfer is affected neither by the I flag nor by the interrupt control register.
- 2. The selectable factors of DMA requests differ with each channel.
- 3. Make sure that no DMAC-related registers (addresses 0020h to 003Fh) are accessed by the DMAC.

b7 b6 b5 b4 b3 b2 b1 b0		C		
	Symbol	Address	After Reset	
┕┰┸┰╩┰╩┰┸┰┸┰┙	DMOSL	03B8h	00h	
	Bit Symbol	Bit Name	Function	RV
L	DSEL0	DMA Request Factor Select Bit	(NOTE 1)	RV
	DSEL1	-		RV
	DSFL2	4		RV
	DSEL3	4		RV
		Nothing is assigned. When w rite	. set to "0".	
	(b5-b4)	When read, their content are "0".	,	-
	()	DMA Request Factor Expansion	0: Basic factor of request	
	DMS	Select Bit	1: Extended factor of request	RV
		Software DMA Request Bit	A DMA request is generated by setting this bit	
		Continuite Dimit Request Dic	to "1" when the DMS bit is "0" (basic factor)	RW
	DSR		and the DSEL3 to DSEL0 bits are "0001b"	
	Dok		(softw are trigger).	
			The value of this bit when read is "0".	
NOTES :				
1. The factors of described belo	w.	-	ion of DMS bit and DSEL3 to DSEL0 bits in the man	ner
1. The factors of described belo	DMS:	=0(Basic Factor of Request)		ner
1. The factors of described belo	ow . DMS Falling Edge	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man	ner
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b	DW DMS Falling Edge Softw are Tri	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man	ner
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b	DMS Falling Edge Softw are Tri Timer A0	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man	ner
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man	ner
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b	DMS: Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man	ner
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b 0 1 0 1 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request)	
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b 0 1 0 1 b 0 1 0 1 b 0 1 1 0 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin	ner
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b 0 1 0 1 b 0 1 1 0 b 0 1 1 1 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin Timer B3	
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 1 0 b 0 1 0 b 0 1 0 1 b 0 1 1 b 0 1 1 b 0 1 1 b 0 1 1 b 0 1 1 b 0 1 1 1 b 1 0 0 0 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1	=0(Basic Factor of Request) of INTO Pin	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin Timer B3 Timer B4	
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 1 0 b 0 1 0 b 0 1 0 1 b 0 1 1 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 1 1 b 1 0 0 1 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2	=0(Basic Factor of Request) of INTO Pin igger	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin Timer B3	
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 1 0 b 0 1 0 0 b 0 1 0 1 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 0 0 1 b 1 0 0 1 b 1 0 1 0 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2 UART0 Trans	=0(Basic Factor of Request) of INTO Pin igger	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin Timer B3 Timer B4	
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 1 1 b 0 1 0 0 b 0 1 1 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 1 1 b 1 0 0 0 b 1 0 1 b 1 0 1 b 1 0 1 b 1 0 1 b 1 0 1 b 1 0 1 1 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2 UARTO Trans UARTO Rece	=0(Basic Factor of Request) of INTO Pin igger smit	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin Timer B3 Timer B4	
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 1 1 b 1 0 0 0 b 1 0 1 0 b 1 0 1 0 b 1 0 1 0 b 1 0 1 1 b 1 0 1 0 b 1 0 1 1 b 1 1 0 0 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2 UART0 Trans UART0 Rece UART2 Trans	=0(Basic Factor of Request) of INTO Pin igger smit sive smit	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin Timer B3 Timer B4	
1. The factors of described belo DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 1 1 b 0 1 0 0 b 0 1 1 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 1 1 b 1 0 0 0 b 1 0 1 b 1 0 1 b 1 0 1 b 1 0 1 b 1 0 1 b 1 0 1 1 b	DMS Falling Edge Softw are Tri Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2 UARTO Trans UARTO Rece	=0(Basic Factor of Request) of INTO Pin igger smit swit swit swit	ion of DMS bit and DSEL3 to DSEL0 bits in the man DMS=1(Extended Factor of Request) Two Edges of INTO Pin Timer B3 Timer B4	

Figure 14.2 DM0SL Register

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MA1 Request Fa	actor Select	Pagistar		
•		Register		
b7 b6 b5 b4 b3 b2 b1 b0	1			
	Symbol	Address	After Reset	
	DM1SL	03BAh	00h	
	Bit Symbol	Bit Name	Function	RW
	DSEL0	DMA Request factor Select Bit	(NOTE 1)	RW
	DSEL1	1		RW
	DSEL2	1		RW
	DSEL3	1		RW
	_	Nothing is assigned. When write,	set to "0".	
	(b5-b4)	When read, their contents are "0"		-
	DMS	DMA Request Factor Expansion Select Bit	0: Basic factor of request 1: Extended factor of request	RW
	DSR	Softw are DMA Request Bit	A DMA request is generated by setting this bit to "1" w hen the DMS bit is "0" (basic factor) and the DSEL3 to DSEL0 bits are "0001b" (softw are trigger). The value of this bit w hen read is "0".	RW
NOTES : 1. The factors (
described be	elow.	-	on of DMS bit and DSEL3 to DSEL0 bits in the man	ner 1
described be DSEL3 to DSEL0	elow . DMS	=0(Basic Factor of Request)	on of DMS bit and DSEL3 to DSEL0 bits in the man	ner
described be DSEL3 to DSEL0 0 0 0 0 b	elow . DMS Falling Edge	=0(Basic Factor of Request) of INT1 Pin		ner
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b	elow . DMS Falling Edge Softw are Tr	=0(Basic Factor of Request) of INT1 Pin		ner
described be DSEL3 to DSEL0 0 0 0 0 b	elow . DMS Falling Edge	=0(Basic Factor of Request) of INT1 Pin		ner
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1	=0(Basic Factor of Request) of INT1 Pin		ner
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b	elow . DMS Falling Edge Softw are Tr Timer A0	=0(Basic Factor of Request) of INT1 Pin	DMS=1(Extended Factor of Request)	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2	=0(Basic Factor of Request) of INT1 Pin	DMS=1(Extended Factor of Request) SVO3	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 1 b 0 1 0 0 b 0 1 0 1 b 0 1 0 1 b 0 1 0 1 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4	=0(Basic Factor of Request) of INT1 Pin	DMS=1(Extended Factor of Request) SVO3 SVO4	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b 0 1 0 1 b 0 1 0 1 b 0 1 1 1 b 0 1 1 1 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0	=0(Basic Factor of Request) of INT1 Pin	DMS=1(Extended Factor of Request) SVO3	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b 0 1 0 1 b 0 1 1 0 b 0 1 1 1 b 0 1 1 1 b 1 0 0 0 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1	=0(Basic Factor of Request) of INT1 Pin	DMS=1(Extended Factor of Request) SVO3 SVO4	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 1 b 0 0 1 0 b 0 1 0 b 0 1 0 0 b 0 1 0 1 b 0 1 0 1 b 0 1 1 0 b 0 1 1 1 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0	=0(Basic Factor of Request) of INTT Pin igger	DMS=1(Extended Factor of Request) SVO3 SVO4	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 1 1 b 0 1 0 0 b 0 1 1 1 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 0 0 1 b 1 0 0 1 b 1 0 0 1 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2 UART0 Tran	e=0(Basic Factor of Request) of INTT Pin igger	DMS=1(Extended Factor of Request) SVO3 SVO4	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 1 0 b 0 0 1 1 b 0 1 0 0 b 0 1 0 1 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 0 0 1 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2	eO(Basic Factor of Request) of INTT Pin igger	DMS=1(Extended Factor of Request) SVO3 SVO4	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 1 1 b 0 1 0 0 b 0 1 0 1 b 0 1 1 0 b 0 1 1 1 b 1 0 0 0 b 1 0 0 1 b 1 0 1 0 b 1 0 1 1 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2 UART0 Tran UART0 Rece	s=0(Basic Factor of Request) of INTT Pin igger ismit eive/ACK0 ismit	DMS=1(Extended Factor of Request) SVO3 SVO4	
described be DSEL3 to DSEL0 0 0 0 0 b 0 0 0 1 b 0 0 1 0 b 0 1 0 0 b 0 1 0 1 b 0 1 0 0 b 0 1 1 1 b 1 0 0 0 b 1 0 1 0 b 1 0 1 0 b 1 0 1 1 b 1 0 1 0 b 1 0 1 1 b 1 0 0 b	elow . DMS Falling Edge Softw are Tr Timer A0 Timer A1 Timer A2 Timer A3 Timer A4 Timer B0 Timer B1 Timer B2 UART0 Tran UART0 Rece UART2 Tran	s=0(Basic Factor of Request) of INTT Pin igger issmit eive/ACK0 ismit eive/ACK2	DMS=1(Extended Factor of Request) SVO3 SVO4	

Figure 14.3 DM1SL Register

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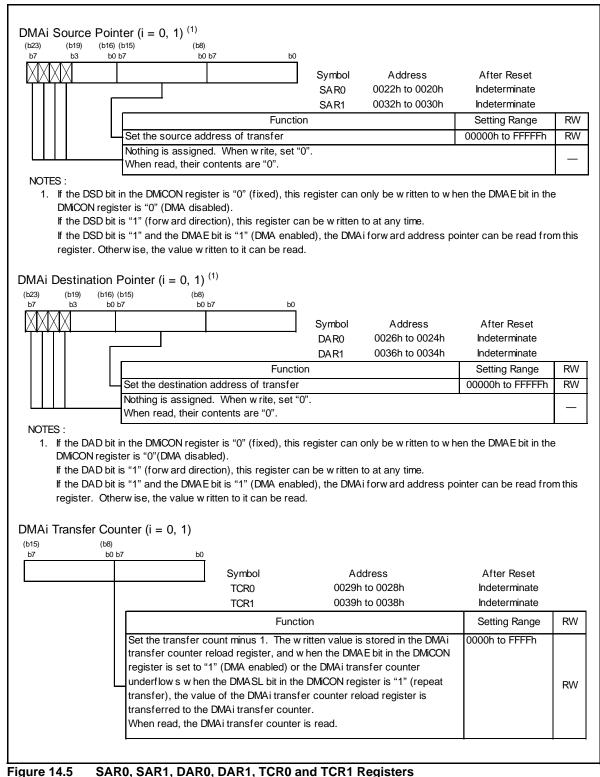
b7 b6 b5	b4 b3 b2 b1 b0				
XX I		Symbol	Address	After Reset	
		DM0CON	002Ch	00000X00b	
		DM1CON	003Ch	00000X00b	
		Bit Symbol	Bit Name	Function	RW
		DMBIT	Transfer Unit Bit Select Bit	0 : 16 bits 1 : 8 bits	RW
		DMASL	Repeat Transfer Mode Select Bit	0 : Single transfer 1 : Repeat transfer	RW
		DMAS	DMA Request Bit	0 : DMA not requested 1 : DMA requested	RW
		DMAE	DMA Enable Bit	0 : Disabled 1 : Enabled	RW
		DSD	Source Address Direction Select Bit ⁽²⁾	0 : Fixed 1 : Forw ard	RW
		DAD	Destination Address Direction Select Bit ⁽²⁾	0 : Fixed 1 : Forw ard	RW
		 (b7-b6)	Nothing is assigned. When w rite, set to When read, their contents are "0".	· "0".	- -

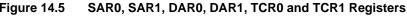
1. The DMAS bit can be set to "0" by writing "0" in a program (This bit remains unchanged even if "1" is written).

2. At least one of the DAD and DSD bits must be "0" (address direction fixed).









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14.1 Transfer Cycles

The transfer cycle consists of a memory or SFR read (source read) bus cycle and a write (destination write) bus cycle. The number of read and write bus cycles is affected by the source and destination addresses of transfer. During memory extension and microprocessor modes, it is also affected by the BYTE pin level. Furthermore, the bus cycle itself is extended by a software wait or \overline{RDY} signal.

14.1.1 Effect of Source and Destination Addresses

If the transfer unit and data bus both are 16 bits and the source address of transfer begins with an odd address, the source read cycle consists of one more bus cycle than when the source address of transfer begins with an even address.

Similarly, if the transfer unit and data bus both are 16 bits and the destination address of transfer begins with an odd address, the destination write cycle consists of one more bus cycle than when the destination address of transfer begins with an even address.

14.1.2 Effect of BYTE Pin Level

During memory extension and microprocessor modes, if 16 bits of data are to be transferred on an 8-bit data bus (input on the BYTE pin = high), the operation is accomplished by transferring 8 bits of data twice. Therefore, this operation requires two bus cycles to read data and two bus cycles to write data. Furthermore, if the DMAC is to access the internal area (internal ROM, internal RAM, or SFR), unlike in the case of the CPU, the DMAC does it through the data bus width selected by the BYTE pin.

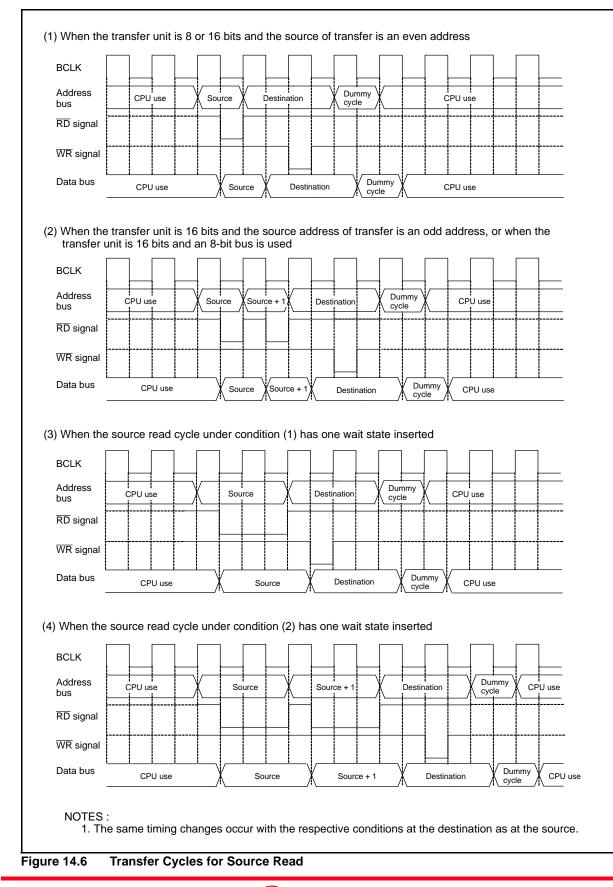
14.1.3 Effect of Software Wait

For memory or SFR accesses in which one or more software wait states are inserted, the number of bus cycles required for that access increases by an amount equal to software wait states.

14.1.4 Effect of RDY Signal

During memory extension and microprocessor modes, DMA transfers to and from an external area are affected by the RDY signal. Refer to **8.2.6 RDY Signal**.

Figure 14.6 shows the example of the Transfer Cycles for Source Read. For convenience, the destination write cycle is shown as one cycle and the source read cycles for the different conditions are shown. In reality, the destination write cycle is subject to the same conditions as the source read cycle, with the transfer cycle changing accordingly. When calculating transfer cycles, take into consideration each condition for the source read and the destination write cycle, respectively. For example, when data is transferred in 16 bit units using an 8-bit bus ((2) on Figure 14.6), two source read bus cycles and two destination write bus cycles are required.



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14.2 DMA Transfer Cycles

Any combination of even or odd transfer read and write addresses is possible. Table 14.2 lists the DMA Transfer Cycles. Table 14.3 lists the Coefficient j, k.

The number of DMAC transfer cycles can be calculated as follows:

No. of transfer cycles per transfer unit = No. of read cycles $\times j$ + No. of write cycles $\times k$

Table 14.2 DMA Transfer Cycl

Transfer Unit	Bus Width	Access	Single-C	hip Mode	Memory Expansion Mode Microprocessor Mode	
Transier Unit	Bus Width	Address	No. of Read Cycles	No. of Write Cycles	No. of Read Cycles	No. of Write Cycles
8-bit Transfers	16-bit	Even	1	1	1	1
(DMBIT= 1)	(BYTE= L)	Odd	1	1	1	1
	8-bit	Even	_	_	1	1
	(BYTE = H)	Odd			1	1
16-bit Transfers	16-bit	Even	1	1	1	1
(DMBIT= 0)	(BYTE = L)	Odd	2	2	2	2
	8-bit	Even	_	_	2	2
	(BYTE = H)	Odd			2	2

- : This condition does not exist.

Table 14.3 Coefficient j, k

		Internal	Area				Ex	ternal Ar	ea		
	Internal ROM, RAM		SFR		Separate Bus				Multiplex Bus		
	No Wait	With	1-Wait	2-Wait	No	W	/ith Wait ((1)	W	/ith Wait	[1)
	NO Wait	Wait	(2)	(2)	Wait	1-Wait	2-Wait	3-Wait	1-Wait	2-Wait	3-Wait
j	1	2	2	3	1	2	3	4	3	3	4
k	1	2	2	3	2	2	3	4	3	3	4

NOTES:

1. Depends on the set value of CSE register.

2. Depends on the set value of PM20 bit in the PM2 register.

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14.3 DMA Enable

When a data transfer starts after setting the DMAE bit in the DMiCON register (i = 0, 1) to "1" (enabled), the DMAC operates as follows:

- (1) Reload the forward address pointer with the SARi register value when the DSD bit in the DMiCON register is "1" (forward) or the DARi register value when the DAD bit in the DMiCON register is "1" (forward).
- (2) Reload the DMAi transfer counter with the DMAi transfer counter reload register value.

If the DMAE bit is set to "1" again while it remains set, the DMAC performs the above operation. However, if a DMA request may occur simultaneously when the DMAE bit is being written, follow the steps below.

Step 1: Write "1" to the DMAE bit and DMAS bit in the DMiCON register simultaneously.

Step 2: Make sure that the DMAi is in an initial state as described above (1) and (2) in a program.

If the DMAi is not in an initial state, the above steps should be repeated.

14.4 DMA Request

The DMAC can generate a DMA request as triggered by the factor of request that is selected with the DMS and DSEL3 to DSEL0 bits in the DMiSL register (i = 0, 1) on either channel. Table 14.4 lists the Timing at Which the DMAS Bit Changes State.

Whenever a DMA request is generated, the DMAS bit is set to "1" (DMA requested) regardless of whether or not the DMAE bit is set. If the DMAE bit was set to "1" (enabled) when this occurred, the DMAS bit is set to "0" (DMA not requested) immediately before a data transfer starts. This bit cannot be set to "1" in a program (it can only be set to "0").

The DMAS bit may be set to "1" when the DMS or the DSEL3 to DSEL0 bits change state. Therefore, always be sure to set the DMAS bit to "0" after changing the DMS or the DSEL3 to DSEL0 bits.

Because if the DMAE bit is "1", a data transfer starts immediately after a DMA request is generated, the DMAS bit in almost all cases is "0" when read in a program. Read the DMAE bit to determine whether the DMAC is enabled.

DMA Factor	DMAS Bit of the	DMiCON Register					
	Timing at which the bit is set to "1"	Timing at which the bit is set to "0"					
Software Trigger	When the DSR bit in the DMiSL register is set to "1"	 Immediately before a data transfer starts When set by writing "0" in a program 					
Peripheral Function	When the interrupt control register for the peripheral function that is selected by the DSEL3 to DSEL0 and DMS bits in the DMiSL register has its IR bit set to "1"						

Table 14.4 Timing at Which the DMAS Bit Changes State

14.5 Channel Priority and DMA Transfer Timing

If both DMA0 and DMA1 are enabled and DMA transfer request signals from DMA0 and DMA1 are detected active in the same sampling period (one period from a falling edge to the next falling edge of BCLK), the DMAS bit on each channel is set to "1" (DMA requested) at the same time. In this case, the DMA requests are arbitrated according to the channel priority, DMA0 > DMA1. The following describes DMAC operation when DMA0 and DMA1 requests are detected active in the same sampling period. Figure 14.7 shows an example of DMA Transfer by External Factors.

DMA0 request having priority is received first to start a transfer when a DMA0 request and DMA1 request are generated simultaneously. After one DMA0 transfer is completed, a bus arbitration is returned to the CPU. When the CPU has completed one bus access, a DMA1 transfer starts. After one DMA1 transfer is completed, the bus arbitration is again returned to the CPU.

In addition, DMA requests cannot be counted up since each channel has one DMAS bit. Therefore, when DMA requests, as DMA1 in Figure 14.7, occurs more than one time, the DMAS bit is set to "0" as soon as getting the bus arbitration. The bus arbitration is returned to the CPU when one transfer is completed.

Refer to 8.2.7 Hold Signal for details about bus arbitration between the CPU and DMA.

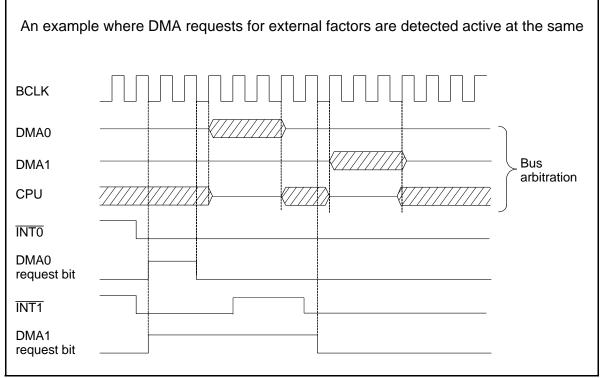


Figure 14.7 DMA Transfer by External Factors

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15. Timers

Note

The M16C/62P (80-pin version) and M16C/62PT (80-pin version) do not include TA1IN, TA1OUT, TA2IN, TA2OUT and TB pins. Do not use the function which needs these pins.

Eleven 16-bit timers, each capable of operating independently of the others, can be classified by function as either Timer A (five) and Timer B (six). The count source for each timer acts as a clock, to control such timer operations as counting, reloading, etc. Figures 15.1 and 15.2 show block diagrams of Timer A and Timer B configuration, respectively.

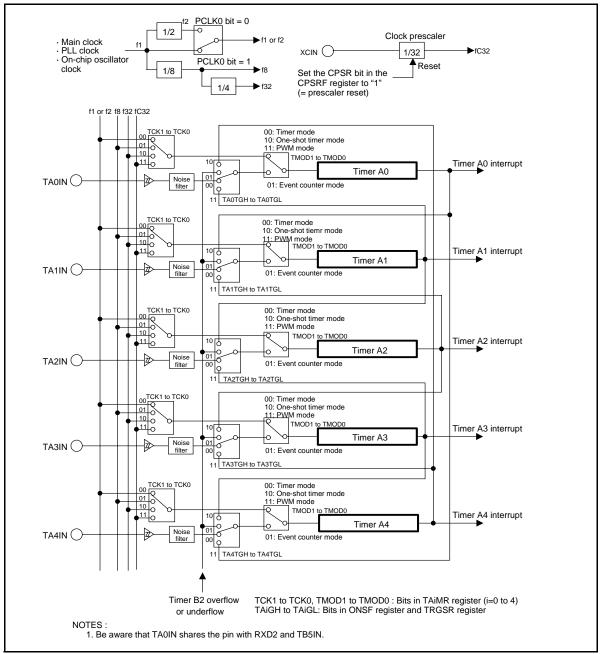


Figure 15.1 Timer A Configuration

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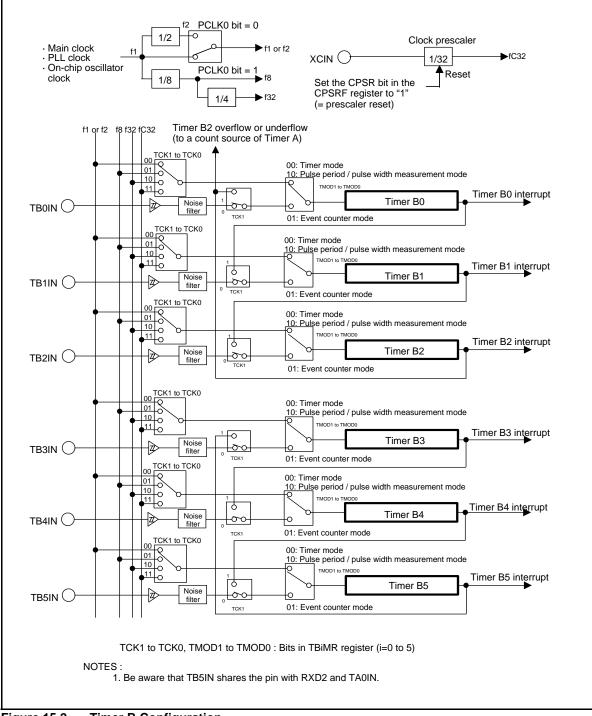


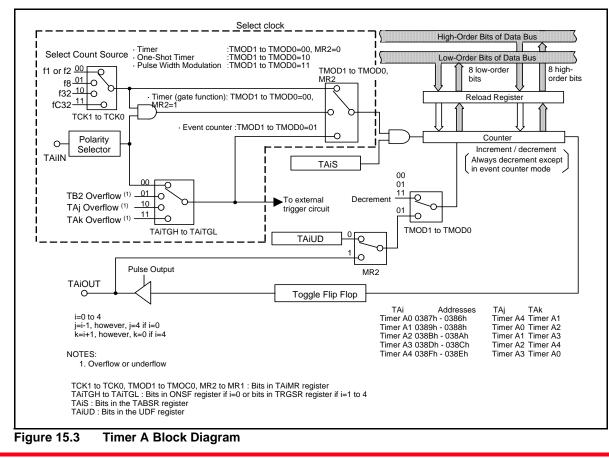
Figure 15.2 Timer B Configuration

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15.1	Timer A Note	
	· 1	rsion) and M16C/62PT (80-pin version) do not include TA1IN and TA1OUT pins nd TA2OUT pins of Timer A2.
		using Timer A1 and Timer A2]
	• Timer Mode	The Gate Function and the Pulse Output Function cannot be used. Set the MR2 to MR0 bits in the TA1MR and TA2MR registers to "000b" when using Timer Mode.
	• Event Counter Mode	The Pulse Output Function cannot be used and external input signals cannot be counted. Two-phase Pulse Signal of Timer A2 cannot be used. Set the MR2 to MR0 bits in the TA1MR and TA2MR registers to "000b" when using the Event Counter Mode.
	• One-shot Timer Mode	The Pulse Output Function cannot be used and count start by the external trigger cannot be counted. Set the MR1 to MR0 bits in the TA1MR and TA2MR registers to "00b" when using the One-shot Timer Mode.
	Pulse Width Modulation Mode	PWM pulse cannot be outputted.

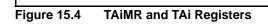
Figure 15.3 shows a Timer A Block Diagram. Figures 15.4 to 15.7 show registers related to Timer A. Timer A supports the following four modes. Except in event counter mode, Timers A0 to A4 all have the same function. Use the TMOD1 to TMOD0 bits in the TAiMR register (i = 0 to 4) to select the desired mode.

- Timer Mode: The timer counts an internal count source.
 Event Counter Mode: The timer counts pulses from an external device or overflows and
- One-shot Timer Mode: underflows of other timers. The timer outputs a pulse only once before it reaches the minimum count "0000h".
- Pulse Width Modulation (PWM) Mode: The timer outputs pulses in a given width successively.



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b7 b6 b5 b4 b3 b2 b1 b0				-	
┯┹┯┹┯┹┯┹┯┹	Symbol			ter Reset	
	TA0MR to TA	AMR 0396h to 039 Bit Name		00h Function	
	Bit Symbol	peration Mode Select Bit		UNCTION	R
-			00: Timer mode		R
			0 1 : Event counter m	node	
🗀	TMOD1		1 0 : One-shot timer r		R
			1 1 : Pulse width mod	Julation (PWM) mode	
└──	MR0	_	Function varies with	each operation mode	R
└───	MR1				R
	MR2				R
	- MR3				R
	TCK0 Cc TCK1	ount Source Select Bit	Function varies with	each operation mode	R' R'
mer Ai Register (. ,	Symbol ∞ TA0	Address 0387h, 0386h	After Reset Indeterminate	
7 b0 b	7 t		0389h, 0388h	Indeterminate	
 			038Bh, 038Ah	Indeterminate	
		TA3	038Dh, 038Ch	Indeterminate	
		TA4	038Fh, 038Eh	Indeterminate	
!	Mode		Function	Setting Range	RW
Ľ	Timer Mode		rce by n + 1 w here n = set	0000h to FFFFh	RW
I	Event Counter	Value		0000h to FFFFh	—
I	Mode		rce by FFFFh – n + 1 w here counting up or by n + 1 w hen		RW
I		counting dow n $^{(5)}$. .		
	One-Shot Timer Mode	Divide the count sour and factor the timer t	rce by n w here n = set value to stop	0000h to FFFFh ^(2, 4)	wo
	Pulse Width	Modify the pulse wid		0000h to FFFEh ^(3, 4)	
	Modulation Mode (16-Bit PWM)	 PWM period: (2¹⁶ – 1) High level PWM pulse 			wo
			, fj = count source frequency		
	Pulse Width	Modify the pulse wid		00h to FEh	
	Modulation Mode			(High-order address)	
I	(8-Bit PWM)	High level PWM pulse w here n = high-orde		00h to FFh (Low -order address)	wo
		-	ss set value, fj = count	(3, 4)	
	1				
		source frequency			
NOTES :					
1. The register m		in 16-bit units.			
 The register m If the TAi regis 	ster is set to "0000	in 16-bit units. 0h", the counter does no	t work and timer Ai interrupt r		ted
 The register m If the TAi regis either. Further 	ster is set to "0000 more, if "pulse ou	I in 16-bit units. 0h", the counter does no utput" is selected, no puls	ses are output from the TAiOL	Л pin.	
 The register m If the TAi regis either. Furtheri If the TAi regis 	ster is set to "0000 more, if "pulse ou ster is set to "0000	I in 16-bit units. Oh", the counter does no utput" is selected, no puls Oh", the pulse w idth mod		JT pin. put level on the TAiOUT	pin



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ЦЦ			Syn	nbol Address	After Reset	
				3SR 0380h	00h	
			Bit Symbol	Bit Name	Function	RW
		╽╽╽┕─	TAOS	Timer A0 Count Start Flag	0 : Stops counting	RW
			TA1S	Timer A1 Count Start Flag	1 : Starts counting	RW
			TA2S	Timer A2 Count Start Flag		RW
			TA3S	Timer A3 Count Start Flag		RV
			TA4S	Timer A4 Count Start Flag		RV
	L		TB0S	Timer B0 Count Start Flag		RV
			TB1S	Timer B1 Count Start Flag		RV
			TB2S	Timer B2 Count Start Flag		RV
•		Flag ⁽¹⁾	Symb	ol Address	After Reset	
		0	Symb		After Reset	
•		0	UDF		After Reset 00h Function	RW
		0	,	- 0384h	00h	
		0	UDF Bit Symbol	- 0384h Bit Name	00h Function	RV
		0	UDF Bit Symbol TA0UD	= 0384h Bit Name Timer A0 Up/Dow n Flag	00h Function 0 : Dow n count 1 : Up count Enabled by setting the MR2 bit in the TAiMR	RV RV
		0	UDF Bit Symbol TA0UD TA1UD	- 0384h Bit Name Timer A0 Up/Dow n Flag Timer A1 Up/Dow n Flag	00h Function 0 : Dow n count 1 : Up count Enabled by setting the MR2 bit in the TAiMR register to "0" (=sw itching source in UDF	RW RW RW RW
•		0	UDF Bit Symbol TA0UD TA1UD TA2UD	Timer A0 Up/Dow n Flag Timer A1 Up/Dow n Flag Timer A2 Up/Dow n Flag Timer A2 Up/Dow n Flag	00h Function 0 : Dow n count 1 : Up count Enabled by setting the MR2 bit in the TAiMR	RV RV RV
		0	UDF Bit Symbol TA0UD TA1UD TA2UD TA2UD	Timer A0 Up/Dow n Flag Timer A1 Up/Dow n Flag Timer A2 Up/Dow n Flag Timer A2 Up/Dow n Flag Timer A3 Up/Dow n Flag	00h Function 0 : Dow n count 1 : Up count Enabled by setting the MR2 bit in the TAiMR register to "0" (=sw itching source in UDF	RV RV RV RV RV
		0	UDF Bit Symbol TA0UD TA1UD TA2UD TA2UD TA3UD TA4UD	Timer A0 Up/Dow n Flag Timer A1 Up/Dow n Flag Timer A2 Up/Dow n Flag Timer A2 Up/Dow n Flag Timer A3 Up/Dow n Flag Timer A4 Up/Dow n Flag Timer A2 Tw o-Phase Pulse	00h Function 0 : Dow n count 1 : Up count Enabled by setting the MR2 bit in the TAiMR register to "0" (=sw itching source in UDF register) during event counter mode. 0 : tw o-phase pulse signal processing	RV RV RV RV
		0	UDF Bit Symbol TA0UD TA1UD TA2UD TA2UD TA3UD TA4UD TA2P	0384h Bit Name Timer A0 Up/Dow n Flag Timer A1 Up/Dow n Flag Timer A2 Up/Dow n Flag Timer A3 Up/Dow n Flag Timer A4 Up/Dow n Flag Timer A4 Up/Dow n Flag Timer A2 Tw o-Phase Pulse Signal Processing Select Bit Timer A3 Tw o-Phase Pulse	00h Function 0 : Dow n count 1 : Up count Enabled by setting the MR2 bit in the TAiMR register to "0" (=sw itching source in UDF register) during event counter mode. 0 : tw o-phase pulse signal processing disabled 1 : tw o-phase pulse signal processing	RV RV RV RV RV

Figure 15.5 TABSR and UDF Registers

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	0 04 00	3 b2 b1 b0	Symbol	Address	After Reset	
┕┱┹┱┹┓	┍┵┰┵┰	┷┰┵┰┙	ONSF	0382h	O0h	
			Bit Symbol	Bit Name	Function	RW
			TA0OS	Timer A0 One-Shot Start Flag	The timer starts counting by setting this bit to "1" w hile the TMOD1 to TMOD0 bits in the TAiMR	RW
			TA10S	Timer A1 One-Shot Start Flag	register $i = 0$ to 4) = 10b (= one-shot timer mode)	RW
		L	TA2OS	Timer A2 One-Shot Start Flag	and the MR2 bit in the TAIMR register = 0 (=TAIOS	RW
	-		TA3OS TA4OS	Timer A3 One-Shot Start Flag	bit enabled). When read, its content is 0".	RW
			1A405	Timer A4 One-Shot Start Flag		RW
			TAZIE	Z-Phase Input Enable Bit	0 : Z-phase input disabled 1 : Z-phase input enabled	RW
			TA0TGL	Bit	^{b7 b6} 0 0 : Input on TA0IN is selected ⁽¹⁾	RW
					0 1 : TB2 is selected ⁽²⁾	
			TA0TGH		1 0 : TA4 is selected ⁽²⁾ 1 1 : TA1 is selected ⁽²⁾	RW
		lect Reg	jister			
		-	gister Symbol TRGSR	Address 0383h	After Reset 00h	
		-	Symbol	0383h		RW
		-	Symbol TRGSR	0383h	00h Function	RW
		-	Symbol TRGSR Bit Symbol	0383h Bit Name	00h Function	
		-	Symbol TRGSR Bit Symbol	0383h Bit Name	00h Function t Bit b0 0 0 : Input on TA1IN is selected ⁽¹⁾	
		-	Symbol TRGSR Bit Symbol TA1TGL	0383h Bit Name	00h Function t Bit b1 b0 0 0 : Input on TA1IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA0 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾	RW
		-	Symbol TRGSR Bit Symbol TA1TGL TA1TGH	0383h Bit Name Timer A1 Event/Trigger Select Timer A2 Event/Trigger Select	00h Function t Bit b1 b0 0 0 : Input on TA1IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA0 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾ t Bit b3 b2 0 0 : Input on TA2IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA1 is selected ⁽²⁾ 1 0 : TA1 is selected ⁽²⁾ 1 1 : TA3 is selected ⁽²⁾	RW RW RW
		-	Symbol TRGSR Bit Symbol TA1TGL TA1TGH TA2TGL	0383h Bit Name Timer A1 Event/Trigger Select	O0h Function t Bit b1 b0 0 0 : Input on TA1IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA0 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾ t Bit b3 b2 0 0 : Input on TA2IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA1 is selected ⁽²⁾ 1 1 : TA3 is selected ⁽²⁾ t Bit b5 b4 0 0 : Input on TA3IN is selected ⁽¹⁾	RW RW RW
		-	Symbol TRGSR Bit Symbol TA1TGL TA1TGH TA2TGL TA2TGH	0383h Bit Name Timer A1 Event/Trigger Select Timer A2 Event/Trigger Select Timer A3 Event/Trigger Select	O0h Function t Bit b1 b0 0 0 : Input on TA1IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA0 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾ t Bit b3 b2 0 0 : Input on TA2IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA1 is selected ⁽²⁾ 1 1 : TA3 is selected ⁽²⁾ t Bit b5 b4 0 0 : Input on TA3IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ t Bit b5 b4 0 0 : Input on TA3IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA2 is selected ⁽²⁾ 1 1 : TA4 is selected ⁽²⁾	RW
		-	Symbol TRGSR Bit Symbol TA1TGL TA1TGH TA2TGL TA2TGL TA2TGH	0383h Bit Name Timer A1 Event/Trigger Select Timer A2 Event/Trigger Select	O0h Function t Bit b1 b0 0 0 : Input on TA1IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA0 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾ 1 1 : TA2 is selected ⁽²⁾ t Bit b3 b2 0 0 : Input on TA2IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA1 is selected ⁽²⁾ 1 1 : TA3 is selected ⁽²⁾ t Bit b5 b4 0 0 : Input on TA3IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ t Bit b5 b4 0 0 : Input on TA3IN is selected ⁽¹⁾ 0 1 : TB2 is selected ⁽²⁾ 1 0 : TA2 is selected ⁽²⁾ 1 1 : TA4 is selected ⁽²⁾	RW RW RW RW



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b7 b6 b5	b4 b3 b2 b1 b0				
\perp \wedge \wedge		Symbol	Address	After Reset	
		CPSRF	0381h	0XXXXXXb	
		Bit Symbol	Bit Name	Function	RW
		 (b6-b0)	Nothing is assigned. When w rite, set When read, their contents are indeter		_
		CPSR	Clock Prescaler Reset Flag	Setting this bit to "1" initializes the prescaler for the timekeeping clock. (When read, its content is "0".)	RW

Figure 15.7 CPSRF Register

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15.1.1 Timer Mode

In timer mode, the timer counts a count source generated internally (see Table 15.1). Figure 15.8 shows TAiMR Register in Timer Mode.

Item	Specification
Count source	f1, f2, f8, f32, fC32
Count Operation	 Down-count When the timer underflows, it reloads the reload register contents and continues counting
Divide Ratio	1/(n+1) n: set value of TAi register (i= 0 to 4) 0000h to FFFFh
Count Start Condition	Set TAiS bit in TABSR register to "1" (= start counting)
Count Stop Condition	Set TAiS bit to "0" (= stop counting)
Interrupt Request Generation Timing	Timer underflow
TAiIN Pin Function	I/O port or gate input
TAiOUT Pin Function	I/O port or pulse output
Read from Timer	Count value can be read by reading TAi register
Write to Timer	 When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select Function	 Gate function Counting can be started and stopped by an input signal to TAiIN pin Pulse output function Whenever the timer underflows, the output polarity of TAiOUT pin is inverted. When TAiS bit is set to "0" (stop counting), the pin outputs a low.

Table 15.1 Specifications in Timer Mode

b7 b6 b5	b4 b3 b2 b1 b0					
ЦЦ			mbol	Address	After Reset	
			to TA4MR	0396h to 039Ah	00h	
		Bit Symbol		Bit Name	Function	RW
		TMOD0	Operation M	ode Select Bit	b1 b0	RW
		TMOD1			0 0 : Timer mode	RW
		MRO	Pulse Outpu	t Function Select Bit	 0 : Pulse is not output (TAiOUT pin is a normal port pin) 1 : Pulse is output ⁽¹⁾ (TAiOUT pin is a pulse output pin) 	RW
		MR1	Gate Functio	on Select Bit	b4 b3 0 0 : Cate function not available 0 1 : (TAilN pin functions as VO port)	RW
		MR2			 Counts w hile input on the TAilN pin is low ⁽²⁾ 1 1 : Counts w hile input on the TAilN pin is high ⁽²⁾ 	RW
		MR3	Set to "0" in	timer mode		RW
		TCK0	Count Sourc	e Select Bit	^{b7 b6} 0 0 : f1 or f2 ⁽³⁾	RW
		TCK1	•		0 1 : f8 1 0 : f32 1 1 : fC32	RW

The port direction bit for the TAilN pin is set to "0" (= input mode).

3. Selected by PCLK0 bit in the PCLKR register.

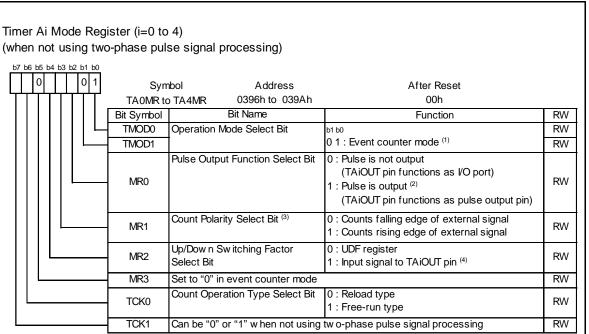
Figure 15.8 TAiMR Register in Timer Mode

15.1.2 Event Counter Mode

In event counter mode, the timer counts pulses from an external device or overflows and underflows of other timers. Timer A2, A3 and A4 can count two-phase external signals. Table 15.2 lists Specifications in Event Counter Mode (when not processing two-phase pulse signal). Table 15.3 lists Specifications in Event Counter Mode (when processing two-phase pulse signal with Timer A2, A3 and A4). Figure 15.9 shows TAiMR Register in Event Counter Mode (when not using two-phase pulse signal processing). Figure 15.10 shows TA2MR to TA4MR Registers in Event Counter Mode (when using two-phase pulse signal processing with Timer A2, A3 and A4).

Table 15.2	Specifications in Event Counter Mode	(when not processing two-phase pulse signal)
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Item	Specification
Count Source	 External signals input to TAilN pin (i=0 to 4) (effective edge can be selected in program) Timer B2 overflows or underflows, Timer Aj (j=i-1, except j=4 if i=0) overflows or underflows, Timer Ak (k=i+1, except k=0 if i=4) overflows or underflows
Count Operation	 Up-count or down-count can be selected by external signal or program When the timer overflows or underflows, it reloads the reload register contents and continues counting. When operating in free-running mode, the timer continues counting without reloading.
Divided Ratio	1/ (FFFFh - n + 1) for up-count 1/ (n + 1) for down-count n : set value of TAi register 0000h to FFFFh
Count Start Condition	Set TAiS bit in the TABSR register to "1" (= start counting)
Count Stop Condition	Set TAiS bit to "0" (= stop counting)
Interrupt Request Generation Timing	Timer overflow or underflow
TAiIN Pin Function	I/O port or count source input
TAiOUT Pin Function	I/O port, pulse output, or up/down-count select input
Read from Timer	Count value can be read by reading TAi register
Write to Timer	 When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select Function	 Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded to it Pulse output function Whenever the timer underflows or underflows, the output polarity of TAiOUT pin is inverted. When TAiS bit is set to "0" (stop counting), the pin outputs a low.



NOTES :

1. During event counter mode, the count source can be selected using the ONSF and TRGSR registers.

2. TA0OUT pin is N-channel open drain output.

3. Effective when the TAITGH and TAITGL bits in the ONSF or TRGSR register are "00b" (TAIIN pin input).

4. Count dow n w hen input on TAiOUT pin is low or count up w hen input on that pin is high. The port direction bit for TAiOUT pin is set to "0" (= input mode).

Figure 15.9 TAiMR Register in Event Counter Mode (when not using two-phase pulse signal processing)

Count Source • Two-phase pulse signals input to TAilN or TAiOUT pins (i=2 to 4) Count Operation • Up-count or down-count can be selected by two-phase pulse signal • When the timer overflows or underflows, it reloads the reload register cor and continues counting, When operating in free-running mode, the timer continues counting without reloading. Divide Ratio 1/ (FFFFh - n + 1) for up-count 1/ (n + 1) for down-count n : set value of TAi register 0000h to FFFFh Count Start Condition Set TAIS bit of TABSR register to "1" (= start counting) Count Stop Condition Set TAIS bit of "0" (= stop counting) Interrupt Request Timer overflow or underflow Generation Timing Two-phase pulse input TA2OUT Pin Function Two-phase pulse input TA2OUT Pin Function Two-phase pulse input Value written to TAi register is written to both reload register and counter when reloaded next) Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function ⁽¹⁾ • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAJIN when niput signal on TAJOUT pin is "H". TAjOUT TAjOUT TAJOUT pin is "H". * Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAKIN(K=3, 4) pin g	Item	Specification
Count Operation • Up-count or down-count can be selected by two-phase pulse signal • When the timer overflows or underflows, it reloads the reload register con and continues counting, When operating in free-running mode, the timer continues counting without reloading. Divide Ratio 1/ (FFFFh - n + 1) for up-count n : set value of TAi register 0000h to FFFFh Count Start Condition Set TAIS bit of TABSR register to "1" (= start counting) Count Stop Condition Set TAIS bit to "0" (= stop counting) Interrupt Request Generation Timing TA2DUT Pin Function Two-phase pulse input Read from Timer Count value can be read by reading Timer A2, A3 or A4 register Write to Timer •When not counting and until the 1st count source is input after counting Value written to TAi register is written to both reload register and counte • When counting (after 1st count source input) Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function (1) •Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAjIN when input signal on TAkOUT pin is "H". If the phase relationship is such that TAkIN (k=3, 4) ping oses "H" when th input signal on TAkOUT pin is "H", the timer counts up rising and falling edges on TAkOUT pin is "H," the timer counts up rising and falling edges or rown takkIN pins. TAkIN (k=3, 4)	Count Source	
1/ (n + 1) for down-count n : set value of TAi register 0000h to FFFFh Count Start Condition Set TAIS bit of TABSR register to "1" (= start counting) Count Stop Condition Set TAIS bit to "0" (= stop counting) Interrupt Request Timer overflow or underflow Generation Timing Two-phase pulse input TA2N Pin Function Two-phase pulse input Read from Timer Count value can be read by reading Timer A2, A3 or A4 register Write to Timer • When not counting and until the 1st count source is input after counting Value written to TAi register is written to both reload register and counte • When counting (after 1st count source input) Value written to Tai register is written to reload register (Transferred to counter when reloaded next) Select Function (1) • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAjIN when input signals on TAkOUT pin is "H". TAjOUT TajOUT TAjOUT TAkIN (ij=2, 3) Up- Up- Down- Down- • Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) If the phase relationship is such that TAkIN goes "L" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT and TAkIN pins. TAkOUT If the adges Count down al	Count Operation	 Up-count or down-count can be selected by two-phase pulse signal When the timer overflows or underflows, it reloads the reload register contents and continues counting. When operating in free-running mode, the timer
Count Stop Condition Set TAIS bit to "0" (= stop counting) Interrupt Request Timer overflow or underflow Generation Timing Two-phase pulse input TA2IN Pin Function Two-phase pulse input Read from Timer Count value can be read by reading Timer A2, A3 or A4 register Write to Timer •When not counting and until the 1st count source is input after counting Value written to TAi register is written to both reload register and counte • When counting (after 1st count source input) Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function ⁽¹⁾ • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAjIN when input signals on TAjOUT pin is "H". TAjOUT TAjOUT TAjOUT TAjOUT TAjOUT TAjOUT TAjOUT TAjOUT TAjOUT TAjOUT TAjOUT and TAkUN pins. If the phase relationship is such that TAkIN goes "L" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT pin all edges TAkIN Count up all edges Count d	Divide Ratio	1/ (n + 1) for down-count n : set value of TAi register 0000h to FFFh
Interrupt Request Generation Timing Timer overflow or underflow TA2IN Pin Function Two-phase pulse input Read from Timer Count value can be read by reading Timer A2, A3 or A4 register Write to Timer • When not counting and until the 1st count source is input after counting Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) • When counting (after 1st count source input) Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function ⁽¹⁾ • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAjIN when input signals on TAjOUT pin is "H". TAjIN Up- count Up- count Down- count Down- count • Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) pin goes "H" when th input signal on TAkOUT pin is "H," the timer counts up rising and falling e on TAkOUT and TAkIN pins. If the phase relationship is such that TAkIN goes "L" when the input signal on TAkOUT pin is "H," the timer counts or rising and falling edges on TAkOUT and TAkIN pins. TAkOUT If the signal on TAkOUT pin is "H," the timer counts or rising and falling edges on TAkOUT and TAkIN pins. TAkOUT If the input signal on TAkOUT pin is "H," the timer count down all edges TAkIN Count up all edges Count down all edge	Count Start Condition	Set TAiS bit of TABSR register to "1" (= start counting)
Generation Timing TA2IN Pin Function Two-phase pulse input Read from Timer Count value can be read by reading Timer A2, A3 or A4 register Write to Timer •When not counting and until the 1st count source is input after counting value written to TAi register is written to both reload register and counter •When counting (after 1st count source input) •Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function ⁽¹⁾ •Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAjIN when input signals on TAjOUT pin is "H". TAjOUT TAjOUT TAjOUT TAjOUT *Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) pin goes "H" when th input signal on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT and TAkIN pins. If the phase relationship is such that TAkIN goes "L" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT and TAkIN pins. TAkOUT Count up all edges Count down all edges TAkIN Count up all edges Count down all edges	Count Stop Condition	Set TAiS bit to "0" (= stop counting)
TA2OUT Pin Function Two-phase pulse input Read from Timer Count value can be read by reading Timer A2, A3 or A4 register Write to Timer • When not counting and until the 1st count source is input after counting Value written to TAi register is written to both reload register and counte • When counting (after 1st count source input) • When counting (after 1st count source input) Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function ⁽¹⁾ • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAjIN when input signals on TAjOUT pin is "H". TAjOUT • Normal processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) pin goes "H" when th input signal on TAkOUT pin is "H," the timer counts count on TAkOUT and TAkIN pins. If the phase relationship is such that TAkIN goes "L" when the input signal on TAkOUT pin is "H," the timer counts or rising and falling edges on TAkOUT and TAKIN pins. TAkOUT • Out up all edges • Count down all edges TAkIN (k=3, 4) • Out up all edges • Count down all edges		Timer overflow or underflow
Read from Timer Count value can be read by reading Timer A2, A3 or A4 register Write to Timer • When not counting and until the 1st count source is input after counting Value written to TAi register is written to both reload register and counte • When counting (after 1st count source input) Value written to TAi register is written to both reload register (Transferred to counter when reloaded next) Select Function ⁽¹⁾ • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAjIN when input signals on TAjOUT pin is "H". TAjIOUT TAjIOUT TAjIN Up- Up- Down- Down- count count • Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(K=3, 4) pin goes "H" when the input signal on TAkOUT pin is "H," the timer counts or rising and falling edges on TAkOUT pin is "H," the timer counts or rising and falling edges on TAkOUT and TAkIN pins. TAkOUT It the phase relationship is such that TAkIN pins. TAkOUT It the phase relationship is such that TAkIN pins. TAkOUT It the phase relationship is such that TAkIN pins. TAkOUT It the phase relationship is such that TAkIN pins. If the phase relationship is such that TAkIN pins. It the timer counts or rising and falling edges on TAkOUT and TAkIN pins. TAkOUT It the phase relationship is such that TakI	TA2IN Pin Function	Two-phase pulse input
Write to Timer • When not counting and until the 1st count source is input after counting Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function (1) • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAJIN when input signals on TAJOUT pin is "H". TAjOUT TAjOUT TAjOUT TAjOUT • Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) pin goes "H" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT and TAkIN pins. TAkOUT • TAkOUT TAkOUT • Count up all edges Count down all edges Count down all edges	TA2OUT Pin Function	Two-phase pulse input
Value written to TĂi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to reload register (Transferred to counter when reloaded next) Select Function ⁽¹⁾ • Normal processing operation (Timer A2 and Timer A3) The timer counts up rising edges or counts down falling edges on TAJIN when input signals on TAJOUT pin is "H". TAJOUT TAJIN (j=2, 3) Up- count count count count count count • Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAKIN(k=3, 4) pin goes "H" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT and TAKIN pins. If the phase relationship is such that TAKIN goes "L" when the input signal on TAkOUT and TAKIN pins. TAkOUT TAKOUT TAKOUT TAKOUT TAKOUT TAKIN (k=3, 4) Output all edges TAKIN (k=3, 4)	Read from Timer	
The timer counts up rising edges or counts down falling edges on TAjIN when input signals on TAjOUT pin is "H". TAjOUT TAjIN (j=2, 3) Up- Count Up- Count Up- Count Count Count Count Count Count • Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) pin goes "H" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling edges on TAkOUT and TAkIN pins. If the phase relationship is such that TAKIN goes "L" when the input signal on TAkOUT pin is "H," the timer counts count TAkOUT TAKOUT and TAKIN pins. TAKOUT TAKOUT Count up all edges TAkIN (k=3, 4) Count up all edges Count down all edges	Write to Timer	Value written to TAi register is written to reload register
TAjIN (j=2, 3) Up- count Up- count Count Count Count Count Count Count • Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) pin goes "H" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling efforts on TAkOUT and TAkIN pins. If the phase relationship is such that TAkIN goes "L" when the input signal on TAkOUT pin is "H," the timer counts of rising and falling edges on TAkOUT and TAkIN pins. TAkOUT $TAkOUT$ $T_{Count up all edges}$ Count down all edges TAkIN (k=3, 4) $T_{Count up all edges}$ Count down all edges	Select Function ⁽¹⁾	The timer counts up rising edges or counts down falling edges on TAjIN pin
goes "L" when the input signal on TAKOUT pin is "H," the timer counts of rising and falling edges on TAKOUT and TAkIN pins. TAKOUT Count up all edges Count down all edges TAKIN (k=3, 4) Count up all edges Count down all edges		 TAJIN (j=2, 3) Up- count Count Up- count Count Count Count Count Count Count Multiply-by-4 processing operation (Timer A3 and Timer A4) If the phase relationship is such that TAkIN(k=3, 4) pin goes "H" when the input signal on TAkOUT pin is "H," the timer counts up rising and falling edges
TAkIN (k=3, 4) Count up all edges Count down all edges		goes "L" when the input signal on TAkOUT pin is "H," the timer counts down rising and falling edges on TAkOUT and TAkIN pins.
(k=3, 4) Count up all edges Count down all edges		Count up all edges Count down all edges
		Count up all edges Count down all edges
Counter initialization by Z-phase input (Timer A3) The timer count value is initialized to 0 by Z-phase input. NOTES:		 Counter initialization by Z-phase input (Timer A3) The timer count value is initialized to 0 by Z-phase input.

Table 15.3Specifications in Event Counter Mode (when processing two-phase pulse signal with
Timer A2, A3 and A4)

NOTES:

1. Only Timer A3 is selectable. Timer A2 is fixed to normal processing operation, and Timer A4 is fixed to multiply-by-4 processing operation.

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15.	Timers

				gister (i=2 t ase pulse s		essing)		
b7 b	6 b5 b4	1 1	b1 b0	Syn		Address	After Reset	
					o TA4MR	0398h to 039Ah	00h	
				Bit Symbol		Bit Name	Function	RW
				TMOD0	Operation N	Node Select Bit	^{b1 b0} 0 1 : Event counter mode	RW
				TMOD1				RW
			MR0	To use tw o	-phase pulse signal proc	essing, set this bit to "0".	RW	
				MR1	To use tw o	-phase pulse signal proc	essing, set this bit to "0".	RW
				MR2	To use tw o	-phase pulse signal proc	essing, set this bit to "1".	RW
				MR3	To use tw o	-phase pulse signal proc	essing, set this bit to "0".	RW
				ТСК0	Count Oper	ation Type Select Bit	0 : Reload type 1 : Free-run type	RW
				TCK1		pulse signal processing ype Select Bit ^(1, 2)	0 : Normal processing operation 1 : Multiply-by-4 processing operation	RW

1. TCK1 bit is valid for Timer A3 mode register. No matter how this bit is set, Timer A2 and A4 alw ays operate in normal processing mode and x4 processing mode, respectively.

2. If two-phase pulse signal processing is desired, following register settings are required:

• Set the TAiP bit in the UDF register to "1" (tw o-phase pulse signal processing function enabled).

• Set the TAiTGH and TAiTGL bits in the TRGSR register to "00b" (TAilN pin input).

• Set the port direction bits for TAilN and TAiOUT to "0" (input mode).

Figure 15.10 TA2MR to TA4MR Registers in Event Counter Mode (when using two-phase pulse signal processing with Timer A2, A3 and A4)

15.1.2.1 Counter Initialization by Two-Phase Pulse Signal Processing

This function initializes the timer count value to "0" by Z-phase (counter initialization) input during two-phase pulse signal processing.

This function can only be used in Timer A3 event counter mode during two-phase pulse signal processing, freerunning type, x4 processing, with Z-phase entered from the ZP pin.

Counter initialization by Z-phase input is enabled by writing "0000h" to the TA3 register and setting the TAZIE bit in the ONSF register to "1" (= Z-phase input enabled).

Counter initialization is accomplished by detecting Z-phase input edge. The active edge can be chosen to be the rising or falling edge by using the POL bit in the INT2IC register. The Z-phase pulse width applied to the $\overline{INT2}$ pin must be equal to or greater than one clock cycle of Timer A3 count source.

The counter is initialized at the next count timing after recognizing Z-phase input. Figure 15.11 shows the Relationship Between the Two-Phase Pulse (A phase and B phase) and the Z-Phase.

If Timer A3 overflow or underflow coincides with the counter initialization by Z-phase input, a Timer A3 interrupt request is generated twice in succession. Do not use Timer A3 interrupt when using this function.

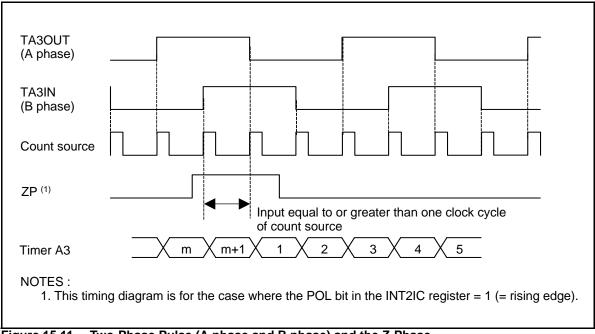


Figure 15.11 Two-Phase Pulse (A phase and B phase) and the Z-Phase

15.1.3 One-shot Timer Mode

In one-shot timer mode, the timer is activated only once by one trigger (see Table 15.4). When the trigger occurs, the timer starts up and continues operating for a given period. Figure 15.12 shows the TAiMR Register in One-Shot Timer Mode.

Item	Specification
Count Source	f1, f2, f8, f32, fC32
Count Operation	 Down-count When the counter reaches "0000h," it stops counting after reloading a new value If a trigger occurs when counting, the timer reloads a new count and restarts counting
Divide Ratio	1/n n : set value of TAi register (i=0 to 4) 0000h to FFFFh However, the counter does not work if the divide-by-n value is set to "0000h".
Count start Condition	 TAiS bit in the TABSR register = 1 (start counting) and one of the following triggers occurs. External trigger input from the TAiIN pin Timer B2 overflow or underflow, Timer Aj (j=i-1, except j=4 if i=0) overflow or underflow, Timer Ak (k=i+1, except k=0 if i=4) overflow or underflow The TAiOS bit in the ONSF register is set to "1"(= timer starts)
Count Stop Condition	 When the counter is reloaded after reaching "0000h" TAiS bit is set to "0" (= stop counting)
Interrupt Request Generation Timing	When the counter reaches "0000h"
TAiIN Pin Function	I/O port or trigger input
TAiOUT Pin Function	I/O port or pulse output
Read from Timer	An indeterminate value is read by reading TAi register
Write to Timer	 When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select Function	 Pulse output function The timer outputs a low when not counting and a high when counting.

 Table 15.4
 Specifications in One-shot Timer Mode

Г

b7 b	06 b5 b	94 b3 I	1 0	0			
Щ	Ľ۲,	┍╀┯╀	μμ	Sym		After Reset	
				TA0MR to			_
				Bit Symbol	Bit Name	Function	RV
			╷╷┕─	TMOD0	Operation Mode Select Bit	b1 b0	RV
				TMOD1		1 0 : One-shot timer mode	RV
				MRO	Pulse Output Function Select Bit	 0 : Pulse is not output (TAiOUT pin functions as I/O port) 1 : Pulse is output ⁽¹⁾ (TAiOUT pin functions as a pulse output pin) 	RV
				MR1	External Trigger Select Bit ⁽²⁾	0 : Falling edge of input signal to TAilN pin ⁽³⁾ 1 : Rising edge of input signal to TAilN pin ⁽³⁾	RV
				MR2	Trigger Select Bit	0 : TAiOS bit is enabled 1 : Selected by TAiTGH to TAiTGL bits	RV
				MR3	Set to "0" in one-shot timer m	node	RV
				TCK0	Count Source Select Bit	b7 b6 0 0 : f1 or f2 ⁽⁴⁾	RV
				TCK1		0 1 : f8 1 0 : f32 1 1 : fC32	RV

2. Effective when the TAiTGH and TAiTGL bits in the ONSF or TRGSR register are "00b" (TAilN pin input).

3. The port direction bit for the TAilN pin is set to "0" (= input mode).

4. Selected by PCLK0 bit in the PCLKR register.

Figure 15.12	TAIMR Register in One-Shot Timer Mode

15.1.4 Pulse Width Modulation (PWM) Mode

In PWM mode, the timer outputs pulses of a given width in succession (see Table 15.5). The counter functions as either 16-bit pulse width modulator or 8-bit pulse width modulator. Figure 15.13 shows TAiMR Register in PWM Mode. Figures 15.14 and 15.15 show Example of 16-bit Pulse Width Modulator Operation and Example of 8-bit Pulse Width Modulator Operation.

Item	Specification
Count Source	f1, f2, f8, f32, fC32
Count Operation	 Down-count (operating as an 8-bit or a 16-bit pulse width modulator) The timer reloads a new value at a rising edge of PWM pulse and continues counting The timer is not affected by a trigger that occurs during counting
16-bit PWM	 High level width n / fj n : set value of TAi register (i=o to 4) Cycle time (2¹⁶-1) / fj fixed fj: count source frequency (f1, f2, f8, f32, fC32)
8-bit PWM	 High level width n × (m+1) / fj n : set value of TAi register high-order address Cycle time (2⁸-1) × (m+1) / fj m : set value of TAi register low-order address
Count Start Condition	 TAiS bit of TABSR register is set to "1" (= start counting) The TAiS bit = 1 and external trigger input from the TAilN pin The TAiS bit = 1 and one of the following external triggers occurs Timer B2 overflow or underflow, Timer Aj (j=i-1, except j=4 if i=0) overflow or underflow, Timer Ak (k=i+1, except k=0 if i=4) overflow or underflow
Count Stop Condition	TAiS bit is set to "0" (= stop counting)
Interrupt Request Generation Timing	On the falling edge of PWM pulse
TAiIN Pin Function	I/O port or trigger input
TAiOUT Pin Function	Pulse output
Read from Timer	An indeterminate value is read by reading TAi register
Write to Timer	 When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)

Table 15.5 Specifications in PWM Mode

Timer	Ai I	Mode F	Regi	ster (i= 0 to	o 4)			
b7 b6 t	b5 b4	b3 b2 b1	b0					
		1	1	Symbo		Address	After Reset	
			_ ا	TA0MR to T	TA4MR	0396h to 039Ah	00h	
				Bit Symbol		Bit Name	Function	RW
			Ч	TMOD0	Operatio	on Mode Select Bit	b1 b0	RW
				TMOD1			1 1 : PWM mode ⁽¹⁾	RW
				MR0	Pulse O Select E	utput Function bit ⁽⁴⁾	 0 : Pulse is not output (TAiOUT pin functions as I/O port) 1 : Pulse is output ⁽¹⁾ (TAiOUT pin functions as a pulse output pin) 	RW
				MR1	External Bit ⁽²⁾	Trigger Select	0 : Falling edge of input signal to TAilN pin ⁽³⁾ 1 : Rising edge of input signal to TAilN pin ⁽³⁾	RW
				MR2	Trigger	Select Bit	0 : Write "1" to TAiS bit in the TASF register 1 : Selected by TAiTGH to TAiTGL bits	RW
				MR3	16/8-Bit Bit	PWM Mode Select	0 : Functions as a 16-bit pulse w idth modulator 1 : Functions as an 8-bit pulse w idth modulator	RW
				TCK0	Count S	ource Select Bit	^{b7 b6} 0 0 : f1 or f2 ⁽⁵⁾ 0 1 : f8	RW
				TCK1			1 0 : f32 1 1 : fC32	RW

NOTES :

1. TA0OUT pin is N-channel open drain output.

2. Effective when the TAiTGH and TAiTGL bits in the ONSF or TRGSR register are "00b" (TAilN pin input).

3. The port direction bit for the TAilN pin is set to "0" (= input mode).

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4. Set this bit to "1" (Pulse is output) to output PWM pulse.

5. Selected by PCLK0 bit in the PCLKR register.

Figure 15.13 TAIMR Register in PWM Mode

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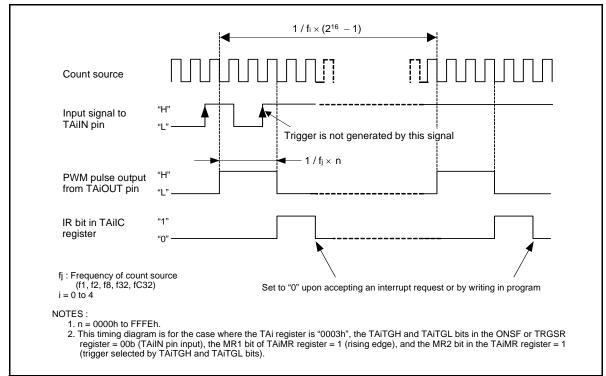
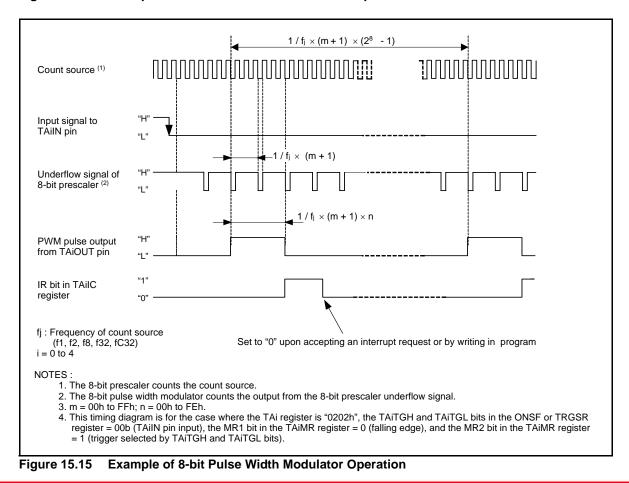


Figure 15.14 Example of 16-bit Pulse Width Modulator Operation



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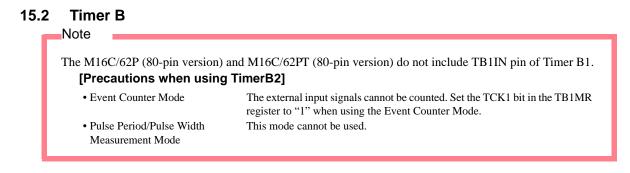


Figure 15.16 shows a Timer B Block Diagram. Figures 15.17 and 15.18 show registers related to the Timer B. Timer B supports the following three modes. Use the TMOD1 and TMOD0 bits in the TBiMR register (i = 0 to 5) to select the desired mode.

- Timer Mode:
- Event Counter Mode:

The timer counts an internal count source.

The timer counts pulses from an external device or overflows or underflows of other timers.

• Pulse Period/Pulse Width Measurement Mode:

The timer measures pulse period or pulse width of an external signal.

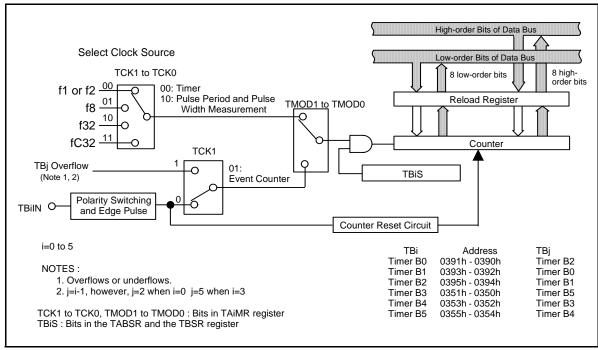
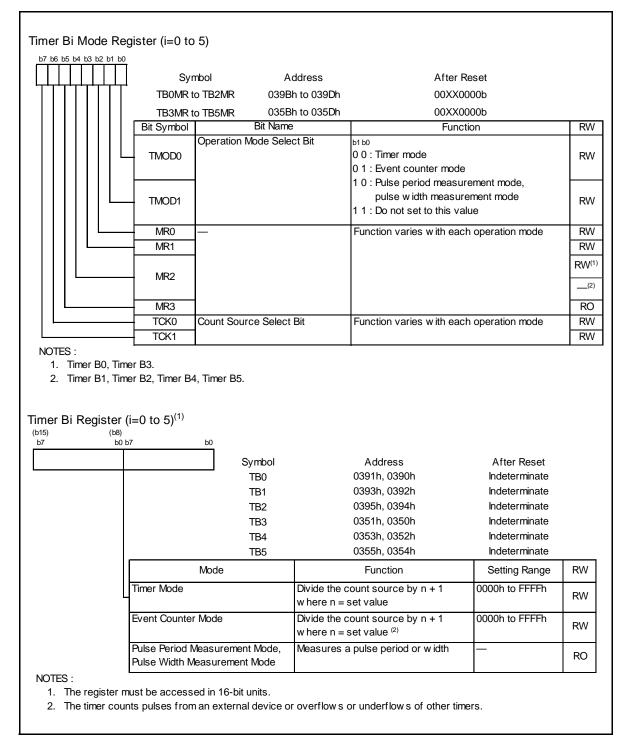


Figure 15.16 Timer B Block Diagram

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o7 b6 b5 b4 b3 b2 b1 b0	1			
		mbol Address	After Reset	
		BSR 0380h	00h	
	Bit Symbol	Bit Name	Function	R
╵╵╵╵╵╵└	TA0S	Timer A0 Count Start Flag	0 : Stops counting	R
	TA1S	Timer A1 Count Start Flag	1 : Starts counting	R
	TA2S	Timer A2 Count Start Flag		R
	TA3S	Timer A3 Count Start Flag		R
	TA4S	Timer A4 Count Start Flag		R
	- TB0S	Timer B0 Count Start Flag		R
	TB1S	Timer B1 Count Start Flag		R
	TB2S	Timer B2 Count Start Flag		R
	Bit Symbol	Bit Name	Function	R
	Sym	ool Address	After Reset	
	TBS Bit Symbol		000XXXXXb	DI
		Nothing is assigned. When write		
	(b4-b0)	When read, their contents are in		_
	(b4-b0) TB3S			
	, ,	When read, their contents are in	determinate.	
	TB3S	When read, their contents are in Timer B3 Count Start Flag	determinate. 0 : Stops counting	R
DCK Prescaler R 7 66 105 104 103 102 101 100	TB3S TB4S TB5S Ceset Flag Symbol	When read, their contents are in Timer B3 Count Start Flag Timer B4 Count Start Flag Timer B5 Count Start Flag Address	0 : Stops counting 1 : Starts counting After Reset	R\
	TB3S TB4S TB5S Ceset Flag Symbol CPSRF	When read, their contents are in Timer B3 Count Start Flag Timer B4 Count Start Flag Timer B5 Count Start Flag	determinate. 0 : Stops counting 1 : Starts counting	R\
	TB3S TB4S TB5S Ceset Flag Symbol	When read, their contents are in Timer B3 Count Start Flag Timer B4 Count Start Flag Timer B5 Count Start Flag Address 0381h Bit Name	determinate. 0 : Stops counting 1 : Starts counting After Reset 0XXXXXXb Function	R\ R\ R\ R\
	TB3S TB4S TB5S Ceset Flag Symbol CPSRF	When read, their contents are in Timer B3 Count Start Flag Timer B4 Count Start Flag Timer B5 Count Start Flag Address 0381h	determinate. 0 : Stops counting 1 : Starts counting After Reset 0XXXXXXb Function set to "0".	R

Figure 15.18 TABSR, TBSR and CPSRF Registers

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15.2.1 Timer Mode

In timer mode, the timer counts a count source generated internally (see Table 15.6). Figure 15.19 shows TBiMR Register in Timer Mode.

Item	Specification
Count Source	f1, f2, f8, f32, fC32
Count Operation	 Down-count When the timer underflows, it reloads the reload register contents and
	continues counting
Divide Ratio	1/(n+1) n: set value of TBi register (i= 0 to 5) 0000h to FFFFh
Count Start Condition	Set TBiS bit ⁽¹⁾ to "1" (= start counting)
Count Stop Condition	Set TBiS bit to "0" (= stop counting)
Interrupt Request Generation Timing	Timer underflow
TBiIN Pin Function	I/O port
Read from Timer	Count value can be read by reading TBi register
Write to Timer	• When not counting and until the 1st count source is input after counting start Value written to TBi register is written to both reload register and counter
	 When counting (after 1st count source input) Value written to TBi register is written to only reload register
	(Transferred to counter when reloaded next)

Table 15.6 Specifications in Timer Mode

NOTES:

1. The TB0S to TB2S bits are assigned to the bit 5 to bit 7 in the TABSR register, and the TB3S to TB5S bits are assigned to the bit 5 to bit 7 in the TBSR register.

b7 b6	b5 b4	b3 b2 b1 b0						
ЦЦ	Щ		Syn		Address		After Reset	
				DTB2MR	039Bh to 039E		00XX0000b	
			TB3MR to	D TB5MR	035Bh to 035E	h	00XX0000b	
			Bit Symbol		Bit Name		Function	RV
			TMOD0	Operation	Mode Select Bit	b1 b0		RV
			TMOD1			00:Timer	mode	RV
			MR0	Has no eff	ect in timer mode			RV
			MR1	Can be set	t to "0" or "1"			RV
		MR2	Set to "0" TB1MR, TE Nothing is	33MR registers in timer mode 32MR, TB4MR, TB5 assigned. When v d, its content is inc	v rite, set to "0".		RV	
			MR3		e in timer mode, se d in timer mode, its		erminate.	RC
			TCK0	Count Sou	rce Select Bit	^{b7 b6} 0 0 : f1 or f 0 1 : f8	2 (1)	RV
			TCK1			1 0 : f32 1 1 : fC32		RV

Figure 15.19 TBiMR Register in Timer Mode

Rev.2.41 Jan 10, 2006 Page 159 of 390 **RENESAS** REJ09B0185-0241 In event counter mode, the timer counts pulses from an external device or overflows and underflows of other timers (see Table 15.7). Figure 15.20 shows TBiMR Register in Event Counter Mode.

Item	Specification			
Count Source	• External signals input to TBilN pin (i=0 to 5) (effective edge can be selected in program)			
	• Timer Bj overflow or underflow (j=i-1, except j=2 if i=0, j=5 if i=3)			
Count Operation	 Down-count When the timer underflows, it reloads the reload register contents and continues counting 			
Divide Ratio	1/(n+1) n: set value of TBi register 0000h to FFFFh			
Count Start Condition	Set TBiS bit ⁽¹⁾ to "1" (= start counting)			
Count Stop Condition	Set TBiS bit to "0" (= stop counting)			
Interrupt Request Generation Timing	Timer underflow			
TBiIN Pin Function	Count source input			
Read from Timer	Count value can be read by reading TBi register			
Write to Timer	• When not counting and until the 1st count source is input after counting start Value written to TBi register is written to both reload register and counter			
	 When counting (after 1st count source input) 			
	Value written to TBi register is written to only reload register			
	(Transferred to counter when reloaded next)			

 Table 15.7
 Specifications in Event Counter Mode

NOTES:

1. The TB0S to TB2S bits are assigned to the bit 5 to bit 7 in the TABSR register, and the TB3S to TB5S bits are assigned to the bit 5 to bit 7 in the TBSR register.

b7 b6 b5	b4 b3 b2 b1 b0					
	0 1	Sy	mbol	Address	After Reset	
		TB0MR	to TB2MR	039Bh to 039Dh	00XX0000b	
		TB3MR	to TB5MR	035Bh to 035Dh	00XX0000b	
		Bit Symbol		Bit Name	Function	RW
	-	TMOD0	Operation N	lode Select Bit	b1 b0	RW
		TMOD1			0 1 : Event counter mode	RW
		MR0	Count Polari	ty Select Bit ⁽¹⁾	b3 b2 0 0 : Counts falling edges of external signal 0 1 : Counts rising edges of external signal	RW
		MR1			 1 0 : Counts falling and rising edges external signal 1 1 : Do not set to this value 	RW
		MEG		BMR registers n event counter mode		RW
		MR2	Nothing is a	2MR, TB4MR, TB5MR assigned. When w rite , its content is indeter	, set to "0".	_
		MR3		in event counter mod in event counter mod	e, set to "0". e, its content is indeterminate.	RC
		TCK0		ct in event counter m to "0" or "1".	ode.	RW
		TCK1	Event Clock	Select	0 : Input from TBilN pin ⁽²⁾ 1 : TBj overflow or underflow (j = i - 1, how ever, j = 2 if i = 0, j = 5 if i = 3)	RW

1. Effective when the TCK1 bit = 0 (input from TBilN pin). If the TCK1 bit = 1 (TBj overflow or underflow), these bits can be set to "0" or "1".

2. The port direction bit for the TBilN pin must be set to "0" (= input mode).

Figure 15.20 TBiMR Register in Event Counter Mode

15.2.3 Pulse Period and Pulse Width Measurement Mode

In pulse period and pulse width measurement mode, the timer measures pulse period or pulse width of an external signal (see Table 15.8). Figure 15.21 shows TBiMR Register in Pulse Period and Pulse Width Measurement Mode. Figure 15.22 shows the Operation Timing when Measuring a Pulse Period. Figure 15.23 shows the Operation Timing when Measuring a Pulse Width.

Item	Specification		
Count Source	f1, f2, f8, f32, fC32		
Count Operation	• Up-count		
	Counter value is transferred to reload register at an effective edge of		
	measurement pulse. The counter value is set to "0000h" to continue counting.		
Count Start Condition	Set TBiS (i=0 to 5) bit ⁽³⁾ to "1" (= start counting)		
Count Stop Condition	Set TBiS bit to "0" (= stop counting)		
Interrupt Request Generation Timing	 When an effective edge of measurement pulse is input ⁽¹⁾ Timer overflow. When an overflow occurs, MR3 bit in the TBiMR register is set to "1" (overflowed) simultaneously. MR3 bit is set to "0" (no overflow) by writing to TBiMR register at the next count timing or later after MR3 bit was set to "1". At this time, make sure TBiS bit is set to "1" (start counting). 		
TBiIN Pin Function	Measurement pulse input		
Read from Timer	Contents of the reload register (measurement result) can be read by reading TBi register ⁽²⁾		
Write to Timer	Value written to TBi register is written to neither reload register nor counter		

Table 15.8 Specifications in Pulse Period and Pulse Width Measurement Mode

NOTES:

- 1. Interrupt request is not generated when the first effective edge is input after the timer started counting.
- 2. Value read from TBi register is indeterminate until the second valid edge is input after the timer starts counting.
- 3. The TB0S to TB2S bits are assigned to the bit 5 to bit 7 in the TABSR register, and the TB3S to TB5S bits are assigned to the bit 5 to bit 7 in the TBSR register.

Timer Bi	Mode Reg	ister (i=0 to	o 5)		
	b4 b3 b2 b1 b0				
		Symb TB0MR to TB3MR to	TB2MR 039Bh to 039Dh	After Reset 00XX0000b 00XX0000b	
		Bit Symbol	Bit Name	Function	RW
	∟	TMOD0	Operation Mode Select Bit	b1 b0	RW
		TMOD1		1 0 : Pulse period / pulse width measurement mode	RW
		MRO	Measurement Mode Select Bit	 b3 b2 0 0 : Pulse period measurement (Measurement betw een a falling edge and the next falling edge of measured pulse) 0 1 : Pulse period measurement (Measurement betw een a rising edge and the next falling edge of measured pulse) 	RW
		MR1		 the next rising edge of measured pulse) 1 0 : Pulse width measurement (Measurement betw een a falling edge and the next rising edge of measured pulse and betw een a rising edge and the next falling edge) 1 1 : Do not set to this value 	RW
			TB0MR, TB3MR registers Set to "0" in pulse period ar	I d pulse width measurement mode	RW
		MR2	TB1MR, TB2MR, TB4MR, TB Nothing is assigned. When When read, its content is in	w rite, set to "0".	_
		MR3	Timer Bi Overflow Flag ⁽¹⁾	0 : Timer did not overflow 1 : Timer has overflow ed	RO
		TCK0	Count Source Select Bit	^{b7} ^{b6} 0 0 : f1 or f2 ⁽²⁾	RW
		TCK1]	0 1 : f8 1 0 : f32 1 1 : fC32	RW
NOTES				1 (start counting), the MP2 bit is cleared to "0" (no c	

This flag is indeterminate after reset. When the TBiS bit = 1 (start counting), the MR3 bit is cleared to "0" (no overflow) by writing to the TBiMR register at the next count timing or later after the MR3 bit was set to "1" (overflow ed). The MR3 bit cannot be set to "1" in a program. The TB0S to TB2S bits are assigned to the bit 5 to bit 7 in the TABSR register, and the TB3S to TB5S bits are assigned to the bit 5 to bit 7 in the TBSR register.

2. Selected by PCLK0 bit in the PCLKR register.



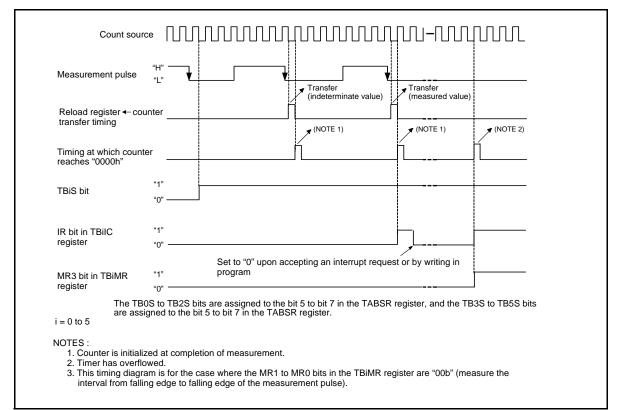
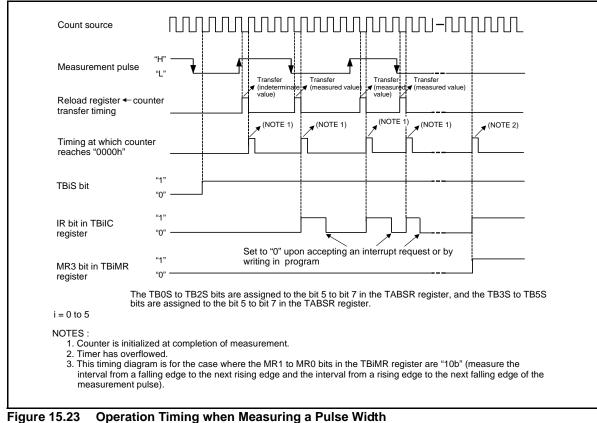


Figure 15.22 **Operation Timing when Measuring a Pulse Period**



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16. Three-Phase Motor Control Timer Function

Note

The M16C/62P (80-pin version) and M16C/62PT (80-pin version) do not use this function.

Timers A1, A2, A4 and B2 can be used to output three-phase motor drive waveforms. Table 16.1 lists the Three-phase Motor Control Timer Functions Specifications. Figure 16.1 shows the Three-phase Motor Control Timer Functions Block Diagram. Also, the related registers are shown on Figure 16.2 to Figure 16.8.

Item	Specification
Three-Phase Waveform Output Pin	Six pins (U, \overline{U} , V, \overline{V} , W, \overline{W})
Forced Cutoff Input(1)	Input "L" to MII pin
Used Timers	Timer A4, A1, A2 (used in the one-shot timer mode) Timer A4: U- and U-phase waveform control Timer A1: V- and V-phase waveform control Timer A2: W- and W-phase waveform control Timer B2 (used in the timer mode) Carrier wave cycle control
	Dead time timer (3 eight-bit timer and shared reload register) Dead time control
Output Waveform	Triangular wave modulation, Sawtooth wave modification Enable to output "H" or "L" for one cycle Enable to set positive-phase level and negative-phase level respectively
Carrier Wave Cycle	Triangular wave modulation: count source x (m+1) x 2 Sawtooth wave modulation: count source x (m+1) m: Setting value of TB2 register, 0000h to FFFFh Count source: f1, f2, f8, f32, fC32
Three-Phase PWM Output Width	Triangular wave modulation: count source x n x 2 Sawtooth wave modulation: count source x n n: Setting value of TA4, TA1 and TA2 register (of TA4, TA41, TA1, TA11, TA2 and TA21 registers when setting the INV11 bit to "1"), 0001h to FFFFh Count source: f1, f2, f8, f32, fC32
Dead Time	Count source x p, or no dead time p: Setting value of DTT register, 01h to FFh Count source: f1, f2, f1 divided by 2, f2 divided by 2
Active Level	Enable to select "H" or "L"
Positive and Negative-Phase Concurrent Active Disable Function	Positive and negative-phases concurrent active disable function Positive and negative-phases concurrent active detect function
Interrupt Frequency	For Timer B2 interrupt, select a carrier wave cycle-to-cycle basis through 15 times carrier wave cycle-to-cycle basis

 Table 16.1
 Three-phase Motor Control Timer Functions Specifications

NOTES:

 Forced cutoff with NMI input is effective when the IVPCR1 bit in the TB2SC register is set to "1" (three-phase output forcible cutoff by NMI input enabled). If an "L" signal is applied to the NMI pin when the IVPCR1 bit is "1," the related pins go to a high-impedance state regardless of which functions of those pins are being used.

Related pins P7_2/CLK2/TA1OUT/V, P7_3/CTS2/RTS2/TA1IN/V, P7_4/TA2OUT/W, P7_5/TA2IN/W, P8_0/TA4OUT/U, P8_1/TA4IN/U

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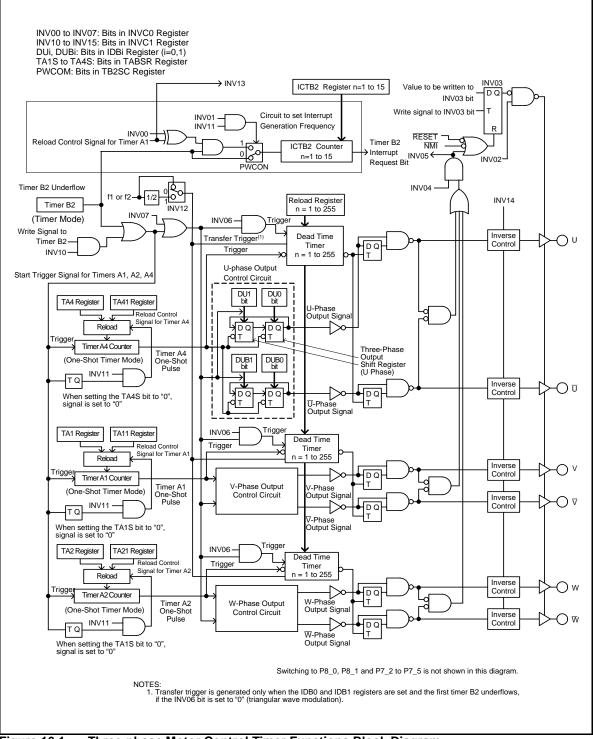


Figure 16.1 Three-phase Motor Control Timer Functions Block Diagram

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		Symbol	Address	After Reset	
		INV CO	0348h	00h	
		Bit Symbol	Bit Name	Function	R\
		INV 00	Interrupt Enable Output Polarity Select Bit ⁽³⁾	 0 : The ICTB2 counter is incremented by one on the rising edge of Timer A1 reload control signal 1 : The ICTB2 counter is incremented by one on the falling edge of Timer A1 reload control signal 	R
		INV01	Interrupt Enable Output Specification Bit ^(2, 3)	 0 : ICTB2 counter is incremented by one when Timer B2 underflows 1 : Selected by the INV00 bit 	R\
		INV02	Mode Select Bit ^(4, 5)	0 : No three-phase control timer functions 1 : Three-phase control timer function	R\
		INV03	Output Control Bit ^(5, 6)	0 : Disables three-phase control timer output 1 : Enables three-phase control timer output	R\
		INV04	Positive and Negative-Phases Concurrent Active Disable Function Enable Bit	0 : Enables concurrent active output 1 : Disables concurrent active output	R\
		INV 05	Positive and Negative-Phases Concurrent Active Output Detect Flag ⁽⁷⁾	0 : Not detected 1 : Detected	R\
		INV 06	Modulation Mode Select ^(8, 9)	0 : Triangular w ave modulation mode 1 : Saw tooth w ave modulation mode	R۱
		INV07	Softw are Trigger Select	Transfer trigger is generated when the INV07 bit is set to "1". Trigger to the dead time timer is also generated when setting the INV06 bit to "1". Its value is "0" when read.	R\
Rewr	ite the INVC	0 to INV02 and	PRC1 bit in the PRCR register is s INV06 bits when Timers A1, A2, A4 ting the ICTB2 register.	et to "1" (write enable).	ed

When the INV00 bit is set to "1", the first interrupt is generated when Timer B2 underflows n-1 times, if n is the value set in the ICTB2 counter. Subsequent interrupts are generated every n times Timer B2 underflows.

4. Set the INV02 bit to "1" to operate the dead time timer, U-, V-and W-phase output control circuits and ICTB2 counter.

5. When the INVC03 bit is set to "1", the pins applied to U/V/W output three-phase PWM.

The U, U, V, V, W and W pins, including pins shared with other output functions, are all placed in high-impedance states when the following conditions are all met.

- The INV02 bit is set to "1" (three-phase control timer function)
- The INV03 bit is set to "0" (three-phase control timer output disabled)
- Direction registers of each port are set to "0" (input mode)
- The INV03 bit is set to "0" when the followings conditions are all met.
 Reset
 - A concurrent active state occurs while INV04 bit is set to "1"
 - The INV03 bit is set to "0" by program
 - A signal applied to the NMI pin changes "H" to "L"
 - When both the INVC04 and INVC05 bits are set to "1", the INVC03 bit is set to "0".
- 7. The INV05 bit can not be set to "1" by program. Set the INV04 bit to "0", as well, when setting the INV05 bit to "0".
- 8. The following table describes how the INV06 bit works

Item	INV06=0	INV06=1
Mode	Triangular wav e modulation mode	Sawtooth wave modulation mode
Timing to Transfer from the IDB0 and IDB1 Registers to Three Phase Output Shift Register	Transferred once by generating a transfer trigger after setting the IDB0 and IDB1 registers	Transferred every time a transfer trigger is generated
Timing to Trigger the Dead Time Timer when the INV16 Bit=0	On the falling edge of a one-shot pulse of the timer A1, A2 or A4	By a transfer trigger, or the falling edge o a one-shot pulse of the timer A1, A2 or A
INV13 Bit	Enabled when the INV11 bit=1 and the INV06 bit=0	Disabled

Transfer trigger : Timer B2 underflows and write to the INV07 bit, or write to the TB2 register when INV10 = 1

9. When the INV06 bit is set to "1", set the INV11 bit to "0" (three-phase mode 0) and the PWCON bit in the TB2SC register to "0" (reload Timer B2 with Timer B2 underflow).

Figure 16.2 INVC0 Register

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	Symbol	Address		After Reset	
	INVC1	0349h		00h	
	Bit Symbol	Bit Name		Function	R
	INV10	Timer A1, A2 and A4 Start Trigger Select Bit	1 : Timer B2	underflow and write to Timer B2	R
	INV11	Timer A1-1, A2-1 and A4-1 Control Bit ^(2, 3)	0 : Three-ph 1 : Three-ph		R
	INV12	Dead Time Timer Count Source Select Bit	0 : f1 or f2 1 : f1 divided	d-by-2 or f2 divided-by-2	R
	INV 13	Carrier Wave Detect Bit (4)		reload control signal is "0" reload control signal is "1"	R
	INV 14	Output Polarity Control Bit		" of an output w aveform " of an output w aveform	R
	INV 15	Dead Time Disable Bit	0 : Enables o 1 : Disables		R
	INV 16	Dead Time Timer Trigger Select Bit	A2, A4 (5)		
			-	ge of the three-phase output shift U-, V-, W-phase)	R
	(b7) VC1 register a	Reserved Bit after the PRC1 bit in the PRC B2 must be stopped during r	register (Set to "0" R register is s	U-, V-, W-phase)	R
 Rew rite the IN The timers A1, The follow ing the follo	(b7) VC1 register a , A2, A4, and table lists how	after the PRC1 bit in the PRC B2 must be stopped during r / the INV11 bit w orks.	register (Set to "0" R register is s	U-, V-, W-phase) et to "1" (w rite enable).	
 Rew rite the IN The timers A1, The follow ing to Item 	(b7) VC1 register a , A2, A4, and table lists how	after the PRC1 bit in the PRC B2 must be stopped during r / the INV11 bit w orks. INV11=0	register (Set to "0" R register is s	U-, V-, W-phase) et to "1" (w rite enable).	_
 Rew rite the IN The timers A1, The follow ing the follo	(b7) VC1 register a , A2, A4, and table lists how	after the PRC1 bit in the PRC B2 must be stopped during r / the INV11 bit w orks.	register (Set to "0" R register is s	U-, V-, W-phase) et to "1" (w rite enable).	
 Rew rite the IN The timers A1, The follow ing to Item Mode TA11, TA21 and T 	(b7) VC1 register a , A2, A4, and table lists how	after the PRC1 bit in the PRC B2 must be stopped during r / the INV11 bit w orks. INV11=0 Three-phase mode 0	register (Set to "0" R register is s rew rite.	U-, V-, W-phase) et to "1" (w rite enable). INV11=1 Three-phase mode 1	
1. Rew rite the IN The timers A1, 2. The follow ing to Item Mode TA11, TA21 and T Registers INV00 and INV01 E	(b7) VC1 register a , A2, A4, and table lists how TA41 Bit	after the PRC1 bit in the PRC B2 must be stopped during r / the INV11 bit w orks. INV11=0 Three-phase mode 0 Not used Disabled. The ICTB2 counter is increr w henever Timer B2 underf Disabled	register (Set to "0" R register is s rew rite.	U-, V-, W-phase) et to "1" (w rite enable). INV11=1 Three-phase mode 1 Used	

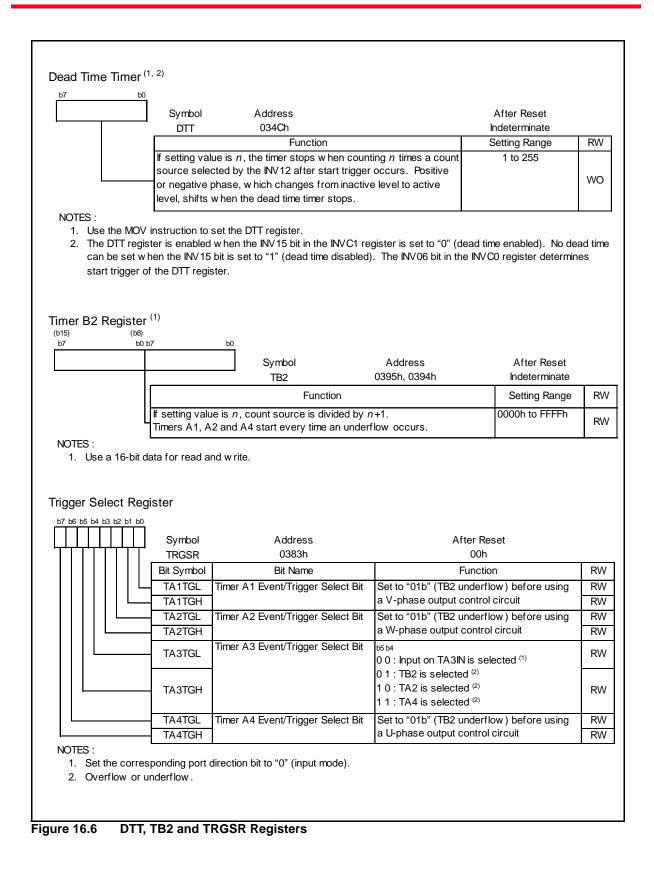
VМ		Current al		Address	After Depet	
ĄΨ		Symbol ICTB2		Address 034Dh	After Reset	
		ICTD2	Fi	unction	Setting Range	F
		/hen the INV01 b		e ICTB2 counter increments whenev		+-
			•	ng value is <i>n</i> , Timer B2 interrupt is		
	g	enerated every <i>i</i>	th time Timer B2	underflow occurs.		
			•	e INV00 bit selects count timing of th	ıe	V
			-	<i>n</i> , Timer B2 interrupt is generated		
		W00 bit occurs.	er bz undernow	meeting the condition selected in th	e	
	N	othing is assigne	ed. When write, s	set to "0".		
2. If If 3. If	the INV01 bit is the INV01 bit is 2 underflow s. the INV00 bit is	set to "1", set th set to "0" and th set to "1", the fir	e TB2S bit to "1"	w hen the TB2S bit is set to "0" (Tim (Timer B2 counter start), do not set nerated w hen Timer B2 underflow s enerated every <i>n</i> times Timer B2 un	the ICTB2 register when n-1 times, <i>n</i> being the va	
imer ^{b15)} b7	Ai, Ai-1 Regi (b8) b0 b		4) ^{(1, 2, 3, 4, 5, 6,}			
ļ			Symbol	Address	After Reset Indeterminate	
			TA1, TA2 TA4	0389h to 0388h, 038Bh to 038Ah 038Fh to 038Eh	Indeterminate	
				0343h to 0342h, 0345h to 0344h	Indeterminate	
			TA41	0347h to 0346h	Indeterminate	
			F	unction	Setting Range	1
		If setting value	is <i>n</i> , the timer st	ops when the <i>n</i> th count source is	0000h to FFFFh	+
			a start trigger is g			
	-		o o	ative phase, and vice versa, when		1
		Timers A1, A2	and A4 stop.			
NOT		ata for read and				
1.		0		ounters start and no Timer Ai interru	ipt is generated.	
1. 2				registers. o "0" (dead timer enabled), phase sv	witches from an inactive	
1. 2 3			time timer stops.	0 0 (dead timer enabled), phase s		
1. 2 3		1 bit is set to "0"	' (three-phase mo	ode 0), the value of the TAi register	is transferred to the reloa	ad
1. 2 3				ode 1), the value of the TAi1 register	r is first transferred to th	е
1. 2 3 4	register by a T		· ·	the value of the TAi register is tran		
1. 2 3 4	register by a T When the INV1	1 bit is set to "1"	art trigger. Then,		r with every Timer Ai sta	art
1. 2 3 4	register by a T When the INV1 reload register	1 bit is set to "1" by a Timer Ai st		rred alternately to the reload registe		
1. 2 3 4	register by a T When the INV1 reload register	1 bit is set to "1" by a Timer Ai st		rred alternately to the reload registe		
1. 2 3 4	register by a T When the INV1 reload register values of the T trigger.	1 bit is set to "1" by a Timer Ai st Ai1 and TAi regi				
1. 2 3 4 5	register by a T When the INV1 reload register values of the T trigger. Do not w rite to	1 bit is set to "1" by a Timer Ai st TAi1 and TAi regi these registers	isters are transfe	B2 underflow s.		
1. 2 3 4 5	register by a T When the INV1 reload register values of the T trigger. Do not w rite to Follow the pro (a) Write value	1 bit is set to "1" by a Timer Ai st TAi1 and TAi region these registers cedure below to le to the TAi1 region	isters are transfe w hen the Timer I set the TAi1 regi gister,	B2 underflow s.		
1. 2 3 4 5	register by a T When the INV1 reload register values of the T trigger. Do not w rite to Follow the pro (a) Write valu (b) Wait one	1 bit is set to "1" by a Timer Ai st TAi1 and TAi region these registers cedure below to le to the TAi1 reg Timer Ai count so	isters are transfe w hen the Timer I set the TAi1 regi	B2 underflow s. ster.		

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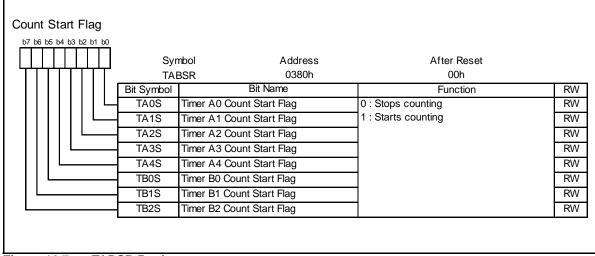
		Symbo TB2S0	C 039Eh	After Reset XXXXXX00b	
		Bit Symbol	Bit Name	Function	RV
			Timer B2 Reload Timing Switching Bit	0 : Timer B2 underflow 1 : Timer A output at odd-numbered occurrences ⁽²⁾	RW
		IVPCR1	Three Phase Output Port NM Control Bit 1(3)	 0 : Three-phase output forcible cutoff by NMI input (high-impedance) disabled 1 : Three-phase output forcible cutoff by NMI input (high-impedance) enabled 	RW
			Nothing is assigned. When w When read, their contents are		-
				pedance state regardless of which functions of those p	oins are
'nree-Pha	-			NMI pin and set IVPCR1 bit to "0": this forced cutoff will	be reset
b7 b6 b5 b4 b	se Outp	ut Buffer Re	gister i ⁽¹⁾ (i=0, 1)		be reset
	se Outp	ut Buffer Re Symbol	gister i ⁽¹⁾ (i=0, 1) Address	After Reset	be rese
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol IDB0, IDB1	gister i ⁽¹⁾ (i=0, 1)		be reset
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol	gister i ⁽¹⁾ (i=0, 1) Address 034Ah, 034Bh	After Reset 00h	RV
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol IDB0, IDB1 Bit Symbol	gister i ⁽¹⁾ (i=0, 1) Address 034Ah, 034Bh Bit Name	After Reset 00h Function Write output level 0 : Active level 1 : Inactive level	RV RV
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol IDB0, IDB1 Bit Symbol DUi	gister i ⁽¹⁾ (i=0, 1) Address 034Ah, 034Bh Bit Name U-Phase Output Buffer i	After Reset 00h Function Write output level 0 : Active level	RV RV RV
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol IDB0, IDB1 Bit Symbol DUi DUBi	gister i ⁽¹⁾ (i=0, 1) Address 034Ah, 034Bh Bit Name U-Phase Output Buffer i Ū-Phase Output Buffer i V-Phase Output Buffer i V-Phase Output Buffer i	After Reset 00h Function Write output level 0 : Active level 1 : Inactive level When read, the value of the three-phase shift	RV RV RV
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol IDB0, IDB1 Bit Symbol DUi DUBi DVi	gister i ⁽¹⁾ (i=0, 1) Address 034Ah, 034Bh Bit Name U-Phase Output Buffer i Ū-Phase Output Buffer i V-Phase Output Buffer i V-Phase Output Buffer i W-Phase Output Buffer i	After Reset 00h Function Write output level 0 : Active level 1 : Inactive level When read, the value of the three-phase shift	RV RV RV RV
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol IDB0, IDB1 Bit Symbol DUi DUBi DV i DV Bi	gister i ⁽¹⁾ (i=0, 1) Address 034Ah, 034Bh Bit Name U-Phase Output Buffer i Ū-Phase Output Buffer i V-Phase Output Buffer i V-Phase Output Buffer i W-Phase Output Buffer i W-Phase Output Buffer i	After Reset 00h Function Write output level 0 : Active level 1 : Inactive level When read, the value of the three-phase shift register is read.	RV RV RV RV
b7 b6 b5 b4 b	se Outp	ut Buffer Re Symbol IDB0, IDB1 Bit Symbol DUi DUBi DVBi DVBi	gister i ⁽¹⁾ (i=0, 1) Address 034Ah, 034Bh Bit Name U-Phase Output Buffer i Ū-Phase Output Buffer i V-Phase Output Buffer i V-Phase Output Buffer i W-Phase Output Buffer i	After Reset 00h Function Write output level 0 : Active level 1 : Inactive level When read, the value of the three-phase shift	

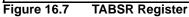


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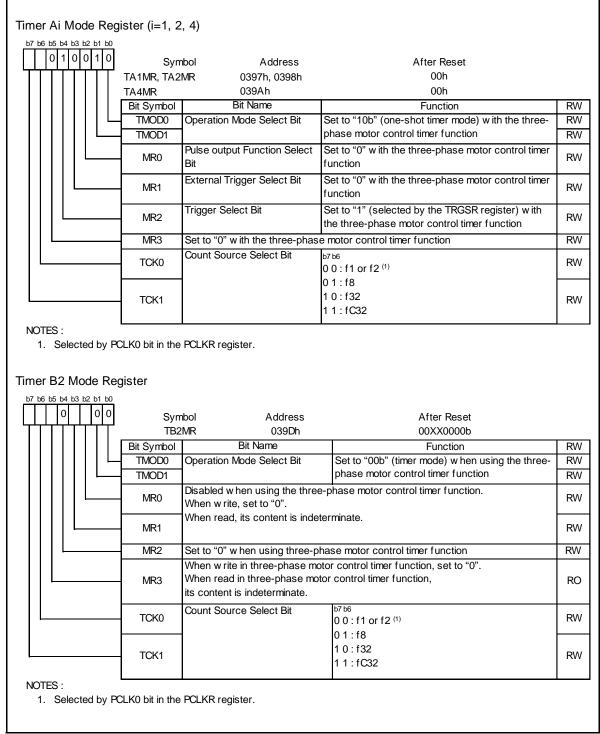


Figure 16.8 TA1MR, TA2MR, TA4MR and TB2MR Registers

Rev.2.41 Jan 10, 2006 Page 173 of 390 **RENESAS** REJ09B0185-0241 The three-phase motor control timer function is enabled by setting the INV02 bit in the INVC0 register to "1". When this function is on, timer B2 is used to control the carrier wave, and timers A4, A1 and A2 are used to control three-phase PWM outputs (U, \overline{U} , V, \overline{V} , W and \overline{W}). The dead time is controlled by a dedicated dead time timer. Figure 16.9 shows the example of Triangular Wave Modulation Operation and Figure 16.10 shows the example of Sawtooth Wave Modulation Operation.

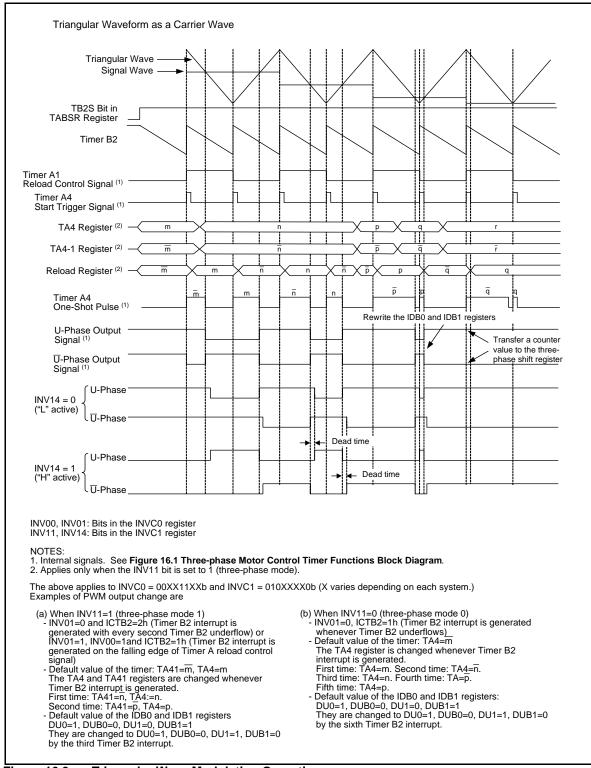


Figure 16.9 Triangular Wave Modulation Operation

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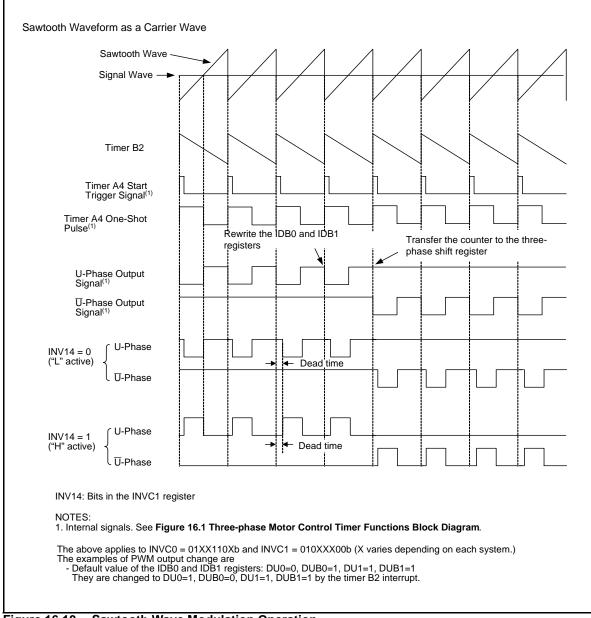


Figure 16.10 Sawtooth Wave Modulation Operation

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17. Serial Interface

Note

The M16C/62P (80-pin version) and M16C/62PT (80-pin version) do not include CLK2, CTS2/RTS2 and SIN pins. Do not use the function which needs these pins.

Serial interface is configured with 5 channels: UART0 to UART2, SI/O3 and SI/O4.

17.1 UARTi (i=0 to 2)

Note

The M16C/62P (80-pin version) and M16C/62PT (80-pin version) do not include CLK2, CTS2/RTS2 pins of UART2.

[Precautions when using UART2]

 Clock synchronous serial I/O mode 	Cannot be used.
• Clock asynchronous serial I/O mode (UART mode)	The CTS2/RTS2 function and the external clock of transfer clock cannot be used. Set the CKDIR bit in the U2MR register to "0" and the CRD bit in the U2C0 register to "1" when using the UART mode.
• Special mode 2	The slave mode cannot be used. Set the CKDIR bit register to "0" when using the Special mode 2.
• Special mode 3	The external clock of transfer clock cannot be used. Set the CKDIR bit register to "0" when using the Special mode 3.
• Special mode 4 (SIM mode)	The external clock of transfer clock cannot be used. Set the CKDIR bit register to "0" when using the Special mode 4 (SIM mode).

UARTi each have an exclusive timer to generate a transfer clock, so they operate independently of each other. Figures 17.1 to 17.3 shows the block diagram of UART0 to UART2. Figure 17.4 shows the UARTi Transmit/ Receive Unit.

UARTi has the following modes:

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode).
- Special mode 1 (I²C mode)
- Special mode 2
- Special mode 3 (Bus collision detection function, IE mode) : UART0, UART1
- Special mode 4 (SIM mode) : UART2

Figures 17.5 to 17.12 show the UARTi-related registers. Refer to tables listing each mode for register setting.

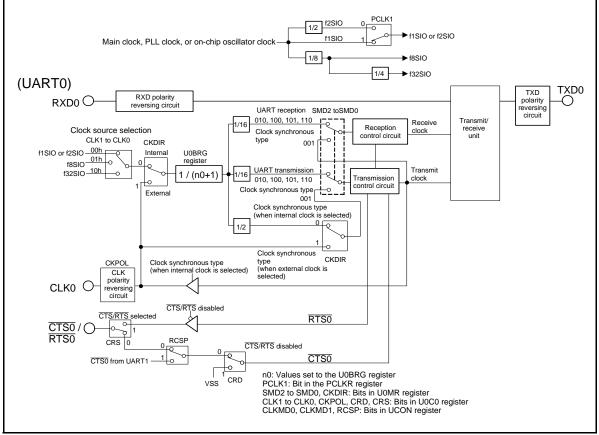


Figure 17.1 UART0 Block Diagram

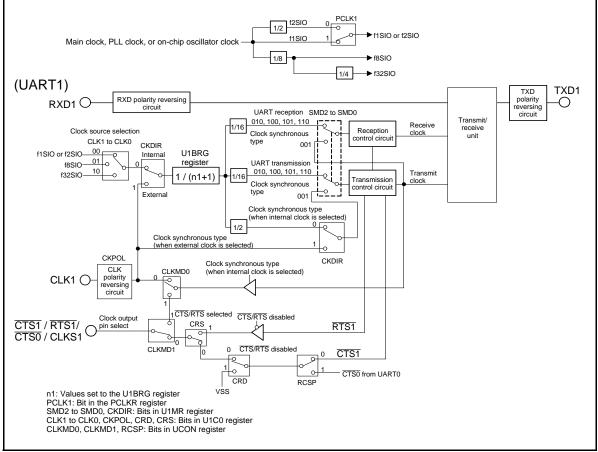


Figure 17.2 UART1 Block Diagram

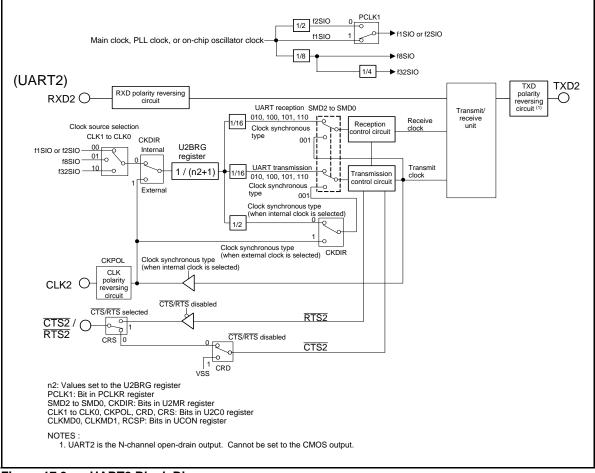


Figure 17.3 UART2 Block Diagram

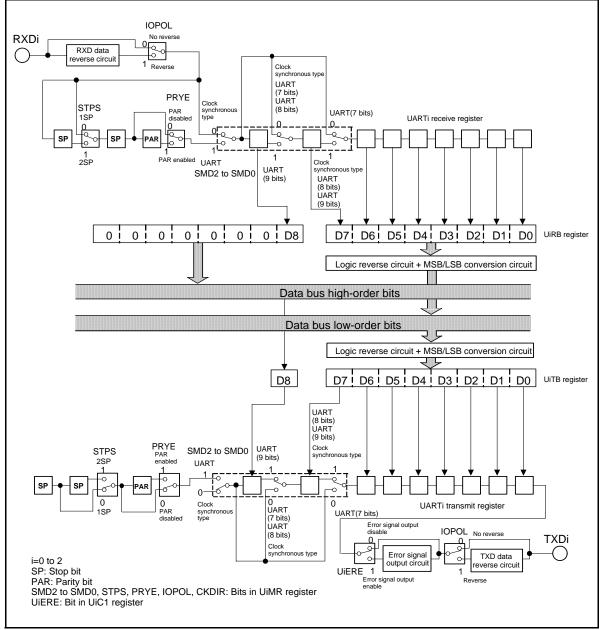
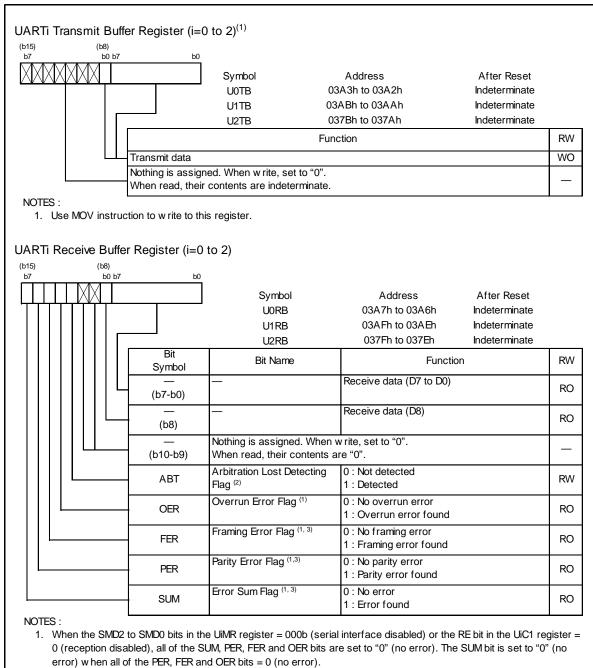


Figure 17.4 UARTi Transmit/Receive Unit

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- Also, the PER and FER bits are set to "0" by reading the low er byte of the UiRB register.
- 2. The ABT bit is set to "0" by writing "0" in a program. (Writing "1" has no effect.)
- These error flags are disabled when the SMD2 to SMD0 bits are set to "001b" (clock synchronous serial VO mode) or to "010b" (PC mode). When read, the contents are indeterminate.



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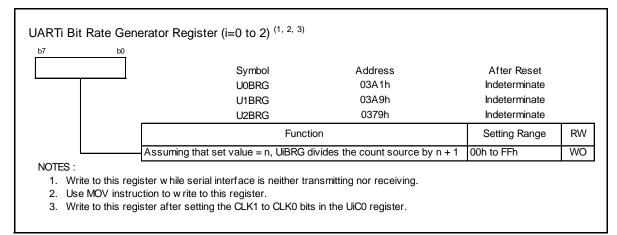


Figure 17.6 UiBRG Register

Г



b7 b6 b	5 b4	o3 b2	o1 b0				
				Symbol	Address	After Reset	
				U0MR to U2	2MR 03A0h, 03A8h, 0378h	00h	
				Bit Symbol	Bit Name	Function	RW
				SMD0	Serial I/O Mode Select Bit ⁽²⁾	^{b2 b1 b0} 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 0 1 0 : PC mode ⁽³⁾	RW
				SMD1		1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long	RW
		L		SMD2		Do not set except above	RW
				CKDIR	Internal/External Clock Select Bit	0 : Internal clock 1 : External clock ⁽¹⁾	RW
	L			STPS	Stop Bit Length Select Bit	0 : 1 stop bit 1 : 2 stop bits	RW
				PRY	Odd/Even Parity Select Bit	Effective w hen PRYE = 1 0 : Odd parity 1 : Even parity	RW
				PRYE	Parity Enable Bit	0 : Parity disabled 1 : Parity enabled	RW
				IOPOL	TXD, RXD I/O Polarity Reverse Bit	0 : No reverse 1 : Reverse	RW

1. Set the corresponding port direction bit for each CLKi pin to "0" (input mode).

2. To receive data, set the corresponding port direction bit for each RXDi pin to "0" (input mode).

3. Set the corresponding port direction bit for SCL and SDA pins to "0" (input mode).

UiMR Register Figure 17.7

o7 b6 l	b5 b4	4 b3 b	2 b1	b0				
					Symbo	Address	After Reset	
	ГТ		ΓT	Т	U0C0 to U2	2C0 03A4h, 03ACh, 03	37Ch 00001000b	
					Bit Symbol	Bit Name	Function	RV
					CLK0	UiBRG Count Source Select Bit ⁽⁶⁾	^{b1 b0} 0 0 : f1SIO or f2SIO is selected ⁽⁵⁾	RV
					CLK1		0 1 : f8SIO is selected 1 0 : f32SIO is selected 1 1 : Do not set to this value	RV
					CRS	CTS/RTS Function Select Bit ⁽⁴⁾	Effective w hen CRD = 0 0 : CTS function is selected ⁽¹⁾ 1 : RTS function is selected	RV
					TXEPT	Transmit Register Empty Flag	 0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed) 	RC
					CRD	CTS/RTS Disable Bit	0 : CTS/RTS function enabled 1 : CTS/RTS function disabled (P6_0, P6_4 and P7_3 can be used as I/O ports)	RV
					NCH	Data Output Select Bit ⁽²⁾	0 : TXDi/SDAi and SCLi pins are CMOS output 1 : TXDi/SDAi and SCLi pins are N-channel open-drain output	RV
					CKPOL	CLK Polarity Select Bit	 0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge 	RV
					UFORM	Transfer Format Select	0 : LSB first 1 : MSB first	RV

- 1. Set the corresponding port direction bit for each $\overline{\text{CLKi}}$ pin to "0" (input mode).
- 2. TXD2/SDA2 and SCL2 are N-channel open-drain output. Cannot be set to the CMOS output. No NCH bit in U2C0 register is assigned. When w rite, set to "0".
- The UFORM bit is enabled when the SMD2 to SMD0 bits in the UiMR register are set to "001b" (clock synchronous serial I/O mode), or "101b" (UART mode, 8-bit transfer data).
 Set this bit to "1" when the SMD2 to SMD0 bits are set to "010b" (I²C mode), and to "0" when the SMD2 to SMD0 bits are set to "100b" (UART mode, 7-bit transfer data) or "110b" (UART mode, 9-bit transfer data).
- CTS1/RTS1 can be used when the CLKMD1 bit in the UCON register = 0 (only CLK1 output) and the RCSP bit in the UCON register = 0 (CTS0/RTS0 not separated).
- 5. Selected by PCLK1 bit in the PCLKR register.
- 6. When changing the CLK1 to CLK0 bits, set the UiBRG register.



	1 1/1/1	ool Address J1C1 03A5h, 03ADh	After Reset 00XX0010b	
	Bit Symbol	Bit Name	Function	RW
	TE	Transmit Enable Bit	0 : Transmission disabled 1 : Transmission enabled	RW
	п	Transmit Buffer Empty Flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RC
	RE	Receive Enable Bit	0 : Reception disabled 1 : Reception enabled	RW
	RI	Receive Complete Flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RC
	 (b5-b4)	Nothing is assigned. When w rite, s When read, these contents are ind		_
	UiLCH	Data Logic Select Bit ⁽¹⁾	0 : No reverse 1 : Reverse	RW
	UiERE	Error Signal Output Enable Bit	0 : Output disabled 1 : Output enabled	RW
		rol Register 1	After Reset	
,	Symbol U2C1	I Address 037Dh	00000010b	RIA
ART2 Trans	Symbol	I Address		
RT2 Trans	Symbol U2C1 Bit Symbol	Address 037Dh Bit Name	00000010b Function 0 : Transmission disabled	RV RV RC
RT2 Trans	Symbol U2C1 Bit Symbol TE	Address 037Dh Bit Name Transmit Enable bit	00000010b Function 0 : Transmission disabled 1 : Transmission enabled 0 : Data present in U2TB register	RW
ART2 Trans	Symbol U2C1 Bit Symbol TE TI	Address 037Dh Bit Name Transmit Enable bit Transmit Buffer Empty Flag	00000010b Function 0 : Transmission disabled 1 : Transmission enabled 0 : Data present in U2TB register 1 : No data present in U2TB register 0 : Reception disabled	RW RC
RT2 Trans	Symbol U2C1 Bit Symbol TE TI RE	Address 037Dh Bit Name Transmit Enable bit Transmit Buffer Empty Flag Receive Enable Bit Receive Complete Flag UART2 Transmit Interrupt Factor Select Bit	00000010b Function 0 : Transmission disabled 1 : Transmission enabled 0 : Data present in U2TB register 1 : No data present in U2TB register 0 : Reception disabled 1 : Reception enabled 0 : No data present in U2RB register 1 : Data present in U2RB register 1 : Data present in U2RB register 0 : Transmit buffer empty (TI = 1) 1 : Transmit is completed (TXEPT = 1)	RW RC RW
RT2 Trans	Symbol U2C1 Bit Symbol TE TI RE RI	Address 037Dh Bit Name Transmit Enable bit Transmit Buffer Empty Flag Receive Enable Bit Receive Complete Flag UART2 Transmit Interrupt Factor	00000010b Function 0 : Transmission disabled 1 : Transmission enabled 0 : Data present in U2TB register 1 : No data present in U2TB register 0 : Reception disabled 1 : Reception enabled 0 : No data present in U2RB register 1 : Data present in U2RB register 0 : Transmit buffer empty (TI = 1)	RW RC RW RC
ART2 Trans	Symbol U2C1 Bit Symbol TE TI RE RI U2IRS	Address 037Dh Bit Name Transmit Enable bit Transmit Buffer Empty Flag Receive Enable Bit Receive Complete Flag UART2 Transmit Interrupt Factor Select Bit UART2 Continuous Receive Mode	00000010b Function 0 : Transmission disabled 1 : Transmission enabled 0 : Data present in U2TB register 1 : No data present in U2TB register 0 : Reception disabled 1 : Reception enabled 0 : No data present in U2RB register 1 : Data present in U2RB register 0 : Transmit buffer empty (TI = 1) 1 : Transmit is completed (TXEPT = 1) 0 : Continuous receive mode disabled	RVA RC RVA RC RVA

Figure 17.9 U0C1 to U2C1 Registers

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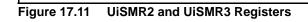
UCON 03B0h X000000b Bit Symbol Bit Name Function UORS UART0 Transmit Interrupt Factor 0 : Transmit buffer empty (TI = 1) 1 Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1) U11RS UART1 Transmit Interrupt Factor 0 : Transmit buffer empty (TI = 1) U11RS UART1 Continuous Receive 0 : Continuous receive mode disabled U0RRM UART1 Continuous Receive 0 : Continuous receive mode enable U11RRM UART1 Continuous Receive 0 : Continuous receive mode enabled U11RRM UART1 CLK/CLKS Select Bit 0 0 : Continuous receive mode enabled U11RRM UART1 CLK/CLKS Select Bit 0 0 : Clock output from CLK1 U11RRM UART1 CLK/CLKS Select Bit 1 0 : CLK output from CLK1 U11RRM UART1 CLK/CLKS Select Bit 1 0 : CLK output from CLK1 U11RRM UART1 CLK/CLKS Select Bit 1 0 : CLK output from CLK1 U11RRM UART1 CLK/CLKS Select Bit 1 0 : CTS/RTS shared pin U11RRM UART1 CLK/CLKS Select Bit 1 0 : CTS/RTS shared pin U111 CLKMD1 1 : CTS/RTS shared pin U111 RCSP CTS/RTS Bit
UORS UART0 Transmit Interrupt Factor 0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1) U1RS UART1 Transmit Interrupt Factor 0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1) U1RS UART1 Transmit Interrupt Factor 0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1) U1RS UART0 Continuous Receive 0 : Continuous receive mode disabled 1 : Continuous receive mode Enable Bit 1 : Continuous receive mode enable U1RRM UART1 Continuous Receive 0 : Continuous receive mode enabled U1RRM UART1 CLK/CLKS Select Bit 0 0 : Continuous receive mode enabled ULRMD0 UART1 CLK/CLKS Select Bit 0 0 : Clock output from CLK1 1 : ClckMD0 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CLK output is only CLK1 1 : CLKMD1 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CLK output from multiple pins function selected RCSP Separate UART0 0 : CTS/RTS shared pin 1 : CTS/RTS Bit 1 : CTS/RTS separated (CTS0 supplied from the P6_4 pin) — Nothing is assigned. When w rite, set to "0". When read, its content is indeterminate. NOTES :
U1IRS Select Bit 1 : Transmission completed (TXEPT = 1) U0RRM UART0 Continuous Receive Mode Enable Bit 0 : Continuous receive mode disabled U1RRM UART1 Continuous Receive Mode Enable Bit 0 : Continuous receive mode disabled U1RRM UART1 Continuous Receive Mode Enable Bit 0 : Continuous receive mode disabled U1RRM UART1 CLK/CLKS Select Bit 0 Effective w hen CLKMD1 = 1 CLKMD0 UART1 CLK/CLKS Select Bit 1 0 : Clock output from CLK1 UART1 CLK/CLKS Select Bit 1 0 : CLK output is only CLK1 1 : Transfer clock output from multiple pins function selected RCSP Separate UART0 CTS/RTS Bit 0 : CTS/RTS shared pin
UORRM Mode Enable Bit 1 : Continuous receive mode enable U1RRM UART1 Continuous Receive 0 : Continuous receive mode disabled U1RRM UART1 CLK/CLKS Select Bit 0 Effective w hen CLKMD1 = 1 CLKMD0 UART1 CLK/CLKS Select Bit 0 Effective w hen CLKMD1 = 1 UART1 CLK/CLKS Select Bit 0 Clck output from CLK1 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CLK output is only CLK1 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CLK output is only CLK1 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CTS/RTS shared pin CLKMD1 Separate UART0 0 : CTS/RTS shared pin RCSP CTS/RTS Bit 1 : CTS/RTS separated (CTS0 supplied from the P6_4 pin) Nothing is assigned. When write, set to "0". When read, its content is indeterminate.
U1RRM Mode Enable Bit 1 : Continuous receive mode enabled UART1 CLK/CLKS Select Bit 0 Effective w hen CLKMD1 = 1 CLKMD0 UART1 CLK/CLKS Select Bit 0 Effective w hen CLKMD1 = 1 UART1 CLK/CLKS Select Bit 0 0 : Clock output from CLK1 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CLK output is only CLK1 CLKMD1 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CLK output is only CLK1 CLKMD1 CLKMD1 0 : CTS/RTS shared pin RCSP Separate UART0 0 : CTS/RTS shared pin TCTS/RTS Bit 1 : CTS/RTS separated (CTS0 supplied from the P6_4 pin) — Nothing is assigned. When w rite, set to "0". When read, its content is indeterminate. NOTES :
CLKMD0 0 : Clock output from CLK1 1 : Clock output from CLKS1 CLKMD1 UART1 CLK/CLKS Select Bit 1 ⁽¹⁾ 0 : CLK output is only CLK1 1 : Transfer clock output from multiple pins function selected RCSP CTS/RTS Bit
CLKMD1 1 : Transfer clock output from multiple pins function selected RCSP Separate UART0 0 : CTS/RTS shared pin TS/RTS Bit 1 : CTS/RTS separated (CTS0 supplied from the P6_4 pin)
RCSP CTS/RTS Bit 1 : CTS/RTS separated (CTS0 supplied from the P6_4 pin) — Nothing is assigned. When w rite, set to "0". (b7) When read, its content is indeterminate. NOTES : Image: CTS/RTS Bit for the P6_4 pin for the P6_4
RCSP RCSP (CTS0 supplied from the P6_4 pin) — Nothing is assigned. When w rite, set to "0". (b7) When read, its content is indeterminate.
(b7) When read, its content is indeterminate.
NOTES :
Bit Symbol Bit Name Function C Mode Select Bit UCM Bit Symbol Bit Name C Mode Select Bit C Mode
Arbitration Lost Detacting Flag 0 : Undate per bit
ABC Arbitration Lost Detecting Flag 0 : Update per bit Control Bit 1 : Update per byte
ABC Control Bit 1 : Update per byte Bus Busy Flag 0 : STOP condition detected
ABC Control Bit 1 : Update per byte BBS Bus Busy Flag 0 : STOP condition detected
ABC Control Bit 1 : Update per byte BBS Bus Busy Flag 0 : STOP condition detected (b3) ⁽⁴⁾ Reserved Bit Set to "0" LSYN ⁽⁴⁾ SCLL sync output enable bit 0 : Disable 1 : Enable 1 : Enable ABSCS Bus Collision Detect Sampling 0 : Rising edge of transfer clock 1 : Underflow signal of Timer Aj ⁽²⁾ 1 : Underflow signal of Timer Aj ⁽²⁾
ABC Control Bit 1 : Update per byte BBS Bus Busy Flag 0 : STOP condition detected (b3) ⁽⁴⁾ Reserved Bit Set to "0" LSYN ⁽⁴⁾ SCLL sync output enable bit 0 : Disable 1 : Enable 1 : Enable ABSCS Bus Collision Detect Sampling Clock Select Bit 0 : Rising edge of transfer clock ACSE Auto Clear Function Select Bit of Transmit Enable Bit 0 : No auto clear function
ABC Control Bit 1 : Update per byte BBS Bus Busy Flag 0 : STOP condition detected (b3) ⁽⁴⁾ Reserved Bit Set to "0" LSYN ⁽⁴⁾ SCLL sync output enable bit 0 : Disable 1 : Enable 1 : Enable ABSCS Bus Collision Detect Sampling 0 : Rising edge of transfer clock 1 : Underflow signal of Timer Aj ⁽²⁾ Auto Clear Function Select Bit 0 : No auto clear function

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$\langle \rangle$			Syı	mbol	Add	ress	After Reset	
	TT	TTT	U0SMR21	to U2SMR2	036Eh, 037	72h, 0376h	X000000b	
			Bit Symbol		t Name		Function	F
			IICM2	PC Mode Selec	t Bit 2	See Table 17.1	3 I ² C Mode Functions	F
			CSC	Clock-Synchro	nous Bit	0 : Disabled 1 : Enabled		F
			SWC	SCL Wait Outp	ut Bit	0 : Disabled 1 : Enabled		F
			ALS	SDA Output St	op Bit	0 : Disabled 1 : Enabled		F
			STAC	UARTi Initializat	tion Bit	0 : Disabled 1 : Enabled		F
			SWC2	SCL Wait Outp	ut Bit 2	0: Transfer cloc 1: "L" output	k	F
			SDHI	SDA Output Dis	sable Bit	0: Enabled 1: Disabled (high	n-impedance)	F
			—	Nothing is assig	gned.	· · · ·		
			(b7)	When w rite, se	t to "0" When	read its content is inc	dotorminato	-
ARTis	-		de register 3	3 (i=0 to 2) ol	Addres 036Dh, 0371h	s	After Reset 000X0X0Xb	
	-		de register 3	3 (i=0 to 2) ol J2SMR3	Addres 036Dh, 0371h ame	s , 0375h	After Reset	R
	-		ode register 3	3 (i=0 to 2) ol J2SMR3 Bit Na Nothing is assig When w rite, se	Addres 036Dh, 0371h ame gned. tt to "0". When	s , 0375h read, its content is inc	After Reset 000X0X0Xb Function Jeterminate.	R
	-		ude register 3 Symb UOSMR3 to 1 Bit Symbol	3 (i=0 to 2) ol J2SMR3 Nothing is assig When w rite, se Clock Phase Se	Addres 036Dh, 0371h ame gned. et to "0". When et Bit [1]	s , 0375h	After Reset 000X0X0Xb Function Jeterminate.	-
	-		de register 3 Symb U0SMR3 to U Bit Symbol (b0)	3 (i=0 to 2) ol J2SMR3 Nothing is assig When w rite, se Clock Phase Se Nothing is assig When w rite, se	Addres 036Dh, 0371h ame gned. et to "0". When et Bit 1 gned. et to "0". When r	s , 0375h read, its content is inc) : Without clock delay ! : With clock delay read, its content is ind	After Reset 000X0X0Xb Function determinate.	-
	-		ode register 3 U0SMR3 to 1 Bit Symbol (b0) CKPH	3 (i=0 to 2) ol J2SMR3 Nothing is assig When w rite, se Clock Phase Se Nothing is assig When w rite, se Clock Output Se	Addres 036Dh, 0371h ame g gned. et to "0". When et Bit 1 gned. et to "0". When r elect Bit 0 1	s , 0375h read, its content is inc) : Without clock delay) : With clock delay	After Reset 000X0X0Xb Function determinate. eterminate.	- R -
	-		de register 3 Symb U0SMR3 to 1 Bit Symbol (b0) CKPH (b2)	3 (i=0 to 2) J2SMR3 Bit Na Nothing is assig When w rite, se Clock Phase Se Nothing is assig When w rite, se Clock Output Se Nothing is assig When w rite, se	Addres 036Dh, 0371h ame gned. et Bit 01 gned. et to "0". When r elect Bit 0 gned. t to "0". When r	s , 0375h read, its content is inc) : Without clock delay : With clock delay read, its content is ind) : CLKi is CMOS output : CLKi is N-channel c read, its content is inc	After Reset 000X0X0Xb Function determinate. eterminate. ut ut upen drain output	- R -
	-		de register 3 UOSMR3 to U Bit Symbol (b0) CKPH (b2) NODC	3 (i=0 to 2) ol J2SMR3 Nothing is assig When w rite, see Clock Phase See Nothing is assig When w rite, see Clock Output Se	Addres 036Dh, 0371h ame gned. et to "0". When et Bit 1 gned. et to "0". When r elect Bit 1 gned. t to "0". When ay 6 0 0	s , 0375h read, its content is inc) : Without clock delay : With clock delay ead, its content is ind) : CLKi is CMOS output : CLKi is N-channel c read, its content is inc 7b6b5 0 0 0 : Without delay 0 1 : 1 to 2 cycle(s) c	After Reset 000X0X0Xb Function determinate. eterminate. ut open drain output determinate.	R R R
	-		de register 3 Symb U0SMR3 to 1 Bit Symbol (b0) CKPH (b2) NODC (b4)	3 (i=0 to 2) ol J2SMR3 Bit Na Nothing is assig When w rite, se Clock Phase Se Nothing is assig When w rite, se Clock Output Se Nothing is assig When w rite, se SDAi Digital Del	Addres 036Dh, 0371h ame gned. et to "0". When et Bit 1 gned. et to "0". When r elect Bit 1 gned. to "0". When ay b 0 0 0 0	s , 0375h read, its content is inc) : Without clock delay : With clock delay ead, its content is ind) : CLKi is CMOS output : CLKi is N-channel c read, its content is inc 7b6b5 0 0 : Without delay	After Reset 000X0X0Xb Function determinate. eterminate. ut open drain output determinate. of UIBRG count source UIBRG count source UIBRG count source UIBRG count source UIBRG count source	- R - R

2. The amount of delay varies with the load on SCLi and SDAi pins. Also, when using an external clock, the amount of delay increases by about 100 ns.



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П	T			mbol to U2SMR4	Addr 036Ch, 037		After Reset 00h	
			Bit Symbol	Bi	t Name		Function	RW
		L	STAREQ	Start Condition C	Generate Bit ⁽¹⁾	0 : Clear 1 : Start		RV
			RSTAREQ	Restart Condition	n Generate Bit ⁽¹⁾	0 : Clear 1 : Start		RW
			STPREQ	Stop Condition G	Generate Bit ⁽¹⁾	0 : Clear 1 : Start		RW
			STSPSEL	SCL,SDA Outpu	t Select Bit		top conditions not output top conditions output	RW
	ļL		ACKD	ACK Data Bit		0 : ACK 1 : NACK		RV
			АСКС	ACK Data Outpu	t Enable Bit	0 : Serial interf 1 : ACK data c	ace data output output	RW
			SCLHI	SCL Output Stop	Enable Bit	0 : Disabled 1 : Enabled		RW
			SWC9	SCL Wait Bit 3		0 : SCL "L" ho 1 : SCL "L" ho		RW

Figure 17.12 UiSMR4 Register

17.1.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. Table 17.1 lists the Clock Synchronous Serial I/O Mode Specifications. Table 17.2 lists the Registers to Be Used and Settings in Clock Synchronous Serial I/O Mode.

Item	Specification
Transfer Data Format	Transfer data length: 8 bits
Transfer Clock	 CKDIR bit in the UiMR(i=0 to 2) register = 0 (internal clock) : fj/ (2(n+1)) fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh CKDIR bit = 1 (external clock) : Input from CLKi pin
Transmission, Reception Control	Selectable from $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function or $\overline{\text{CTS}}/\overline{\text{RTS}}$ function disable
Transmission Start Condition	 Before transmission can start, meet the following requirements ⁽¹⁾ The TE bit in the UiC1 register = 1 (transmission enabled) The TI bit in the UiC1 register = 0 (data present in UiTB register) If CTS function is selected, input on the CTSi pin = L
Reception Start Condition	 Before reception can start, meet the following requirements ⁽¹⁾ The RE bit in the UiC1 register = 1 (reception enabled) The TE bit in the UiC1 register = 1 (transmission enabled) The TI bit in the UiC1 register = 0 (data present in the UiTB register)
Interrupt Request Generation Timing	 For transmission, one of the following conditions can be selected The UiIRS bit ⁽³⁾ = 0 (transmit buffer empty): when transferring data from the UiTB register to the UARTi transmit register (at start of transmission) The UiIRS bit =1 (transfer completed): when the serial interface finished sending data from the UARTi transmit register For reception When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error Detection	Overrun error ⁽²⁾ This error occurs if the serial interface started receiving the next data before reading the UiRB register and received the 7th bit of the next data
Select Function	 CLK polarity selection Transfer data input/output can be chosen to occur synchronously with the rising or the falling edge of the transfer clock LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected Continuous receive mode selection Reception is enabled immediately by reading the UiRB register Switching serial data logic This function reverses the logic value of the transmit/receive data Transfer clock output from multiple pins selection (UART1) The output pin can be selected in a program from two UART1 transfer clock pins that have been set Separate CTS/RTS pins (UART0) CTS0 and RTS0 are input/output from separate pins

 Table 17.1
 Clock Synchronous Serial I/O Mode Specifications

NOTES:

- When an external clock is selected, the conditions must be met while if the CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the external clock is in the high state; if the CKPOL bit in the UiC0 register = 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the low state.
- 2. If an overrun error occurs, the receive data of UiRB register will be indeterminate. The IR bit in the SiRIC register does not change.
- 3. The U0IRS and U1IRS bits respectively are the bits 0 and 1 in the UCON register; the U2IRS bit is the bit 4 in the U2C1 register.

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Register	Bit	Function				
UiTB ⁽³⁾	0 to 7	Set transmission data				
UiRB ⁽³⁾	0 to 7	Reception data can be read				
	OER	Overrun error flag				
UiBRG	0 to 7	Set a bit rate				
UiMR ⁽³⁾	SMD2 to SMD0	Set to "001b"				
	CKDIR	Select the internal clock or external clock				
	IOPOL	Set to "0"				
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register				
	CRS	Select CTS or RTS to use				
	TXEPT	Transmit register empty flag				
	CRD	Enable or disable the CTS or RTS function				
	NCH	Select TXDi pin output mode ⁽²⁾				
	CKPOL	Select the transfer clock polarity				
	UFORM	Select the LSB first or MSB first				
UiC1	TE	Set this bit to "1" to enable transmission/reception				
	TI	Transmit buffer empty flag				
	RE	Set this bit to "1" to enable reception				
	RI	Reception complete flag				
	U2IRS (1)	Select the source of UART2 transmit interrupt				
	U2RRM ⁽¹⁾	Set this bit to "1" to use continuous receive mode				
	UiLCH	Set this bit to "1" to use inverted data logic				
	UiERE	Set to "0"				
UiSMR	0 to 7	Set to "0"				
UiSMR2	0 to 7	Set to "0"				
UiSMR3	0 to 2	Set to "0"				
	NODC	Select clock output mode				
	4 to 7	Set to "0"				
UiSMR4	0 to 7	Set to "0"				
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt				
	U0RRM, U1RRM	Set this bit to "1" to use continuous receive mode				
	CLKMD0	Select the transfer clock output pin when CLKMD1 = 1				
	CLKMD1	Set this bit to "1" to output UART1 transfer clock from two pins				
	RCSP	Set this bit to "1" to accept as input the $\overline{\text{CTS0}}$ signal of the UART0 from the P6_4 pin				
	7	Set to "0"				

Table 17.2 Registers to Be Used and Settings in Clock Synchronous Serial I/O Mode

NOTES:

- 1. Set the bit 4 and bit 5 in the U0C1 and U1C1 register to "0". The U0IRS, U1IRS, U0RRM and U1RRM bits in the UCON register.
- 2. TXD2 pin is N channel open-drain output. Set the NCH bit in the U2C0 register to "0".
- 3. Not all register bits are described above. Set those bits to "0" when writing to the registers in clock synchronous serial I/O mode.

i=0 to 2

Table 17.3 lists the functions of the input/output pins during clock synchronous serial I/O mode. Table 17.3 shows pin functions for the case where the multiple transfer clock output pin select function is deselected. Table 17.4 lists the P6_4 Pin Functions during clock synchronous serial I/O mode. Note that for a period from when the UARTi operating mode is selected to when transfer starts, the TXDi pin outputs an "H" (If the N-channel open-drain output is selected, this pin is in a high-impedance state).

Pin Name	Function	Method of Selection
TXDi (i = 0 to 2) (P6_3, P6_7, P7_0)	Serial Data Output	(Outputs dummy data when performing reception only)
RXDi (P6_2, P6_6, P7_1)	Serial Data Input	PD6_2 bit and PD6_6 bit in the PD6 register = 0, PD7_1 bit in the PD7 register = 0 (Can be used as an input port when performing transmission only)
CLKi (P6_1, P6_5,	Transfer Clock Output	CKDIR bit in the UiMR register = 0
P7_2)	Transfer Clock Input	CKDIR bit = 1 PD6_1 bit and PD6_5 bit in the PD6 register = 0, PD7_2 bit in the PD7 register = 0
CTSi/RTSi (P6_0, P6_4, P7_3)	CTS Input	CRD bit in the UiC0 register = 0 CRS bit in the UiC0 register = 0 PD6_0 and PD6_4 bit in the PD6 register = 0, PD7_3 bit in the PD7 register = 0
	RTS Output	CRD bit = 0 CRS bit = 1
	I/O Port	CRD bit = 1

 Table 17.3
 Pin Functions (when not select multiple transfer clock output pin function)

Table 17.4 P6_4 Pin Functions

	Bit Set Value					
Pin Function	U1C0 Register		UCON Register			PD6 Register
	CRD	CRS	RCSP	CLKMD1	CLKMD0	PD6_4
P6_4	1	-	0	0	-	Input: 0, Output: 1
CTS1	0	0	0	0	-	0
RTS1	0	1	0	0	-	_
CTSO (1)	0	0	1	0	_	0
CLKS1	-	_	-	1 (2)	1	-
						– : "0" or "1"

NOTES:

- In addition to this, set the CRD bit in the U0C0 register to "0" (CTS0/RTS0 enabled) and the CRS bit in the U0C0 register to "1" (RTS0 selected).
- 2. When the CLKMD1 bit = 1 and the CLKMD0 bit = 0, the following logic levels are output:
 •High if the CLKPOL bit in the U1C0 register = 0
 - •Low if the CLKPOL bit = 1

(T) Example of	Transmit Timing (when internal clock is selected)
Transfer clock	
TE bit in UiC1 register	"1" Data is set in the UITB register
TI bit in UiC1 register	"0" Data is transferred from the UiTB register to the UARTi transmit register
CTSi	"H" "L" TCLK "L" TCLK Pulse stops because an "H" signal is Applied to CTSi TCLK TC
CLKi	
TXDi	
TXEPT bit in UiC0 register	
IR bit in SiTIC register	
 CKDIR bit in U CRD bit in UiC CKPOL bit in U UiIRS bit = 0 (U0IRS bit is U1IRS bit is 	Set to "0" by an interrupt request acknowledgement or by program TC = TCLK = 2(n + 1) / fj fj: frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO) taken in at the rising edge of the transfer clock) (an interrupt request occurs when the transmit buffer becomes empty): s bit 0 in UCON register s bit 4 in U2C1 register
(2) Example of RE bit in UiC1 register	Receive Timing (when external clock is selected)
TE bit in UiC1 register	"1" "0"—— Dummy data is set in the to UiTB register
TI bit in UiC1 register	"0" Data is transferred from the UiTB register to the UARTi transmit register
RTSi	"H" "L" An "L" signal is applied when the UiRB register is read
CLKi	
RXDi	D00D102XD3XD4XD5XD6XD7 XD0XD1XD2XD3XD4XD5XD6X D7 XD0XD1XD2XD3XD4XD5XD6X
RI bit in UiC1 register	"1" receive register to the UiRB register
IR bit in SiRIC register	"1" "0"
OER flag in UiRB register	Set to "0" by an interrupt request acknowledgement or by program "1" "0"
i=0 to 2	
as follows: · CKDIR bit in · CRD bit in Ui	g diagram applies to the case where the register bits are set UiMR register = 1 (external clock) C0 register = 0 (CTS/RTS enabled), CRS bit = 1 (RTS selected) UiC0 register = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transfer clock) Make sure the following conditions are met when input in the CLKi pin before receiving data is high: • TE bit in UiC0 register = 1 (transmit enabled) • Re bit in UiC0 register = 1 (receive enabled) • Write dummy data to the UiTB register

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17.1.1.1 Counter Measure for Communication Error Occurs

If a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below.

• Resetting the UiRB register (i=0 to 2)

- (1) Set the RE bit in the UiC1 register to "0" (reception disabled)
- (2) Set the SMD2 to SMD0 bits in the UiMR register to "000b" (Serial interface disabled)
- (3) Set the SMD2 to SMD0 bits in the UiMR register to "001b" (Clock synchronous serial I/O mode)
- (4) Set the RE bit in the UiC1 register to "1" (reception enabled)

• Resetting the UiTB register (i=0 to 2)

- (1) Set the SMD2 to SMD0 bits in the UiMR register "000b" (Serial interface disabled)
- (2) Set the SMD2 to SMD0 bits in the UiMR register "001b" (Clock synchronous serial I/O mode)
- (3) "1" is written to RE bit in the UiC1 register (transmission enabled), regardless of the TE bit in the UiCi register

17.1.1.2 CLK Polarity Select Function

Use the CKPOL bit in the UiC0 register (i = 0 to 2) to select the transfer clock polarity. Figure 17.14 shows the Transfer Clock Polarity.

CLKi	
 TXDi	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
RXDi	$ \begin{array}{c c} & \downarrow \\ \hline \\$
	he CKPOL bit = 1 (transmit data output at the rising edge and the receive ten in at the falling edge of the transfer clock)
CLKi	
TXDi	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
RXDi	$10 \times D1 \times D2 \times D3 \times D4 \times D5 \times D6 \times D7$



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17.1.1.3 LSB First/MSB First Select Function

Use the UFORM bit in the UiC0 register (i = 0 to 2) to select the transfer format. Figure 17.15 shows the Transfer Format.

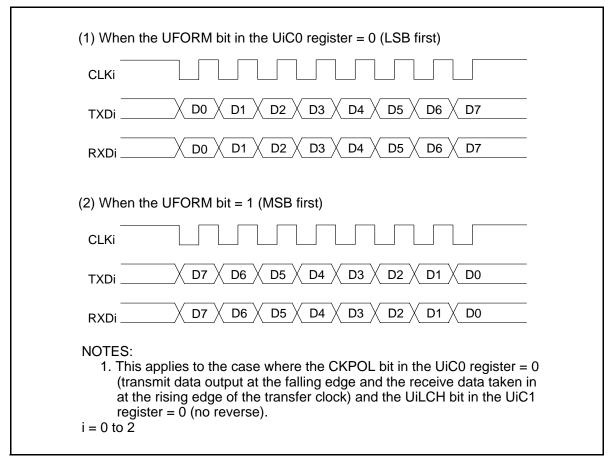


Figure 17.15 Transfer Format

17.1.1.4 Continuous Receive Mode

In continuous receive mode, receive operation becomes enable when the receive buffer register is read. It is not necessary to write dummy data into the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the UiRRM bit (i = 0 to 2) = 1 (continuous receive mode), the TI bit in the UiC1 register is set to "0" (data present in the UiTB register) by reading the UiRB register. In this case, i.e., UiRRM bit = 1, do not write dummy data to the UiTB register in a program. The U0RRM and U1RRM bits are the bit 2 and bit 3 in the UCON register, respectively, and the U2RRM bit is the bit 5 in the U2C1 register.

17.1.1.5 Serial Data Logic Switching Function

When the UiLCH bit in the UiC1 register (i = 0 to 2) = 1 (reverse), the data written to the UiTB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the UiRB register. Figure 17.16 shows Serial Data Logic Switching.

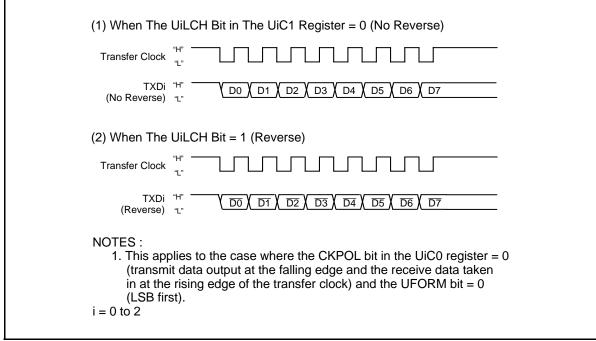


Figure 17.16 Serial Data Logic Switching

17.1.1.6 Transfer Clock Output From Multiple Pins (UART1)

Use the CLKMD1 to CLKMD0 bits in the UCON register to select one of the two transfer clock output pins (see Figure 17.17). This function can be used when the selected transfer clock for UART1 is an internal clock.

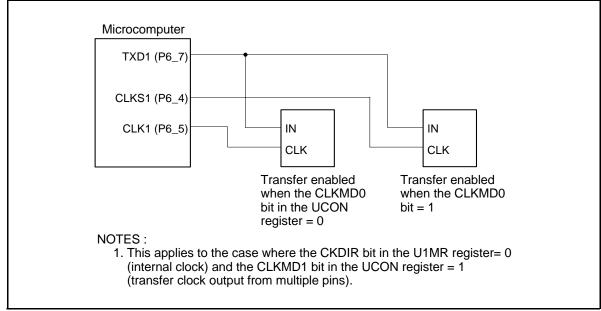


Figure 17.17 Transfer Clock Output from Multiple Pins

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17.1.1.7 CTS/RTS Function

When the $\overline{\text{CTS}}$ function is used transmit and receive operation start when "L" is applied to the $\overline{\text{CTSi}/\text{RTSi}}$ (i=0 to 2) pin. Transmit and receive operation begins when the $\overline{\text{CTSi}/\text{RTSi}}$ pin is held "L". If the "L" signal is switched to "H" during a transmit or receive operation, the operation stops before the next data.

When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTSi}/\text{RTSi}}$ pin outputs on "L" signal when the microcomputer is ready to receive. The output level becomes "H" on the first falling edge of the CLKi pin.

• CRD bit in UiC0 register = 1 (disable $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART0)

CTSi/RTSi pin is programmable I/O function

- CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function is selected)
- CTSi/RTSi pin is CTS function
- CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function is selected) $\overline{\text{CTSi}/\text{RTSi}}$ pin is $\overline{\text{RTS}}$ function

17.1.1.8 CTS/RTS Separate Function (UART0)

This function separates $\overline{\text{CTS0}/\text{RTS0}}$, outputs $\overline{\text{RTS0}}$ from the P6_0 pin, and accepts as input the $\overline{\text{CTS0}}$ from the P6_4 pin. To use this function, set the register bits as shown below.

- CRD bit in U0C0 register = 0 (enable $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART0)
- CRS bit in U0C0 register = 1 (output $\overline{\text{RTS}}$ of UART0)
- CRD bit in U1C0 register = 0 (enable $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART1)
- CRS bit in U1C0 register = 0 (input $\overline{\text{CTS}}$ of UART1)
- RCSP bit in UCON register = 1 (inputs $\overline{\text{CTS0}}$ from the P6_4 pin)
- CLKMD1 bit in UCON register = 0 (CLKS1 not used)

Note that when using the CTS/RTS separate function, CTS/RTS of UART1 separate function cannot be used.

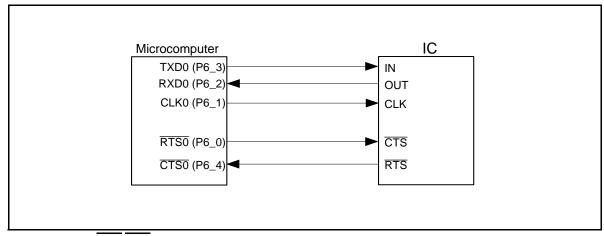


Figure 17.18 CTS/RTS Separate Function

17.1.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows transmitting and receiving data after setting the desired bit rate and transfer data format. Table 17.5 lists the UART Mode Specifications.

Item	Specification
Transfer Data Format	 Character bit (transfer data): Selectable from 7, 8 or 9 bits Start bit: 1 bit Parity bit: Selectable from odd, even, or none
	Stop bit: Selectable from 1 or 2 bits
Transfer Clock	 CKDIR bit in the UiMR(i=0 to 2) register = 0 (internal clock) : fj/ (16(n+1)) fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh CKDIR bit = 1 (external clock) : fEXT/(16(n+1)) fEXT: Input from CLKi pin n :Setting value of UiBRG register 00h to FFh
Transmission, Reception Control	Selectable from CTS function, RTS function or CTS/RTS function disable
Transmission Start Condition	 Before transmission can start, meet the following requirements The TE bit in the UiC1 register= 1 (transmission enabled) The TI bit in the UiC1 register = 0 (data present in UiTB register) If CTS function is selected, input on the CTSi pin = L
Reception Start Condition	Before reception can start, meet the following requirements • The RE bit in the UiC1 register = 1 (reception enabled) • Start bit detection
Interrupt Request Generation Timing	 For transmission, one of the following conditions can be selected The UiIRS bit ⁽²⁾ = 0 (transmit buffer empty): when transferring data from the UiTB register to the UARTi transmit register (at start of transmission) The UiIRS bit =1 (transfer completed): when the serial interface finished sending data from the UARTi transmit register For reception When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error Detection	 Overrun error ⁽¹⁾ This error occurs if the serial interface started receiving the next data before reading the UiRB register and received the bit one before the last stop bit of the next data Framing error ⁽³⁾ This error occurs when the number of stop bits set is not detected Parity error ⁽³⁾ This error occurs when if parity is enabled, the number of "1" in parity and character bits does not match the number of "1" set Error sum flag This flag is set to "1" when any of the overrun, framing or parity errors occur
Select Function	 LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected Serial data logic switch This function reverses the logic of the transmit/receive data. The start and stop bits are not reversed. TXD, RXD I/O polarity switch This function reverses the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data is reversed. Separate CTS/RTS pins (UART0) CTS0 and RTS0 are input/output from separate pins

Table 17.5 UART Mode Specifications

NOTES:

- 1. If an overrun error occurs, the receive data of UiRB register will be indeterminate. The IR bit in the SiRIC register does not change.
- 2. The U0IRS and U1IRS bits are bits 0 and 1 in the UCON register. The U2IRS bit is bit 4 in the U2C1 register.
- 3. The timing at which the framing error flag and the parity error flag are set is detected when data is transferred from the UARTi receive register to the UiRB register.

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Register	Bit	Function					
UiTB	0 to 8	Set transmission data ⁽¹⁾					
UiRB	0 to 8	Reception data can be read ⁽¹⁾					
	OER,FER,PER,SUM	Error flag					
UiBRG	0 to 7	Set a bit rate					
UiMR	SMD2 to SMD0	Set these bits to "100b" when transfer data is 7 bits long					
		Set these bits to "101b" when transfer data is 8 bits long					
		Set these bits to "110b" when transfer data is 9 bits long					
	CKDIR	Select the internal clock or external clock					
	STPS	Select the stop bit					
	PRY, PRYE	Select whether parity is included and whether odd or even					
	IOPOL	Select the TXD/RXD input/output polarity					
UiC0	CLK0, CLK1	Select the count source for the UiBRG register					
	CRS	Select CTS or RTS to use					
	TXEPT	Transmit register empty flag					
	CRD	Enable or disable the CTS or RTS function					
	NCH	Select TXDi pin output mode ⁽³⁾					
	CKPOL	Set to "0"					
	UFORM	LSB first or MSB first can be selected when transfer data is 8 bits long. Set this					
		bit to "0" when transfer data is 7 or 9 bits long.					
UiC1	TE	Set this bit to "1" to enable transmission					
	TI	Transmit buffer empty flag					
	RE	Set this bit to "1" to enable reception					
	RI	Reception complete flag					
	U2IRS ⁽²⁾	Select the source of UART2 transmit interrupt					
	U2RRM ⁽²⁾	Set to "0"					
	UiLCH	Set this bit to "1" to use inverted data logic					
	UiERE	Set to "0"					
UiSMR	0 to 7	Set to "0"					
UiSMR2	0 to 7	Set to "0"					
UiSMR3	0 to 7	Set to "0"					
UiSMR4	0 to 7	Set to "0"					
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt					
	U0RRM, U1RRM	Set to "0"					
	CLKMD0	Invalid because CLKMD1 = 0					
	CLKMD1	Set to "0"					
	RCSP	Set this bit to "1" to accept as input $\overline{\text{CTSO}}$ signal of UARTO from the P6_4 pin					
	7	Set to "0"					

Table 17.6 Registers to Be Used and Settings in UART Mode

NOTES:

1. The bits used for transmit/receive data are as follows: Bit 0 to bit 6 when transfer data is 7 bits long; bit 0 to bit 7 when transfer data is 8 bits long; bit 0 to bit 8 when transfer data is 9 bits long.

2. Set the bit 4 to bit 5 in the U0C1 and U1C1 registers to "0". The U0IRS, U1IRS, U0RRM and U1RRM bits are included in the UCON register.

3. TXD2 pin is N channel open-drain output. Set the NCH bit in the U2C0 register to "0".

i=0 to 2

-: "0" or "1"

Table 17.7 lists the functions of the input/output pins during UART mode. Table 17.8 lists the P6_4 Pin Functions. Note that for a period from when the UARTi operating mode is selected to when transfer starts, the TXDi pin outputs an "H" (If the N-channel open-drain output is selected, this pin is in a high-impedance state).

Pin Name	Function	Method of Selection
TXDi (i = 0 to 2) (P6_3, P6_7, P7_0)	Serial Data Output	("H" outputs when performing reception only)
RXDi (P6_2, P6_6, P7_1)	Serial Data Input	PD6_2 bit and PD6_6 bit in the PD6 register = 0, PD7_1 bit in the PD7 register = 0 (Can be used as an input port when performing transmission only)
CLKi (P6_1, P6_5, P7_2)	Input/Output Port Transfer Clock Input	CKDIR bit in the UiMR register = 0 CKDIR bit = 1 PD6_1 bit and PD6_5 bit in the PD6 register = 0, PD7_2 bit in the PD7 register = 0
CTSi/RTSi (P6_0, P6_4, P7_3)	CTS Input	CRD bit in the UiC0 register = 0 CRS bit in the UiC0 register = 0 PD6_0 bit and PD6_4 bit in the PD6 register = 0, PD7_3 bit in the PD7 register = 0
	RTS Output Input/Output Port	CRD bit = 0 CRS bit = 1 CRD bit = 1

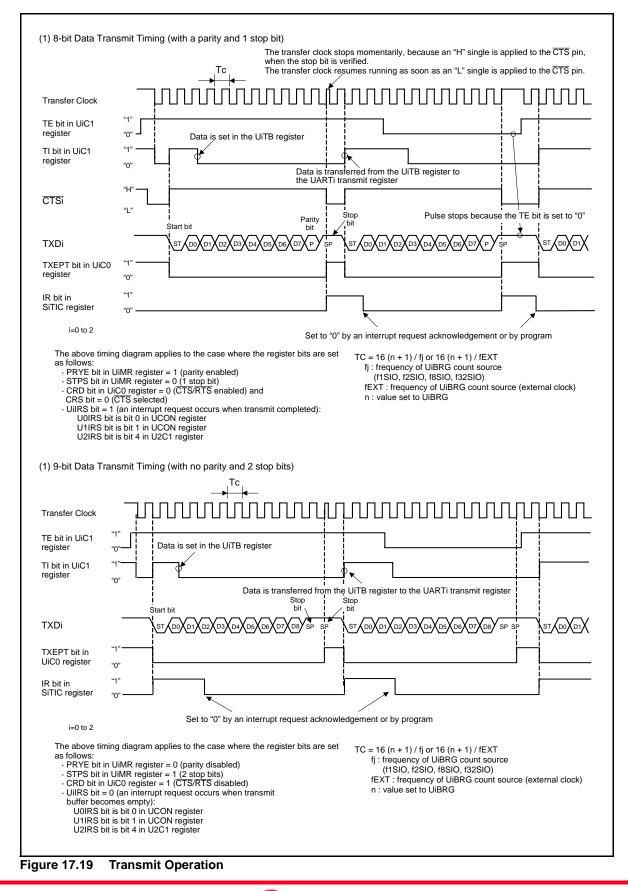
Table 17.7 I/O Pin Functions

Table 17.8 P6_4 Pin Functions

	Bit Set Value					
Pin Function	U1C0 Register		UCON Register		PD6 Register	
	CRD	CRS	RCSP	CLKMD1	PD6_4	
P6_4	1	-	0	0	Input: 0, Output: 1	
CTS1	0	0	0	0	0	
RTS1	0	1	0	0	_	
CTS0 (1)	0	0	1	0	0	

NOTES:

1. In addition to this, set the CRD bit in the U0C0 register to "0" (CTS0/RTS0 enabled) and the CRS bit in the U0C0 register to "1" (RTS0 selected).



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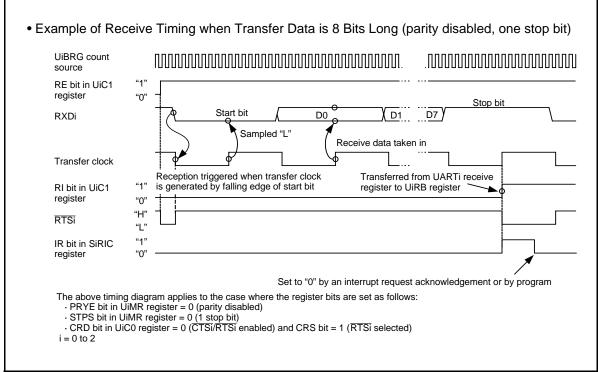


Figure 17.20 Receive Operation

17.1.2.1 Bit Rate

In UART mode, the frequency set by the UiBRG register (i=0 to 2) divided by 16 become the bit rates. Table 17.9 lists Example of Bit Rates and Settings.

Bit Rate	Count Source Peripheral Fun		n Clock : 16MHz	Peripheral Function Clock : 24MHz	
(bps)	of UiBRG	Set Value of UiBRG : n	Bit Rate (bps)	Set value of UiBRG : n	Bit Rate (bps)
1200	f8	103 (67h)	1202	155 (9Bh)	1202
2400	f8	51 (33h)	2404	77 (4Dh)	2404
4800	f8	25 (19h)	4808	38 (26h)	4808
9600	f1	103 (67h)	9615	155 (9Bh)	9615
14400	f1	68 (44h)	14493	103 (67h)	14423
19200	f1	51 (33h)	19231	77 (4Dh)	19231
28800	f1	34 (22h)	28571	51 (33h)	28846
31250	f1	31 (1Fh)	31250	47 (2Fh)	31250
38400	f1	25 (19h)	38462	38 (26h)	38462
51200	f1	19 (13h)	50000	28 (1Ch)	51724

Table 17.9 Example of Bit Rates and Settings

17.1.2.2 Counter Measure for Communication Error Occurs

If a communication error occurs while transmitting or receiving in UART mode, follow the procedures below.

- Resetting the UiRB register (i=0 to 2)
- (1) Set the RE bit in the UiC1 register to "0" (reception disabled)
- (2) Set the RE bit in the UiC1 register to "1" (reception enabled)
- Resetting the UiTB register (i=0 to 2)
- (1) Set the SMD2 to SMD0 bits in the UiMR register "000b" (Serial interface disabled)
- (2) Set the SMD2 to SMD0 bits in the UiMR register "001b", "101b", "110b".
- (3) "1" is written to RE bit in the UiC1 register (transmission enabled), regardless of the TE bit in the UiCi register

17.1.2.3 LSB First/MSB First Select Function

As shown in Figure 17.21, use the UFORM bit in the UiC0 register to select the transfer format. This function is valid when transfer data is 8 bits long.

(1) When the UFORM Bit in the UiC0 Register = 0 (LSB First)	
СЬК	
TXDi ST D0 X D1 X D2 X D3 X D4 X D5 X D6 X D7 X P Y SP	
RXDi ST DO X D1 X D2 X D3 X D4 X D5 X D6 X D7 X P X SP	
(2) When the UFORM Bit = 1 (MSB First)	
TXDi ST (D7 X D6 X D5 X D4 X D3 X D2 X D1 X D0 X P) SP	
RXDi ST D7 D6 D5 D4 D3 D2 D1 D0 P SP	
NOTES : 1. This applies to the case where the CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the UiLCH bit in the UiC1 register = 0 (no reverse), the STPS bit in the UiMR register = 0 (1 stop bit) and the PRYE bit in the UiMR register = 1 (parity enabled).	ST : Start bit P : Parity bit SP : Stop bit i = 0 to 2

Figure 17.21 Transfer Format

17.1.2.4 Serial Data Logic Switching Function

The data written to the UiTB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the UiRB register. Figure 17.22 shows Serial Data Logic Switching.

(1) When the UiLCH bit in the UiC1 Register = 0 (No Reverse)
Transfer Clock
TXDi "H" ST (D0) D1) D2) D3) D4) D5) D6) D7) P SP (No Reverse) "L"
(2) When the UiLCH Bit = 1 (Reverse)
Transfer Clock " ^{H"}
TXDi "H" ST D0 D1 D2 D3 D4 D5 D6 D7 P SP (Reverse) "L" "L" ST ST<
NOTES : 1. This applies to the case where the CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge of the transfer clock), the UFORM bit in the UiC0 register = 0 (LSB first), the STPS bit in the UiMR register = 0 (1 stop bit) and the PRYE bit in the UiMR register = 1 (parity enabled). ST : Start bit P : Parity bit SP : Stop bit i = 0 to 2

Figure 17.22 Serial Data Logic Switching

17.1.2.5 TXD and RXD I/O Polarity Inverse Function

This function inverses the polarities of the TXDi pin output and RXDi pin input. The logic levels of all input/ output data (including the start, stop and parity bits) are inversed. Figure 17.23 shows the TXD and RXD I/O Polarity Inverse.

(1) When the IOPOL Bit in the UiMR Register = 0 (No Reverse)
TXDi "H" ST / D0 / D1 / D2 / D3 / D4 / D5 / D6 / D7 / P / SP
RXDi "H" ST (D0) D1) D2) D3) D4) D5) D6) D7) P) SP
(2) When the IOPOL Bit = 1 (Reverse)
Transfer Clock "H"
TXDi "H" ST (D0) D1) D2 (D3) D4 (D5) D6 (D7) P SP
RXDi "H" ST (D0) D1 (D2) D3 (D4) (D5) (D6) (D7) P SP (Reverse) "L"
NOTES : 1. This applies to the case where the UFORM bit in the UiC0 register = 0 (LSB first), the STPS bit in the UiMR register = 0 (1 stop bit) and the PRYE bit in the UiMR register = 1 (parity enabled). ST : Start bit P : Parity bit SP : Stop bit i = 0 to 2

Figure 17.23 TXD and RXD I/O Polarity Inverse

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17.1.2.6 CTS/RTS Function

When the $\overline{\text{CTS}}$ function is used transmit operation start when "L" is applied to the $\overline{\text{CTSi}/\text{RTSi}}$ (i=0 to 2) pin. Transmit operation begins when the $\overline{\text{CTSi}/\text{RTSi}}$ pin is held "L". If the "L" signal is switched to "H" during a transmit operation, the operation stops before the next data.

When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTSi}/\text{RTSi}}$ pin outputs on "L" signal when the microcomputer is ready to receive. The output level becomes "H" on the first falling edge of the CLKi pin.

• CRD bit in UiC0 register = 1 (disable $\overline{\text{CTS}}/\overline{\text{RTS}}$ function of UART0)

CTSi/RTSi pin is programmable I/O function

- CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function is selected)
- CTSi/RTSi pin is CTS function
- CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function is selected) $\overline{\text{CTSi}/\text{RTSi}}$ pin is $\overline{\text{RTS}}$ function

17.1.2.7 CTS/RTS Separate Function (UART0)

This function separates $\overline{\text{CTS0}/\text{RTS0}}$, outputs $\overline{\text{RTS0}}$ from the P6_0 pin, and accepts as input the $\overline{\text{CTS0}}$ from the P6_4 pin. To use this function, set the register bits as shown below.

- CRD bit in U0C0 register = 0 (enable $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART0)
- CRS bit in U0C0 register = 1 (output $\overline{\text{RTS}}$ of UART0)
- CRD bit in U1C0 register = 0 (enable $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART1)
- CRS bit in U1C0 register = 0 (input $\overline{\text{CTS}}$ of UART1)
- RCSP bit in UCON register = 1 (inputs $\overline{\text{CTS0}}$ from the P6_4 pin)
- CLKMD1 bit in UCON register = 0 (CLKS1 not used)

Note that when using the CTS/RTS separate function, CTS/RTS of UART1 separate function cannot be used.

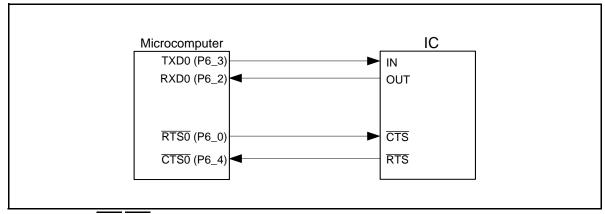


Figure 17.24 CTS/RTS Separate Function

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17.1.3 Special Mode 1 (I²C mode)

I²C mode is provided for use as a simplified I²C interface compatible mode. Table 17.10 lists the specifications of the I²C mode. Table 17.11 to 17.12 lists the registers used in the I²C mode and the register values set. Table 13.13 lists the I²C Mode Functions. Figure 17.25 shows the block diagram for I²C mode. Figure 17.26 shows Transfer to UiRB Register and Interrupt Timing.

As shown in Table 17.13, the microcomputer is placed in I²C mode by setting the SMD2 to SMD0 bits to "010b" and the IICM bit to "1". Because SDAi transmit output has a delay circuit attached, SDAi output does not change state until SCLi goes low and remains stably low.

Item	Specification	
Transfer Data Format	Transfer data length: 8 bits	
Transfer Clock	 During master CKDIR bit in the UiMR (i=0 to 2) register = 0 (internal clock) : fj/ (2(n+1)) fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh During slave CKDIR bit = 1 (external clock) : Input from SCLi pin 	
Transmission Start	Before transmission can start, met the following requirements ⁽¹⁾	
Condition	 The TE bit in the UiC1 register= 1 (transmission enabled) The TI bit in the UiC1 register = 0 (data present in UiTB register) 	
Reception Start Condition	 Before reception can start, met the following requirements ⁽¹⁾ The RE bit in UiC1 register= 1 (reception enabled) The TE bit in UiC1 register= 1 (transmission enabled) The TI bit in UiC1 register= 0 (data present in the UiTB register) 	
Interrupt Request Generation Timing	When start or stop condition is detected, acknowledge undetected, and acknowledge detected	
Error Detection	Overrun error ⁽²⁾ This error occurs if the serial interface started receiving the next data before reading the UiRB register and received the 8th bit of the next data	
Select Function	 Arbitration lost Timing at which the ABT bit in the UiRB register is updated can be selected SDAi digital delay No digital delay or a delay of 2 to 8 UiBRG count source clock cycles selectable Clock phase setting With or without clock delay selectable 	

Table 17.10 I²C Mode Specifications

NOTES:

1. When an external clock is selected, the conditions must be met while the external clock is in the high state.

2. If an overrun error occurs, the value of UiRB register will be indeterminate. The IR bit in the SiRIC register does not change.

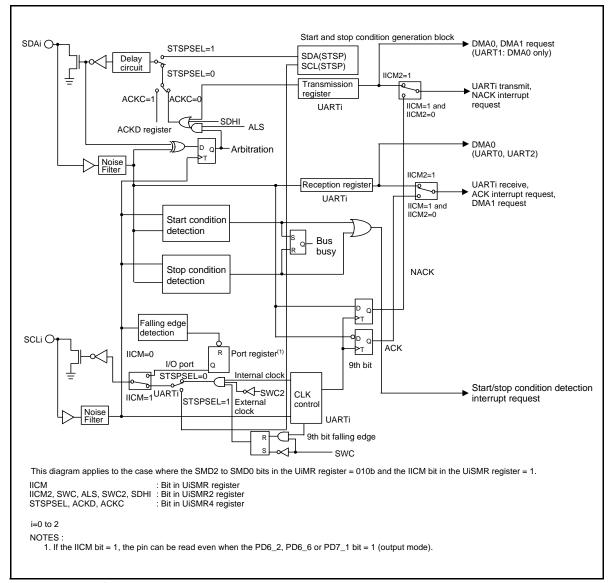


Figure 17.25 I²C Mode Block Diagram

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Register	Bit	Function			
•		Master	Slave		
UiTB (3)	0 to 7	Set transmission data	Set transmission data		
UiRB ⁽³⁾	0 to 7	Reception data can be read	Reception data can be read		
	8	ACK or NACK is set in this bit	ACK or NACK is set in this bit		
	ABT	Arbitration lost detection flag	Invalid		
	OER	Overrun error flag	Overrun error flag		
UiBRG	0 to 7	Set a bit rate	Invalid		
UIMR ⁽³⁾	SMD2 to SMD0	Set to "010b"	Set to "010b"		
•	CKDIR	Set to "0"	Set to "1"		
	IOPOL	Set to "0"	Set to "0"		
UiC0	CLK1, CLK0	Select the count source for the UiBRG register	Invalid		
	CRS	Invalid because CRD = 1	Invalid because CRD = 1		
	TXEPT	Transmit buffer empty flag	Transmit buffer empty flag		
	CRD (4)	Set to "1"	Set to "1"		
	NCH	Set to "1" ⁽²⁾	Set to "1" ⁽²⁾		
	CKPOL	Set to "0"	Set to "0"		
	UFORM	Set to "1"	Set to "1"		
UiC1	TE	Set this bit to "1" to enable transmission	Set this bit to "1" to enable transmission		
0.01	TI	Transmit buffer empty flag	Transmit buffer empty flag		
	RE	Set this bit to "1" to enable reception	Set this bit to "1" to enable reception		
	RI	Reception complete flag	Reception complete flag		
	U2IRS ⁽¹⁾	Invalid	Invalid		
	U2RRM ⁽¹⁾ , UiLCH, UiERE	Set to "0"	Set to "0"		
UiSMR	IICM	Set to "1"	Set to "1"		
	ABC	Select the timing at which arbitration-lost is detected	Invalid		
	BBS	Bus busy flag	Bus busy flag		
	3 to 7	Set to "0"	Set to "0"		
UiSMR2	IICM2	See Table 17.13 I ² C Mode Functions	See Table 17.13 I ² C Mode Functions		
	CSC	Set this bit to "1" to enable clock synchronization	Set to "0"		
	SWC	Set this bit to "1" to have SCLi output fixed to "L" at the falling edge of the 9th bit of clock	Set this bit to "1" to have SCLi output fixed to "L" at the falling edge of the 9th bit of clock		
	ALS	Set this bit to "1" to have SDAi output stopped when arbitration-lost is detected	Set to "0"		
	STAC	Set to "0"	Set this bit to "1" to initialize UARTi at start condition detection		
	SWC2	Set this bit to "1" to have SCLi output forcibly pulled low	Set this bit to "1" to have SCLi output forcibly pulled low		
	SDHI	Set this bit to "1" to disable SDAi output	Set this bit to "1" to disable SDAi output		
	7	Set to "0"	Set to "0"		

 Table 17.11
 Registers to Be Used and Settings in I²C Mode (1)

NOTES:

- 1. Set the bit 4 and bit 5 in the U0C1 and U1C1 register to "0". The U0IRS, U1IRS, U0RRM and U1RRM bits are in the UCON register.
- 2. TXD2 pin is N channel open-drain output. No NCH bit in the U2C0 register is assigned. When write, set to "0".
- 3. Not all register bits are described above. Set those bits to "0" when writing to the registers in I²C mode.
- 4. When using UART1 in I²C mode and enabling the CTS/RTS separate function of UART0, set the CRD bit in the U1C0 register to "0" (CTS/RTS enable) and the CRS bit to "0" (CTS input).

i=0 to 2

Register	Bit	Function		
		Master	Slave	
UiSMR3	0, 2, 4 and NODC	Set to "0"	Set to "0"	
	СКРН	See Table 17.13 I ² C Mode Functions	See Table 17.13 I ² C Mode Functions	
	DL2 to DL0	Set the amount of SDAi digital delay	Set the amount of SDAi digital delay	
UiSMR4	STAREQ	Set this bit to "1" to generate start condition	Set to "0"	
	RSTAREQ	Set this bit to "1" to generate restart condition	Set to "0"	
	STPREQ	Set this bit to "1" to generate stop condition	Set to "0"	
	STSPSEL	Set this bit to "1" to output each condition	Set to "0"	
	ACKD	Select ACK or NACK	Select ACK or NACK	
	ACKC	Set this bit to "1" to output ACK data	Set this bit to "1" to output ACK data	
	SCLHI	Set this bit to "1" to have SCLi output stopped when stop condition is detected	Set to "0"	
	SWC9	Set to "0"	Set this bit to "1" to set the SCLi to "L" hold at the falling edge of the 9th bit of clock	
IFSR2A	IFSR26, ISFR27	Set to "1"	Set to "1"	
UCON U0IRS, U1IRS Invalid		Invalid	Invalid	
	2 to 7	Set to "0"	Set to "0"	

 Table 17.12
 Registers to Be Used and Settings in I²C Mode (2)

i=0 to 2

Function	Clock Synchronous Serial I/O	I ² C Mode (SMD2 to SMD0 = 010b, IICM = 1)			
	Mode (SMD2 to SMD0 = 001b, IICM = 0)	IICM2 = 0 (NACK/ACK interrupt)		IICM2 = 1 (UART transmit/receive interrupt)	
		CKPH = 0 (No clock delay)	CKPH = 1 (Clock delay)	CKPH = 0 (No clock delay)	CKPH = 1 (Clock delay)
Factor of Interrupt Number 6, 7 and 10 ^(1, 5, 7)	1	Start condition dete (See Table 17.14 S			
Factor of Interrupt Number 15, 17 and 19 ^(1, 6)	UARTi transmission Transmission started or completed (selected by UiIRS)	No acknowledgmer detection (NACK) Rising edge of SCL		UARTi transmission Rising edge of SCLi 9th bit	UARTi transmission Falling edge of SCLi next to the 9th bit
Factor of Interrupt Number 16, 18 and 20 ^(1, 6)	UARTi reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment de Rising edge of SCL		UARTi reception Falling edge of SCLi	9th bit
Timing for Transferring Data From the UART Reception Shift Register to the UiRB Register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of SCL	i 9th bit	Falling edge of SCLi 9th bit	Falling and rising edges of SCLi 9th bit
UARTi Transmission Output Delay	Not delayed	Delayed			
Functions of P6_3, P6_7 and P7_0 Pins	TXDi output	SDAi input/output			
Functions of P6_2, P6_6 and P7_1 Pins	RXDi input	SCLi input/output			
Functions of P6_1, P6_5 and P7_2 Pins	CLKi input or output selected	- (Cannot be used	in I ² C mode)		
Noise Filter Width	15ns	200ns			
Read RXDi and SCLi Pin Levels	Possible when the corresponding port direction bit = 0	Always possible no	matter how the co	rresponding port direc	tion bit is set
Initial Value of TXDi and SDAi Outputs	CKPOL = 0 (H) $CKPOL = 1 (L)$	The value set in the	e port register befor	e setting I ² C mode (2)	
Initial and End Values of SCLi	-	Н	L	Н	L
DMA1 Factor ⁽⁶⁾	UARTi reception	Acknowledgment de	etection (ACK)	UARTi reception Falling edge of SCLi	9th bit
Store Received Data	1st to 8th bits of the received data are stored into bits 7 to 0 in the UiRB register	1st to 8th bits of the stored into bits 7 to register		1st to 7th bits of the stored into bits 6 to 0 8th bit is stored into register.) in the UiRB register.
					1st to 8th bits are stored into bits 7 to 0 in the UiRB register ⁽³⁾
Read Received Data	The UiRB register status is read				Bits 6 to 0 in the UiRB register ⁽⁴⁾ are read as bits 7 to 1. Bit 8 in the UiRB register is read as bit 0.

Table 17.13	I ² C Mode	Functions
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NOTES:

1. If the source or factor of any interrupt is changed, the IR bit in the interrupt control register for the changed interrupt may inadvertently be set to "1" (interrupt requested). (Refer to 24.7 Interrupt)

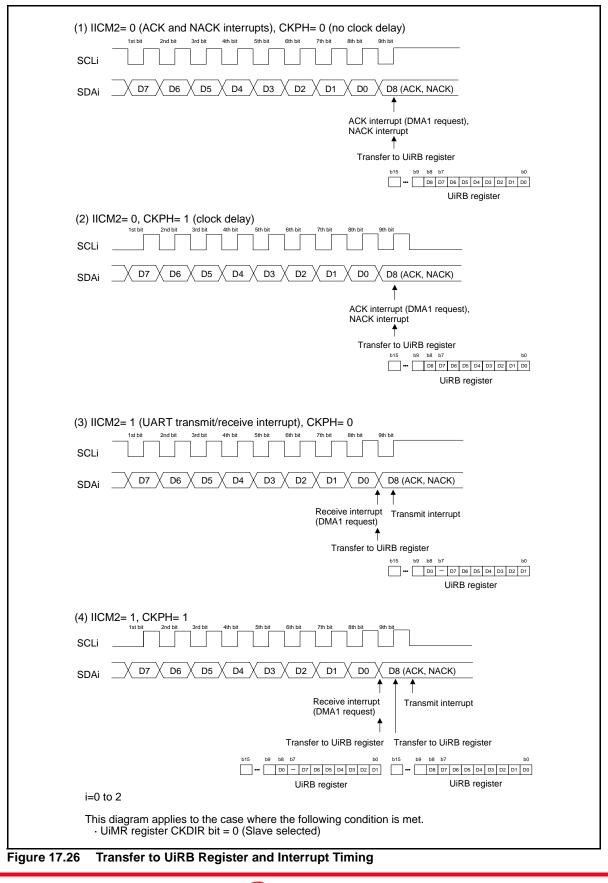
If one of the bits shown below is changed, the interrupt source, the interrupt timing, etc. change. Therefore, always be sure to clear the IR bit to "0" (interrupt not requested) after changing those bits.

SMD2 to SMD0 bits in the UiMR register, IICM bit in the UiSMR register, IICM2 bit in the UiSMR2 register, CKPH bit in the UiSMR3 register

- 2. Set the initial value of SDAi output while the SMD2 to SMD0 bits in the UiMR register = 000b (serial interface disabled).
- 3. Second data transfer to UiRB register (Rising edge of SCLi 9th bit)
- 4. First data transfer to UiRB register (Falling edge of SCLi 9th bit)
- 5. See Figure 17.28 STSPSEL Bit Functions.
- 6. See Figure 17.26 Transfer to UiRB Register and Interrupt Timing.
- 7. When using UARTO, be sure to set the IFSR26 bit in the IFSR2A register to "1" (factor of interrupt: UARTO bus collision).

When using UART1, be sure to set the IFSR27 bit to "1" (factor of interrupt: UART1 bus collision).

i = 0 to 2



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17.1.3.1 Detection of Start and Stop Condition

Whether a start or a stop condition has been detected is determined.

A start condition-detected interrupt request is generated when the SDAi pin changes state from high to low while the SCLi pin is in the high state. A stop condition-detected interrupt request is generated when the SDAi pin changes state from low to high while the SCLi pin is in the high state.

Because the start and stop condition-detected interrupts share the interrupt control register and vector, check the BBS bit in the UiSMR register to determine which interrupt source is requesting the interrupt.

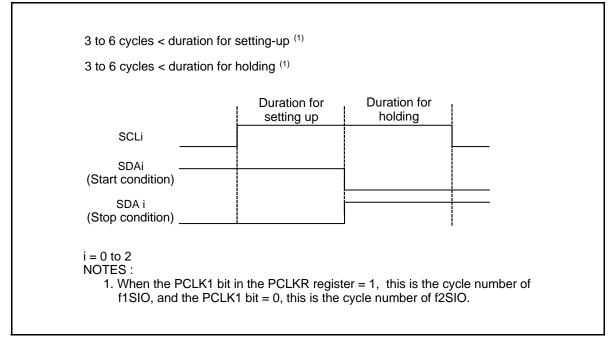


Figure 17.27 Detection of Start and Stop Condition

17.1.3.2 Output of Start and Stop Condition

A start condition is generated by setting the STAREQ bit in the UiSMR4 register (i = 0 to 2) to "1" (start). A restart condition is generated by setting the RSTAREQ bit in the UiSMR4 register to "1" (start). A stop condition is generated by setting the STPREQ bit in the UiSMR4 register to "1" (start). The output procedure is described below.

- (1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to "1" (start).
- (2) Set the STSPSEL bit in the UiSMR4 register to "1" (output).

The function of the STSPSEL bit is shown in Table 17.14 and Figure 17.28.

Function	STSPSEL = 0	STSPSEL = 1
Output of SCLi and SDAi Pins	Output of transfer clock and data Output of start/stop condition is accomplished by a program using ports (not automatically generated in hardware)	Output of a start/stop condition according to the STAREQ, RSTAREQ and STPREQ bit
Start/Stop Condition Interrupt	Start/stop condition detection	Finish generating start/stop
Request Generation Timing		condition

Table 17.14 STSPSEL Bit Functions

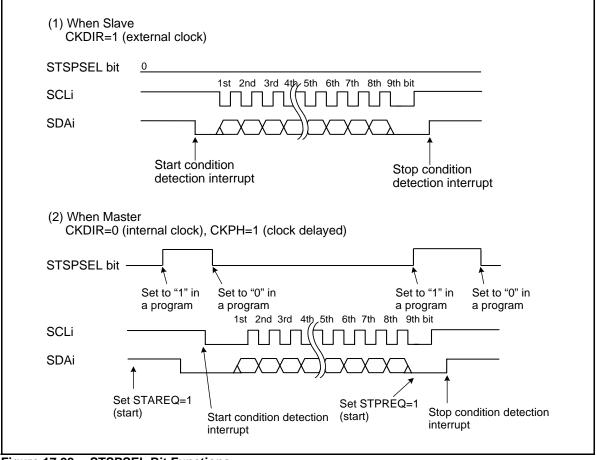


Figure 17.28 STSPSEL Bit Functions

17.1.3.3 Arbitration

Unmatching of the transmit data and SDAi pin input data is checked synchronously with the rising edge of SCLi. Use the ABC bit in the UiSMR register to select the timing at which the ABT bit in the UiRB register is updated. If the ABC bit = 0 (updated bitwise), the ABT bit is set to "1" at the same time unmatching is detected during check, and is cleared to "0" when not detected. In cases when the ABC bit is set to "1", if unmatching is detected even once during check, the ABT bit is set to "1" (unmatching detected) at the falling edge of the clock pulse of 9th bit. If the ABT bit needs to be updated bytewise, clear the ABT bit to "0" (undetected) after detecting acknowledge in the first byte, before transferring the next byte.

Setting the ALS bit in the UiSMR2 register to "1" (SDA output stop enabled) factors arbitration-lost to occur, in which case the SDAi pin is placed in the high-impedance state at the same time the ABT bit is set to "1" (unmatching detected).

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17.1.3.4 Transfer Clock

Data is transmitted/received using a transfer clock like the one shown in Figure 17.26 Transfer to UiRB Register and Interrupt Timing.

The CSC bit in the UiSMR2 register is used to synchronize the internally generated clock (internal SCLi) and an external clock supplied to the SCLi pin. In cases when the CSC bit is set to "1" (clock synchronization enabled), if a falling edge on the SCLi pin is detected while the internal SCLi is high, the internal SCLi goes low, at which time the value of the UiBRG register is reloaded with and starts counting in the low-level interval. If the internal SCLi changes state from low to high while the SCLi pin is low, counting stops, and when the SCLi pin goes high, counting restarts.

In this way, the UARTi transfer clock is comprised of the logical product of the internal SCLi and SCLi pin signal. The transfer clock works from a half period before the falling edge of the internal SCLi 1st bit to the rising edge of the 9th bit. To use this function, select an internal clock for the transfer clock.

The SWC bit in the UiSMR2 register allows to select whether the SCLi pin should be fixed to or freed from low-level output at the falling edge of the 9th clock pulse.

If the SCLHI bit in the UiSMR4 register is set to "1" (enabled), SCLi output is turned off (placed in the highimpedance state) when a stop condition is detected.

Setting the SWC2 bit in the UiSMR2 register = 1 (0 output) makes it possible to forcibly output a low-level signal from the SCLi pin even while sending or receiving data. Clearing the SWC2 bit to "0" (transfer clock) allows the transfer clock to be output from or supplied to the SCLi pin, instead of outputting a low-level signal. If the SWC9 bit in the UiSMR4 register is set to "1" (SCL hold low enabled) when the CKPH bit in the UiSMR3 register = 1, the SCLi pin is fixed to low-level output at the falling edge of the clock pulse next to the 9th. Setting the SWC9 bit = 0 (SCL hold low disabled) frees the SCLi pin from low-level output.

17.1.3.5 SDA Output

The data written to the UiTB register bit 7 to bit 0 (D7 to D0) is sequentially output beginning with D7. The 9th bit (D8) is ACK or NACK.

The initial value of SDAi transmit output can only be set when IICM = 1 (I^2C mode) and the SMD2 to SMD0 bits in the UiMR register = 000b (Serial interface disabled).

The DL2 to DL0 bits in the UiSMR3 register allow to add no delays or a delay of 2 to 8 UiBRG count source clock cycles to SDAi output.

Setting the SDHI bit in the UiSMR2 register = 1 (SDA output disabled) forcibly places the SDAi pin in the high-impedance state. Do not write to the SDHI bit synchronously with the rising edge of the UARTi transfer clock. This is because the ABT bit may inadvertently be set to "1" (detected).

17.1.3.6 SDA Input

When the IICM2 bit = 0, the 1st to 8th bits (D7 to D0) of received data are stored in the UiRB register bit 7 to bit 0. The 9th bit (D8) is ACK or NACK.

When the IICM2 bit = 1, the 1st to 7th bits (D7 to D1) of received data are stored in the UiRB register bit 6 to bit 0 and the 8th bit (D0) is stored in the UiRB register bit 8. Even when the IICM2 bit = 1, providing the CKPH bit = 1, the same data as when the IICM2 bit = 0 can be read out by reading the UiRB register after the rising edge of the corresponding clock pulse of 9th bit.

17.1.3.7 ACK and NACK

If the STSPSEL bit in the UiSMR4 register is set to "0" (start and stop conditions not generated) and the ACKC bit in the UiSMR4 register is set to "1" (ACK data output), the value of the ACKD bit in the UiSMR4 register is output from the SDAi pin.

If the IICM2 bit = 0, a NACK interrupt request is generated if the SDAi pin remains high at the rising edge of the 9th bit of transmit clock pulse. An ACK interrupt request is generated if the SDAi pin is low at the rising edge of the 9th bit of transmit clock pulse.

If ACKi is selected for the factor of DMA1 request, a DMA transfer can be activated by detection of an acknowledge.

17.1.3.8 Initialization of Transmission/Reception

If a start condition is detected while the STAC bit = 1 (UARTi initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the content of the UiTB register is transferred to the transmit shift register. In this way, the serial interface starts sending data synchronously with the next clock pulse applied. However, the UARTi output value does not change state and remains the same as when a start condition was detected until the first bit of data is output synchronously with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data synchronously with the next clock pulse applied.
- The SWC bit is set to "1" (SCL wait output enabled). Consequently, the SCLi pin is pulled low at the falling edge of the 9th clock pulse.

Note that when UARTi transmission/reception is started using this function, the TI does not change state. Note also that when using this function, the selected transfer clock should be an external clock.

17.1.4 Special Mode 2

Multiple slaves can be serially communicated from one master. Transfer clock polarity and phase are selectable. Table 17.15 lists the Special Mode 2 Specifications. Table 17.16 lists the Registers to Be Used and Settings in Special Mode 2. Figure 17.29 shows Serial Bus Communication Control Example (UART2).

Table 17.15	Special	Mode 2	2 Specifications
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ltem	Specification	
Transfer Data Format	Transfer data length: 8 bits	
Transfer Clock	 Master mode CKDIR bit in UiMR(i=0 to 2) register = 0 (internal clock) : fj/ (2(n+1)) fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh Slave mode CKDIR bit = 1 (external clock selected) : Input from CLKi pin 	
Transmit/Receive Control	Controlled by input/output ports	
Transmission Start Condition	 Before transmission can start, meet the following requirements ⁽¹⁾ The TE bit in UiC1 register= 1 (transmission enabled) The TI bit in UiC1 register = 0 (data present in UiTB register) 	
Reception Start Condition	 Before reception can start, meet the following requirements ⁽¹⁾ The RE bit in UiC1 register= 1 (reception enabled) The TE bit in UiC1 register= 1 (transmission enabled) The TI bit in UiC1 register= 0 (data present in the UiTB register) 	
Interrupt Request Generation Timing	 For transmission, one of the following conditions can be selected The UiIRS bit in UiC1 register = 0 (transmit buffer empty): when transferring data from the UiTB register to the UARTi transmit register (at start of transmission) The UiIRS bit =1 (transfer completed): when the serial interface finished sending data from the UARTi transmit register For reception When transferring data from the UARTi receive register to the UiRB register (at completion) 	
Error Detection	Overrun error ⁽²⁾ This error occurs if the serial interface started receiving the next data before reading the UiRB register and received the 7th bit of the next data	
Select Function	Clock phase setting Selectable from four combinations of transfer clock polarities and phases	

NOTES:

 When an external clock is selected, the conditions must be met while if the CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the external clock is in the high state; if the CKPOL bit = 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the low state.

2. If an overrun error occurs, the value of UiRB register will be indeterminate. The IR bit in the SiRIC register does not change.

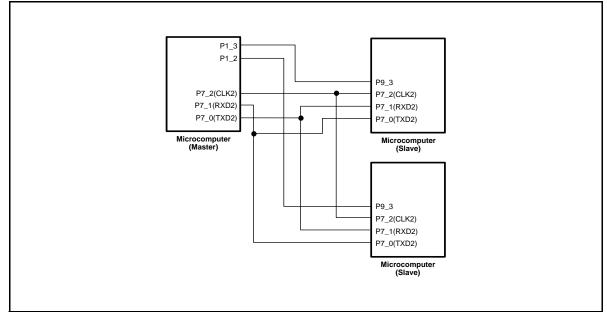


Figure 17.29 Serial Bus Communication Control Example (UART2)

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Register	Bit	Function	
UiTB ⁽³⁾	0 to 7	Set transmission data	
UiRB ⁽³⁾	0 to 7	Reception data can be read	
	OER	Overrun error flag	
UiBRG	0 to 7	Set a bit rate	
UiMR ⁽³⁾	SMD2 to SMD0	Set to "001b"	
	CKDIR	Set this bit to "0" for master mode or "1" for slave mode	
	IOPOL	Set to "0"	
UiC0	CLK1, CLK0	Select the count source for the UiBRG register	
	CRS	Invalid because CRD = 1	
	TXEPT	Transmit register empty flag	
	CRD	Set to "1"	
	NCH	Select TXDi pin output format ⁽²⁾	
	CKPOL	Clock phases can be set in combination with the CKPH bit in the UiSMR3 register	
	UFORM	Set to "0"	
UiC1	TE	Set this bit to "1" to enable transmission	
	TI	Transmit buffer empty flag	
	RE	Set this bit to "1" to enable reception	
	RI	Reception complete flag	
	U2IRS (1)	Select UART2 transmit interrupt factor	
	U2RRM ⁽¹⁾ , UiLCH, UiERE	Set to "0"	
UiSMR	0 to 7	Set to "0"	
UiSMR2	0 to 7	Set to "0"	
UiSMR3	СКРН	Clock phases can be set in combination with the CKPOL bit in the UiC0 register	
	NODC	Set to "0"	
	0, 2, 4 to 7	Set to "0"	
UiSMR4	0 to 7	Set to "0"	
UCON	U0IRS, U1IRS	Select UART0 and UART1 transmit interrupt factor	
	U0RRM, U1RRM	Set to "0"	
	CLKMD0	Invalid because CLKMD1 = 0	
	CLKMD1, RCSP, 7	Set to "0"	

Table 17.16 Registers to Be Used and Settings in Special Mode 2

NOTES:

1. Set the bit 4 and bit 5 in the U0C0 and U1C1 register to "0". The U0IRS, U1IRS, U0RRM and U1RRM bits are in the UCON register.

2. TXD2 pin is N channel open-drain output. No NCH bit in the U2C0 register is assigned. When write, set to "0".

3. Not all register bits are described above. Set those bits to "0" when writing to the registers in Special Mode 2.

i = 0 to 2

17.1.4.1 Clock Phase Setting Function

One of four combinations of transfer clock phases and polarities can be selected using the CKPH bit in the UiSMR3 register and the CKPOL bit in the UiC0 register.

Make sure the transfer clock polarity and phase are the same for the master and salves to be communicated. Figure 17.30 shows the Transmission and Reception Timing in Master Mode (Internal Clock).

Figure 17.31 shows the Transmission and Reception Timing (CKPH=0) in Slave Mode (External Clock) while Figure 17.32 shows the Transmission and Reception Timing (CKPH=1) in Slave Mode (External Clock).

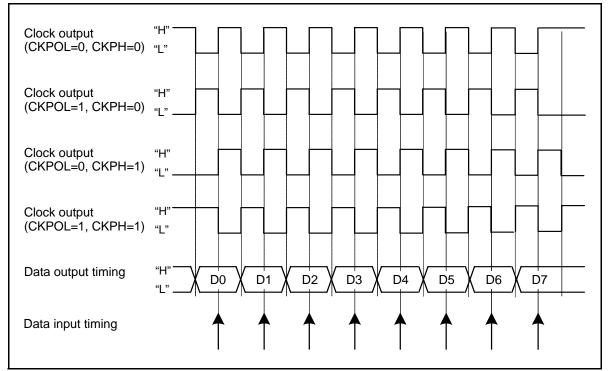


Figure 17.30 Transmission and Reception Timing in Master Mode (Internal Clock)

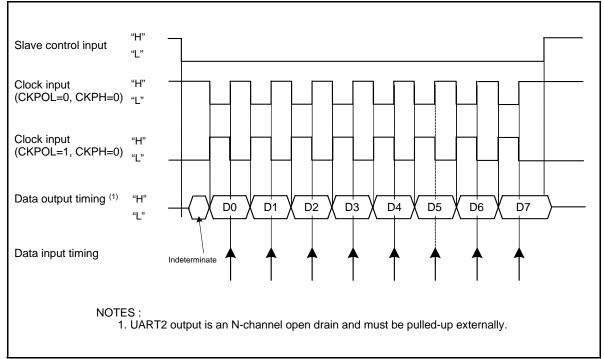


Figure 17.31 Transmission and Reception Timing (CKPH=0) in Slave Mode (External Clock)

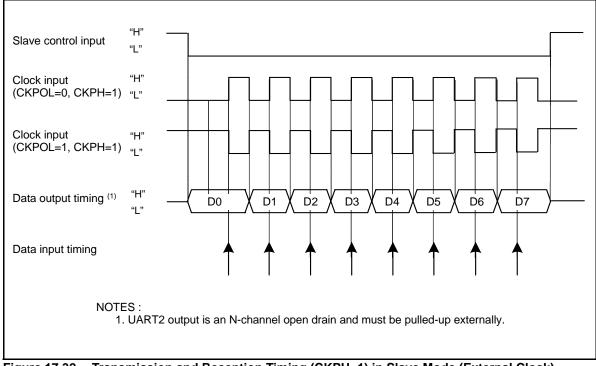


Figure 17.32 Transmission and Reception Timing (CKPH=1) in Slave Mode (External Clock)

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17.1.5 Special Mode 3 (IE mode)

In this mode, one bit of IEBus is approximated with one byte of UART mode waveform.

Table 17.17 lists the Registers to Be Used and Settings in IE Mode. Figure 17.33 shows the Bus Collision Detect Function-Related BitsBus Collision Detect Function-Related Bits.

If the TXDi pin (i = 0 to 2) output level and RXDi pin input level do not match, a UARTi bus collision detect interrupt request is generated.

Use the IFSR26 and IFSR27 bits in the IFSR2A register to enable the UART0/UART1 bus collision detect function.

Register	Bit	Function		
UiTB	0 to 8	Set transmission data		
UiRB ⁽³⁾	0 to 8	Reception data can be read		
	OER, FER, PER, SUM	Error flag		
UiBRG	0 to 7	Set a bit rate		
UiMR	SMD2 to SMD0	Set to "110b"		
	CKDIR	Select the internal clock or external clock		
	STPS	Set to "0"		
	PRY	Invalid because PRYE=0		
	PRYE	Set to "0"		
	IOPOL	Select the TXD/RXD input/output polarity		
UiC0	CLK1, CLK0	Select the count source for the UiBRG register		
	CRS	Invalid because CRD=1		
	TXEPT	Transmit register empty flag		
	CRD	Set to "1"		
	NCH	Select TXDi pin output mode ⁽²⁾		
	CKPOL	Set to "0"		
	UFORM	Set to "0"		
UiC1	TE	Set this bit to "1" to enable transmission		
	TI	Transmit buffer empty flag		
	RE	Set this bit to "1" to enable reception		
	RI	Reception complete flag		
	U2IRS (1)	Select the source of UART2 transmit interrupt		
	U2RRM ^{(1),} UiLCH, UiERE	Set to "0"		
UISMR	0 to 3, 7	Set to "0"		
	ABSCS	Select the sampling timing at which to detect a bus collision		
	ACSE	Set this bit to "1" to use the auto clear function of transmit enable bit		
	SSS	Select the transmit start condition		
UiSMR2	0 to 7	Set to "0"		
UISMR3	0 to 7	Set to "0"		
UiSMR4	0 to 7	Set to "0"		
IFSR2A	IFSR26, IFSR27	Set to "1"		
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt		
	U0RRM, U1RRM	Set to "0"		
	CLKMD0	Invalid because CLKMD1 = 0		
	CLKMD1, RCSP, 7	Set to "0"		

Table 17.17 Registers to Be Used and Settings in IE Mode

NOTES:

- 1. Set the bit 4 and bit 5 in the U0C0 and U1C1 registers to "0". The U0IRS, U1IRS, U0RRM and U1RRM bits are in the UCON register.
- 2. TXD2 pin is N channel open-drain output. No NCH bit in the U2C0 register is assigned. When write, set to "0".

3. Not all register bits are described above. Set those bits to "0" when writing to the registers in IE mode.

i= 0 to 2

	If ABSCS=0, bus collision is determined at the rising edge of the transfer clock
Transfer clock	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
TXDi	
RXDi	Trigger signal is applied to the TAjIN pin
Timer Aj	If ABSCS=1, bus collision is determined when timer
Timer Aj: Timer A3 wł	Aj (one-shot timer mode) underflows. hen UART0; Timer A4 when UART1; Timer A0 when UART2
(2) The ACSE Bit in	the UiSMR Register (Auto clear of transmit enable bit)
Transfer clock	ST D0 D1 D2 D3 D4 D5 D6 D7 D8 SP
TXDi	
RXDi	
IR bit in UiBCNIC register (1)	If ACSE bit = 1 (automatically clear when bus collision occurs TE bit is cleared to "0"
TE bit in UiC1 register	(transmission disabled) when t IR bit in the UiBCNIC register= (unmatching detected).
NOTES : 1. BCNIC register	when UART2.
(3) The SSS Bit in th	ne UiSMR Register (Transmit start condition select)
If SSS bit = 0, the	serial interface starts sending data one transfer clock cycle after the transmission enable condition is r
Transfer clock	ST D0 D1 D2 D3 D4 D5 D6 D7 D8 SP
TXDi	
Transr	nission enable condition is met
If SSS bit = 1, the	serial interface starts sending data at the rising edge ⁽¹⁾ of RXDi
CLKi	ST D0 D1 D2 D3 D4 D5 D6 D7 D8 SP
TXDi	(NOTE 2)
RXDi	
NOTES : 1. The falling edge 2. The transmit co	e of RXDi when IOPOL=0; the rising edge of RXDi when IOPOL =1. andition must be met before the falling edge $^{(1)}$ of RXD.

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17.1.6 Special Mode 4 (SIM Mode) (UART2)

Based on UART mode, this is an SIM interface compatible mode. Direct and inverse formats can be implemented, and this mode allows to output a low from the TXD2 pin when a parity error is detected. Table 17.18 lists the SIM Mode Specifications. Table 17.19 lists the Registers to Be Used and Settings in SIM Mode.

Item	Specification
Transfer Data Format	Direct format Inverse format
Transfer Clock	 CKDIR bit in U2MR register = 0 (internal clock) : fi/ (16(n+1)) fi = f1SIO, f2SIO, f3SIO, f32SIO n: Setting value of U2BRG register 00h to FFh CKDIR bit = 1 (external clock) : fEXT/(16(n+1)) fEXT: Input from CLK2 pin n: Setting value of U2BRG register 00h to FFh
Transmission Start Condition	Before transmission can start, meet the following requirements • The TE bit in the U2C1 register = 1 (transmission enabled) • The TI bit in the U2C1 register = 0 (data present in U2TB register)
Reception Start Condition	Before reception can start, meet the following requirements • The RE bit in the U2C1 register = 1 (reception enabled) • Start bit detection
Interrupt Request Generation Timing ⁽²⁾	 For transmission When the serial interface finished sending data from the U2TB transfer register (U2IRS bit =1) For reception When transferring data from the UART2 receive register to the U2RB register (at completion of reception)
Error Detection	 Overrun error ⁽¹⁾ This error occurs if the serial interface started receiving the next data before reading the U2RB register and received the bit one before the last stop bit of the next data Framing error ⁽³⁾ This error occurs when the number of stop bits set is not detected Parity error ⁽³⁾ During reception, if a parity error is detected, parity error signal is output from the TXD2 pin. During transmission, a parity error is detected by the level of input to the RXD2 pin when a transmission interrupt occurs Error sum flag This flag is set (= 1) when any of the overrun, framing, and parity errors is encountered

Table 17.18	SIM Mode	Specifications
-------------	----------	----------------

NOTES:

- 1. If an overrun error occurs, the value of U2RB register will be indeterminate. The IR bit in the S2RIC register does not change.
- A transmit interrupt request is generated by setting the U2IRS bit to "1" (transmission complete) and U2ERE bit to "1" (error signal output) in the U2C1 register after reset is deserted. Therefore, when using SIM mode, set the IR bit to "0" (no interrupt request) after setting these bits.
- 3. The timing at which the framing error flag and the parity error flag are set is detected when data is transferred from the UARTi receive register to the UiRB register.

Register	Bit	Function		
U2TB ⁽¹⁾	0 to 7	Set transmission data		
U2RB (1)	0 to 7	Reception data can be read		
	OER,FER,PER,SUM	Error flag		
U2BRG	0 to 7	Set a bit rate		
U2MR	SMD2 to SMD0	Set to "101b"		
	CKDIR	Select the internal clock or external clock		
	STPS	Set to "0"		
	PRY	Set this bit to "1" for direct format or "0" for inverse format		
	PRYE	Set to "1"		
	IOPOL	Set to "0"		
U2C0	CLK1, CLK0	Select the count source for the U2BRG register		
	CRS	Invalid because CRD = 1		
	TXEPT	Transmit register empty flag		
	CRD	Set to "1"		
	NCH	Set to "0"		
	CKPOL	Set to "0"		
	UFORM	Set this bit to "0" for direct format or "1" for inverse format		
U2C1	TE	Set this bit to "1" to enable transmission		
	ТІ	Transmit buffer empty flag		
	RE	Set this bit to "1" to enable reception		
	RI	Reception complete flag		
	U2IRS	Set to "1"		
	U2RRM	Set to "0"		
	U2LCH	Set this bit to "0" for direct format or "1" for inverse format		
	U2ERE	Set to "1"		
U2SMR (1)	0 to 3	Set to "0"		
U2SMR2	0 to 7	Set to "0"		
U2SMR3	0 to 7	Set to "0"		
U2SMR4	0 to 7	Set to "0"		

Table 17.19 Registers to Be Used and Settings in SIM Mode

NOTES:

1. Not all register bits are described above. Set those bits to "0" when writing to the registers in SIM mode.

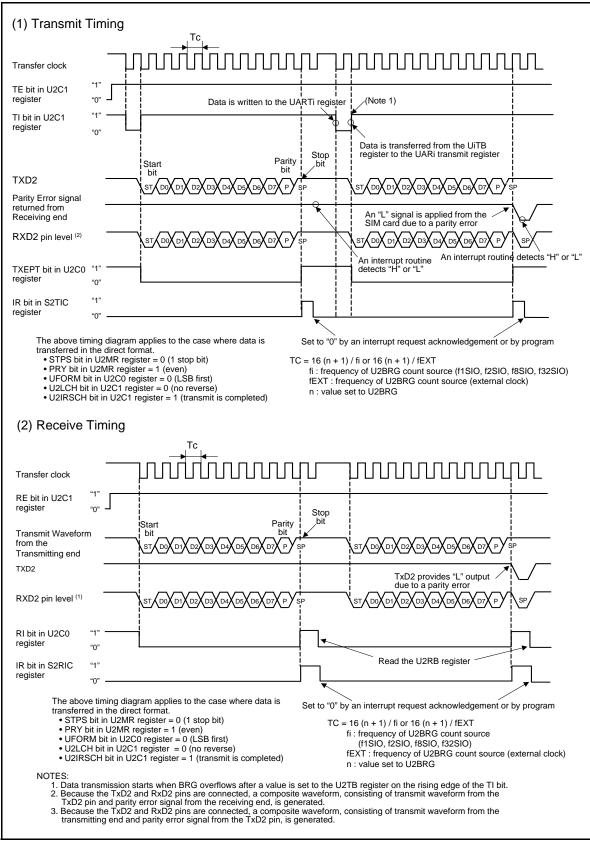
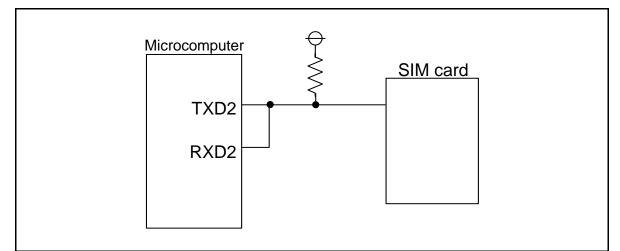


Figure 17.34 Transmit and Receive Timing in SIM Mode

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17.1.6.1 Parity Error Signal Output

The parity error signal is enabled by setting the U2ERE bit in the U2C1 register to "1". The parity error signal is output when a parity error is detected while receiving data. This is achieved by pulling the TXD2 output low with the timing shown in Figure 17.36. If the R2RB register is read while outputting a parity error signal, the PER bit is cleared to "0" and at the same time the TXD2 output is returned high. When transmitting, a transmission-finished interrupt request is generated at the falling edge of the transfer clock pulse that immediately follows the stop bit. Therefore, whether a parity signal has been returned can be determined by reading the port that shares the RXD2 pin in a transmission-finished interrupt routine.

Transfer clock		
RXD2	"H"	<u>\ D7 \ P </u> \ SP
TXD2	"H" (NOTE 1) "L"	
IR bit in U2C1 register	"1" "0"	
This timing di implemented	agram applies to the case where the direct format	P : Even Parity
	put of microcomputer is in the high-impedance staup externally).	SP : Stop bit

Figure 17.36 Parity Error Signal Output Timing

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17.1.6.2 Format

When direct format, set the PRYE bit in the U2MR register to "1", the PRY bit to "1", the UFORM bit in the U2C0 register to "0" and the U2LCH bit in the U2C1 register to "0". When data are transmitted, data set in the U2TB register are transmitted with the even-numbered parity, starting from D0. When data are received, received data are stored in the U2RB register, starting from D0. The even-numbered parity determines whether a parity error occurs.

When inverse format, set the PRYE bit to "1", the PRY bit to "0", the UFORM bit to "1" and the U2LCH bit to "1". When data are transmitted, values set in the U2TB register are logically inversed and are transmitted with the odd-numbered parity, starting from D7. When data are received, received data are logically inversed to be stored in the U2RB register, starting from D7. The odd-numbered parity determines whether a parity error occurs.

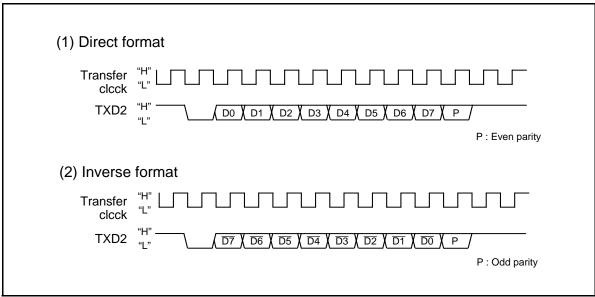


Figure 17.37 SIM Interface Format

17.2 SI/O3 and SI/O4

Note

The M16C/62P (80-pin version) and M16C/62PT (80-pin version) do not include SIN3 pin of SI/O3. SI/O3 is only for transmission. Reception is impossible.

SI/O3 and SI/O4 are exclusive clock-synchronous serial I/Os.

Figure 17.38 shows the SI/O3 and SI/O4 Block Diagram, and Figure 17.39 to Figure 17.40 show the SI/O3 and SI/O4-related registers.

Table 17.20 shows the SI/O3 and SI/O4 Specifications.

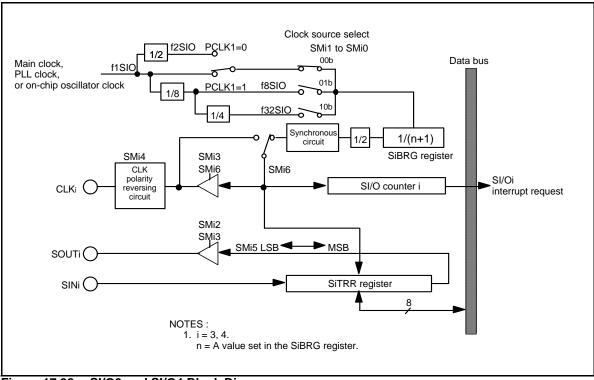


Figure 17.38 SI/O3 and SI/O4 Block Diagram

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b4 b3 b2 b1 b0	ister (i=3, 4)			
	Sym	bol Address	After Reset	
	S3	C 0362h	0100000b	
	S4	C 0366h	0100000b	
	Bit Symbol	Bit Name	Function	RW
	SMiO	Internal Synchronous Clock Select Bit ⁽⁶⁾	b1 b0 0 0 : Selecting f1SIO or f2SIO ⁽⁵⁾ 0 1 : Selecting f8SIO 1 0 : Selecting f32SIO	RW
	SMi1		1 1 : Do not set to this value	RW
	SMi2	SOUTi Output Disable Bit ⁽⁴⁾	0 : SOUTi output 1 : SOUTi output disable (High-Impedance)	RW
	SMi3	S I/Oi Port Select Bit	0 : Input/output port 1 : SOUTi output, CLKi function	RW
	SMi4	CLK Polarity Select Bit	 0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge 	RW
	SMi5	Transfer Direction Select Bit	0 : LSB first 1 : MSB first	RW
	SMi6	Synchronous Clock Select Bit	0 : External clock ⁽²⁾ 1 : Internal clock ⁽³⁾	RW
	SMi7	SOUTi Initial Value Set Bit	Effective w hen SM3 = 0 0 : "L" output 1 : "H" output	RW

NOTES :

- 1. Make sure this register is written to by the next instruction after setting the PRC2 bit in the PRCR register to "1" (write enable).
- 2. Set the SMi3 bit to "1" and the corresponding port direction bit to "0" (input mode).
- 3. Set the SMi3 bit to "1" (SOUTi output, CLKi function).
- 4. When the SMi2 bit is set to "1," the target pin goes to a high-impedance state regardless of which function of the pin is being used.
- 5. Selected by PCLK1 bit in the PCLKR register.
- 6. When changing the SMI1 to SMI0 bits, set the SiBRG register.

Figure 17.39 SiC Register

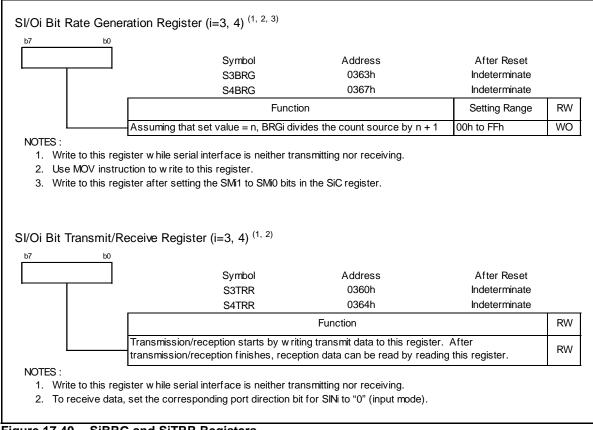


Figure 17.40 SiBRG and SiTRR Registers

Item	Specification
Transfer Data Format	Transfer data length: 8 bits
Transfer Clock	 SMi6 bit in SiC (i=3, 4) register = 1 (internal clock) : fj/ (2(n+1))
	fj = f1SIO, f8SIO, f32SIO. n = Setting value of SiBRG register 00h to FFh.
	 SMi6 bit = 0 (external clock) : Input from CLKi pin ⁽¹⁾
Transmission/Reception	 Before transmission/reception can start, meet the following requirements
Start Condition	Write transmit data to the SiTRR register ^(2, 3)
Interrupt Request	When SMi4 bit in SiC register = 0
Generation Timing	The rising edge of the last transfer clock pulse ⁽⁴⁾
	When SMi4 = 1
	The falling edge of the last transfer clock pulse ⁽⁴⁾
CLKi Pin Function	I/O port, transfer clock input, transfer clock output
SOUTi Pin Function	I/O port, transmit data output, high-impedance
SINi Pin Function	I/O port, receive data input
Select Function	LSB first or MSB first selection
	Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected
	Function for setting an SOUTi initial value set function
	When the SMi6 bit in the SiC register = 0 (external clock), the SOUTi pin output level while not transmitting can be selected.
	CLK polarity selection
	Whether transmit data is output/input timing at the rising edge or falling edge of transfer clock can be selected.

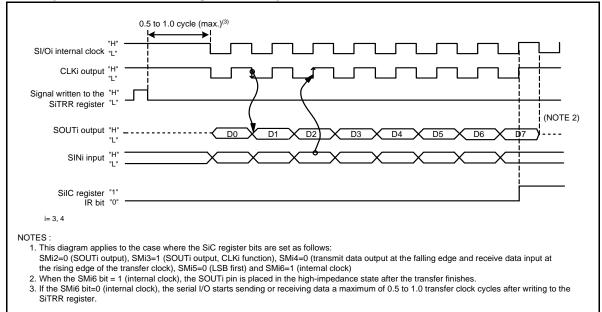
Table 17.20 SI/O3 and SI/O4 Specifications

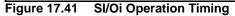
NOTES:

- 1. To set SMi6 bit to "0" (external clock), follow the procedure described below.
 - If the SMi4 bit = 0, write transmit data to the SiTRR register while input on the CLKi pin is high. The same applies when rewriting the SMi7 bit in the SiC register.
 - If the SMi4 bit = 1, write transmit data to the SiTRR register while input on the CLKi pin is low. The same applies when rewriting the SMi7 bit.
 - Because shift operation continues as long as the transfer clock is supplied to the SI/Oi circuit, stop the transfer clock after supplying eight pulses. If the SMi6 bit = 1 (internal clock), the transfer clock automatically stops.
- 2. Unlike UART0 to UART2, SI/Oi (i = 3 to 4) is not separated between the transfer register and buffer. Therefore, do not write the next transmit data to the SiTRR register during transmission.
- 3. When SMi6 bit = 1 (internal clock), SOUTi retains the last data for a 1/2 transfer clock period after completion of transfer and, thereafter, goes to a high-impedance state. However, if transmit data is written to the SiTRR register during this period, SOUTi immediately goes to a high-impedance state, with the data hold time thereby reduced.
- 4. When the SMi6 bit = 1 (internal clock), the transfer clock stops in the high state if the SMi4 bit = 0, or stops in the low state if the SMi4 bit = 1.

17.2.1 SI/Oi Operation Timing

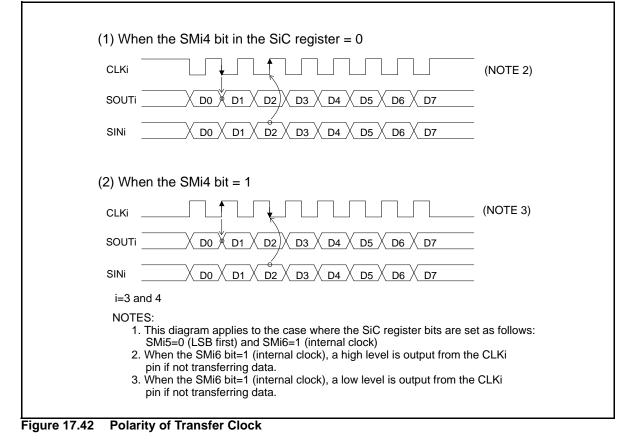






17.2.2 CLK Polarity Selection

The SMi4 bit in the SiC register allows selection of the polarity of the transfer clock. Figure 17.42 shows the Polarity of Transfer Clock.



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17.2.3 Functions for Setting an Souti Initial Value

If the SMi6 bit in the SiC register = 0 (external clock), the SOUTi pin output can be fixed high or low when not transferring. However, the last bit value of the former data is retained between data and data when transmitting the continuous data. Figure 17.43 shows the timing chart for setting an SOUTi initial value and how to set it.

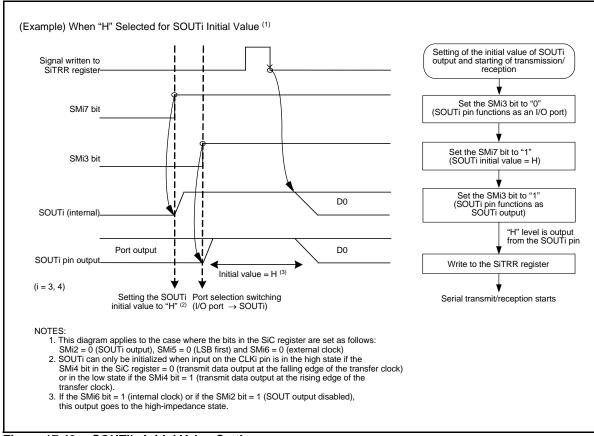


Figure 17.43 SOUTi's Initial Value Setting

18. A/D Converter

The microcomputer contains one A/D converter circuit based on 10-bit successive approximation method configured with a capacitive-coupling amplifier. The analog inputs share the pins with P10_0 to P10_7, P9_5, P9_6, and P0_0 to P0_7, and P2_0 to P2_7. Similarly, $\overline{\text{ADTRG}}$ input shares the pin with P9_7. Therefore, when using these inputs, make sure the corresponding port direction bits are set to "0" (= input mode).

When not using the A/D converter, set the VCUT bit to "0" (= Vref unconnected), so that no current will flow from the VREF pin into the resistor ladder, helping to reduce the power consumption of the chip.

The A/D conversion result is stored in the ADi register bits for ANi, ANO_i, and AN2_i pins (i = 0 to 7).

Table 18.1 shows the Performance of A/D Converter. Figure 18.1 shows the A/D Converter Block Diagram, and Figures 18.2 and 18.3 show the A/D converter-related registers.

Item	Performance
Method of A/D Conversion	Successive approximation (capacitive coupling amplifier)
Analog input Voltage (1)	0V to AVCC (VCC1)
Operating clock ϕ AD ⁽²⁾	fAD/divide-by-2 of fAD/divide-by-3 of fAD/divide-by-4 of fAD/divide-by-6 of fAD/divide-by-12 of fAD
Resolution	8-bit or 10-bit (selectable)
Integral Nonlinearity Error	 When AVCC = VREF = 5V With 8-bit resolution: ±2LSB With 10-bit resolution AN0 to AN7 input, AN0_0 to AN0_7 input and AN2_0 to AN2_7 input : 3LSB ANEX0 and ANEX1 input (including mode in which external Op-Amp is connected) : ±7LSB When AVCC = VREF = 3.3V With 8-bit resolution: ±2LSB With 10-bit resolution: ±2LSB With 10-bit resolution AN0 to AN7 input, AN0_0 to AN0_7 input and AN2_0 to AN2_7 input : ±5LSB ANEX0 and ANEX1 input (including mode in which external Op-Amp is connected) : ±7LSB
Operating Modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, and repeat sweep mode 1
Analog Input Pins ⁽³⁾	8 pins (AN0 to AN7) + 2 pins (ANEX0 and ANEX1) + 8 pins (AN0_0 to AN0_7) + 8 pins (AN2_0 to AN2_7)
A/D Conversion Start Condition	 Software trigger The ADST bit in the ADCON0 register is set to "1" (A/D conversion starts) External trigger (retriggerable) Input on the ADTRG pin changes state from high to low after the ADST bit is set to "1" (A/D conversion starts)
Conversion Speed	 Without sample and hold function 8-bit resolution: 49 \u03c6AD cycles, 10-bit resolution: 59 \u03c6AD cycles With sample and hold function 8-bit resolution: 28 \u03c6AD cycles, 10-bit resolution: 33 \u03c6AD cycles

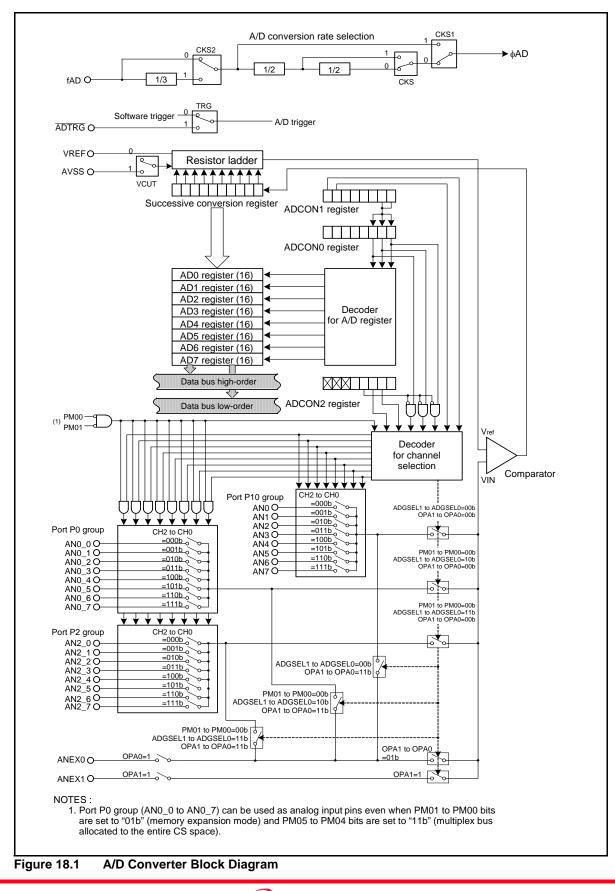
Table 18.1 Performance of A/D Converter

NOTES:

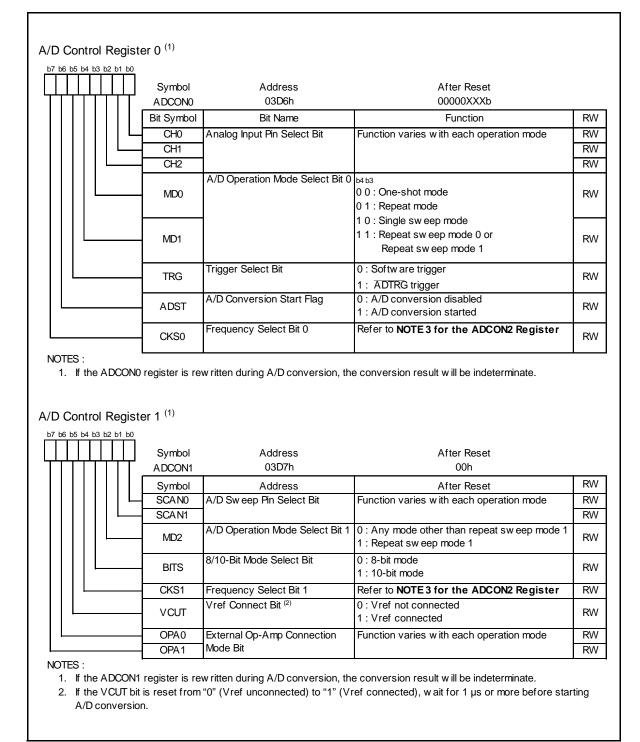
- 1. Does not depend on use of sample and hold function.
- φAD frequency must be 12 MHz or less. And divide the fAD if VCC1 is less than 4.0V, and φAD frequency into 10 MHz or less.
 - When sample & hold is disabled, ϕAD frequency must be 250kHz or more.

When sample & hold is enabled, ϕAD frequency must be 1MHz or more.

3. If VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

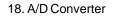


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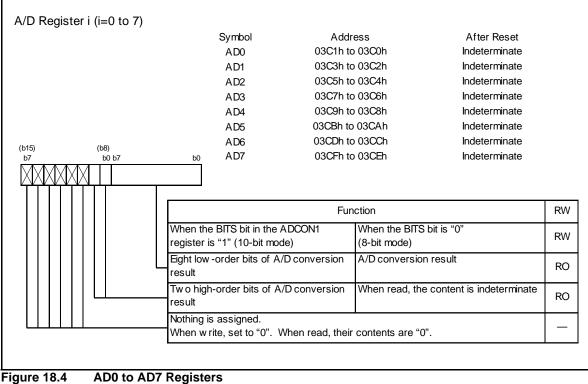


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	b5 b4	TT	2 b1 b0						
XX	X	0		Symbol	Ad	ddress		After Reset	
TT	\square			A DCON2	0)3D4h		00h	
				Bit Symbol	Bi	it Name		Function	RW
			L	SMP	A/D Conversi Bit	ion Method Select	0:Without sa 1:With samp	ample and hold ble and hold	RW
				ADGSEL0	A/D Input Gro	oup Select Bit	^{b2 b1} 0 0 : Port P10 0 1 : Do not s) group is selected	RW
				ADGSEL1	1		1 0 : Port P0 g	group is selected ⁽²⁾ group is selected	RW
				(b3)	Reserved Bit		Set to "0"		RW
				CKS2	Frequency Select Bit 2 ⁽³⁾		 0: Selects fAD, fAD divided by 2, or fAD divided by 4. 1: Selects fAD divided by 3, fAD divided by 6, or fAD divided by 12. 		RW
					Nothing is assigned.			\neg	
				(b7-b5)	When w rite, set to "0". When read, their contents are "0".				
2.	If the formation of the	he A √CC2 e ØA	2 < VC0 D freq	C1, do not use juency must be	ANO_0 to ANO e 12 MHz or les	0_7 and AN2_0 to ss. The selected Ø	AN2_7 as ana ØAD frequency	n result will be indeterminate. alog input pins. y is determined by a combination of CKS2 bit in the ADCON2 register.	the CKS
		CKS	32	CKS1	CKS0	ØA	D	1	
		0 0 0 Divide-by-4 of f							
		0		0	1	Divide-by-2 of f	AD		
		0		1	0	fAD			
		0		1	1				
		1		0	0	Ddivide-by-12 d			
		1	$ \rightarrow $	0	1	Divide-by-6 of f			
		1		1	0	Divide-by-3 of f	AD		

Figure 18.3 ADCON2 Register

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18.1 Mode Description

18.1.1 One-Shot Mode

In one-shot mode, analog voltage applied to a selected pin is converted to a digital code once. Table 18.2 shows the One-Shot Mode Specifications. Figure 18.5 shows the ADCON0 and ADCON1 Registers (One-shot Mode).

Table 18.2	One-Shot Mode Specifications
------------	------------------------------

Item	Specification
Function	The CH2 to CH0 bits in the ADCON0 register, the ADGSEL1 to ADGSEL0 bits in the ADCON2 register and the OPA1 to OPA0 bits in the ADCON1 register select a pin. Analog voltage applied to the pin is converted to a digital code once.
A/D Conversion Start Condition	 When the TRG bit in the ADCON0 register is "0" (software trigger) The ADST bit in the ADCON0 register is set to "1" (A/D conversion starts) When the TRG bit is "1" (ADTRG trigger) Input on the ADTRG pin changes state from high to low after the ADST bit is set to "1" (A/D conversion starts)
A/D Conversion Stop Condition	 Completion of A/D conversion (If a software trigger is selected, the ADST bit is cleared to "0" (A/D conversion halted)) Set the ADST bit to "0"
Interrupt Request Generation Timing	Completion of A/D conversion
Analog Input Pin ⁽¹⁾	Select one pin from AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0 to ANEX1
Reading of Result of A/D Converter	Read one of the AD0 to AD7 registers that corresponds to the selected pin
NOTES	

NOTES:

1. If VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

Г

	A DCON0	Address 03D6h	After Reset 00000XXXb	
	Bit Symbol	Bit Name	Function	RV
	CH0	Analog Input Pin Select Bit ^(2, 3)	^{b2 b1 b0} 0 0 0 : AN0 is selected 0 0 1 : AN1 is selected	RV
	- СН1		0 1 0 : AN2 is selected 0 1 1 : AN3 is selected 1 0 0 : AN4 is selected 1 0 1 : AN5 is selected	RV
	- CH2		1 1 0 : ANG is selected 1 1 1 : AN7 is selected	RV
	MD0	A/D Operation Mode Select	b4 b3	RV
	MD1	Bit 0 ⁽³⁾	0 0 : One-shot mode	RV
	TRG	Trigger Select Bit	0 : Softw are trigger	RV
		A/D Conversion Stort Flog	1 : ADTRG trigger 0 : A/D conversion disabled	_
	ADST	A/D Conversion Start Flag	1 : A/D conversion disabled	RV
	CKS0	Frequency Select Bit 0	Refer to NOTE 3 for the ADCON2 Register	RV
 AN0_0 to AN0_ ADGSEL0 bits AN0_7 and AN After rew riting 	0_7, and AN2_ in the ADCOI N2_0 to AN2_ g the MD1 to N	_0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins.	e conversion result will be indeterminate. ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction.	<u>0</u> to
 If the ADCONO AN0_0 to AN0_ ADGSEL0 bits AN0_7 and AN After rew riting)_7, and AN2_ in the ADCOI N2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits c Address	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset	0 to
 If the ADCON0 AN0_0 to AN0_ ADGSEL0 bits AN0_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2 in the ADCOI N2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits c	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction.	
 If the ADCONO ANO_0 to ANO_ ADGSEL0 bits ANO_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2_ in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 Symbol	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits c Address 03D7h Address	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset 00h After Reset	0 to
 If the ADCONO ANO_0 to ANO_ ADGSEL0 bits ANO_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2 in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 Symbol SCAN0	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits c Address 03D7h	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset 00h	
 If the ADCONO ANO_0 to ANO_ ADGSEL0 bits ANO_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2_ in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 Symbol	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits of Address 03D7h Address A/D Sw eep Pin Select Bit	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset 00h <u>After Reset</u> Invalid in one-shot mode	RV RV
 If the ADCONO ANO_0 to ANO_ ADGSEL0 bits ANO_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2 in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 Symbol SCAN0	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits of Address 03D7h Address A/D Sw eep Pin Select Bit	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset 00h After Reset	RW RW RW
 If the ADCONO ANO_0 to ANO_ ADGSEL0 bits ANO_7 and AN After rew riting /D Control Register // b6 b5 b4 b3 b2 b1 b0)_7, and AN2_ in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 Symbol SCAN0 SCAN1	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits of Address 03D7h Address A/D Sw eep Pin Select Bit	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset 00h <u>After Reset</u> Invalid in one-shot mode	RV RV RV
 If the ADCON0 AN0_0 to AN0_ ADGSEL0 bits AN0_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2_ in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 SCAN0 SCAN1 MD2	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits of Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset 00h After Reset Invalid in one-shot mode Set to "0" w hen one-shot mode is selected 0 : 8-bit mode	RVM RVM RVM RVM
 If the ADCON0 AN0_0 to AN0_ ADGSEL0 bits AN0_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2_ in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 SCAN0 SCAN1 MD2 BITS	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits c Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit	ame w ay as AN0 to AN7. Use the ADGSEL1 to in. How ever, if VCC2 < VCC1, do not use AN0_ over again using another instruction. After Reset 00h After Reset Invalid in one-shot mode Set to "0" w hen one-shot mode is selected 0 : 8-bit mode 1 : 10-bit mode	RW RW RW RW RW
 If the ADCONO ANO_0 to ANO_ ADGSEL0 bits ANO_7 and AN After rew riting /D Control Register /b6 b5 b4 b3 b2 b1 b0)_7, and AN2_ in the ADCOI V2_0 to AN2_ g the MD1 to M er 1 ⁽¹⁾ Symbol ADCON1 SCAN0 SCAN1 MD2 BITS CKS1	0 to AN2_7 can be used in the sa N2 register to select the desired p 7 as analog input pins. //D0 bits, set the CH2 to CH0 bits of Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit Frequency Select Bit 1	After Reset 00h After Reset 00h After Reset 1valid in one-shot mode Set to "0" w hen one-shot mode is selected 0 : 8-bit mode 1 : 10-bit mode Refer to NOTE 3 for the ADCON2 Register	RW

Figure 18.5 ADCON0 and ADCON1 Registers (One-shot Mode)

18.1.2 Repeat Mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 18.3 shows the Repeat Mode Specifications. Figure 18.6 shows the ADCON0 and ADCON1 Registers (Repeat Mode).

Table 18.3	Repeat Mode Specifications
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Item	Specification
Function	The CH2 to CH0 bits in the ADCON0 register, the ADGSEL1 to ADGSEL0 bits in the ADCON2 register and the OPA1 to OPA0 bits in the ADCON1 register select a pin. Analog voltage applied to this pin is repeatedly converted to a digital code.
A/D Conversion Start Condition	 When the TRG bit in the ADCON0 register is "0" (software trigger) The ADST bit in the ADCON0 register is set to "1" (A/D conversion starts) When the TRG bit is "1" (ADTRG trigger) Input on the ADTRG pin changes state from high to low after the ADST bit is set to "1" (A/D conversion starts)
A/D Conversion Stop Condition	Set the ADST bit to "0" (A/D conversion halted)
Interrupt Request Generation timing	None generated
Analog Input Pin ⁽¹⁾	Select one pin from AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0 to ANEX1
Reading of Result of A/D Converter	Read one of the AD0 to AD7 registers that corresponds to the selected pin

NOTES:

1. If VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

07 b6 b5 b4 b		7			
ЦЦЦ		Symbol	Address	After Reset	
		ADCON0	03D6h	00000XXXb	
		Bit Symbol	Bit Name	Function	R
			Analog Input Pin Select Bit ^(2, 3)		
		— СНО		0 0 0 : AN0 is selected 0 0 1 : AN1 is selected	R
			-	0 1 0 : AN2 is selected	
		CLI		0 1 1 : AN3 is selected	R
		CH1		1 0 0 : AN4 is selected	
			4	1 0 1 : AN5 is selected	_
		CH2		1 1 0 : AN6 is selected	B
				1 1 1 : AN7 is selected	
		MD0	A/D Operation Mode Select	b4 b3	R
$ \perp$		MD1	Bit 0 ⁽³⁾	0 1 : Repeat mode	R
			Trigger Select Bit	0 : Softw are trigger	
		TRG		1 : ADTRG trigger	R
		1.507	A/D Conversion Start Flag	0 : A/D conversion disabled	+
		ADST		1 : A/D conversion started	F
2. ANO ADO ANO	0_0 to Al SEL0 bi 0_7 and J	N0_7, and AN2_ its in the ADCON AN2_0 to AN2_7	0 to AN2_7 can be used in the sa I2 register to select the desired pi 7 as analog input pins.	Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. Ime w ay as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_t ver again using another instruction.	
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ its in the ADCON AN2_0 to AN2_7 ing the MD1 to M ster 1 ⁽¹⁾	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins.	Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime way as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0 ver again using another instruction.	
1. If the 2. ANO ADG ANO 3. Afte	0_0 to Al DSEL0 bi 0_7 and 2 or rew riti	N0 register is re N0_7, and AN2_ its in the ADCON AN2_0 to AN2_7 ing the MD1 to M ster 1 ⁽¹⁾ Symbol	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address	Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime way as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0 ver again using another instruction.	
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ its in the ADCON AN2_0 to AN2_7 ing the MD1 to M ster 1 ⁽¹⁾	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o	Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime way as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0 ver again using another instruction.	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 Symbol	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address	Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. Ime w ay as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0 ver again using another instruction. After Reset 00h After Reset	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h	Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. Ime w ay as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0 ver again using another instruction.	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 Symbol	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit	Refer to NOTE 3 for the ADCON2 Register Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime w ay as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_t	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 Symbol SCAN0	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1	Refer to NOTE 3 for the ADCON2 Register Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime way as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 Symbol SCAN0 SCAN1	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit	Refer to NOTE 3 for the ADCON2 Register Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime w ay as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_t	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCOM AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 Symbol SCAN0 SCAN1 MD2	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1	Refer to NOTE 3 for the ADCON2 Register Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime way as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 SCAN0 SCAN1 MD2 BITS	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit	Refer to NOTE 3 for the ADCON2 Register Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime way as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 SCAN0 SCAN1 MD2 BITS CKS1	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit Frequency Select Bit 1	Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. me way as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0	0 to
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 SCAN0 SCAN0 SCAN1 MD2 BITS CKS1 VCUT	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit Frequency Select Bit 1 Vref Connect Bit ⁽²⁾ External Op-Amp Connection	Refer to NOTE 3 for the ADCON2 Register Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. ime w ay as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0	R 0 to R R R R R R R R R
 If the ANO ADG ANO 3. Afte 	0_0 to Al SSEL0 bi 0_7 and <i>b</i> or rew riti	N0 register is re N0_7, and AN2_ ts in the ADCON AN2_0 to AN2_1 ing the MD1 to M ster 1 ⁽¹⁾ Symbol ADCON1 SCAN0 SCAN0 SCAN1 MD2 BITS CKS1 VCUT	w ritten during A/D conversion, th 0 to AN2_7 can be used in the sa 12 register to select the desired pi 7 as analog input pins. ID0 bits, set the CH2 to CH0 bits o Address 03D7h Address A/D Sw eep Pin Select Bit A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit Frequency Select Bit 1 Vref Connect Bit ⁽²⁾ External Op-Amp Connection	Refer to NOTE 3 for the ADCON2 Register Refer to NOTE 3 for the ADCON2 Register e conversion result will be indeterminate. Ime w ay as AN0 to AN7. Use the ADGSEL1 to n. How ever, if VCC2 < VCC1, do not use AN0_0	0 to

Figure 18.6 ADCON0 and ADCON1 Registers (Repeat Mode)

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18.1.3 Single Sweep Mode

In single sweep mode, analog voltage that is applied to selected pins is converted one-by-one to a digital code. Table 18.4 shows the Single Sweep Mode Specifications. Figure 18.7 shows the ADCON0 Register and ADCON1 Register (Single Sweep Mode).

Table 10.4 Single Sweep Mode Specifications	Table 18.4	Single Sweep Mode Specifications
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Item	Specification
Function	The SCAN1 to SCAN0 bits in the ADCON1 register and the ADGSEL1 to ADGSEL0 bits in the ADCON2 register select pins. Analog voltage applied to this pins is converted one-by-one to a digital code.
A/D Conversion Start Condition	 When the TRG bit in the ADCON0 register is "0" (software trigger) The ADST bit in the ADCON0 register is set to "1" (A/D conversion starts) When the TRG bit is "1" (ADTRG trigger) Input on the ADTRG pin changes state from high to low after the ADST bit is set to "1" (A/D conversion starts)
A/D Conversion Stop Condition	 Completion of A/D conversion (If a software trigger is selected, the ADST bit is cleared to "0" (A/D conversion halted)) Set the ADST bit to "0"
Interrupt Request Generation timing	Completion of A/D conversion
Analog Input Pin	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), AN0 to AN7 (8 pin) ⁽¹⁾
Reading of Result of A/D Converter	Read one of the AD0 to AD7 registers that corresponds to the selected pin

NOTES:

1. AN0_0 to AN0_7, and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. However, if VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

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Symbol			
,	Address	After Reset	
ADCON0	03D6h	00000XXXb	
Bit Symbol	Bit Name	Function	RV
CH0	Analog Input Pin Select Bit	Invalid in single sw eep mode	RV
CH1 CH2	4		RV RV
	A/D Operation Mode Select	b4 b3	RV
MD1	Bit 0	1 0 : Single sweep mode	RV
	Trigger Select Bit	0 : Softw are trigger	
TRG		1 : ADTRG trigger	RV
ADST	A/D Conversion Start Flag	0 : A/D conversion disabled	RV
 ADST		1 : A/D conversion started	
CKS0	Frequency Select Bit 0	Refer to NOTE 3 for the ADCON2 Register	RV
Symbol ADCON1	Address 03D7h	After Reset 00h	
(Address	After Reset	RW
Symbol	A/D Sw eep Pin Select Bit ⁽²⁾	When single sw eep mode is selected	
SCA NO		b1 b0	RW
		0 0 : AN0 to AN1 (2 pins)	
		· · · /	
SCAN1		1 1 : AN0 to AN7 (8 pins)	RV
MD2	A/D Operation Mode Select Bit 1	Set to "0" when single sweep mode is selected	RW
впс	8/10-Bit Mode Select Bit	0 : 8-bit mode 1 : 10-bit mode	RV
- CKS1	Frequency Select Bit 1	Refer to NOTE 3 for the ADCON2 Register	RV
VCUT	Vref Connect Bit (3)	1 : Vref connected	RW
OPA0	External Op-Amp Connection Mode Bit	^{b7 b6} 0 0 : ANEX0 and ANEX1 are not used	RV
- OPA1		0 1 : Do not set to this value 1 0 : Do not set to this value 1 1 : External op-amp connection mode	RV
BITS CKS1 VCUT OPA0	8/10-Bit Mode Select Bit Frequency Select Bit 1 Vref Connect Bit ⁽³⁾ External Op-Amp Connection	0 1 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN5 (6 pins) 1 1 : AN0 to AN7 (8 pins) Set to "0" w hen single sw eep mode is selected 0 : 8-bit mode 1 : 10-bit mode Refer to NOTE 3 for the ADCON2 Register 1 : Vref connected ^{b7 b6} 0 0 : ANEX0 and ANEX1 are not used 0 1 : Do not set to this value 1 0 : Do not set to this value	F F F

Figure 18.7 ADCON0 Register and ADCON1 Register (Single Sweep Mode)

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18.1.4 Repeat Sweep Mode 0

In repeat sweep mode 0, analog voltage applied to selected pins is repeatedly converted to a digital code. Table 18.5 shows the Repeat Sweep Mode 0 Specifications. Figure 18.8 shows the ADCON0 Register and ADCON1 Registers (Repeat Sweep Mode 0).

Table 18.5Repeat Sweep Mode 0 Specifications
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Item	Specification
Function	The SCAN1 to SCAN0 bits in the ADCON1 register and the ADGSEL1 to ADGSEL0 bits in the ADCON2 register select pins. Analog voltage applied to the pins is repeatedly converted to a digital code.
A/D Conversion Start Condition	 When the TRG bit in the ADCON0 register is "0" (software trigger) The ADST bit in the ADCON0 register is set to "1" (A/D conversion starts) When the TRG bit is "1" (ADTRG trigger) Input on the ADTRG pin changes state from high to low after the ADST bit is set to "1" (A/D conversion starts)
A/D Conversion Stop Condition	Set the ADST bit to "0" (A/D conversion halted)
Interrupt Request Generation timing	None generated
Analog Input Pin	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), AN0 to AN7 (8 pin) ⁽¹⁾
Reading of Result of A/D Converter	Read one of the AD0 to AD7 registers that corresponds to the selected pin
Generation timing Analog Input Pin Reading of Result of A/D	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins AN0 to AN7 (8 pin) ⁽¹⁾

NOTES:

1. AN0_0 to AN0_7, and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. However, if VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

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1	Symbol	Address	After Reset	
	A DCON0	03D6h	00000XXXb	
	Bit Symbol	Bit Name	Function	R\
	CH0	Analog Input Pin Select Bit	Invalid in repeat sweep mode 0	R\
	CH1			R\
	CH2			R١
	MD0	A/D Operation Mode Select Bit 0	^{b4 b3} 1 1 : Repeat sw eep mode 0 or Repeat sw eep mode 1	R
	MD1			R\
	TRG	Trigger Select Bit	0 : Softw are trigger 1 : ADTRG trigger	R\
	ADST	A/D Conversion Start Flag	0 : A/D conversion disabled 1 : A/D conversion started	R\
	CKS0	Frequency Select Bit 0	Refer to NOTE 3 for the ADCON2 Register	R١
		03D7h	00h	
	ADCON1	03D7h	00h	
	ADCON1 Symbol SCAN0	03D7h Address A/D Sw eep Pin Select Bit ⁽²⁾	After Reset When repeat sw eep mode 0 is selected b1 b0	RV RV
	Symbol	Address	After Reset When repeat sw eep mode 0 is selected b1 b0 0 0 : AN0 to AN1 (2 pins) 0 1 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN5 (6 pins)	RV
	Symbol SCA N0	Address	After Reset When repeat sw eep mode 0 is selected b1 b0 0 0 : AN0 to AN1 (2 pins) 0 1 : AN0 to AN3 (4 pins)	RV
	Symbol SCA N0 SCA N1	Address A/D Sw eep Pin Select Bit ⁽²⁾	After Reset When repeat sw eep mode 0 is selected b1 b0 0 0 : AN0 to AN1 (2 pins) 0 1 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN3 (6 pins) 1 1 : AN0 to AN7 (8 pins) Set to "0" w hen repeat sw eep mode 0 is	RV RV RV
	Symbol SCA N0 SCA N1 MD2	Address A/D Sw eep Pin Select Bit ⁽²⁾ A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit Frequency Select Bit 1	After Reset When repeat sw eep mode 0 is selected b1 b0 0 0 : AN0 to AN1 (2 pins) 0 1 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN5 (6 pins) 1 1 : AN0 to AN7 (8 pins) Set to "0" w hen repeat sw eep mode 0 is selected 0 : 8-bit mode	
	Symbol SCA N0 SCA N1 MD2 BITS	Address A/D Sw eep Pin Select Bit ⁽²⁾ A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit	After Reset When repeat sw eep mode 0 is selected ^{b1 b0} 0 0 : AN0 to AN1 (2 pins) 0 1 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN3 (6 pins) 1 1 : AN0 to AN5 (6 pins) 1 1 : AN0 to AN7 (8 pins) Set to "0" w hen repeat sw eep mode 0 is selected 0 : 8-bit mode 1 : 10-bit mode	RV RV RV RV RV
	Symbol SCA N0 SCA N1 MD2 BITS CKS1	Address A/D Sw eep Pin Select Bit ⁽²⁾ A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit Frequency Select Bit 1	After Reset When repeat sw eep mode 0 is selected ^{b1 b0} 0 0 : AN0 to AN1 (2 pins) 0 1 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN3 (6 pins) 1 1 : AN0 to AN5 (6 pins) 1 1 : AN0 to AN7 (8 pins) Set to "0" w hen repeat sw eep mode 0 is selected 0 : 8-bit mode 1 : 10-bit mode Refer to NOTE 3 for the ADCON2 Register 1 : Vref connected ^{b7 b6} 0 0 : ANEX0 and ANEX1 are not used	RV RV RV RV
	Symbol SCA N0 SCA N1 MD2 BITS CKS1 VCUT	Address A/D Sw eep Pin Select Bit ⁽²⁾ A/D Operation Mode Select Bit 1 8/10-Bit Mode Select Bit Frequency Select Bit 1 Vref Connect Bit ⁽³⁾ External Op-Amp Connection	After Reset When repeat sw eep mode 0 is selected ^{b1 b0} 0 0 : AN0 to AN1 (2 pins) 0 1 : AN0 to AN3 (4 pins) 1 0 : AN0 to AN3 (6 pins) 1 1 : AN0 to AN5 (6 pins) 1 1 : AN0 to AN7 (8 pins) Set to "0" w hen repeat sw eep mode 0 is selected 0 : 8-bit mode 1 : 10-bit mode Refer to NOTE 3 for the ADCON2 Register 1 : Vref connected ^{b7 b6}	RI RI RI RI

Figure 18.8 ADCON0 Register and ADCON1 Registers (Repeat Sweep Mode 0)

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18.1.5 **Repeat Sweep Mode 1**

In repeat sweep mode 1, analog voltage selectively applied to all pins is repeatedly converted to a digital code. Table 18.6 shows the Repeat Sweep Mode 1 Specifications. Figure 18.9 shows the ADCON0 Register and ADCON1 Register (Repeat Sweep Mode 1).

Item	Specification		
Function	The input voltages on all pins selected by the ADGSEL1 to ADGSEL0 bits in the ADCON2 register are A/D converted repeatedly, with priority given to pins selected by the SCAN1 to SCAN0 bits in the ADCON1 register and ADGSEL1 to ADGSEL0 bits. Example : If AN0 selected, input voltages are A/D converted in order of AN0→AN1→AN0→AN2→AN0→AN3, and so on.		
A/D Conversion Start Condition	 When the TRG bit in the ADCON0 register is "0" (software trigger) The ADST bit in the ADCON0 register is set to "1" (A/D conversion starts) When the TRG bit is "1" (ADTRG trigger) Input on the ADTRG pin changes state from high to low after the ADST bit is set to "1" (A/D conversion starts) 		
A/D Conversion Stop Condition	Set the ADST bit to "0" (A/D conversion halted)		
Interrupt Request Generation timing	None generated		
Analog Input Pins to be Given Priority when A/D Converted	Select from AN0 (1 pin), AN0 to AN1 (2 pins), AN0 to AN2 (3 pins), AN0 to AN3 (4 pins) ⁽¹⁾		
Reading of Result of A/D Converter	Read one of the AD0 to AD7 registers that corresponds to the selected pin		

Table 18.6	Repeat Sweep	Mode 1	Specifications
------------	--------------	--------	----------------

NOTES:

1. AN0_0 to AN0_7, and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. However, if VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

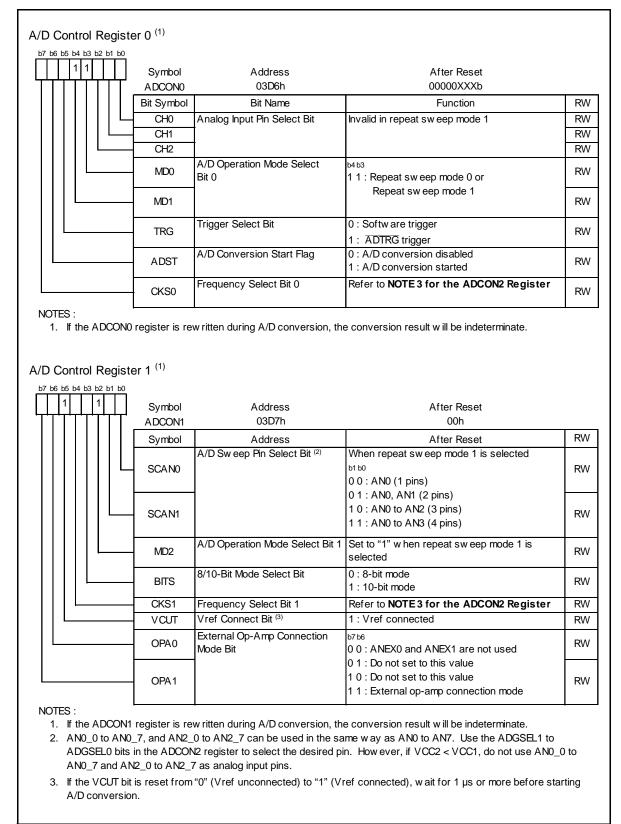


Figure 18.9 ADCON0 Register and ADCON1 Register (Repeat Sweep Mode 1)

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18.2 Function

18.2.1 Resolution Select Function

The desired resolution can be selected using the BITS bit in the ADCON1 register. If the BITS bit is set to "1" (10-bit conversion accuracy), the A/D conversion result is stored in the bit 0 to bit 9 in the ADi register (i = 0 to 7). If the BITS bit is set to "0" (8-bit conversion accuracy), the A/D conversion result is stored in the bit 0 to bit 7 in the ADi register.

18.2.2 Sample and Hold

If the SMP bit in the ADCON2 register is set to "1" (with sample-and-hold), the conversion speed per pin is increased to 28 ϕ AD cycles for 8-bit resolution or 33 ϕ AD cycles for 10-bit resolution. Sample and Hold is effective in all operating modes. Select whether or not to use the Sample and Hold function before starting A/D conversion.

18.2.3 Extended Analog Input Pins

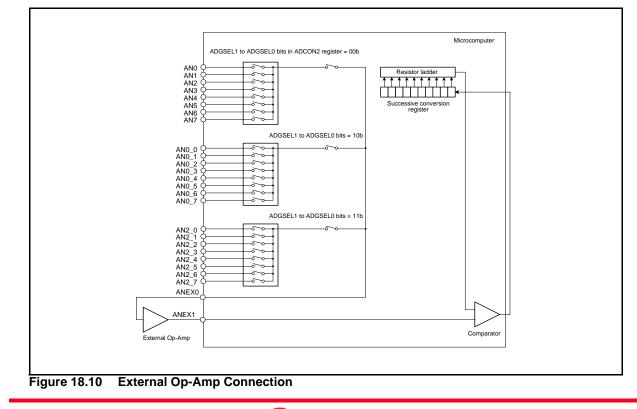
In one-shot and repeat modes, the ANEX0 and ANEX1 pins can be used as analog input pins. Use the OPA1 to OPA0 bits in the ADCON1 register to select whether or not use ANEX0 and ANEX1.

The A/D conversion results of ANEX0 and ANEX1 inputs are stored in the AD0 and AD1 registers, respectively.

18.2.4 18.2.4 External Operation Amplifier (Op-Amp) Connection Mode

Multiple analog inputs can be amplified using a single external op-amp via the ANEX0 and ANEX1 pins. Set the OPA1 to OPA0 bits in the ADCON1 register to "11b" (external op-amp connection mode). The inputs from ANi (i = 0 to 7) (1) are output from the ANEX0 pin. Amplify this output with an external op-amp before sending it back to the ANEX1 pin. The A/D conversion result is stored in the corresponding ADi register. The A/D conversion speed depends on the response characteristics of the external op-amp. Figure 18.10 shows an example of How to Connect the Pins in External Op-Amp.

1. AN0_i and AN2_i can be used the same as ANi. However, if VCC2 < VCC1, do not use AN0_i and AN2_i as analog input pins.



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18.2.5 18.2.5 Current Consumption Reducing Function

When not using the A/D converter, its resistor ladder and reference voltage input pin (VREF) can be separated using the VCUT bit in the ADCON1 register. When separated, no current will flow from the VREF pin into the resistor ladder, helping to reduce the power consumption of the chip.

To use the A/D converter, set the VCUT bit to "1" (Vref connected) and then set the ADST bit in the ADCON0 register to "1" (A/D conversion start). The VCUT and ADST bits cannot be set to "1" at the same time. Nor can the VCUT bit be set to "0" (Vref unconnected) during A/D conversion.

Note that this does not affect VREF for the D/A converter (irrelevant).

18.2.6 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 18.11 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

VC is generally VC= VIN
$$\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$$

And when t = T, VC = VIN $-\frac{X}{Y}$ VIN = VIN $\left(1 - \frac{X}{Y}\right)$
 $e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$
 $-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$
Hence, R0= $-\frac{T}{C \bullet \ln\frac{X}{Y}} - R$

Figure 18.11 shows Analog Input Pin and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN-(0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB.

When $f(\phi AD) = 10$ MHz, T = 0.3 µs in the A/D conversion mode with sample & hold. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.3 µs, R = 7.8 kΩ, C = 1.5 pF, X = 0.1, and Y = 1024. Hence,
R0=
$$-\frac{0.3 \times 10^{-6}}{1.5 \times 10^{-12} \cdot \ln \frac{0.1}{1024}} - 7.8 \times 10^3 = 13.9 \times 10^3$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 13.9 k Ω maximum.

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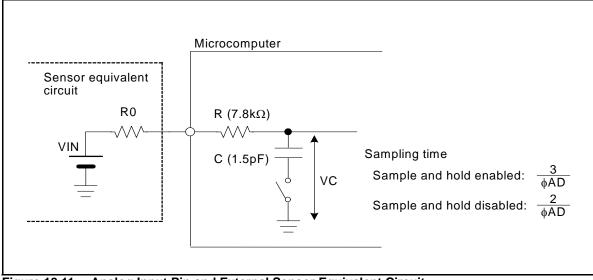


Figure 18.11 Analog Input Pin and External Sensor Equivalent Circuit

19. D/A Converter

This is an 8-bit, R-2R type D/A converter. These are two independent D/A converters.

D/A conversion is performed by writing to the DAi register (i = 0 to 1). To output the result of conversion, set the DAiE bit in the DACON register to "1" (output enabled). Before D/A conversion can be used, the corresponding port direction bit must be cleared to "0" (input mode). Setting the DAiE bit to "1" removes a pull-up from the corresponding port.

Output analog voltage (V) is determined by a set value (n : decimal) in the DAi register.

V = VREF X n / 256 (n = 0 to 255)

VREF : reference voltage

Table 19.1 lists the D/A Converter Performance. Figure 19.1 shows the D/A Converter Block Diagram. Figure 19.2 shows the D/A converter related registers. Figure 19.3 shows the D/A Converter Equivalent Circuit.

Table 19.1 D/A Converter Performance

Item	Performance
D/A Conversion Method	R-2R method
Resolution	8 bits
Analog Output Pin	2 channels (DA0 and DA1)

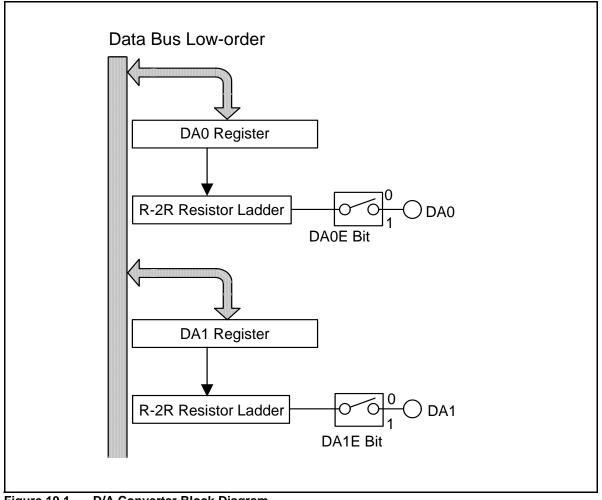
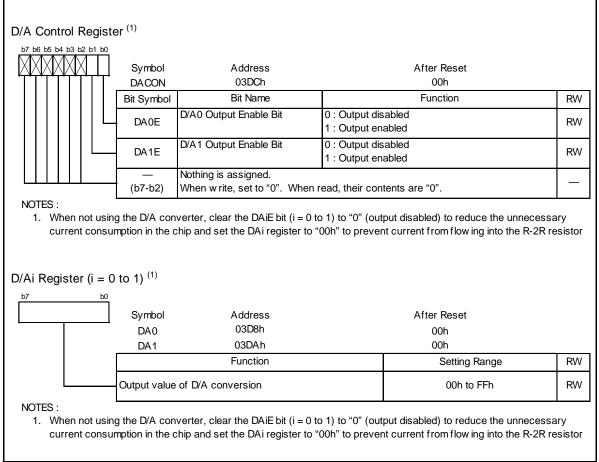
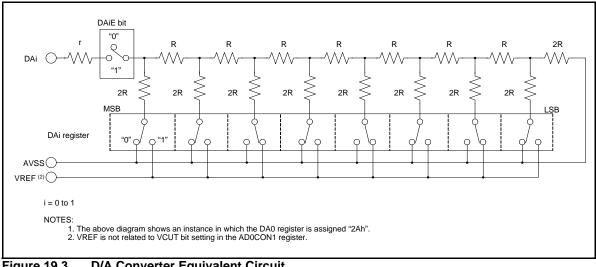


Figure 19.1 D/A Converter Block Diagram

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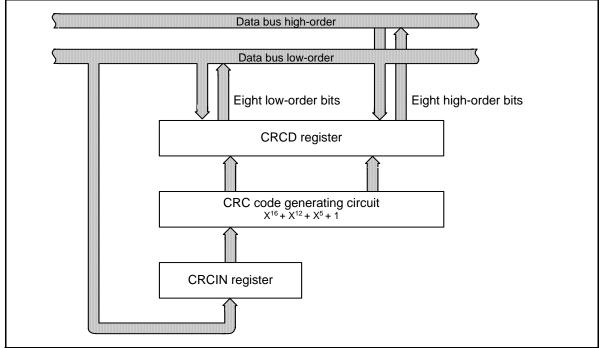
20. CRC Calculation

The Cyclic Redundancy Check (CRC) operation detects an error in data blocks. The microcomputer uses a generator polynomial of CRC_CCITT $(X^{16} + X^{12} + X^5 + 1)$ to generate CRC code.

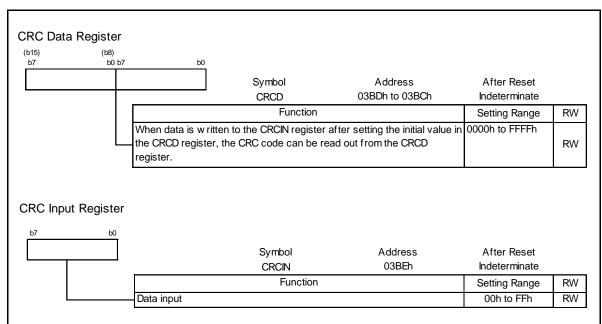
The CRC code consists of 16 bits which are generated for each data block in given length, separated in 8 bit units. After the initial value is set in the CRCD register, the CRC code is set in that register each time one byte of data is written to the CRCIN register. CRC code generation for one-byte data is finished in two cycles.

Figure 20.1 shows the CRC Circuit Block Diagram. Figure 20.2 shows the CRC-related Registers.

Figure 20.3 shows the Calculation Example using the CRC Operation.









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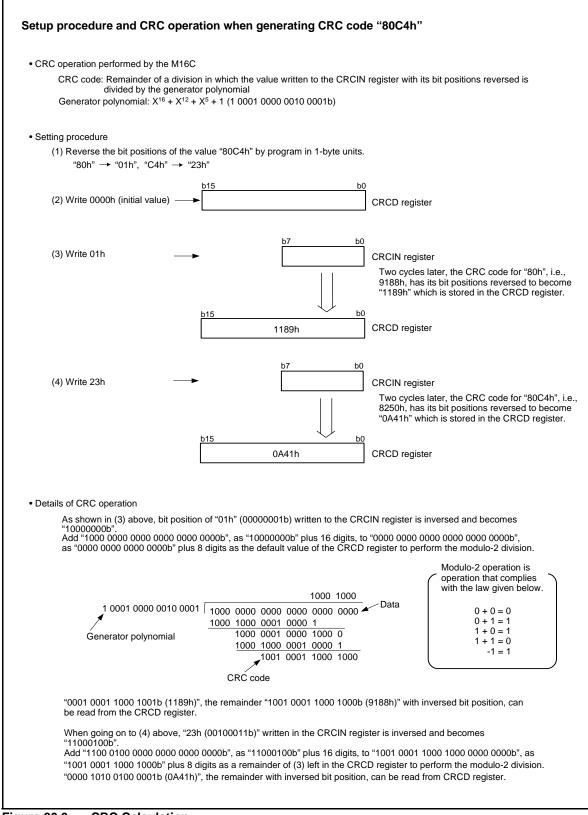


Figure 20.3 CRC Calculation

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21. Programmable I/O Ports

Note

There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in the M16C/62P (80-pin version) and the M16C/62PT (80-pin version). Set the direction bits in these ports to "1" (output mode), and set the output data to "0" ("L") using the program.

Moreover, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0 and P14_1 pins do not exist. Therefore, P11 to P13, PC14 and PUR13 register do not exist.

The programmable input/output ports (hereafter referred to simply as I/O ports) consist of 113 lines P0 to P14 for the 128-pin version, 87 lines P0 to P10 for the 100-pin version, or 70 lines P0 to P10 for the 80-pin version. Each port can be set for input or output every line by using a direction register, and can also be chosen to be or not be pulled high every 4 lines. P8_5 is an input-only port and does not have a pull-up resistor. Port P8_5 shares the pin with $\overline{\text{NMI}}$, so that the $\overline{\text{NMI}}$ input level can be read from the P8 register P8_5 bit.

Table 21.1 lists the Number of Pins of the Programmable I/O Ports of Each Package. Figure 21.1 to Figure 21.5 show the I/O ports. Figure 21.6 shows the I/O Pins.

Each pin functions as an I/O port, a peripheral function input/output, or a bus control pin.

For details on how to set peripheral functions, refer to each functional description in this manual. If any pin is used as a peripheral function input or D/A converter output pin, set the direction bit for that pin to "0" (input mode). Any pin used as an output pin for peripheral functions other than the D/A converter is directed for output no matter how the corresponding direction bit is set.

When using any pin as a bus control pin, refer to 8.2 Bus Control.

P0 to P5, P12, and P13 are capable of VCC2-level input/output; P6 to P11 and P14 are capable of VCC1- level input/ output.

	128-pin Version	100-pin Version	80-pin version ⁽¹⁾
Programmable	P0_0 to P0_7,	P0_0 to P0_7,	P0_0 to P0_7,
I/O Ports	P1_0 to P1_7,	P1_0 to P1_7,	P2_0 to P2_7,
	P2_0 to P2_7,	P2_0 to P2_7,	P3_0 to P3_7,
	P3_0 to P3_7,	P3_0 to P3_7,	P4_0 to P4_3,
	P4_0 to P4_7,	P4_0 to P4_7,	P5_0 to P5_7,
	P5_0 to P5_7,	P5_0 to P5_7,	P6_0 to P6_7,
	P6_0 to P6_7,	P6_0 to P6_7,	P7_0, P7_1, P7_6, P7_7,
	P7_0 to P7_7,	P7_0 to P7_7,	P8_0 to P8_4, P8_6, P8_7
	P8_0 to P8_4, P8_6, P8_7	P8_0 to P8_4, P8_6, P8_7	(P8_5 is an input port),
	(P8_5 is an input port),	(P8_5 is an input port),	P9_0, P9_2 to P9_7,
	P9_0 to P9_7,	P9_0 to P9_7,	P10_0 to P10_7,
	P10_0 to P10_7,	P10_0 to P10_7,	
	P11_0 to P11_7,		
	P12_0 to P12_7,		
	P13_0 to P13_7,		
	P14_0, P14_1		
Total	113 pins	87 pins	70 pins

Table 21.1 Number of Pins of the Programmable I/O Ports of Each Package

NOTES:

1. There is no connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

21.1 Port Pi Direction Register (PDi Register, i = 0 to 13)

Figure 21.7 shows the PDi Registers.

This register selects whether the I/O port is to be used for input or output. The bits in this register correspond one for one to each port.

During memory extension and microprocessor modes, the PDi registers for the pins functioning as bus control pins (A0 to A19, D0 to D15, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{RD}}$, $\overline{\text{WRL}/\text{WR}}$, $\overline{\text{WRH}/\text{BHE}}$, ALE, $\overline{\text{RDY}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$, and BCLK) cannot be modified.

No direction register bit for P8_5 is available.

21.2 Port Pi Register (Pi Register, i = 0 to 13)

Figure 21.8 shows the Pi Registers.

Data input/output to and from external devices are accomplished by reading and writing to the Pi register.

The Pi register consists of a port latch to hold the input/output data and a circuit to read the pin status. For ports set for input mode, the input level of the pin can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register.

For ports set for output mode, the port latch can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register. The data written to the port latch is output from the pin. The bits in the Pi register correspond one for one to each port.

During memory extension and microprocessor modes, the PDi registers for the pins functioning as bus control pins (A0 to A19, D0 to D15, CS0 to CS3, RD, WRL/WR, WRH/BHE, ALE, RDY, HOLD, HLDA, and BCLK) cannot be modified.

21.3 Pull-up Control Register 0 to Pull-up Control Register 3 (PUR0 to PUR3 Registers)

Figure 21.9 and Figure 21.11 shows the PURi Registers.

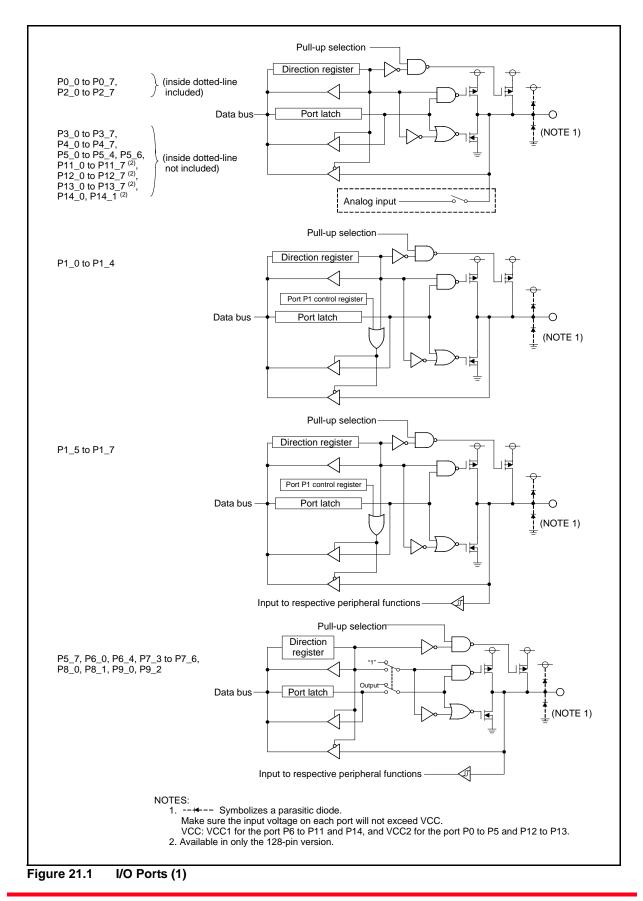
The PUR0 to PUR2 register bits can be used to select whether or not to pull the corresponding port high in 4 bit units. The port chosen to be pulled high has a pull-up resistor connected to it when the direction bit is set for input mode. To use ports P11 to P14, set the PU37 bit in the PUR3 register to "1".

However, the pull-up control register has no effect on P0 to P3, P4_0 to P4_3, and P5 during memory extension and microprocessor modes. Although the register contents can be modified, no pull-up resistors are connected.

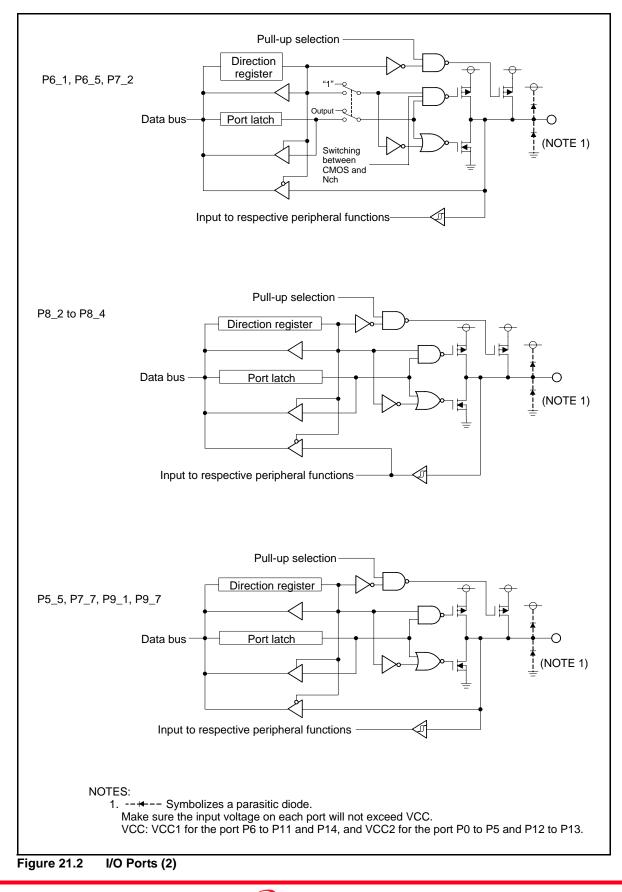
21.4 Port Control Register (PCR Register)

Figure 21.12 shows the PCR Register.

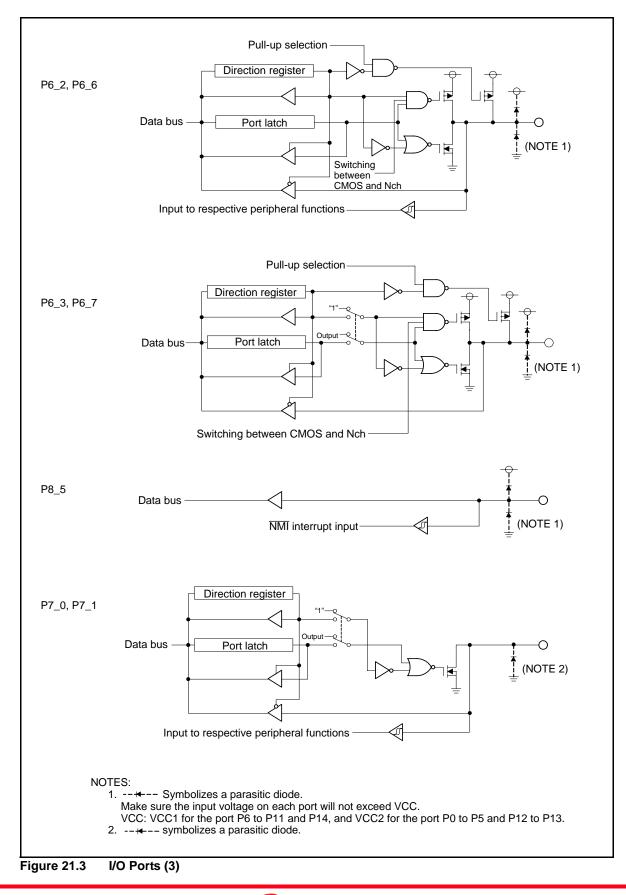
When the P1 register is read after setting the PCR0 bit in the PCR register to "1", the corresponding port latch can be read no matter how the PD1 register is set.



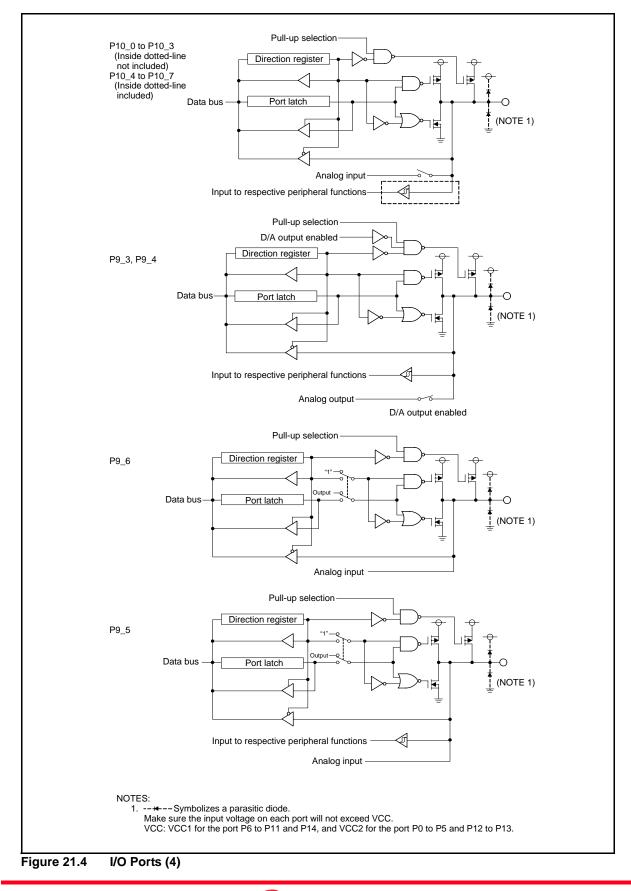
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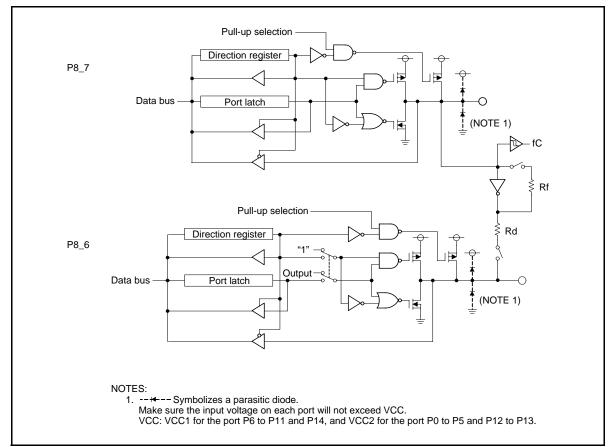
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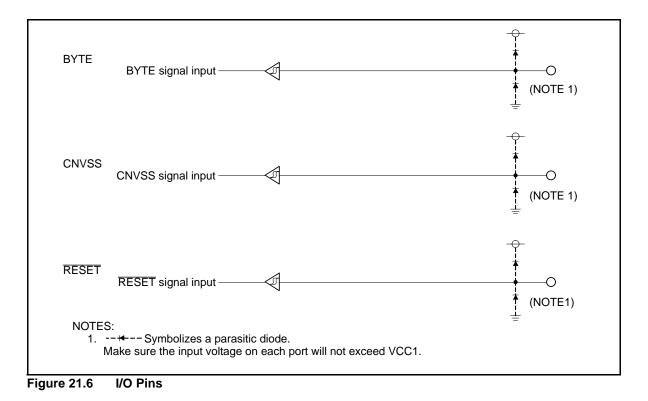
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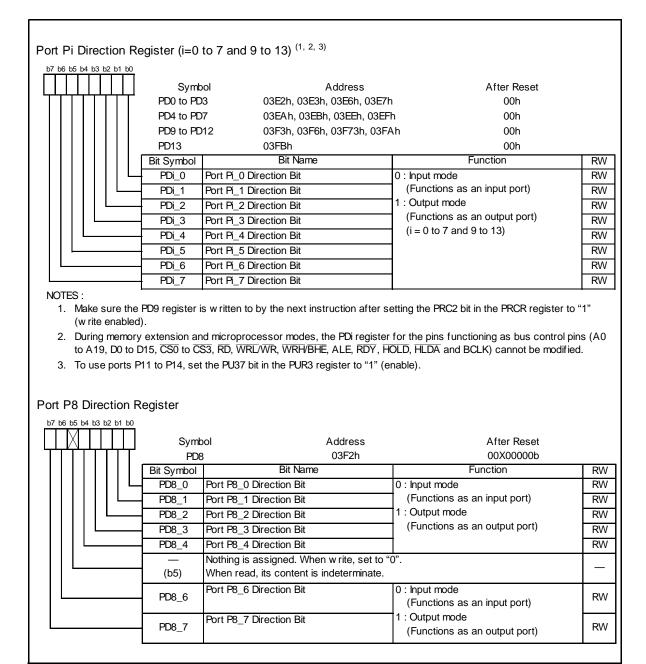


Figure 21.7 PDi Registers

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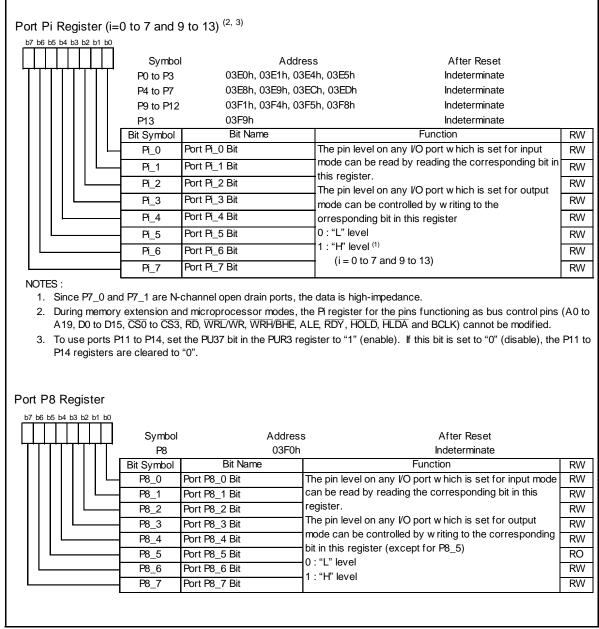
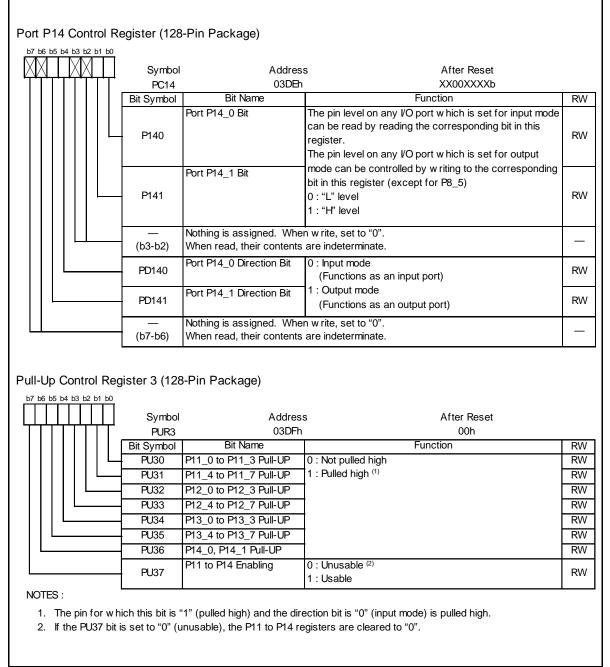
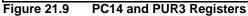


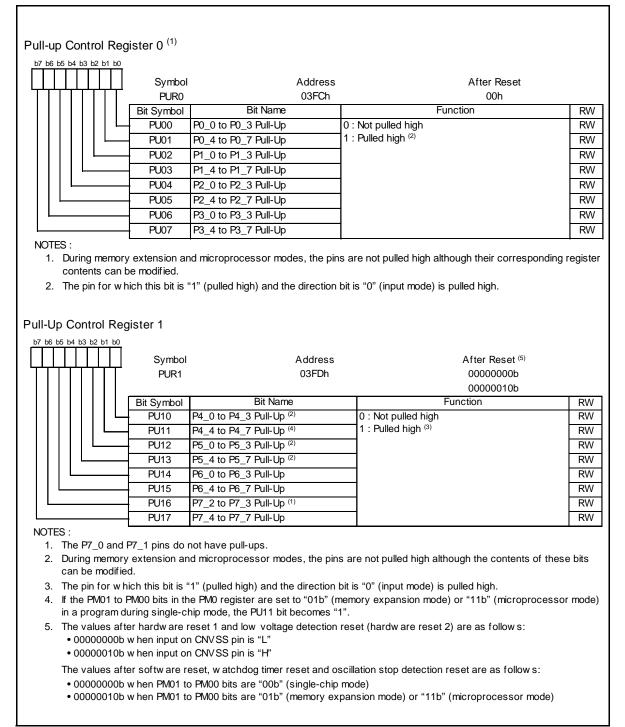
Figure 21.8 Pi Registers

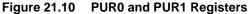
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ЩĶ	Щ		Ц	Symbol	Address	s A	fter Reset
				PUR2 Bit Symbol	03FEh Bit Name	Functio	00h on R
				PU20	P8 0 to P8 3 Pull-Up	0 : Not pulled high	R\
				PU21	P8_4 to P8_7 Pull-Up ⁽²⁾	1 : Pulled high (1)	R
				PU22	P9_0 to P9_3 Pull-Up		R
				PU23	P9_4 to P9_7 Pull-Up		R
				PU24	P10_0 to P10_3 Pull-Up		R
				PU25	P10_4 to P10_7 Pull-Up		R
				 (b7-b6)	Nothing is assigned. When wr When read, their contenta are '		-

Figure 21.11 PUR2 Register

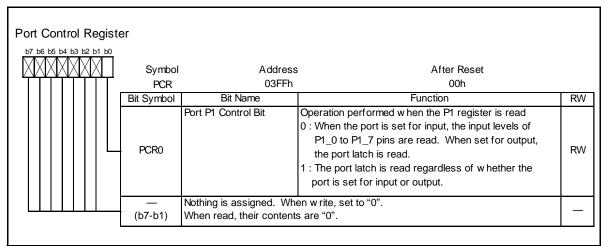


Figure 21.12 PCR Register

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Pin Name	Connection
Ports P0 to P7,	After setting for input mode, connect every pin to VSS via a resistor (pull-
P8_0 to P8_4, P8_6 to P8_7,	down);
P9 to P14	or after setting for output mode, leave these pins open. (1, 2, 3, 5)
XOUT ⁽⁴⁾	Open
NMI	Connect via resistor to VCC1 (pull-up)
AVCC	Connect to VCC1
AVSS, VREF, BYTE	Connect to VSS

Table 21.2 Unassigned Pin Handling in Single-chip Mode

NOTES:

 When setting the port for output mode and leave it open, be aware that the port remains in input mode until it is switched to output mode in a program after reset. For this reason, the voltage level on the pin becomes indeterminate, causing the power supply current to increase while the port remains in input mode.

Furthermore, by considering a possibility that the contents of the direction registers could be changed by noise or noise-induced runaway, it is recommended that the contents of the direction registers be periodically reset in software, for the increased reliability of the program.

- 2. Make sure the unused pins are processed with the shortest possible wiring from the microcomputer pins (within 2 cm).
- 3. When the ports P7_0 and P7_1 are set for output mode, make sure a low-level signal is output from the pins.

The ports P7_0 and P7_1 are N-channel open-drain outputs.

- 4. With external clock input to XIN pin.
- 5. Process the port without a pin in the 80-pin version and the 100-pin version as follows.
 - 80-pin version
 - Set the direction bits in these ports to "1" (output mode), and set the output data to "0" ("L") using the program.

•Ports P11 to P14 do not exist.

100-pin version

•After reset, PU37 bit is "0" (P11 to P14 do not used).

- Do not write "1" to PU37 bit. When read, value of PU37 bit is indeterminate.
- •The port direction bit in the P11 to P14 can be set "0" or "1".

Pin Name	Connection
Ports P0 to P7, P8_0 to P8_4, P8_6 to P8_7, P9 to P14	After setting for input mode, connect every pin to VSS via a resistor (pull- down); or after setting for output mode, leave these pins open. (1, 2, 3, 4, 7)
P4_5/CS1 to P4_7/CS3	Connect to VCC2 via a resistor (pulled high) by setting the corresponding direction bit in the PD4 register for \overline{CSi} (i=1 to 3) to "0" (input mode) and the CSi bit in the CSR register to "0" (chip select disabled).
BHE, ALE, HLDA, XOUT ⁽⁵⁾ , BCLK ⁽⁶⁾	Open
HOLD, RDY	Connect via resistor to VCC2 (pull-up)
NMI (P8_5)	Connect via resistor to VCC1 (pull-up)
AVCC	Connect to VCC1
AVSS, VREF	Connect to VSS

Table 21.3	Unassigned Pin Handling in Memory Expansion Mode and Microprocessor Mode
------------	--

NOTES:

1. When setting the port for output mode and leave it open, be aware that the port remains in input mode until it is switched to output mode in a program after reset. For this reason, the voltage level on the pin becomes indeterminate, causing the power supply current to increase while the port remains in input mode.

Furthermore, by considering a possibility that the contents of the direction registers could be changed by noise or noise-induced runaway, it is recommended that the contents of the direction registers be periodically reset in software, for the increased reliability of the program.

- 2. Make sure the unused pins are processed with the shortest possible wiring from the microcomputer pins (within 2 cm).
- 3. If the CNVSS pin has the VSS level applied to it, these pins are set for input ports until the processor mode is switched over in a program after reset. For this reason, the voltage levels on these pins become indeterminate, causing the power supply current to increase while they remain set for input ports.
- 4. When the ports P7_0 and P7_1 are set for output mode, make sure a low-level signal is output from the pins.

The ports P7_0 and P7_1 are N-channel open-drain outputs.

- 5. With external clock input to XIN pin.
- 6. If the PM07 bit in the PM0 register is set to "1" (BCLK not output), connect this pin to VCC2 via a resistor (pulled high).
- 7. Process the port without a pin in the 100-pin version as follows.
 - •After reset, PU37 bit is "0" (P11 to P14 do not used).
 - Do not write "1" to PU37 bit. When read, value of PU37 bit is indeterminate.
 - •The port direction bit in the P11 to P14 can be set "0" or "1".

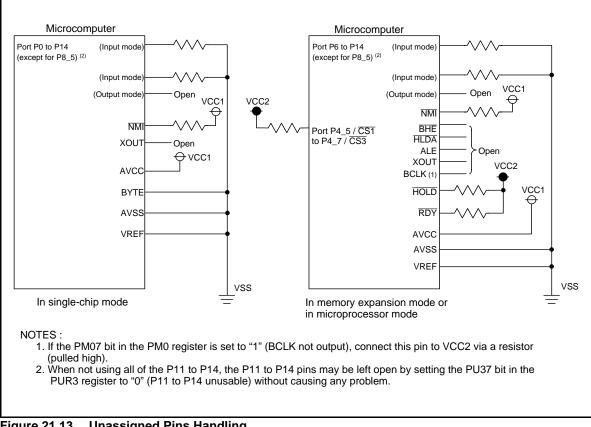


Figure 21.13 Unassigned Pins Handling

22. Flash Memory Version

Aside from the built-in flash memory, the flash memory version microcomputer has the same functions as the masked ROM version.

In the flash memory version, the flash memory can perform in three rewrite modes: CPU rewrite mode, standard serial I/O mode and parallel I/O mode.

Table 22.1 lists specifications of the flash memory version. See **Table 1.1 to Table 1.3 Performance outline of M16C/62PT group** for the items not listed in Table 22.1.

Table 22.1	Flash Memory Version Specifications
------------	-------------------------------------

Item		Specification	
Flash Memory Rewrite Mode		3 modes (CPU rewrite, standard serial I/O, parallel I/O)	
		See Figure 22.1 Flash Memory Block Diagram	
	Boot ROM Area	1 block (4 Kbytes) ⁽¹⁾	
Program Method		In units of word, in units of byte ⁽²⁾	
Erase Method		Collective erase, block erase	
Program and Erase Control Method		Program and erase controlled by software command	
Protect Method		The lock bit protects each block	
Number of Commands		8 commands	
Program and Erase Endurance		100 times, 1,000 times/10,000 times (option) ^(3, 4)	
Data Retention		10 years	
ROM Code Protection	۱	Parallel I/O and standard serial I/O modes are supported	

NOTES:

1. The boot ROM area contains a standard serial I/O mode rewrite control program which is stored in it when shipped from the factory. This area can only be rewritten in parallel input/output mode.

- 2. Can be programmed in byte units in only parallel input/output mode.
- 3. Block 1 and block A are 10,000 times of programming and erasure. All other blocks are 1,000 times of programming and erasure.
- 4. Definition of program and erase endurance

The programming and erasure times are defined to be per-block erasure times. For example, assume a case where a 4-Kbyte block A is programmed in 2,048 operations by writing one word at a time and erased thereafter.

In this case, the block is reckoned as having been programmed and erased once.

If a product is 100 times of programming and erasure, each block in it can be erased up to 100 times. When 10,000 times of programming and erasure, block 1 and block A can each be erased up to 10,000 times. All other blocks can each be erased up to 1,000 times.

Flash Memory Rewrite Mode	CPU rewrite Mode ⁽¹⁾	Standard Serial I/O Mode	Parallel I/O Mode
Function	The User ROM area is rewritten when the CPU executes software commands. EW0 mode: Rewrite in areas other than flash memory ⁽²⁾ EW1 mode: Can be rewritten in the flash memory	The user ROM area is rewritten using a dedicated serial programmer. Standard serial I/O mode 1: Clock synchronous serial I/O Standard serial I/O mode 2: UART	The boot ROM area and user ROM area is rewritten using a dedicated parallel programmer.
Areas which can be Rewritten	User ROM area	User ROM area	User ROM area Boot ROM area
Operating Mode	Single-chip mode Memory expansion mode (EW0 mode) Boot mode (EW0 mode)	Boot mode	Parallel I/O mode
ROM Programmer	None	Serial programmer	Parallel programmer

Table 22.2Flash Memory Rewrite Modes Overview

NOTES:

- The PM13 bit remains set to "1" while the FMR01 bit in the FMR0 register = 1 (CPU rewrite mode enabled). The PM13 bit is reverted to its original value by clearing the FMR01 bit to "0" (CPU rewrite mode disabled). However, if the PM13 bit is changed during CPU rewrite mode, its changed value is not reflected until after the FMR01 bit is cleared to "0".
- 2. When in CPU rewrite mode, the PM10 and PM13 bits in the PM1 register are set to "1". The rewrite control program can only be executed in the internal RAM or in an external area that is enabled for use when the PM13 bit = 1. When the PM13 bit = 0 and the flash memory is used in 4-Mbyte mode, the extended accessible area (40000h to BFFFFh) cannot be used.

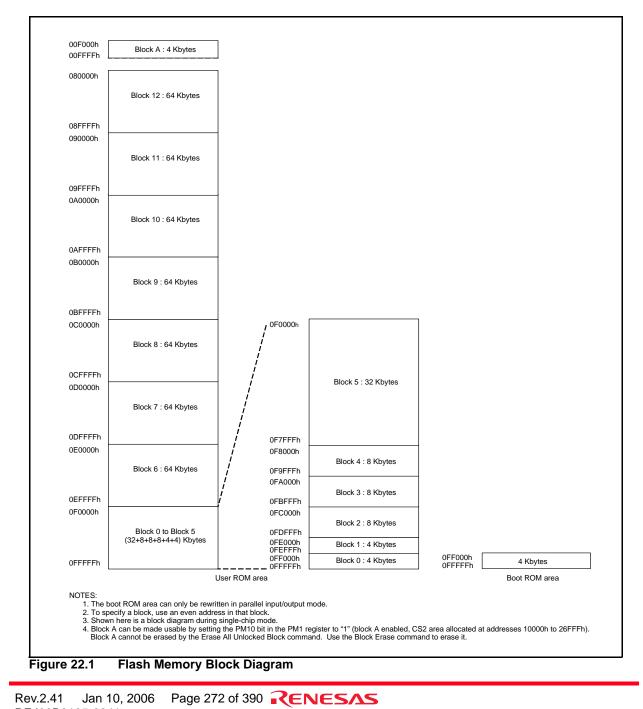
22.1 Memory Map

The flash memory contains the user ROM area and the boot ROM area. The user ROM area has space to store the microcomputer operating program in single-chip mode or memory expansion mode and a separate 4-Kbyte space as the block A. Figure 22.1 shows a Flash Memory Block Diagram.

The user ROM area is divided into several blocks, each of which can be protected (locked) from program or erase. The user ROM area can be rewritten in CPU rewrite, standard serial I/O and parallel I/O modes.

Block A is enabled for use by setting the PM10 bit in the PM1 register to "1" (block A enabled, CS2 area at addresses 10000h to 26FFFh).

The boot ROM area is located at the same addresses as the user ROM area. It can only be rewritten in parallel I/O mode (refer to **22.1.1 Boot Mode**). A program in the boot ROM area is executed after a hardware reset occurs while an "H" signal is applied to the CNVSS and P5_0 pins and an "L" signal is applied to the P5_5 pin (refer to **22.1.1 Boot Mode**). A program in the user ROM area is executed after a hardware reset occurs while an "L" signal is applied to the CNVSS pin. However, the boot ROM area cannot be read.



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22.1.1 Boot Mode

The microcomputer enters boot mode when a hardware reset occurs while an "H" signal is applied to the CNVSS and P5_0 pins and an "L" signal is applied to the P5_5 pin. A program in the boot ROM area is executed.

In boot mode, the FMR05 bit in the FMR0 register selects access to the boot ROM area or the user ROM area. The rewrite control program for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area can be rewritten in parallel I/O mode only. If any rewrite control program using erase-write mode (EW0 mode) is written in the boot ROM area, the flash memory can be rewritten according to the system implemented.

22.2 Functions To Prevent Flash Memory from Rewriting

The flash memory has a built-in ROM code protect function for parallel I/O mode and a built-in ID code check function for standard I/O mode to prevent the flash memory from reading or rewriting.

22.2.1 ROM Code Protect Function

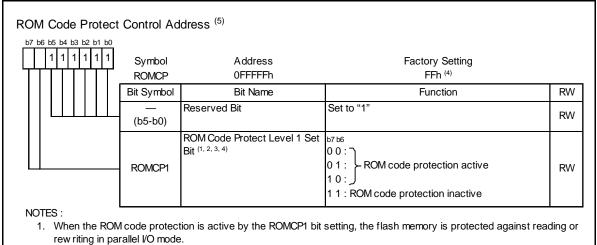
The ROM code protect function inhibits the flash memory from being read or rewritten during parallel input/ output mode. Figure 22.2 shows the ROMCP Register. The ROMCP register is located in the user ROM area. The ROM code protect function is enabled when the ROMCR bits are set to other than "11b". In this case, set the bit 5 to bit 0 to "111111b".

When exiting ROM code protect, erase the block including the ROMCP1 register by the CPU rewrite mode or the standard serial I/O mode.

22.2.2 ID Code Check Function

Use the ID code check function in standard serial I/O mode. The ID code sent from the serial programmer is compared with the ID code written in the flash memory for a match. If the ID codes do not match, commands sent from the serial programmer are not accepted. However, if the four bytes of the reset vector are "FFFFFFFFh", ID codes are not compared, allowing all commands to be accepted.

The ID codes are 7-byte data stored consecutively, starting with the first byte, into addresses 0FFFDFh, 0FFFE3h, 0FFFE3h, 0FFFE3h, 0FFFF3h, 0FFFF7h, and 0FFFFBh. The flash memory must have a program with the ID codes set in these addresses.



- Set the bit 5 to bit 0 to "111111b" when the ROMCP1 bit is set to a value other than "11b".
 If the bit 5 to bit 0 are set to values other than "111111b", the ROM code protection may not become active by setting the ROMCP1 bit to a value other than "11b".
- 3. To make the ROM code protection inactive, erase a block including the ROMCP address in standard serial I/O mode or CPU rew rite mode.
- 4. The ROMCP address is set to "FFh" when a block, including the ROMCP address, is erased.
- 5. When a value of the ROMCP address is "00h" or "FFh", the ROM code protect function is disabled.

Figure 22.2 ROMCP Register

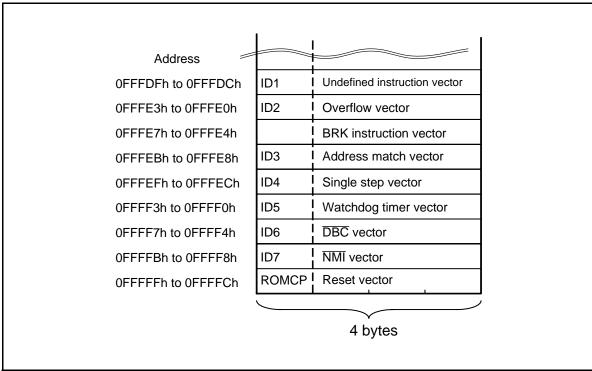


Figure 22.3 Address for ID Code Stored

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22.3 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten when the CPU executes software commands.

The user ROM area can be rewritten with the microcomputer mounted on a board without using a parallel or serial programmer.

In CPU rewrite mode, only the user ROM area shown in Figure 22.1 can be rewritten. The boot ROM area cannot be rewritten. Program and the block erase command are executed only in the user ROM area.

Erase-write 0 (EW0) mode and erase-write 1 (EW1) mode are provided as CPU rewrite mode. Table 22.3 lists differences between erase-write 0 (EW0) and erase-write 1 (EW1) modes.

Item	EW0 Mode	EW1 Mode
Operating Mode	Single-chip mod	Single-chip mode
	 Memory expansion mode 	
	Boot mode	
Space where the	User ROM area	User ROM area
rewrite control	Boot ROM area	
program can be		
placed		
Space where the	The rewrite control program must be	The rewrite control program can be
rewrite control	transferred to any space other than the	executed in the user ROM area
program can be	flash memory (e.g., RAM) before being	
executed	executed ⁽²⁾	
Space which can be	User ROM area	User ROM area
rewritten		However, this excludes blocks with the
		rewrite control program
Software Command	None	 Program and block erase commands
Restriction		cannot be executed in a block having
		the rewrite control program.
		 Erase all unlocked block command
		cannot be executed when the lock bit
		in a block having the rewrite control
		program is set to "1" (unlocked) or
		when the FMR02 bit in the FMR0
		register is set to "1" (lock bit disabled).
		 Read status register command cannot
		be used.
Mode after Program	Read status register mode	Read array mode
or Erasing		
CPU State during	Operating	Maintains hold state (I/O ports maintains
Auto Write and Auto		the state before the command was
Erase		executed) ⁽¹⁾
Flash Memory State	 Read the FMR00, FMR06 and FMR07 	Read the FMR00, FMR06 and FMR07
Detection	bits in the FMR0 register by program	bits in the FMR0 register by program
	 Execute the read status register 	
	command to read the SR7, SR5 and	
	SR4 bits in the status register.	

Table 22.3 EW0 Mode and EW1 Mode

NOTES:

- 1. Do not generate an interrupt (except NMI interrupt) or DMA transfer.
- 2. 2. When in CPU rewrite mode, the PM10 and PM13 bits in the PM1 register are set to "1". The rewrite control program can only be executed in the internal RAM or in an external area that is enabled for use when the PM13 bit = 1. When the PM13 bit = 0 and the flash memory is used in 4M-byte mode, the extended accessible area (40000h to BFFFFh) cannot be used.

22.3.1 EW0 Mode

The microcomputer enters CPU rewrite mode by setting the FMR01 bit in the FMR0 register to "1" (CPU rewrite mode enabled) and is ready to accept commands. EW0 mode is selected by setting the FMR11 bit in the FMR1 register to "0". To set the FMR01 bit to "1", set to "1" after first writing "0".

The software commands control programming and erasing. The FMR0 register or the status register indicates whether a program or erase operation is completed as expected or not.

22.3.2 EW1 Mode

EW1 mode is selected by setting the FMR11 bit to "1" after the FMR01 bit is set to "1". (Both bits must be set to "0" first before setting to "1".)

The FMR0 register indicates whether or not a program or erase operation has been completed as expected. The status register cannot be read in EW1 mode.

When an erase/program operation is initiated the CPU halts all program execution until the operation is completed or erase-suspend is requested.

22.3.3 Flash memory Control Register (FIDR, FMR0 and FMR1 registers)

Figure 22.4 to Figure 22.6 show the FIDR, FMR0 and FMR1 Registers.

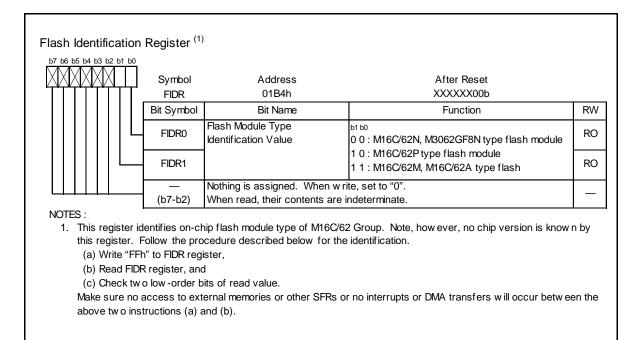


Figure 22.4 FIDR Register

0	Symbol	Address	After Reset	
	FMR0	01B7h	0000001b	
	Bit Symbol	Bit Name	Function	R
	FMR00	RY/BY Status Flag	0 : Busy (being w ritten or erased) 1 : Ready	R
	FMR01	CPU Rew rite Mode Select Bit ⁽¹⁾	0 : Disables CPU rew rite mode 1 : Enables CPU rew rite mode	R\
	FMR02	Lock Bit Disable Select Bit ⁽²⁾	0 : Enables lock bit 1 : Disables lock bit	R۱
	 FMSTP	Flash Memory Stop Bit ^(3, 5)	0 : Enables flash memory operation 1 : Stops flash memory operation (placed in low pow er mode, flash memory initialized)	R۱
	(b4)	Reserved Bit	Set to "0"	R
	FMR05	User ROM Area Select Bit ⁽³⁾ (Effective in Only Boot Mode)	0 : Boot ROM area is accessed 1 : User ROM area is accessed	R\
	FMR06	Program Status Flag ⁽⁴⁾	0 : Terminated normally 1 : Terminated in error	R
	FMR07	Erase Status Flag ⁽⁴⁾	0 : Terminated normally 1 : Terminated in error	R

than the flash memory.

Enter read array mode and set this bit to "0".

- 2. To set this bit to "1," w rite "0" and then "1" in succession when the FMR01 bit = 1. Make sure no interrupts or no DMA transfers w ill occur before w riting "1" after w riting "0".
- 3. Write to this bit from a program in other than the flash memory.
- 4. This flag is cleared to "0" by executing the Clear Status command.
- 5. Effective when the FMR01 bit = 1 (CPU rew rite mode). If the FMR01 bit = 0, although the FMR03 bit can be set to "1" by writing "1" in a program, the flash memory is neither placed in low pow er mode nor initialized.
- 6. This status includes writing or reading with the Lock Bit Program or Read Lock Bit Status command.

Figure 22.5 FMR0 Register

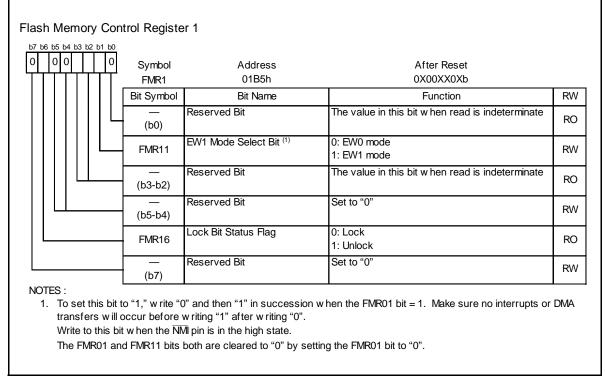


Figure 22.6 FMR1 Register

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22.3.3.1 FMR00 Bit

This bit indicates the flash memory operating state. It is set to "0" while the program, block erase, erase all unlocked block, lock bit program, or read lock bit status command is being executed; otherwise, it is set to "1".

22.3.3.2 FMR01 Bit

The microcomputer can accept commands when the FMR01 bit is set to "1" (CPU rewrite mode). Set the FMR05 bit to "1" (user ROM area access) as well if in boot mode.

22.3.3.3 FMR02 Bit

The lock bit is disabled by setting the FMR02 bit to "1" (lock bit disabled). (Refer to **22.3.6 Data Protect Function**.) The lock bit is enabled by setting the FMR02 bit to "0" (lock bit enabled).

The FMR02 bit does not change the lock bit status but disables the lock bit function. If the block erase or erase all unlocked block command is executed when the FMR02 bit is set to "1", the lock bit status changes "0" (locked) to "1" (unlocked) after command execution is completed.

22.3.3.4 FMSTP Bit

The FMSTP bit resets the flash memory control circuits and minimizes power consumption in the flash memory. Access to the flash memory is disabled when the FMSTP bit is set to "1". Set the FMSTP bit by program in a space other than the flash memory.

- Set the FMSTP bit to "1" if one of the followings occurs: A flash memory access error occurs while erasing or programming in EW0 mode (FMR00 bit does not switch back to "1" (ready)).
- Low-power consumption mode or on-chip oscillator low-power consumption mode is entered

Use the following the procedure to change the FMSTP bit setting.

- (1) Set the FMSTP bit to "1"
- (2) Set tps (the wait time to stabilize flash memory circuit)
- (3) Set the FMSTP bit to "0"
- (4) Set tps (the wait time to stabilize flash memory circuit)

Figure 22.9 shows a Flow Chart Illustrating How To Start and Stop the Flash Memory Processing Before and After Low Power Dissipation Mode or On-chip Oscillator Low-Power Consumption Mode. Follow the procedure on this flow chart.

When entering stop or wait mode, the flash memory is automatically turned off. When exiting stop or wait mode, the flash memory is turned back on. The FMR0 register does not need to be set.

22.3.3.5 FMR05 Bit

This bit selects the boot ROM or user ROM area in boot mode. Set to "0" to access (read) the boot ROM area or to "1" (user ROM access) to access (read, write or erase) the user ROM area.

22.3.3.6 FMR06 Bit

This is a read-only bit indicating an auto program operation state. The FMR06 bit is set to "1" when a program error occurs; otherwise, it is set to "0". Refer to **22.3.8 Full Status Check**.

22.3.3.7 FMR07 Bit

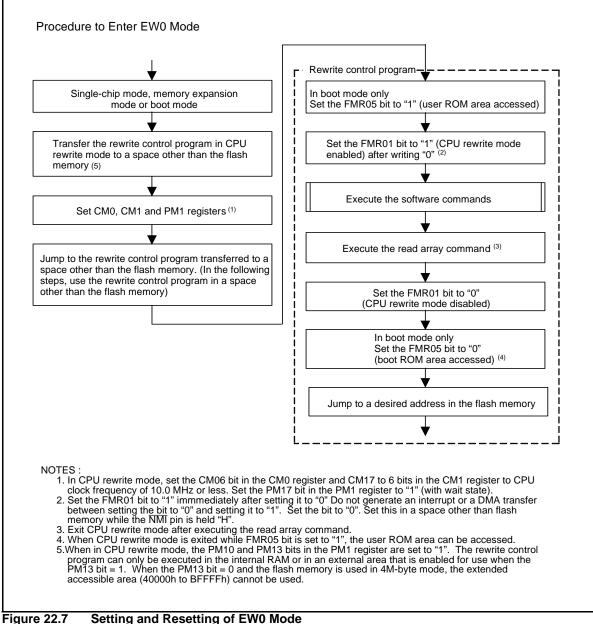
This is a read-only bit indicating the auto erase operation status. The FMR07 bit is set to "1" when an erase error occurs; otherwise, it is set to "0". For details, refer to **22.3.8 Full Status Check**. Figure 22.7 shows Setting and Resetting of EW0 Mode. Figure 22.8 show Setting and Resetting of EW1 Mode.

22.3.3.8 FMR11 Bit

EW0 mode is entered by setting the FMR11 bit to "0" (EW0 mode). EW1 mode is entered by setting the FMR11 bit to "1" (EW1 mode).

22.3.3.9 FMR16 Bit

This is a read-only bit indicating the execution result of the read lock bit status command. When the block, where the read lock bit status command is executed, is locked, the FMR16 bit is set to "0". When the block, where the read lock bit status command is executed, is unlocked, the FMR16 bit is set to "1".



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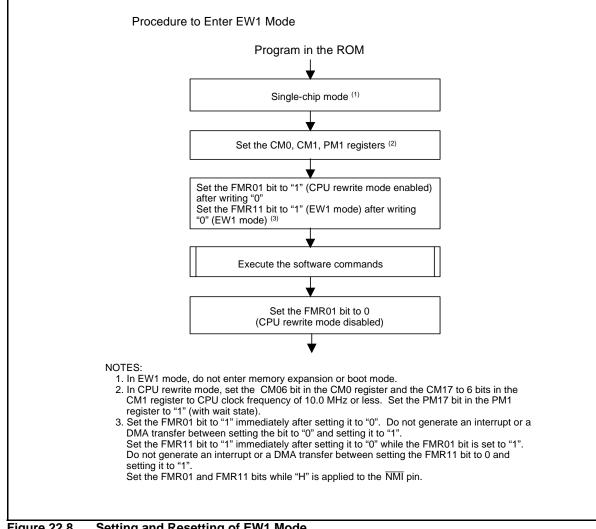
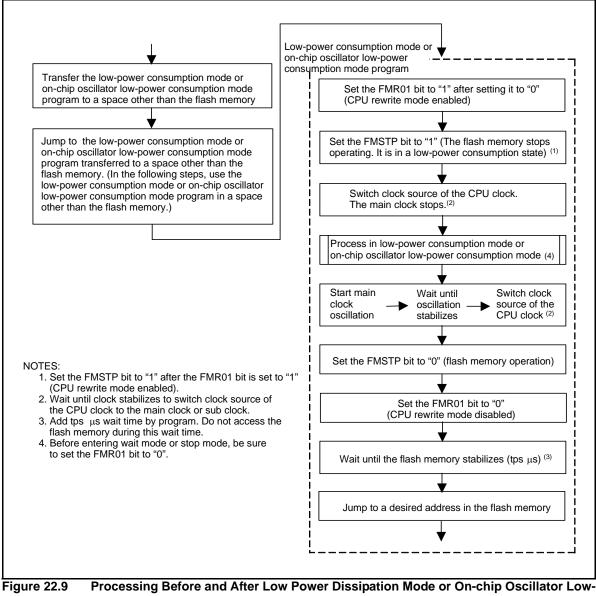


Figure 22.8 Setting and Resetting of EW1 Mode

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Power Consumption Mode

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22.3.4 Precautions on CPU Rewrite Mode

22.3.4.1 Operating Speed

Set the CM06 bit in the CM0 register and the CM17 to CM16 bits in the CM1 register to a CPU clock frequency of 10 MHz or less before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to "1" (wait state).

22.3.4.2 Prohibited Instructions

The following instructions cannot be used in EW0 mode because the CPU tries to read data in the flash memory: the UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

22.3.4.3 Interrupts (EW0 mode)

- To use interrupts having vectors in a relocatable vector table, the vectors must be relocated to the RAM area.
- The NMI and watchdog timer interrupts are available since the FMR0 and FMR1 registers are forcibly reset when either interrupt occurs. Allocate the jump addresses for each interrupt service routines to the fixed vector table. Flash memory rewrite operation is suspended when the NMI or watchdog timer interrupt occurs. Execute the rewrite program again after exiting the interrupt routine.
- The address match interrupt is not available since the CPU tries to read data in the flash memory.

22.3.4.4 Interrupts (EW1 mode)

- Do not acknowledge any interrupts with vectors in the relocatable vector table or address match interrupt during the auto program or auto erase period.
- Do not use the watchdog timer interrupt.
- The $\overline{\text{NMI}}$ interrupt is available since the FMR0 and FMR1 registers are forcibly reset when the interrupt occurs. Allocate the jump address for the interrupt service routine to the fixed vector table. Flash memory rewrite operation is suspended when the $\overline{\text{NMI}}$ interrupt occurs. Execute the rewrite program again after exiting the interrupt service routine.

22.3.4.5 22.3.4.5 How to Access

To set the FMR01, FMR02 or FMR11 bit to "1", write "1" after first setting the bit to "0". Do not generate an interrupt or a DMA transfer between the instruction to set the bit to "0" and the instruction to set the bit to "1". Set the bit while an "H" signal is applied to the $\overline{\text{NMI}}$ pin.

22.3.4.6 22.3.4.6 Rewriting in the User ROM Area (EW0 mode)

If the supply voltage drops while rewriting the block where the rewrite control program is stored, the flash memory cannot be rewritten because the rewrite control program is not correctly rewritten. If this error occurs, rewrite the user ROM area while in standard serial I/O mode or parallel I/O mode.

22.3.4.7 22.3.4.7 Rewriting in the User ROM Area (EW1 mode)

Avoid rewriting any block in which the rewrite control program is stored.

22.3.4.8 22.3.4.8 DMA Transfer

In EW1 mode, do not perform a DMA transfer while the FMR00 bit in the FMR0 register is set to "0" (auto programming or auto erasing).

22.3.4.9 Writing Command and Data

Write commands and data to even addresses in the user ROM area.

22.3.4.10 Wait Mode

When entering wait mode, set the FMR01 bit to "0" (CPU rewrite mode disabled) before executing the WAIT instruction.

22.3.4.11 Stop Mode

When entering stop mode, the following settings are required:

• Set the FMR01 bit to "0" (CPU rewrite mode disabled). Disable DMA transfer before setting the CM10 bit to "1" (stop mode).

22.3.4.12 Low-Power Consumption Mode and On-chip Oscillator Low-power Consumption Mode

If the CM05 bit is set to "1" (main clock stopped), do not execute the following commands:

- Program
- Block erase
- Erase all unlocked blocks
- · Lock bit program
- Read lock bit status

22.3.5 Software Commands

Software commands are described below. The command code and data must be read and written in 16-bit units, to and from even addresses in the user ROM area. When writing command code, the 8 high-order bits (D15 to D8) are ignored.

	F	First Bus Cyc	le	Second Bus Cycle			
Command	Mode	Address	Data	Mode	Address	Data	
			(D0 to D7)			(D0 to D7)	
Read Array	Write	Х	xxFFh				
Read Status Register	Write	Х	xx70h	Read	Х	SRD	
Clear Status Register	Write	Х	xx50h				
Program	Write	WA	xx40h	Write	WA	WD	
Block Erase	Write	Х	xx20h	Write	BA	xxD0h	
Erase All Unlocked Block	Write	Х	xxA7h	Write	Х	xxD0h	
Lock Bit Program	Write	BA	xx77h	Write	BA	xxD0h	
Read Lock Bit Status	Write	Х	xx71h	Write	BA	xxD0h	

NOTES:

1. Blocks 0 to 12 can be erased by the erase all unlocked block command.

- Block A cannot be erased. The block erase command must be used to erase the block A.
 - SRD: Data in the SRD register (D7 to D0)
 - WA: Address to be written (The address specified in the first bus cycle is the same even address as the address specified in the second bus cycle.)
 - WD: 16-bit write data
 - BA: Highest-order block address (must be an even address)
 - X: Any even address in the user ROM space
- xx: 8 high-order bits of command code (ignored)

22.3.5.1 Read Array Command (FFh)

The read array command reads the flash memory.

By writing command code "xxFFh" in the first bus cycle, read array mode is entered. Content of a specified address can be read in 16-bit units after the next bus cycle.

The microcomputer remains in read array mode until another command is written. Therefore, contents from multiple addresses can be read consecutively.

22.3.5.2 Read Status Register Command (70h)

The read status register command reads the status register (refer to **22.3.7 Status Register** for detail). By writing command code "xx70h" in the first bus cycle, the status register can be read in the second bus cycle. Read an even address in the user ROM area. Do not execute this command in EW1 mode.

Do not execute this command in EW1 mode.

22.3.5.3 Clear Status Register Command (50h)

The clear status register command clears the status register. By writing "xx50h" in the first bus cycle, the FMR07 to FMR06 bits in the FMR0 register are set to "00b" and the SR5 to SR4 bits in the status register are set to "00b".

22.3.5.4 Program Command (40h)

The program command writes 2-byte data to the flash memory. By writing "xx40h" in the first bus cycle and data to the write address in the second bus cycle, an auto program operation (data program and verify) will start. The address value specified in the first bus cycle must be the same even address as the write address specified in the second bus cycle.

The FMR00 bit in the FMR0 register indicates whether an auto program operation has been completed. The FMR00 bit is set to "0" (busy) during auto program and to "1" (ready) when an auto program operation is completed.

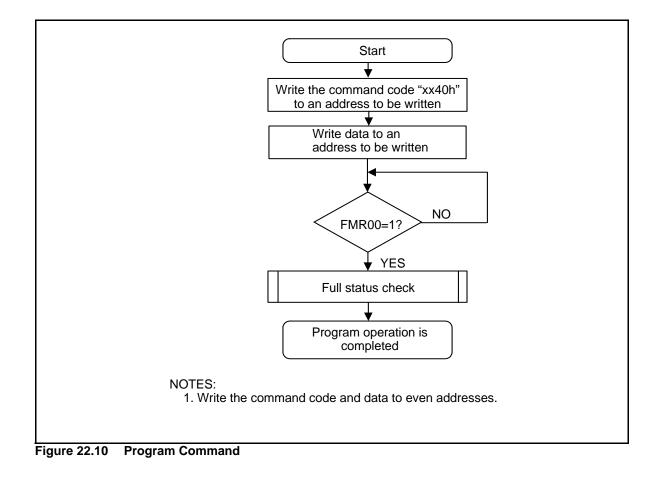
After the completion of an auto program operation, the FMR06 bit in the FMR0 register indicates whether or not the auto program operation has been completed as expected. (Refer to **22.3.8 Full Status Check**.) An address that is already written cannot be altered or rewritten.

Figure 22.10 shows a Flow Chart of the Program Command Programming.

The lock bit protects each block from being programmed inadvertently. (Refer to **22.3.6 Data Protect Function**.)

In EW1 mode, do not execute this command on the block where the rewrite control program is allocated.

In EW0 mode, the microcomputer enters read status register mode as soon as an auto program operation starts. The status register can be read. The SR7 bit in the status register is set to "0" at the same time an auto program operation starts. It is set to "1" when auto program operation is completed. The microcomputer remains in read status register mode until the read array command is written. After completion of an auto program operation, the status register indicates whether or not the auto program operation has been completed as expected.



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22.3.5.5 Block Erase Command

The block erase command erases each block.

By writing "xx20h" in the first bus cycle and "xxD0h" to the highest-order even address of a block in the second bus cycle, an auto erase operation (erase and verify) will start in the specified block.

The FMR00 bit in the FMR0 register indicates whether an auto erase operation has been completed.

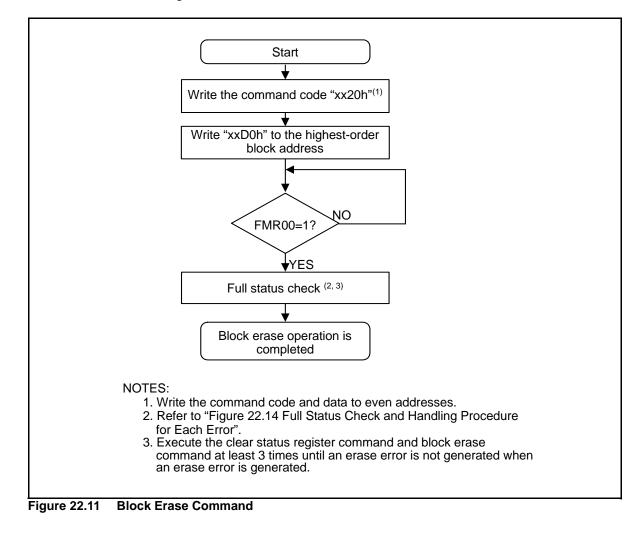
The FMR00 bit is set to "0" (busy) during auto erase and to "1" (ready) when the auto erase operation is completed.

After the completion of an auto erase operation, the FMR07 bit in the FMR0 register indicates whether or not the auto erase operation has been completed as expected. (Refer to **22.3.8 Full Status Check**.)

Figure 22.11 shows a Flow Chart of the Block Erase Command Programming.

The lock bit protects each block from being programmed inadvertently. (Refer to **22.3.6 Data Protect Function**.)

In EW1 mode, do not execute this command on the block where the rewrite control program is allocated. In EW0 mode, the microcomputer enters read status register mode as soon as an auto erase operation starts. The status register can be read. The SR7 bit in the status register is set to "0" at the same time an auto erase operation starts. It is set to "1" when an auto erase operation is completed. The microcomputer remains in read status register mode until the read array command or read lock bit status command is written. Also execute the clear status register command and block erase command at least 3 times until an erase error is not generated when an erase error is generated.



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22.3.5.6 Erase All Unlocked Block

The erase all unlocked block command erases all blocks except the block A.

By writing "xxA7h" in the first bus cycle and "xxD0h" in the second bus cycle, an auto erase (erase and verify) operation will run continuously in all blocks except the block A.

The FMR00 bit in the FMR0 register indicates whether an auto erase operation has been completed.

After the completion of an auto erase operation, the FMR07 bit in the FMR0 register indicates whether or not the auto erase operation has been completed as expected.

The lock bit can protect each block from being programmed inadvertently. (Refer to **22.3.6 Data Protect Function**.)

In EW1 mode, do not execute this command when the lock bit for any block storing the rewrite control program is set to "1" (unlocked) or when the FMR02 bit in the FMR0 register is set to "1" (lock bit disabled).

In EW0 mode, the microcomputer enters read status register mode as soon as an auto erase operation starts. The status register can be read. The SR7 bit in the status register is set to "0" (busy) at the same time an auto erase operation starts. It is set to "1" (ready) when an auto erase operation is completed. The microcomputer remains in read status register mode until the read array command or read lock bit status command is written.

Only blocks 0 to 12 can be erased by the erase all unlocked block command. The block A cannot be erased. Use the block erase command to erase the block A.

22.3.5.7 Lock Bit Program Command

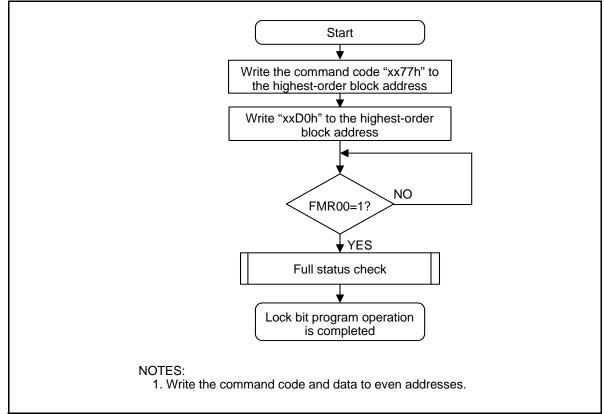
The lock bit program command sets the lock bit for a specified block to "0" (locked).

By writing "xx77h" in the first bus cycle and "xxD0h" to the highest-order even address of a block in the second bus cycle, the lock bit for the specified block is set to "0". The address value specified in the first bus cycle must be the same highest-order even address of a block specified in the second bus cycle.

Figure 22.12 shows a Flow Chart of the Lock Bit Program Command Programming. Execute read lock bit status command to read lock bit state (lock bit data).

The FMR00 bit in the FMR0 register indicates whether a lock bit program operation is completed.

Refer to 22.3.6 Data Protect Function for details on lock bit functions and how to set it to "1" (unlocked).





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22.3.5.8 Read Lock Bit Status Command (71h)

The read lock bit status command reads the lock bit state of a specified block.

By writing "xx71h" in the first bus cycle and "xxD0h" to the highest-order even address of a block in the second bus cycle, the FMR16 bit in the FMR1 register stores information on whether or not the lock bit of a specified block is locked. Read the FMR16 bit after the FMR00 bit in the FMR0 register is set to "1" (ready). Figure 22.13 shows a Flow Chart of the Read Lock Bit Status Command Programming.

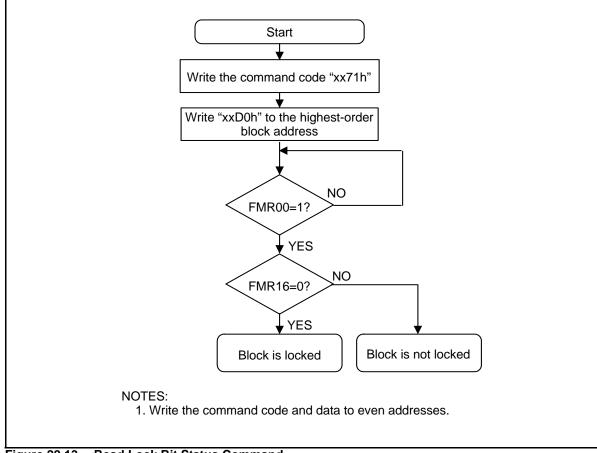


Figure 22.13 Read Lock Bit Status Command

22.3.6 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR02 bit to "0" (lock bit enabled). The lock bit allows each block to be individually protected (locked) against program and erase. This helps prevent data from being inadvertently written to or erased from the flash memory.

- When the lock bit status is set to "0", the block is locked (block is protected against program and erase).
- When the lock bit status is set to "1", the block is not locked (block can be programmed or erased).

The lock bit status is set to "0" (locked) by executing the lock bit program command and to "1" (unlocked) by erasing the block. The lock bit status cannot be set to "1" by any commands. The lock bit status can be read by the read lock bit status command.

The lock bit function is disabled by setting the FMR02 bit to "1". All blocks are unlocked. However, individual lock bit status remains unchanged. The lock bit function is enabled by setting the FMR02 bit to "0". Lock bit status is retained.

If the block erase or erase all unlocked block command is executed while the FMR02 bit is set to "1", the target block or all blocks are erased regardless of lock bit status. The lock bit status of each block are set to "1" after an erase operation is completed.

Refer to 22.3.5 Software Commands for details on each command.

22.3.7 Status Register

The status register indicates the flash memory operation state and whether or not an erase or program operation is completed as expected. The FMR00, FMR06 and FMR07 bits in the FMR0 register indicate status register states.

Table 22.5 shows the Status Register.

In EW0 mode, the status register can be read when the followings occur.

- Any even address in the user ROM area is read after writing the read status register command.
- Any even address in the user ROM area is read from when the program, block erase, erase all unlocked block, or lock bit program command is executed until when the read array command is executed.

22.3.7.1 Sequence Status (SR7 and FMR00 Bits)

The sequence status indicates the flash memory operation state. It is set to "0" while the program, block erase, erase all unlocked block, lock bit program, or read lock bit status command is being executed; otherwise, it is set to "1".

22.3.7.2 Erase Status (SR5 and FMR07 Bits)

Refer to 22.3.8 Full Status Check.

22.3.7.3 Program Status (SR4 and FMR06 Bits)

Refer to 22.3.8 Full Status Check.

Bits in Status	Bit in FMR0	Status name	Defin	Value after	
Register	Register	Status name	"0"	"1"	Reset
SR0 (D0)	-	Reserved	-	-	-
SR1 (D1)	-	Reserved	-	-	-
SR2 (D2)	-	Reserved	-	-	-
SR3 (D3)	-	Reserved	-	-	-
SR4 (D4)	FMR06	Program status	Terminated normally	Terminated in error	0
SR5 (D5)	FMR07	Erase status	Terminated normally	Terminated in error	0
SR6 (D6)	-	Reserved	-	-	-
SR7 (D7)	FMR00	Sequencer status	Busy	Ready	1

Table 22.5 Status Register

• D0 to D7: These data buses are read when the read status register command is executed.

• The FMR07 bit (SR5) and FMR06 bit (SR4) are set to "0" by executing the clear status register command.

• When the FMR07 bit (SR5) or FMR06 bit (SR4) is set to "1," the program, block erase, erase all unlocked block and lock bit program commands are not accepted.

22.3.8 Full Status Check

If an error occurs when a program or erase operation is completed, the FMR06 to FMR07 bits in the FMR0 register are set to "1", indicating a specific error. Therefore, execution results can be confirmed by checking these bits (full status check).

Table 22.6 lists Errors and FMR0 Register State. Figure 22.14 shows a flow chart of the Full Status Check and Handling Procedure for Each Error.

FMR00 Register			
(Status Register) State		Error	Error Occurrence Conditions
FMR07 bit	FMR06 bit	Enor	
(SR5 bit)	(SR4 bit)		
		Command	 Command is written incorrectly
1	1	Sequence error	 A value other than "xxD0h" or "xxFFh" is written in the
I	I		second bus cycle of the lock bit program, block erase or
			erase all unlocked block command ⁽¹⁾
		Erase error	• The block erase command is executed on a locked block
1	0		• The block erase or erase all unlocked block command is
I	0		executed on an unlock block and auto erase operation is
			not completed as expected ⁽²⁾
		Program error	The program command is executed on locked blocks
			• The program command is executed on unlocked blocks
0	1		but program operation is not completed as expected
			• The lock bit program command is executed but program
			operation is not completed as expected ⁽²⁾

Table 22.6 Errors and FMR0 Register State

NOTES:

- 1. The flash memory enters read array mode by writing command code "xxFFh" in the second bus cycle of these commands. The command code written in the first bus cycle becomes invalid.
- 2. When the FMR02 bit is set to "1" (lock bit disabled), no error occurs even under the conditions above.

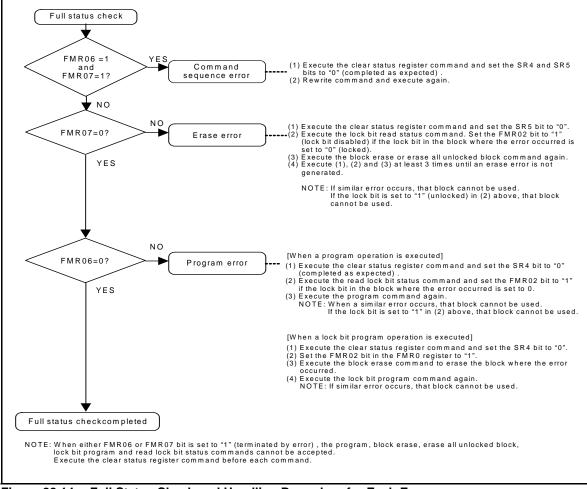


Figure 22.14 Full Status Check and Handling Procedure for Each Error

22.4 Standard Serial I/O Mode

In standard serial I/O mode, the serial programmer supporting the M16C/62P Group (M16C/62P, M16C/62PT) can be used to rewrite the flash memory user ROM area in the microcomputer mounted on a board.

For more information about the serial programmer, contact your serial programmer manufacturer. Refer to the user's manual included with your serial programmer for instructions.

Table 22.7 lists Pin Functions (Flash Memory Standard Serial I/O Mode). Figure 22.15 to Figure 22.18 show Pin Connections in Serial I/O Mode.

22.4.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer matches those written in the flash memory. (Refer to **22.2 Functions To Prevent Flash Memory from Rewriting**.)

VCC1, VCC2, VSS Power Input Apply the Flash Program, Erase Voltage to VCC1 pin and VCC2 to the VCC2 apply condition is that VCC2 ≤ VCC1. Apply 0 V to VSS pin. CNVSS CNVSS I VCC1 Connect to VCC1 pin. RESET Reset Input I VCC1 Connect to VCC1 pin. RESET Reset Input I VCC1 Connect to VCC1 pin. XIN Clock Input I VCC1 Connect to VCC1 pin. XOUT Clock Output O VCC1 Connect A ceramic resonator or crystal oscillator XOUT Clock Output O VCC1 Connect AVSS to VSS and AVCC to VCC1, respectively. BYTE BYTE I VCC2 Input Port PO I AVCC, AVSS Analog Power Supply Input Connect AVSS to VSS and AVCC to VCC1, respectively. Connect AVSS to VSS and AVCC to VCC1, respectively. VREF Reference Voltage Input I VCC2 Input Port To " "Level signal or open. P1_0 to P1_7 Input Port P1 I VCC2 Input H"r or "L" level signal or open. P2_0 to P4_7 Input Port P3 I VCC2 Input H"r or "L" level signal or open. P5_6 F5_7 F5_6	Pin	Name	I/O	Power Supply	Description
RESET Reset Input I VCC1 Reset input pin. While RESET pin is "L" level, input a 20 cycle or longer clock to XIN pin. XIN Clock Input I VCC1 Connect a ceramic resonator or crystal oscillator between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin and open XOUT pin. BYTE BYTE I VCC1 Connect this pin to VCC1 or VSS. AVCC, AVSS Analog Power Supply Input I VCC1 Connect this pin to VCC1 or VCS1, respectively. VREF Reference Voltage Input I VCC2 Input "H" or "L" level signal or open. P1_0 to P1_7 Input Port P0 I VCC2 Input "H" or "L" level signal or open. P3_0 to P2_7 Input Port P3 I VCC2 Input "H" or "L" level signal or open. P3_0 to P3_7 Input Port P4 I VCC2 Input "H" or "L" level signal or open. P5_1 to P5_4, P5_7 Input Port P5 I VCC2 Input "H" or "L" level signal. P6_5_5 EPM Input I VCC2 Input "H" or "L" level signal or open. P6_5_6 Input Port P6 I VCC1 Input "H" or "L" leve	VCC1, VCC2, VSS	Power Input		-	Apply the Flash Program, Erase Voltage to VCC1 pin and VCC2 to the VCC2 pin. The VCC apply condition is
cycle or longer clock to XIN pin. XIN Clock Input I VCC1 Connect a ceramic resonator or crystal oscillator XOUT Clock Output O VCC1 Connect a ceramic resonator or crystal oscillator BYTE BYTE I VCC1 Connect AVSS to VSS and AVCC to VCC1, respectively. RAVC, AVSS Analog Power Supply Input I Connect AVSS to VSS and AVCC to VCC1, respectively. VREF Reference Voltage Input I Enter the reference voltage for A/D from this pin. P0_0 to P0_7 Input Port P0 I VCC2 Input "H" or "L" level signal or open. P3_0 to P2_7 Input Port P1 I VCC2 Input "H" or "L" level signal or open. P3_0 to P4_7 Input Port P3 I VCC2 Input "H" or "L" level signal or open. P5_1 to P5_4, Input Port P5 I VCC2 Input "H" or "L" level signal. P6_0 to P6_3 Input Port P6 I VCC2 Input "H" or "L" level signal or open. P5_5 EPM Input I VCC2 Input "H" or "L" level signal or open. P6_6/RXD1 SCLK In	CNVSS	CNVSS	I	VCC1	Connect to VCC1 pin.
XOUTClock OutputOVCC1between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin and open XOUT pin.BYTEBYTEIVCC1Connect AVSS to VSS and AVCC to VCS.AVCC, AVSSAnalog Power Supply InputIVCC1Connect AVSS to VSS and AVCC to VCC1, respectively.VREFReference Voltage InputIEnter the reference voltage for A/D from this pin.P0_0 to P0_7Input Port P0IVCC2Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P1IVCC2Input "H" or "L" level signal or open.P2_0 to P2_7Input Port P3IVCC2Input "H" or "L" level signal or open.P3_0 to P3_7Input Port P3IVCC2Input "H" or "L" level signal or open.P4_0 to P4_7Input Port P5IVCC2Input "H" or "L" level signal or open.P5_1 to P5_4, P5_6P5_7Input Port P5IVCC2P5_0CE InputIVCC2Input "H" or "L" level signal.P5_5EPM InputIVCC2Input "H" or "L" level signal.P5_6, P5_7P6_0 to P6_3Input Port P6IVCC1P6_0 to P6_3Input Port P6IVCC2Input "H" or "L" level signal.P5_5EPM InputOVCC1Standard serial I/O mode 1: Serial clock input pinP6_0 to P6_3Input Port P6IVCC1Standard serial I/O mode 1: Serial clock input pinP6_6/RD1SCLK InputIVCC1Serial data input pin.<	RESET	Reset Input	I	VCC1	
BYTEBYTEIVCC1Connect this pin to VCC1 or VSS.AVCC, AVSSAnalog Power Supply InputIConnect AVSS to VSS and AVCC to VCC1, respectively.VREFReference Voltage InputIEnter the reference voltage for A/D from this pin.P0_0 to P0_7Input Port P0IVCC2P1_0 to P1_7Input Port P1IVCC2P2_0 to P2_7Input Port P1IVCC2P3_0 to P3_7Input Port P3IVCC2P4_0 to P4_7Input Port P4IVCC2P5_6, P5_7Input Port P5IVCC2P5_0CE InputIVCC2P5_0CE InputIVCC2Input "H" or "L" level signal or open.P5_5EPM InputIVCC2P6_0 to P6_3Input Port P6IVCC2P6_6/RXD1SCLK InputIVCC2P6_6/RXD1SCLK InputIVCC1P6_6/RXD1RXD InputIVCC1P6_7/TXD1TXD InputOVCC1P6_6/RXD1RXD InputIVCC1P7_0 to P7_7Input Port P7IP8_6, P8_7P8_4P8_4 inputIVCC1Serial data output pin.P6_5/CLK1SCLK InputIVCC1Serial data output pin.P6_6/RXD1RXD InputIVCC1Input "H" or "L" level signal or open.P8_6, P8_7P8_4P8_4P8_4 inputIVCC1Input "H" or "L" level signal or op	XIN	Clock Input	I	VCC1	
AVCC, AVSS Analog Power Supply Input Connect AVSS to VSS and AVCC to VCC1, respectively. VREF Reference Voltage Input I Enter the reference voltage for A/D from this pin. P0_0 to P0_7 Input Port P0 I VCC2 Input "H" or "L" level signal or open. P1_0 to P1_7 Input Port P1 I VCC2 Input "H" or "L" level signal or open. P2_0 to P2_7 Input Port P3 I VCC2 Input "H" or "L" level signal or open. P3_0 to P4_7 Input Port P3 I VCC2 Input "H" or "L" level signal or open. P4_0 to P4_7 Input Port P4 I VCC2 Input "H" or "L" level signal or open. P5_1 to P5_4, Input Port P5 I VCC2 Input "H" or "L" level signal. P5_5 EPM Input I VCC2 Input "H" or "L" level signal or open. P6_4/RTS1 BUSY Output O VCC1 Input "H" or "L" level signal output pin. P6_5/CLK1 SCLK Input I VCC1 Standard serial I/O mode 1: BUSY signal output pin P6_6/RXD1 RXD Input I VCC1 Standard serial I/O mode 1: Serial clock input pin P6_6/RXD1 RXD Input	XOUT	Clock Output	0	VCC1	
Inputrespectively.VREFReference Voltage InputIEnter the reference voltage for A/D from this pin.P0_0 to P0_7Input Port P0IVCC2Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P1IVCC2Input "H" or "L" level signal or open.P2_0 to P2_7Input Port P2IVCC2Input "H" or "L" level signal or open.P3_0 to P3_7Input Port P3IVCC2Input "H" or "L" level signal or open.P4_0 to P4_7Input Port P4IVCC2Input "H" or "L" level signal or open.P5_6, P5_7Input Port P5IVCC2Input "H" or "L" level signal.P5_5EPM InputIVCC2Input "H" or "L" level signal.P5_5EPM InputIVCC2Input "H" or "L" level signal or open.P6_4/RTS1BUSY OutputOVCC1Istandard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 1: Serial clock input pinP6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data output pin.P7_0 to P7_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_0 to P8_3Input Port P8IVCC1Input "H" or "L" level signal or open.P8_0 to P8_3Input Port P8IVCC1Input "H" or "L" level signal or open.P8_0 to P7_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputI<	BYTE	BYTE	I	VCC1	Connect this pin to VCC1 or VSS.
P0_0 to P0_7 Input Port P0 I VCC2 Input "H" or "L" level signal or open. P1_0 to P1_7 Input Port P1 I VCC2 Input "H" or "L" level signal or open. P2_0 to P2_7 Input Port P2 I VCC2 Input "H" or "L" level signal or open. P3_0 to P3_7 Input Port P3 I VCC2 Input "H" or "L" level signal or open. P4_0 to P4_7 Input Port P4 I VCC2 Input "H" or "L" level signal or open. P5_1 to P5_4, P5_6, P5_7 Input Port P5 I VCC2 Input "H" or "L" level signal. P5_5 EPM Input I VCC2 Input "H" or "L" level signal. P6_6, 0 to P6_3 Input Port P6 I VCC1 Input "H" or "L" level signal or open. P6_4/RTS1 BUSY Output O VCC1 Input "H" or "L" level signal output pin Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Input "L". P6_6/RXD1 RXD Input I VCC1 Serial data input pin. P6_6/RXD1 RXD Input I VCC1 Serial data input pin. P6_6/RXD1 RXD Input	AVCC, AVSS				
PI_0 to P1_7 Input Port P1 I VCC2 Input "H" or "L" level signal or open. P2_0 to P2_7 Input Port P2 I VCC2 Input "H" or "L" level signal or open. P3_0 to P3_7 Input Port P3 I VCC2 Input "H" or "L" level signal or open. P4_0 to P4_7 Input Port P4 I VCC2 Input "H" or "L" level signal or open. P5_6, P5_7 Input Port P5 I VCC2 Input "H" or "L" level signal. P5_5 EPM Input I VCC2 Input "H" or "L" level signal. P5_5 EPM Input I VCC2 Input "H" or "L" level signal. P6_0 CE Input I VCC2 Input "H" or "L" level signal. P5_5 EPM Input I VCC2 Input "H" or "L" level signal or open. P6_4/RTS1 BUSY Output O VCC1 Input a standard serial I/O mode 1: BUSY signal output pin standard serial I/O mode 1: Serial clock input pin. P6_6/RXD1 RXD Input I VCC1 Serial data output pin. P6_0 to P7_7 Input Port P7 I VCC1 Input "H" or	VREF	Reference Voltage Input	I		Enter the reference voltage for A/D from this pin.
P2_0 to P2_7Input Port P2IVCC2Input "H" or "L" level signal or open.P3_0 to P3_7Input Port P3IVCC2Input "H" or "L" level signal or open.P4_0 to P4_7Input Port P4IVCC2Input "H" or "L" level signal or open.P5_1 to P5_4,Input Port P5IVCC2Input "H" or "L" level signal or open.P5_6, P5_7P5_0CE InputIVCC2Input "H" or "L" level signal.P5_5EPM InputIVCC2Input "H" or "L" level signal.P6_0 to P6_3Input Port P6IVCC1Input "H" or "L" level signal or open.P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 1: Serial clock input pinP6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 1: Serial clock input pinP6_6/RXD1RXD InputIVCC1Serial data input pin.P6_7/TXD1TXD InputOVCC1Serial data output pin.P7_0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputIVCC1Input "H" or "L" level signal or open.P8_5/NMINMI InputIVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P10_7Input Port P10I </td <td>P0_0 to P0_7</td> <td>Input Port P0</td> <td>Ι</td> <td>VCC2</td> <td>Input "H" or "L" level signal or open.</td>	P0_0 to P0_7	Input Port P0	Ι	VCC2	Input "H" or "L" level signal or open.
P2_0 to P2_7 Input Port P2 I VCC2 Input "H" or "L" level signal or open. P3_0 to P3_7 Input Port P3 I VCC2 Input "H" or "L" level signal or open. P4_0 to P4_7 Input Port P4 I VCC2 Input "H" or "L" level signal or open. P5_1 to P5_4, Input Port P5 I VCC2 Input "H" or "L" level signal or open. P5_5 FFM Input Port P5 I VCC2 Input "H" or "L" level signal. P5_5 FPM Input I VCC2 Input "H" or "L" level signal. P6_0 to P6_3 Input Port P6 I VCC1 Input "H" or "L" level signal or open. P6_4/RTS1 BUSY Output O VCC1 Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 1: Serial clock input pin. P6_5/CLK1 SCLK Input I VCC1 Standard serial I/O mode 1: Serial clock input pin. P6_6/RXD1 RXD Input I VCC1 Serial data output pin. P6_6/RXD1 RXD Input Port P7 I VCC1 Input "H" or "L" level signal or open. P8_6, P8_7 Input Port P8 <td>P1_0 to P1_7</td> <td>Input Port P1</td> <td>Ι</td> <td>VCC2</td> <td>Input "H" or "L" level signal or open.</td>	P1_0 to P1_7	Input Port P1	Ι	VCC2	Input "H" or "L" level signal or open.
P4_0 to P4_7Input Port P4IVCC2Input "H" or "L" level signal or open.P5_1 to P5_4, P5_6, P5_7Input Port P5IVCC2Input "H" or "L" level signal or open.P5_0CE InputIVCC2Input "H" or "L" level signal.P5_5EPM InputIVCC2Input "H" or "L" level signal.P6_0 to P6_3Input Port P6IVCC1Input "H" or "L" level signal or open.P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.P6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data output pin.P6_7/TXD1TXD InputOVCC1Input "H" or "L" level signal or open.P7_0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_6, P8_7P8_4P8_4 inputIVCC1Input "H" or "L" level signal or open.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P1_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P1_0 to P10_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0 to P12_7Input Port P12	P2_0 to P2_7	Input Port P2	I	VCC2	Input "H" or "L" level signal or open.
P5_1 to P5_4, P5_6, P5_7Input Port P5IVCC2Input "H" or "L" level signal or open.P5_6, P5_7CE F5_0CE EPM InputIVCC2Input "H" level signal.P5_5EPM InputIVCC2Input "L" level signal.P6_0 to P6_3Input Port P6IVCC1Input "H" or "L" level signal or open.P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.P6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data input pin.P6_7/TXD1TXD InputOVCC1Serial data output pin. (2)P7_0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_6, P8_7P8_4P8_4 inputIVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputIVCC1Input "H" or "L" level signal or open.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P1_0_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P1_0_0 to P12_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0_0 to P12_7Input Port P12IVCC1Input "H" or "L" level signal or open.P1_0_0 to P13_7Input Port P12IVCC2Input "H" or "	P3_0 to P3_7	Input Port P3	I	VCC2	Input "H" or "L" level signal or open.
P5_6, P5_7CEInputIVCC2Input "H" level signal.P5_0CEInputIVCC2Input "L" level signal.P5_5EPM InputIVCC2Input "H" or "L" level signal or open.P6_0 to P6_3Input Port P6IVCC1Input "H" or "L" level signal or open.P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.P6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data input pin.P6_6/7/TXD1TXD InputOVCC1Input "H" or "L" level signal or open.P6_6, P8_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_6, P8_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputIVCC1Input "H" or "L" level signal or open.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P1_0_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P1_0_0 to P12_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0_0 to P13_7Input Port P12IVCC2Input "H" or "L" level signal or open.P1_0_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open.P1_0_0 to P13_7Input Port P13I	P4_0 to P4_7	Input Port P4	I	VCC2	Input "H" or "L" level signal or open.
P5_5EPM InputIVCC2Input "L" level signal.P6_0 to P6_3Input Port P6IVCC1Input "H" or "L" level signal or open.P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.P6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data input pin.P6_7/TXD1TXD InputOVCC1Serial data output pin.P6_7/TXD1TXD InputOVCC1Input "H" or "L" level signal or open.P8_0 to P8_3, P8_6, P8_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputIVCC1Input "H" or "L" level signal or open.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P1_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P1_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P1_0 to P11_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0 to P12_7Input Port P12IVCC1Input "H" or "L" level signal or open.P1_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open.P1_0 to P13_7Input Port P13IV	P5_1 to P5_4, P5_6, P5_7	Input Port P5	I	VCC2	Input "H" or "L" level signal or open.
P6_0 to P6_3Input Port P6IVCC1Input "H" or "L" level signal or open.P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.P6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data input pin.P6_7/TXD1TXD InputOVCC1Serial data output pin.P6_7/TXD1TXD InputOVCC1Serial data output pin.P6_7/TXD1TXD InputOVCC1Input "H" or "L" level signal or open.P8_0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_6, P8_7P8_4P8_4 inputIVCC1Input "L" level signal. (3)P8_5/NMINMI InputIVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P11_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P12_7Input Port P11IVCC1Input "H" or "L" level signal or open.P12_0 to P12_7Input Port P12IVCC2Input "H" or "L" level signal or open. (1)P13_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open. (1)	P5_0	CE Input		VCC2	Input "H" level signal.
P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.P6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data input pin.P6_7/TXD1TXD InputOVCC1Serial data output pin.P6_7/0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_0 to P8_3, P8_6, P8_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_4 inputIVCC1Input "H" or "L" level signal or open.P8_5/NMINMI InputIVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P9IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P10IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P12IVCC2Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P13IVCC2Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P11IVCC2Input "H" or "L" level signal or open. <td>P5_5</td> <td>EPM Input</td> <td> </td> <td>VCC2</td> <td>Input "L" level signal.</td>	P5_5	EPM Input		VCC2	Input "L" level signal.
P6_4/RTS1BUSY OutputOVCC1Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.P6_5/CLK1SCLK InputIVCC1Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Standard serial I/O mode 2: Input "L".P6_6/RXD1RXD InputIVCC1Serial data input pin.P6_7/TXD1TXD InputOVCC1Serial data output pin.P6_7/0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_0 to P8_3, P8_6, P8_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_4 inputIVCC1Input "H" or "L" level signal or open.P8_5/NMINMI InputIVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P9IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P10IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P11IVCC1Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P12IVCC2Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P13IVCC2Input "H" or "L" level signal or open.P1_0 to P1_7Input Port P11IVCC2Input "H" or "L" level signal or open. <td>P6_0 to P6_3</td> <td>Input Port P6</td> <td>1</td> <td>VCC1</td> <td>Input "H" or "L" level signal or open.</td>	P6_0 to P6_3	Input Port P6	1	VCC1	Input "H" or "L" level signal or open.
P6_6/RXD1RXD InputIVCC1Serial data input pin.P6_6/RXD1TXD InputOVCC1Serial data output pin. (2)P7_0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_0 to P8_3, P8_6, P8_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputIVCC1Input "L" level signal. (3)P8_5/NMINMI InputIVCC1Connect this pin to VCC1.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P11_7Input Port P12IVCC1Input "H" or "L" level signal or open. (1)P13_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open. (1)	P6_4/RTS1	BUSY Output	0	VCC1	Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program
P6_7/TXD1TXD InputOVCC1Serial data output pin. (2)P7_0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_0 to P8_3, P8_6, P8_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputIVCC1Input "L" level signal. (3)P8_5/NMINMI InputIVCC1Connect this pin to VCC1.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P11_7Input Port P11IVCC1Input "H" or "L" level signal or open.P12_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open. (1)	P6_5/CLK1	SCLK Input	I	VCC1	
P7_0 to P7_7Input Port P7IVCC1Input "H" or "L" level signal or open.P8_0 to P8_3, P8_6, P8_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_4P8_4 inputIVCC1Input "L" level signal. (3)P8_5/NMINMI InputIVCC1Connect this pin to VCC1.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P11_7Input Port P11IVCC1Input "H" or "L" level signal or open.P12_0 to P12_7Input Port P12IVCC2Input "H" or "L" level signal or open. (1)P13_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open. (1)	P6_6/RXD1	RXD Input	I	VCC1	Serial data input pin.
P8_0 to P8_3, P8_6, P8_7Input Port P8IVCC1Input "H" or "L" level signal or open.P8_6, P8_7P8_4 inputIVCC1Input "L" level signal. (3)P8_4P8_4 inputIVCC1Connect this pin to VCC1.P8_5/NMINMI InputIVCC1Connect this pin to VCC1.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P11_7Input Port P11IVCC1Input "H" or "L" level signal or open. (1)P12_0 to P12_7Input Port P12IVCC2Input "H" or "L" level signal or open. (1)P13_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open. (1)	P6_7/TXD1	TXD Input	0	VCC1	Serial data output pin. ⁽²⁾
P8_6, P8_7IVCC1Input "L" level signal. (3)P8_4P8_4 inputIVCC1Input "L" level signal. (3)P8_5/NMINMI InputIVCC1Connect this pin to VCC1.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P11_7Input Port P11IVCC1Input "H" or "L" level signal or open. (1)P12_0 to P12_7Input Port P12IVCC2Input "H" or "L" level signal or open. (1)P13_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open. (1)	P7_0 to P7_7	Input Port P7	I	VCC1	Input "H" or "L" level signal or open.
P8_5/NMI NMI Input I VCC1 Connect this pin to VCC1. P9_0 to P9_7 Input Port P9 I VCC1 Input "H" or "L" level signal or open. P10_0 to P10_7 Input Port P10 I VCC1 Input "H" or "L" level signal or open. P11_0 to P11_7 Input Port P11 I VCC1 Input "H" or "L" level signal or open. P12_0 to P12_7 Input Port P12 I VCC2 Input "H" or "L" level signal or open. P13_0 to P13_7 Input Port P13 I VCC2 Input "H" or "L" level signal or open.	P8_0 to P8_3, P8_6, P8_7	Input Port P8	Ι	VCC1	Input "H" or "L" level signal or open.
P8_5/NMINMI InputIVCC1Connect this pin to VCC1.P9_0 to P9_7Input Port P9IVCC1Input "H" or "L" level signal or open.P10_0 to P10_7Input Port P10IVCC1Input "H" or "L" level signal or open.P11_0 to P11_7Input Port P11IVCC1Input "H" or "L" level signal or open.P12_0 to P12_7Input Port P12IVCC2Input "H" or "L" level signal or open.P13_0 to P13_7Input Port P13IVCC2Input "H" or "L" level signal or open.	P8_4	P8_4 input	I	VCC1	Input "L" level signal. ⁽³⁾
P9_0 to P9_7 Input Port P9 I VCC1 Input "H" or "L" level signal or open. P10_0 to P10_7 Input Port P10 I VCC1 Input "H" or "L" level signal or open. P11_0 to P11_7 Input Port P11 I VCC1 Input "H" or "L" level signal or open. P12_0 to P12_7 Input Port P12 I VCC2 Input "H" or "L" level signal or open. P13_0 to P13_7 Input Port P13 I VCC2 Input "H" or "L" level signal or open.	 P8_5/NMI		I	VCC1	
P10_0 to P10_7 Input Port P10 I VCC1 Input "H" or "L" level signal or open. P11_0 to P11_7 Input Port P11 I VCC1 Input "H" or "L" level signal or open. (1) P12_0 to P12_7 Input Port P12 I VCC2 Input "H" or "L" level signal or open. (1) P13_0 to P13_7 Input Port P13 I VCC2 Input "H" or "L" level signal or open. (1)	 P9_0 to P9_7		I		
P11_0 to P11_7 Input Port P11 I VCC1 Input "H" or "L" level signal or open. ⁽¹⁾ P12_0 to P12_7 Input Port P12 I VCC2 Input "H" or "L" level signal or open. ⁽¹⁾ P13_0 to P13_7 Input Port P13 I VCC2 Input "H" or "L" level signal or open. ⁽¹⁾	P10_0 to P10_7		I	VCC1	
P12_0 to P12_7 Input Port P12 I VCC2 Input "H" or "L" level signal or open. ⁽¹⁾ P13_0 to P13_7 Input Port P13 I VCC2 Input "H" or "L" level signal or open. ⁽¹⁾	 P11_0 to P11_7	•	I		
P13_0 to P13_7 Input Port P13 I VCC2 Input "H" or "L" level signal or open. (1)	P12_0 to P12_7	•	I	VCC2	
P14_0, P14_1 Input Port P14 I VCC1 Input "H" or "L" level signal or open. (1)	P13_0 to P13_7		I	VCC2	
	P14_0, P14_1	Input Port P14	I	VCC1	Input "H" or "L" level signal or open. (1)

Table 22.7 Pin Functions (Flash Memory Standard Serial I/O Mode)

- 1. Available in only the 128-pin version.
- 2. When using the standard serial I/O mode, the internal pull-up is enabled for the TXD1 (P6_7) pin while the RESET pin is "L".
- 3. When using the standard serial I/O mode, the P0_0 to P0_7, P1_0 to P1_7 pins may become indeterminate while the P8_4 pin is "H" and the RESET pin is "L". If this causes a program, apply "L" to the P8_4 pin.

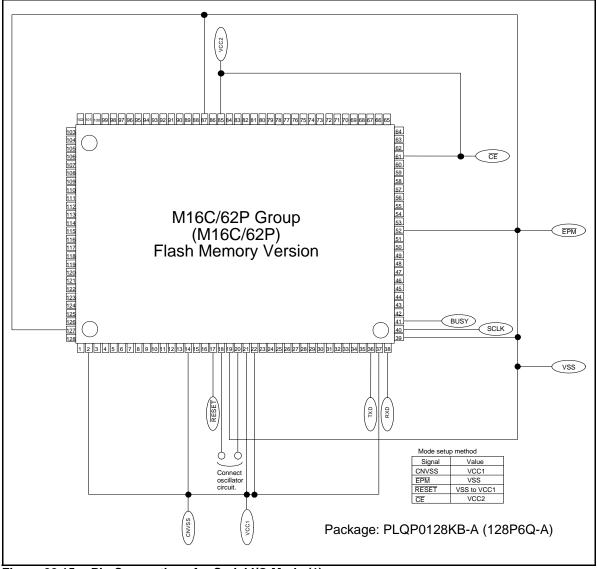
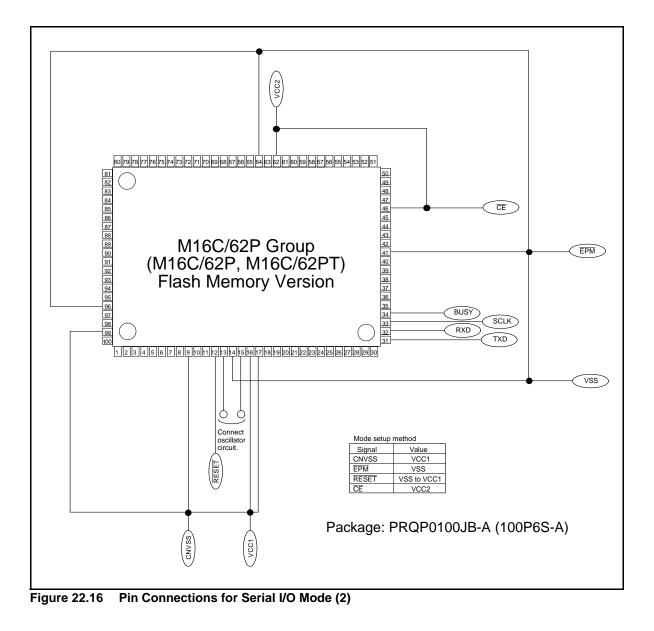


Figure 22.15 Pin Connections for Serial I/O Mode (1)

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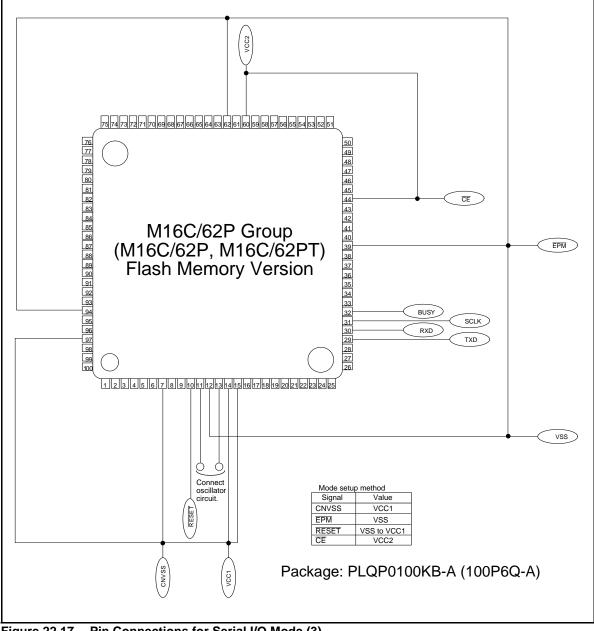


Figure 22.17 Pin Connections for Serial I/O Mode (3)

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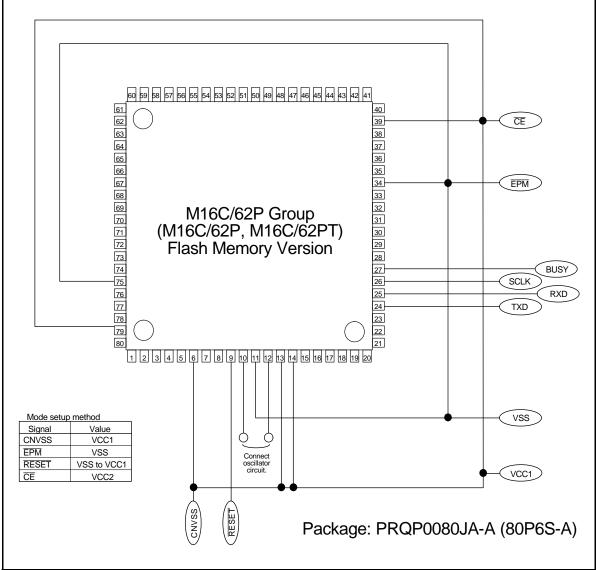
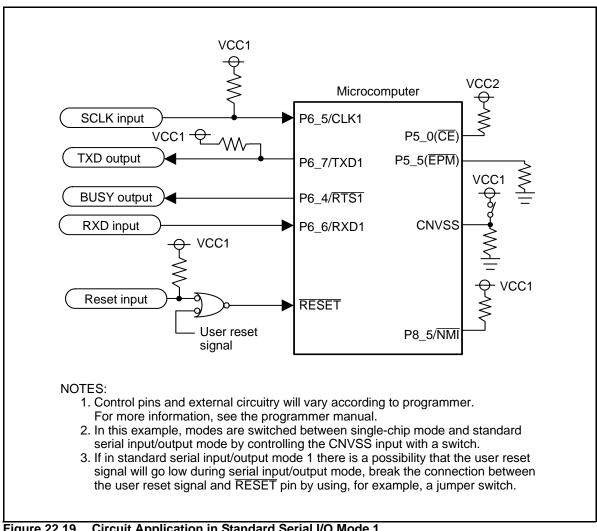


Figure 22.18 Pin Connections for Serial I/O Mode (4)

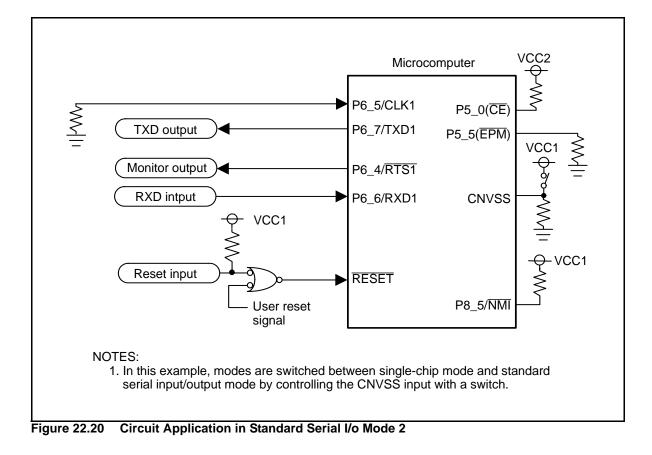
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Example of Circuit Application in the Standard Serial I/O Mode 22.4.2

Figure 22.19 and Figure 22.20 show example of Circuit Application in Standard Serial I/O Mode 1 and Mode 2, respectively. Refer to the user's manual of your serial programmer to handle pins controlled by the serial programmer.



Circuit Application in Standard Serial I/O Mode 1 Figure 22.19



22.5 Parallel I/O Mode

In parallel I/O mode, the user ROM area and the boot ROM area can be rewritten by a parallel programmer supporting the M16C/62P Group (M16C/62P, M16C/62PT). Contact your parallel programmer manufacturer for more information on the parallel programmer. Refer to the user's manual included with your parallel programmer for instructions.

22.5.1 User ROM and Boot ROM Areas

An erase block operation in the boot ROM area is applied to only one 4 Kbyte block. The rewrite control program in standard serial I/O mode is written in the boot ROM area before shipment. Do not rewrite the boot ROM area if using the serial programmer.

In parallel I/O mode, the boot ROM area is located in addresses 0FF000h to 0FFFFFh. Rewrite this address range only if rewriting the boot ROM area. (Do not access addresses other than addresses 0FF000h to 0FFFFFh.)

22.5.2 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten in parallel I/O mode. (Refer to **22.2 Functions To Prevent Flash Memory from Rewriting**.)

23. Electrical Characteristics

23.1 Electrical Characteristics (M16C/62P)

Table 23.1 Absolute Maximum Ratings

Symbol		Parameter	Condition	Rated Value	Unit
VCC1, VCC2	Supply Voltage		Vcc1=AVcc	-0.3 to 6.5	V
VCC2	Supply Voltage		Vcc2	-0.3 to Vcc1+0.1	V
AVcc	Analog Supply V	/oltage	Vcc1=AVcc	-0.3 to 6.5	V
VI	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		-0.3 to Vcc1+0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	V
		P7_0, P7_1		-0.3 to 6.5	V
Vo	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		-0.3 to Vcc1+0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	V
		P7_0, P7_1		-0.3 to 6.5	V
Pd	Power Dissipation	on	–40°C <topr≤85°c< td=""><td>300</td><td>mW</td></topr≤85°c<>	300	mW
Topr	Operating Ambient	When the Microcomputer is Operating		-20 to 85 / -40 to 85	°C
	Temperature	Flash Program Erase		0 to 60	
Tstg	Storage Temper	ature		-65 to 150	°C

NOTES:

1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Cumphel	Parameter			Unit		
Symbol		Faldinelei			Max.	Unit
VCC1, VCC2	Supply Voltage	e (Vcc1 ≥ Vcc2)		5.0	5.5	V
AVcc	Analog Supply V	/oltage		Vcc1		V
Vss	Supply Voltage			0		V
AVss	Analog Supply V	/oltage		0		V
Vih	HIGH Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8Vcc2		VCC2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8Vcc2		Vcc2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0.5Vcc2		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8Vcc1		Vcc1	V
		P7_0, P7_1	0.8Vcc1		6.5	V
VIL	LOW Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2Vcc2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2Vcc2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0		0.16Vcc2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2Vcc	V
IOH(peak)	HIGH Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-10.0	mA
IOH(avg)	HIGH Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-5.0	mA
IOL(peak)	LOW Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
IOL(avg)	LOW Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

 Table 23.2
 Recommended Operating Conditions (1) (1)

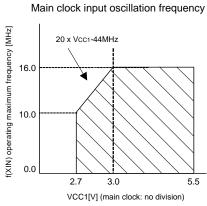
- 1. Referenced to Vcc1 = Vcc2 = 2.7 to 5.5V at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified.
- 2. The Average Output Current is the mean value within 100ms.
- 3. The total IOL(peak) for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80mA max. The total IOL(peak) for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total IOH(peak) for ports P0, P1, and P2 must be -40mA max. The total IOH(peak) for ports P3, P4, P5, P12, and P13 must be -40mA max. The total IOH(peak) for ports P3, P4, P5, P12, and P13 must be -40mA max. The total IOH(peak) for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total IOH(peak) for ports P8_6, P8_7, P9, P10, P14_0, and P14_1 must be -40mA max. Set Average Output Current to 1/2 of peak. The total IOH(peak) for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be -40mA max.
- As for 80-pin version, the total IOL(peak) for all ports and IOH(peak) must be 80mA. max. due to one Vcc and one Vss.
- 4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

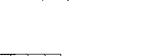
Symbol	Parameter			Standard			
Symbol	Falameter			Тур.	Max.	Unit	
f(XIN)	Main Clock Input Oscillation Frequency ⁽²⁾	VCC1=3.0V to 5.5V	0		16	MHz	
		VCC1=2.7V to 3.0V	0		20×Vcc1 -44	MHz	
f(XCIN)	Sub-Clock Oscillation Frequency			32.768	50	kHz	
f(Ring)	On-chip Oscillation Frequency		0.5	1	2	MHz	
f(PLL)	PLL Clock Oscillation Frequency ⁽²⁾	VCC1=3.0V to 5.5V	10		24	MHz	
		VCC1=2.7V to 3.0V	10		46.67×Vcc1 -116	MHz	
f(BCLK)	CPU Operation Clock	CPU Operation Clock			24	MHz	
ts∪(PLL)	PLL Frequency Synthesizer Stabilization	VCC1=5.5V			20	ms	
	Wait Time	VCC1=3.0V			50	ms	

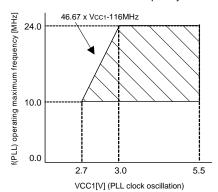
 Table 23.3
 Recommended Operating Conditions (2) ⁽¹⁾

1. Referenced to Vcc1 = Vcc2 = 2.7 to 5.5V at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified.

2. Relationship between main clock oscillation frequency, and supply voltage.







PLL clock oscillation frequency

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Symbol	Parameter		Measuring Condition		Standard			Unit
Symbol	Falalliet	ei	1	Measuring Condition	Min.	Тур.	Max.	Unit
-	Resolution		Vref=V	/CC1			10	Bits
INL	Integral Non-Linearity Error	10bit	VREF= VCC1= 5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			VREF= VCC1= 3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	Vref=V	/cc1=5V, 3.3V			±2	LSB
_	Absolute Accuracy	10bit	VREF= VCC1= 5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			VREF= VCC1 =3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	VREF=VCC1=5V, 3.3V				±2	LSB
_	Tolerance Level Impeda	nce				3		kΩ
DNL	Differential Non-Linearity	/ Error					±1	LSB
_	Offset Error						±3	LSB
-	Gain Error						±3	LSB
RLADDER	Ladder Resistance		Vref=V	/CC1	10		40	kΩ
tCONV	10-bit Conversion Time, Available	it Conversion Time, Sample & Hold ilable		/cc1=5V, ∳AD=12MHz	2.75			μS
tCONV	8-bit Conversion Time, S Available	Sample & Hold	Vref=V	/cc1=5V, ∳AD=12MHz	2.33			μS
tSAMP	Sampling Time				0.25			μS
Vref	Reference Voltage				2.0		Vcc1	V
VIA	Analog Input Voltage				0		Vref	V

 Table 23.4
 A/D Conversion Characteristics ⁽¹⁾

1. Referenced to Vcc1=AVcc=VREF=3.3 to 5.5V, Vss=AVss=0V at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified.

2. If Vcc1 > Vcc2, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

3. ϕ AD frequency must be 12 MHz or less. And divide the fAD if Vcc1 is less than 4.0V, and ϕ AD frequency into 10 MHz or less.

4. When sample & hold is disabled, ϕ AD frequency must be 250 kHz or more, in addition to the limitation in Note 3.

When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

Table 23.5	DIA Conversion Characteristics	.)				
Symbol	Parameter	Magguring Condition		Standard		Unit
Symbol	Farameter	Measuring Condition	Min.	Тур.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
ts∪	Setup Time				3	μS
Ro	Output Resistance		4	10	20	kΩ
IVREF	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

Table 23.5 D/	A Conversion	Characteristics ⁽¹⁾
---------------	--------------	--------------------------------

1. Referenced to Vcc1=VREF=3.3 to 5.5V, Vss=AVss=0V at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified.

 This applies when using one D/A converter, with the D/A register for the unused D/A converter set to "00h". The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not "00h", the IVREF will flow even if Vref id disconnected by the A/D control register.

Table 23.6Flash Memory Version Electrical Characteristics (1) for 100 cycle products (D3, D5, U3, U5)

Symbol	Parameter		Standard			Unit
Symbol	Parameter	rarameter		Тур.	Max.	Unit
_	Program and Erase Endurance ⁽³⁾		100			cycle
_	Word Program Time (Vcc1=5.0V)			25	200	μS
_	Lock Bit Program Time			25	200	μS
_	Block Erase Time	4-Kbyte block		0.3	4	s
_	(Vcc1=5.0V)	8-Kbyte block		0.3	4	S
_	7	32-Kbyte block		0.5	4	S
_	7	64-Kbyte block		0.8	4	S
_	Erase All Unlocked Blocks Time ⁽²⁾				4×n	S
tPS	Flash Memory Circuit Stabilization Wait Time				15	μS
-	Data Hold Time ⁽⁵⁾		10			year

Table 23.7Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (D7, D9,
U7, U9) (Block A and Block 1 (7))

Symbol	Symbol Parameter		Standard			Unit
Symbol			Min.	Тур.	Max.	Unit
-	Program and Erase Endurance (3, 8, 9)		10,000 (4)			cycle
-	Word Program Time (Vcc1=5.0V)			25		μS
-	Lock Bit Program Time			25		μS
-	Block Erase Time (Vcc1=5.0V)	4-Kbyte block		0.3		S
tPS	Flash Memory Circuit Stabilization Wait Time				15	μS
-	Data Hold Time ⁽⁵⁾		10			year

NOTES:

- 1. Referenced to Vcc1=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C (D3, D5, U3, U5) unless otherwise specified.
- 2. n denotes the number of block erases.
- 3. Program and Erase Endurance refers to the number of times a block erase can be performed. If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times. For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
- 4. Maximum number of E/W cycles for which operation is guaranteed.
- 5. Topr = -40 to 85 °C (D3, D7, U3, U7) / -20 to 85 °C (D5, D9, U5, U9).
- 6. Referenced to Vcc1 = 4.5 to 5.5V, 3.0 to 3.6V at Topr = -40 to 85 °C (D7, U7) / -20 to 85 °C (D9, U9) unless otherwise specified.
- 7. Table 23.7 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 23.6.
- To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to
 unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For
 example, an 8-word program can be written 256 times maximum before erase becomes necessary.
 Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the
 total number of times erasure is used.
- 9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
- 10. Set the PM17 bit in the PM1 register to "1" (wait state) when executing more than 100 times rewrites (D7, D9, U7 and U9).
- 11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 23.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics (at Topr = 0 to 60 °C(D3, D5, U3, U5), Topr = -40 to 85 °C(D7, U7) / Topr = -20 to 85 °C(D9, U9))

Flash Program, Erase Voltage	Flash Read Operation Voltage
$VCC1 = 3.3 V \pm 0.3 V \text{ or } 5.0 V \pm 0.5 V$	Vcc1=2.7 to 5.5 V

Symbol	Parameter	Manauring Condition		Unit		
		Measuring Condition	Min.	Тур.	Max.	Unit
Vdet4	Low Voltage Detection Voltage (1)	Vcc1=0.8V to 5.5V	3.3	3.8	4.4	V
Vdet3	Reset Level Detection Voltage (1, 2)		2.2	2.8	3.6	V
Vdet4-Vdet3	Electric potential difference of Low Voltage Detection and Reset Level Detection		0.3			V
Vdet3s	Low Voltage Reset Retention Voltage				0.8	V
Vdet3r	Low Voltage Reset Release Voltage (3)	7	2.2	2.9	4.0	V

Table 23.9 Low Voltage Detection Circuit Electrical Characteristics

NOTES:

1. Vdet4 > Vdet3.

 Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.

3. Vdet3r > Vdet3 is not guaranteed.

4. The voltage detection circuit is designed to use when VCC1 is set to 5V.

Table 23.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard	Standard		Unit
	raiaillelei	measuring Condition	Min.	Тур.	Max.	Unit
td(P-R)	Time for Internal Power Supply Stabilization During Powering-On	Vcc1=2.7V to 5.5V			2	ms
td(R-S)	STOP Release Time				150	μS
td(W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	μS
td(S-R)	Brown-out Detection Reset (Hardware Reset 2) Release Wait Time	VCC1=Vdet3r to 5.5V		6 (1)	20	ms
td(E-A)	Low Voltage Detection Circuit Operation Start Time	Vcc1=2.7V to 5.5V			20	μS

NOTES:

1. When Vcc1 = 5V.

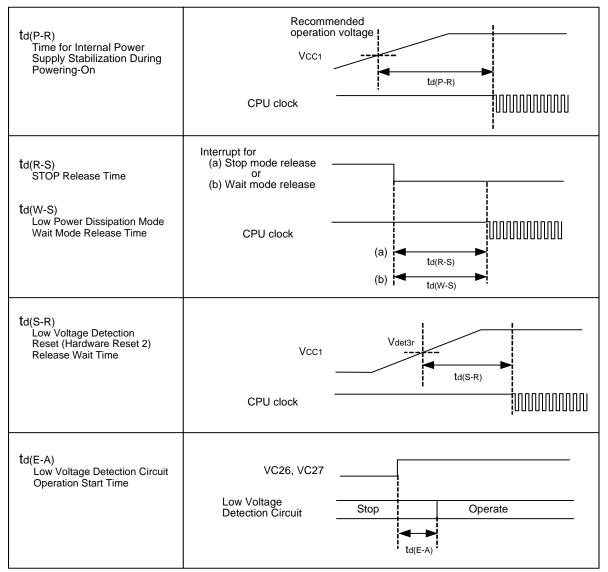


Figure 23.1 Power Supply Circuit Timing Diagram

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Symbol		Parameter		Measuring Condition		andard		Unit
•				-	Min.	Тур.	Max.	0
Vон	HIGH Output Voltage ⁽³⁾	P6_0 to P6_7, P7_2 to P7_7 P8_6, P8_7, P9_0 to P9_7, I P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	IOH=-5mA	Vcc1-2.0		Vcc1	v
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOH=-5mA ⁽²⁾	Vcc2-2.0		Vcc2	
Vон	HIGH Output Voltage ⁽³⁾	P6_0 to P6_7, P7_2 to P7_7 P8_6, P8_7, P9_0 to P9_7, I P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	ОН=-200μА	Vcc1-0.3		Vcc1	.,
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	, P5_0 to P5_7,	IOH=-200μA ⁽²⁾	Vcc2-0.3		Vcc2	V
Vон	HIGH Outpu	t Voltage XOUT	HIGHPOWER	IOH=-1mA	Vcc1-2.0		VCC1	
			LOWPOWER	IOH=-0.5mA	Vcc1-2.0		VCC1	V
	HIGH Outpu	t Voltage XCOUT	HIGHPOWER	With no load applied		2.5		
			LOWPOWER	With no load applied		1.6		V
Vol	LOW Output Voltage ⁽³⁾	P6_0 to P6_7, P7_0 to P7_7 P8_6, P8_7, P9_0 to P9_7, I P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	IOL=5mA			2.0	v
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOL=5mA (2)			2.0	
Vol	LOW Output Voltage ⁽³⁾	P6_0 to P6_7, P7_0 to P7_7 P8_6, P8_7, P9_0 to P9_7, I P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	IOL=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	, P5_0 to P5_7,	IOL=200μA ⁽²⁾			0.45	-
Vol	LOW Output	Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	
			LOWPOWER	IOL=0.5mA			2.0	V
	LOW Output	Voltage XCOUT	HIGHPOWER	With no load applied		0		v
			LOWPOWER	With no load applied		0		v
Vt+-Vt-	Hysteresis	HOLD, RDY, TAOIN to TA4II INTO to INT5, NMI, ADTRG, I TAOOUT to TA4OUT, KIO to SCL0 to SCL2, SDA0 to SD/	CTS0 to CTS2, CLK0 to CLK4, KI3, RXD0 to RXD2,		0.2		1.0	v
VT+-VT-	Hysteresis	RESET			0.2		2.5	V
Ін	HIGH Input Current ⁽³⁾	P0_0 to P0_7, P1_0 to P1_7,	12_7, P13_0 to P13_7,	VI=5V			5.0	μΑ
lı∟	LOW Input Current ⁽³⁾		12_7, P13_0 to P13_7,	VI=0V			-5.0	μA
Rpullup	Pull-Up Resistance	P0_0 to P0_7, P1_0 to P1_7, P4_0 to P4_7, P5_0 to P5_7	, P2_0 to P2_7, P3_0 to P3_7, , P6_0 to P6_7, P7_2 to P7_7, P9_0 to P9_7, P10_0 to P10_7,	Vi=0V	30	50	170	kΩ
Rfxin	Feedback R	esistance XIN				1.5		MΩ
RfxCIN	Feedback R					1.5		MΩ
		ion Voltage		At stop mode	2.0	.0	<u> </u>	V

Table 23.11 Electrical Characteristics (1) (1)

NOTES: 1. Referenced to Vcc1=Vcc2=4.2 to 5.5V, Vss = 0V at Topr = -20 to 85°C / -40 to 85°C, f(BCLK)=24MHz unless otherwise

specified. 2. Where the product is used at Vcc1 = 5 V and Vcc2 = 3 V, refer to the 3 V version value for the pin specified value on Vcc2 port side.

3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Symbol	Paramete		Maga	uring Condition	Ş	Standard	d	Unit
Symbol	Falamete	÷1	Ivieas	Measuring Condition		Min. Typ. Max.		Unin
lcc		In single-chip mode, the output	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
	·	pins are open and other pins are Vss		No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
			,	No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=5.0V		15		mA
	Erase VC Mask ROM f(X	f(BCLK)=10MHz, VCC1=5.0V		25		mA		
		f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μΑ		
				f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		50		μA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5		μA
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		2.0		μA
				Stop mode Topr =25°C		0.8	3.0	μA
Idet4	Low Voltage Detection Diss	ipation Current (4)				0.7	4	μA
Idet3	Reset Area Detection Dissip	pation Current ⁽⁴⁾				1.2	8	μA

Table 23.12 Electrical Characteristics (2) ⁽¹⁾

NOTES:
1. Referenced to Vcc1=Vcc2=4.2 to 5.5V, Vss = 0V at Topr = -20 to 85°C / -40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. Idet is dissipation current when the following bit is set to "1" (detection circuit enabled).

Idet4: VC27 bit in the VCR2 register

Idet3: VC26 bit in the VCR2 register

Timing Requirements

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.13 External Clock Input (XIN input) (1)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Onit
tc	External Clock Input Cycle Time	62.5		ns
tw(H)	External Clock Input HIGH Pulse Width	25		ns
tw(L)	External Clock Input LOW Pulse Width	25		ns
tr	External Clock Rise Time		15	ns
tr	External Clock Fall Time		15	ns

NOTES:

1. The condition is Vcc1=Vcc2=3.0 to 5.0V.

Table 23.14 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Star	Standard		
Symbol	Falailletei	Min.	Max.	Unit	
tac1(RD-DB)	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns	
tac2(RD-DB)	Data Input Access Time (for setting with wait)		(NOTE 2)	ns	
tac3(RD-DB)	Data Input Access Time (when accessing multiplex bus area)		(NOTE 3)	ns	
tsu(DB-RD)	Data Input Setup Time	40		ns	
tsu(RDY-BCLK)	RDY Input Setup Time	30		ns	
tsu(HOLD-BCLK)	HOLD Input Setup Time	40		ns	
th(RD-DB)	Data Input Hold Time	0		ns	
th(BCLK-RDY)	RDY Input Hold Time	0		ns	
th(BCLK-HOLD)	HOLD Input Hold Time	0		ns	

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)x10^9}{f(BCLK)} - 45[ns]$$
n is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

n

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Timing Requirements

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.15 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tc(TA)	TAilN Input Cycle Time	100		ns
tw(TAH)	TAilN Input HIGH Pulse Width	40		ns
tw(TAL)	TAilN Input LOW Pulse Width	40		ns

Table 23.16 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tc(TA)	TAilN Input Cycle Time	400		ns
tw(TAH)	TAilN Input HIGH Pulse Width	200		ns
tw(TAL)	TAilN Input LOW Pulse Width	200		ns

Table 23.17 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tc(TA)	TAilN Input Cycle Time	200		ns
tw(TAH)	TAilN Input HIGH Pulse Width	100		ns
tw(TAL)	TAIIN Input LOW Pulse Width	100		ns

Table 23.18 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Onit
tw(TAH)	TAIIN Input HIGH Pulse Width	100		ns
tw(TAL)	TAIIN Input LOW Pulse Width	100		ns

Table 23.19 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Onit
tc(UP)	TAiOUT Input Cycle Time	2000		ns
tw(UPH)	TAiOUT Input HIGH Pulse Width	1000		ns
tw(UPL)	TAiOUT Input LOW Pulse Width	1000		ns
tsu(UP-TIN)	TAiOUT Input Setup Time	400		ns
th(TIN-UP)	TAiOUT Input Hold Time	400		ns

Table 23.20 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tc(TA)	TAiIN Input Cycle Time	800		ns
tsu(TAIN-TAOUT)	TAiOUT Input Setup Time	200		ns
tsu(TAOUT-TAIN)	TAIIN Input Setup Time	200		ns

Timing Requirements

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.21 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Star	ndard	Unit
	Falameter	Min.	Max.	Unit
tc(TB)	TBiIN Input Cycle Time (counted on one edge)	100		ns
tw(TBH)	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
tw(TBL)	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
tc(TB)	TBiIN Input Cycle Time (counted on both edges)	200		ns
tw(TBH)	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
tw(TBL)	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 23.22 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit	
	Farameter	Min.	Max.	Onit	
tc(TB)	TBiIN Input Cycle Time	400		ns	
tw(TBH)	TBiIN Input HIGH Pulse Width	200		ns	
tw(TBL)	TBiIN Input LOW Pulse Width	200		ns	

Table 23.23 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Stan	dard	Unit
	Farameter	Min.	Max.	Offic
tc(TB)	TBiIN Input Cycle Time	400		ns
tw(TBH)	TBiIN Input HIGH Pulse Width	200		ns
tw(TBL)	TBiIN Input LOW Pulse Width	200		ns

Table 23.24 A/D Trigger Input

Symbol	Parameter	Stan	dard	Unit
	Farameter	Min.	Max.	Offic
tc(AD)	ADTRG Input Cycle Time	1000		ns
tw(ADL)	ADTRG input LOW Pulse Width	125		ns

Table 23.25 Serial Interface

Symbol	Parameter	Standard	Unit	
Symbol	Falanielei	Min.	Max.	Offic
tc(CK)	CLKi Input Cycle Time	200		ns
tw(CKH)	CLKi Input HIGH Pulse Width	100		ns
tw(CKL)	CLKi Input LOW Pulse Width	100		ns
td(C-Q)	TXDi Output Delay Time		80	ns
th(C-Q)	TXDi Hold Time	0		ns
tsu(D-C)	RXDi Input Setup Time	70		ns
t h(C-D)	RXDi Input Hold Time	90		ns

Table 23.26 External Interrupt INTi Input

Symbol	Symbol	Parameter	Stan	dard	Unit
	Falanielei	Min.	Min. Max.	Onit	
tw(IN	IH)	INTi Input HIGH Pulse Width	250		ns
tw(IN	IL)	INTi Input LOW Pulse Width	250		ns

Switching Characteristics

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Currente a l	Parameter		Stan	dard	Unit
Symbol	Farameter		Min.	Max.	Unit
td(BCLK-AD)	Address Output Delay Time			25	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			25	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			15	ns
th(BCLK-ALE)	ALE Signal Output Hold Time	Co.o.	-4		ns
td(BCLK-RD)	RD Signal Output Delay Time	See Figure 23.2		25	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			25	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

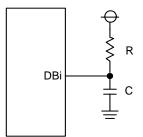
$$\frac{0.5 \times 10^9}{f(BCLK)} - 40[ns] \qquad f(BCLK) \text{ is } 12.5 \text{MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

= 6.7ns.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus. Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value. Hold time of data bus is expressed in t = -CR X ln (1-VoL / Vcc2) by a circuit of the right figure. For example, when VoL = 0.2Vcc2, C = 30pF, R = 1kΩ, hold time of output "L" level is t = -30pF X 1k Ω X ln(1-0.2Vcc2 / Vcc2)



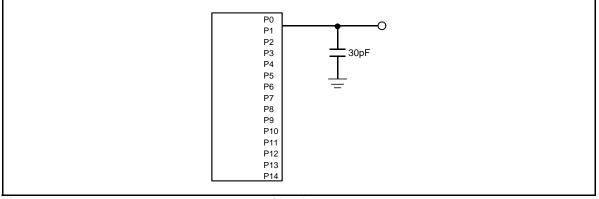


Figure 23.2 Ports P0 to P14 Measurement Circuit

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Switching Characteristics

(Vcc1 = Vcc2 = 5V, Vss = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.28	Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external
	area access)

Symbol	Parameter		Stan	dard	Unit	
Symbol	Falanelei		Min. Max.		Onic	
td(BCLK-AD)	Address Output Delay Time			25	ns	
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns	
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns	
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns	
td(BCLK-CS)	Chip Select Output Delay Time			25	ns	
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns	
td(BCLK-ALE)	ALE Signal Output Delay Time			15	ns	
th(BCLK-ALE)	ALE Signal Output Hold Time	0	-4		ns	
td(BCLK-RD)	RD Signal Output Delay Time	See Figure 23.2		25	ns	
th(BCLK-RD)	RD Signal Output Hold Time	1 igure 23.2	0		ns	
td(BCLK-WR)	WR Signal Output Delay Time			25	ns	
th(BCLK-WR)	WR Signal Output Hold Time		0		ns	
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns	
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns	
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns	
th(WR-DB)	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns	
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns	

NOTES:

1. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5)x10^9}{f(BCLK)} - 40[ns]$

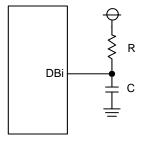
n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. (BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 x 10^9}{f(BCLK)} - 10[ns]$$

= 6.7ns.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus. Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value. Hold time of data bus is expressed in $t = -CR X \ln (1 - VoL / Vcc2)$ by a circuit of the right figure. For example, when VoL = 0.2Vcc2, C = 30pF, R = 1k\Omega, hold time of output "L" level is $t = -30pF X 1k\Omega X \ln(1-0.2Vcc2 / Vcc2)$



Switching Characteristics

(Vcc1 = Vcc2 = 5V, Vss = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.29	Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area
	access and multiplex bus selection)

Symbol	Parameter		Stan	dard	Unit
Symbol	Falameter		Min.	Max.	Unit
td(BCLK-AD)	Address Output Delay Time			25	ns
t h(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
t h(RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
t h(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip Select Output Delay Time			25	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
t h(RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			25	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			25	ns
th(BCLK-WR)	WR Signal Output Hold Time	See	0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)	Figure 23.2		40	ns
t h(BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
t h(WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns
td(BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			15	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		-4		ns
td(AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
th(AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
td(AD-RD)	RD Signal Output Delay From the End of Address		0		ns
td(AD-WR)	WR Signal Output Delay From the End of Address		0		ns
tdz(RD-AD)	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

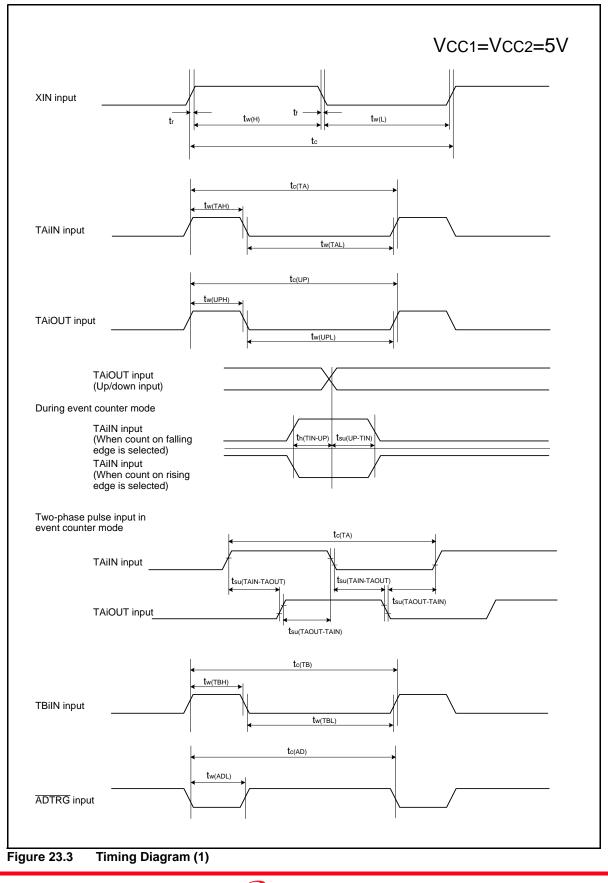
2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)x10^9}{f(BCLK)} - 40[ns] \qquad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

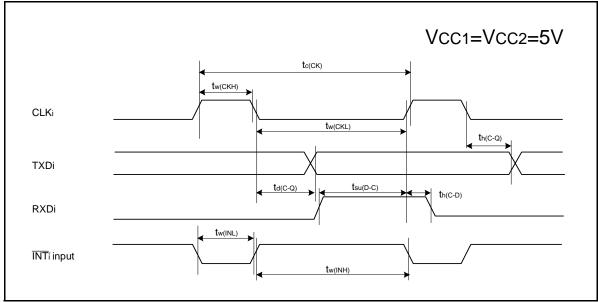
3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25[ns]$$

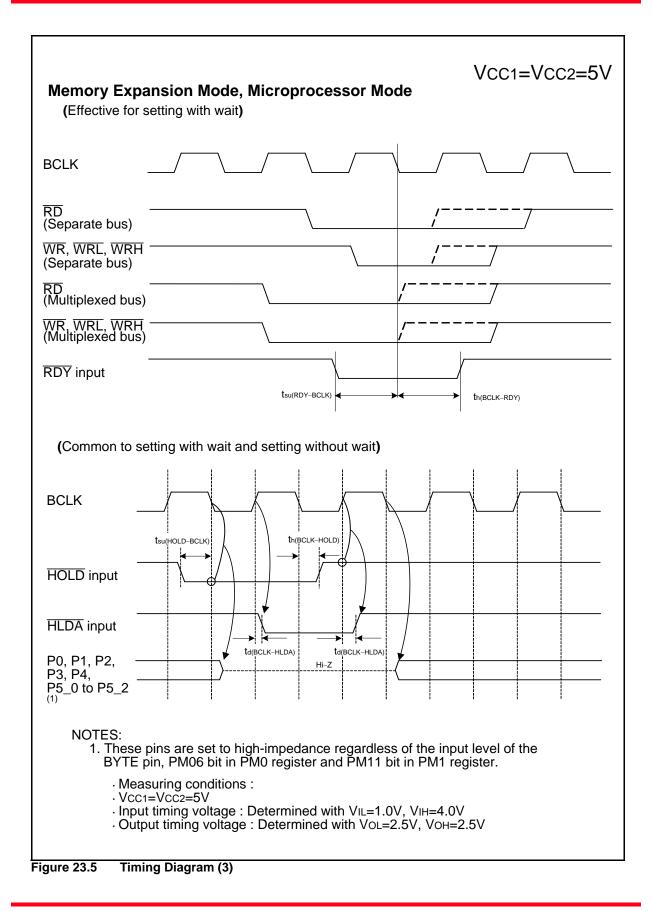
4. Calculated according to the BCLK frequency as follows:



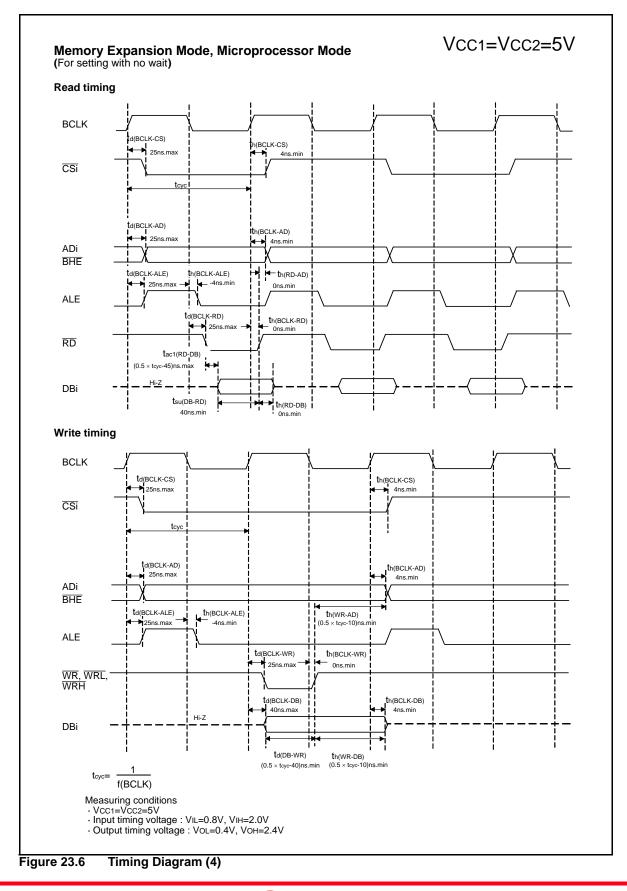
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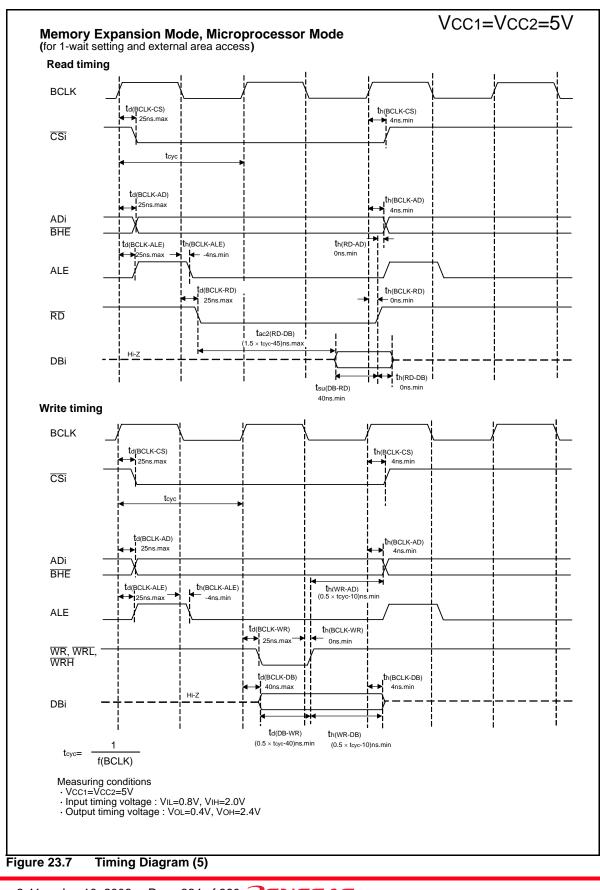




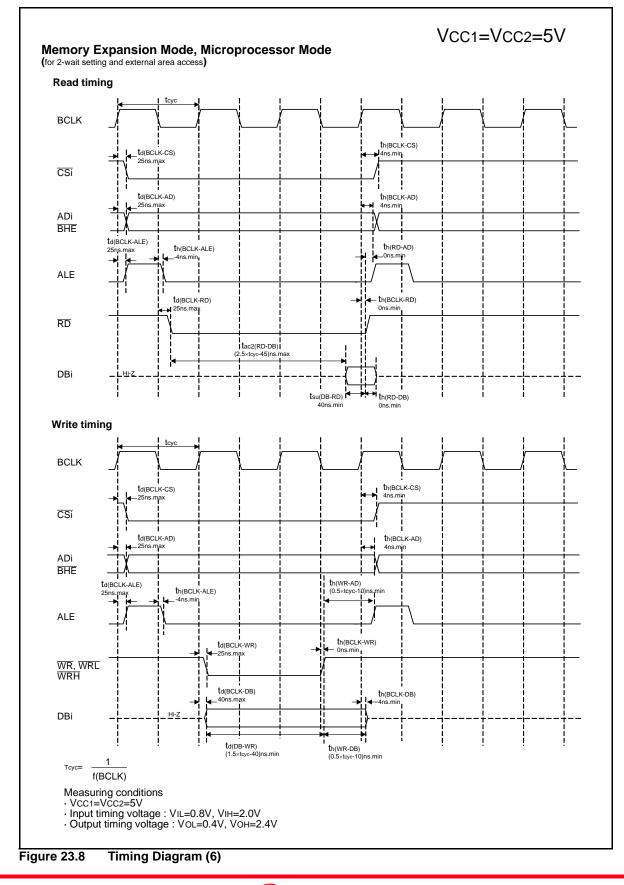
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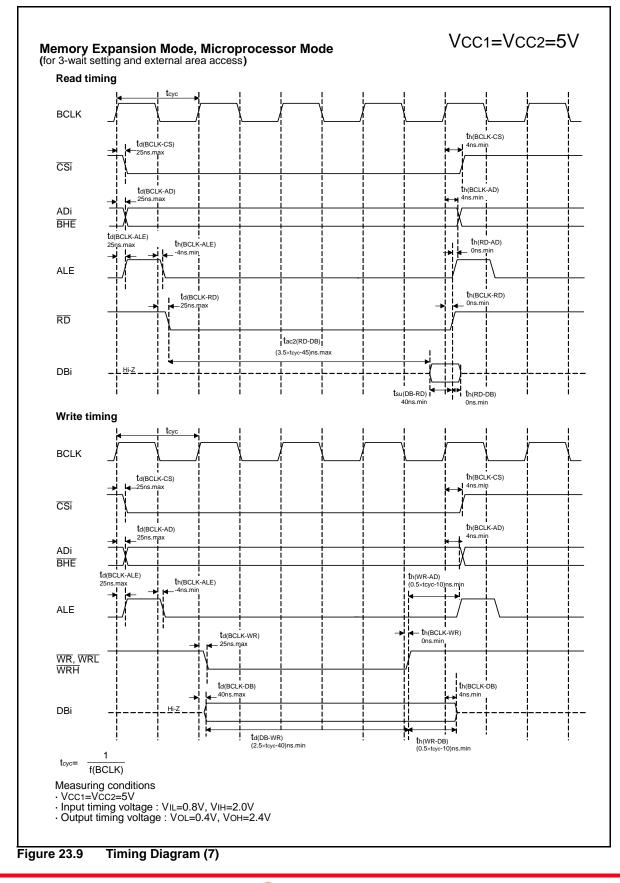
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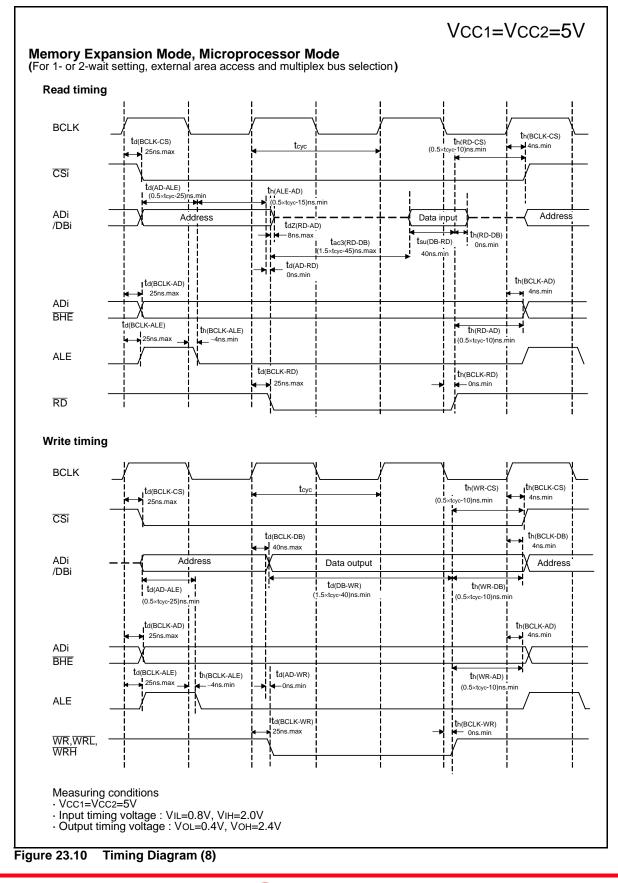
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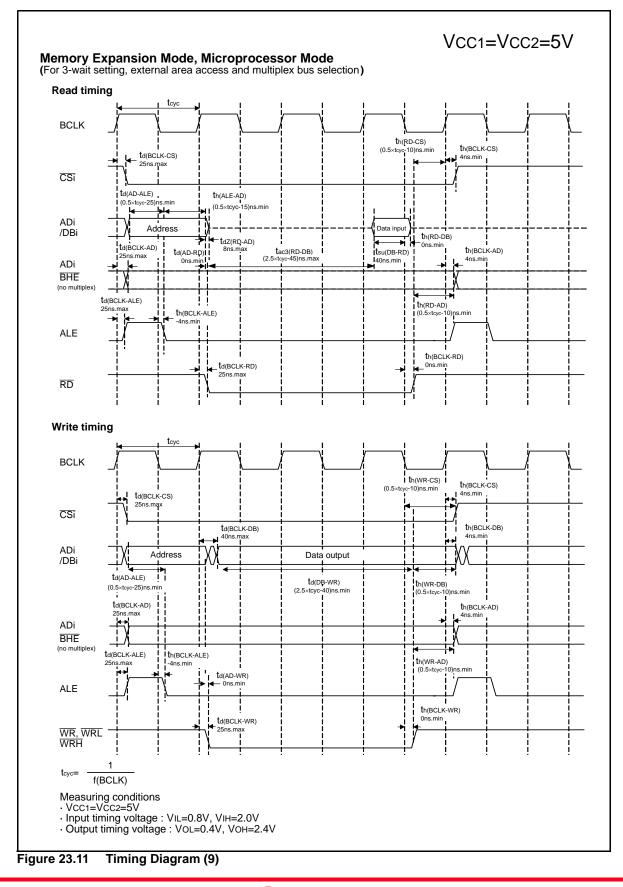
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Symbol	Parameter		Measuring Condition	Standard			Unit	
Symbol		Farameter		weasuring condition	Min.	Тур.	Max.	011
Vон	HIGH Output Voltage ⁽³⁾			IOH=-1mA	Vcc1-0.5		Vcc1	v
		P0_0 to P0_7, P1_0 to P1_ P3_0 to P3_7, P4_0 to P4_ P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOH=-1mA ⁽²⁾	Vcc2-0.5		Vcc2	v
Vон	HIGH Output	Voltage XOUT	HIGHPOWER	IOH=-0.1mA	Vcc1-0.5		Vcc1	v
			LOWPOWER	ІОН=-50μА	Vcc1-0.5		VCC1	
	HIGH Output	Voltage XCOUT	HIGHPOWER	With no load applied		2.5		v
			LOWPOWER	With no load applied		1.6		l v
Vol	LOW Output Voltage ⁽³⁾	P6_0 to P6_7, P7_0 to P7_ P8_6, P8_7, P9_0 to P9_7, P11_0 to P11_7, P14_0, P1	P10_0 to P10_7,	IOL=1mA			0.5	v
		P0_0 to P0_7, P1_0 to P1_ P3_0 to P3_7, P4_0 to P4_ P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOL=1mA ⁽²⁾			0.5	
Vol	LOW Output \	/oltage XOUT	HIGHPOWER	IOL=0.1mA			0.5	v
			LOWPOWER	IOL=50μA			0.5	ľ
LOW Output	/oltage XCOUT	HIGHPOWER	With no load applied		0		v	
			LOWPOWER	With no load applied		0		v
Vt+-Vt-	Hysteresis	HOLD, RDY, TA0IN to TA4 TB0IN to TB5IN, INTO to IN ADTRG, CTS0 to CTS2, CL TA0OUT to TA4OUT, KI0 to SCL0 to SCL2, SDA0 to SD	T5, NMI, .K <u>0 to</u> CLK4, o KI3, RXD0 to RXD2,		0.2		0.8	v
Vt+-Vt-	Hysteresis	RESET			0.2	(0.7)	1.8	V
Ін	HIGH Input Current ⁽³⁾	P0_0 to P0_7, P1_0 to P1_ P3_0 to P3_7, P4_0 to P4_ P6_0 to P6_7, P7_0 to P7_ P9_0 to P9_7, P10_0 to P1 P12_0 to P12_7, P13_0 to 1 XIN, RESET, CNVSS, BYT	7, P5_0 to P5_7, 7, P8_0 to P8_7, 0_7, P11_0 to P11_7, P13_7, P14_0, P14_1,	VI=3V			4.0	μΑ
lı.	LOW Input Current ⁽³⁾	P0_0 to P0_7, P1_0 to P1_ P3_0 to P3_7, P4_0 to P4_ P6_0 to P6_7, P7_0 to P7_ P9_0 to P9_7, P10_0 to P1 P12_0 to P12_7, P13_0 to 1 XIN, RESET, CNVSS, BYT	7, P5_0 to P5_7, 7, P8_0 to P8_7, 0_7, P11_0 to P11_7, P13_7, P14_0, P14_1,	VI=0V			-4.0	μΑ
Rpullup	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_ to P3_7, P4_0 to P4_7, P5_ P6_7, P7_2 to P7_7, P8_0 P9_0 to P9_7, P10_0 to P10_ P11_0 to P11_7, P12_0 to P P14_0, P14_1	7, P2_0 to P2_7, P3_0 _0 to P5_7, P6_0 to to P8_4, P8_6, P8_7, 0_7,	VI=0V	50	100	500	kΩ
Rfxin	Feedback Res	sistance XIN				3.0		MC
Rfxcin	Feedback Res	sistance XCIN				25		MΩ
Vram	RAM Retentio	n Voltage		At stop mode	2.0			V

Table 23.30 Electrical Characteristics (1) (1)

NOTES:

 Referenced to Vcc1 = Vcc2 = 2.7 to 3.3V, Vss = 0V at Topr = -20 to 85°C / -40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.

2. Vcc1 for the port P6 to P11 and P14, and Vcc2 for the port P0 to P5 and P12 to P13

3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

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Symbol			Massuring Condition		Standard		Unit	
Symbol			Min.	Тур.	Max.	Uni		
lcc		mode, the output pins are open and		f(BCLK)=10MHz No division		8	11	mA
	pins are open and other pins are Vss Flash Memory Flash Memory Flash Memory			No division, On-chip oscillation		1		mA
			f(BCLK)=10MHz, No division		8	13	mA	
		No division, On-chip oscillation		1.8		mA		
		f(BCLK)=10MHz, VCC1=3.0V		12		mA		
		f(BCLK)=10MHz, VCC1=3.0V		22		mA		
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μΑ
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		45		μA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		6.0		μΑ
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		1.8		μA
				Stop mode Topr =25°C		0.7	3.0	μA
Idet4	Low Voltage Detection Diss	ipation Current (4)				0.6	4	μA
Idet3	Reset Area Detection Dissip	pation Current (4)				0.4	2	μA

 Table 23.31
 Electrical Characteristics (2) (1)

NOTES:

Referenced to Vcc1=Vcc2=2.7 to 3.3V, Vss = 0V at Topr = -20 to 85°C / -40 to 85°C, f(BCLK)=10MHz unless otherwise specified.
With one timer operated using fC32.
This indicates the memory in which the program to be executed exists.
Idet is dissipation current when the following bit is set to "1" (detection circuit enabled).

Idet4: VC27 bit in the VCR2 register

Idet3: VC26 bit in the VCR2 register

Timing Requirements

(Vcc1 = Vcc2 = 3V, Vss = 0V, at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified)

Table 23.32 External Clock Input (XIN input)⁽¹⁾

Symbol	Parameter	Stan	Unit	
	Farameter	Min.	Max.	Onit
tc	External Clock Input Cycle Time	(NOTE 2)		ns
tw(H)	External Clock Input HIGH Pulse Width	(NOTE 3)		ns
ťw(L)	External Clock Input LOW Pulse Width	(NOTE 3)		ns
tr	External Clock Rise Time		(NOTE 4)	ns
tr	External Clock Fall Time		(NOTE 4)	ns

NOTES:

- 1. The condition is Vcc1=Vcc2=2.7 to 3.0V.
- 2. Calculated according to the Vcc1 voltage as follows:

 $\frac{10^{-6}}{20 \times V \text{CC2} - 44} \text{ [ns]}$

3. Calculated according to the Vcc1 voltage as follows:

 10^{-6} $\frac{10}{20\times V\text{CC1}-44}\times 0.4\,[\text{ns}]$

4. Calculated according to the Vcc1 voltage as follows:

-10 × Vcc1 + 45 [ns]

Table 23.33 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Star	Standard		
	Palameter	Min.	Max.	Unit	
tac1(RD-DB)	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns	
tac2(RD-DB)	Data Input Access Time (for setting with wait)		(NOTE 2)	ns	
tac3(RD-DB)	Data Input Access Time (when accessing multiplex bus area)		(NOTE 3)	ns	
tsu(DB-RD)	Data Input Setup Time	50		ns	
tsu(RDY-BCLK)	RDY Input Setup Time	40		ns	
tsu(HOLD-BCLK)	HOLD Input Setup Time	50		ns	
th(RD-DB)	Data Input Hold Time	0		ns	
th(BCLK-RDY)	RDY Input Hold Time	0		ns	
th(BCLK-HOLD)	HOLD Input Hold Time	0		ns	

NOTES:

1. Calculated according to the BCLK frequency as follows:

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5)x10^9}{f(BCLK)} - 60[ns]$$
 n is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5)x10^9}{f(BCLK)} = 60[ns]$ n is "2" for 2-wait setting, "3" for 3-wait setting.

Timing Requirements

(VCC1 = VCC2 = 3V, VSS = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.34 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
	Farameter	Min.	Max.	Offic
tc(TA)	TAiIN Input Cycle Time	150		ns
tw(TAH)	TAIIN Input HIGH Pulse Width	60		ns
tw(TAL)	TAIIN Input LOW Pulse Width	60		ns

Table 23.35 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Stan	Unit	
	Farameter	Min.	Max.	Offic
tc(TA)	TAilN Input Cycle Time	600		ns
tw(TAH)	TAilN Input HIGH Pulse Width	300		ns
tw(TAL)	TAIIN Input LOW Pulse Width	300		ns

Table 23.36 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Stan	Unit	
	Falameter	Min.	Max.	Offic
tc(TA)	TAilN Input Cycle Time	300		ns
tw(TAH)	TAilN Input HIGH Pulse Width	150		ns
tw(TAL)	TAIIN Input LOW Pulse Width	150		ns

Table 23.37 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tw(TAH)	TAIIN Input HIGH Pulse Width	150		ns
tw(TAL)	TAIIN Input LOW Pulse Width	150		ns

Table 23.38 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tc(UP)	TAiOUT Input Cycle Time	3000		ns
tw(UPH)	TAiOUT Input HIGH Pulse Width	1500		ns
tw(UPL)	TAiOUT Input LOW Pulse Width	1500		ns
tsu(UP-TIN)	TAiOUT Input Setup Time	600		ns
th(TIN-UP)	TAiOUT Input Hold Time	600		ns

Table 23.39 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
Symbol	Farameter	Min.	Max.	Offic
tc(TA)	TAiIN Input Cycle Time	2		μs
tsu(TAIN-TAOUT)	TAiOUT Input Setup Time	500		ns
tsu(TAOUT-TAIN)	TAIIN Input Setup Time	500		ns

Timing Requirements

(VCC1 = VCC2 = 3V, VSS = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.40 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Star	Standard		
		Min.	Max.	Unit	
tc(TB)	TBiIN Input Cycle Time (counted on one edge)	150		ns	
tw(TBH)	TBiIN Input HIGH Pulse Width (counted on one edge)	60		ns	
tw(TBL)	TBiIN Input LOW Pulse Width (counted on one edge)	60		ns	
tc(TB)	TBiIN Input Cycle Time (counted on both edges)	300		ns	
tw(TBH)	TBiIN Input HIGH Pulse Width (counted on both edges)	120		ns	
tw(TBL)	TBiIN Input LOW Pulse Width (counted on both edges)	120		ns	

Table 23.41 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tc(TB)	TBilN Input Cycle Time	600		ns
tw(TBH)	TBilN Input HIGH Pulse Width	300		ns
tw(TBL)	TBiIN Input LOW Pulse Width	300		ns

Table 23.42 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tc(TB)	TBilN Input Cycle Time	600		ns
tw(TBH)	TBiIN Input HIGH Pulse Width	300		ns
tw(TBL)	TBiIN Input LOW Pulse Width	300		ns

Table 23.43 A/D Trigger Input

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Onit
tc(AD)	ADTRG Input Cycle Time	1500		ns
tw(ADL)	ADTRG Input LOW Pulse Width	200		ns

Table 23.44 Serial Interface

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Onit
tc(CK)	CLKi Input Cycle Time	300		ns
tw(CKH)	CLKi Input HIGH Pulse Width	150		ns
tw(CKL)	CLKi Input LOW Pulse Width	150		ns
td(C-Q)	TXDi Output Delay Time		160	ns
th(C-Q)	TXDi Hold Time	0		ns
tsu(D-C)	RXDi Input Setup Time	100		ns
th(C-D)	RXDi Input Hold Time	90		ns

Table 23.45 External Interrupt INTi Input

Symbol	Parameter	Stan	Unit	
		Min.	Max.	Offic
tw(INH)	INTi Input HIGH Pulse Width	380		ns
tw(INL)	INTi Input LOW Pulse Width	380		ns

Switching Characteristics

(Vcc1 = Vcc2 = 3V, Vss = 0V, at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified)

Symbol	Parameter		Stan	dard	Unit
Symbol	Parameter		Min.	Max.	Unit
td(BCLK-AD)	Address Output Delay Time			30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time	0	-4		ns
td(BCLK-RD)	RD Signal Output Delay Time	See Figure 23.12		30	ns
th(BCLK-RD)	RD Signal Output Hold Time	I Igure 25.12	0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

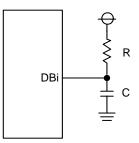
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40[ns] \qquad f(BCLK) \text{ is } 12.5 \text{MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} = 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus. Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value. Hold time of data bus is expressed in t = -CR X ln (1-VoL / Vcc2) by a circuit of the right figure. For example, when VoL = 0.2Vcc2, C = 30pF, R = 1kΩ, hold time of output "L" level is t = -30pF X 1k Ω X ln(1-0.2Vcc2 / Vcc2) = 6.7ns.



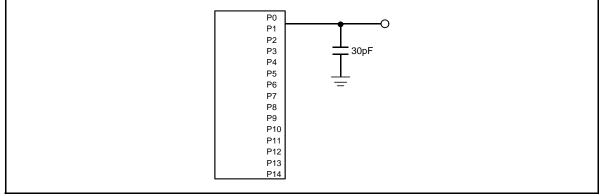


Figure 23.12 Ports P0 to P14 Measurement Circuit

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Switching Characteristics

(Vcc1 = Vcc2 = 5V, Vss = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.47	Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external
	area access)

Symbol	Parameter		Stan	dard	Unit
Symbol	Farameter		Min.	Max.	Unit
td(BCLK-AD)	Address Output Delay Time			30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		-4		ns
td(BCLK-RD)	RD Signal Output Delay Time	End See Figure 23.12		30	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5)x10^9}{f(BCLK)} - 40[ns]$

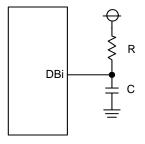
n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. (BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 x 10^9}{f(BCLK)} - 10[ns]$$

= 6.7ns.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus. Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value. Hold time of data bus is expressed in $t = -CR X \ln (1 - VoL / Vcc2)$ by a circuit of the right figure. For example, when VoL = 0.2Vcc2, C = 30pF, R = 1k\Omega, hold time of output "L" level is $t = -30pF X 1k\Omega X \ln(1-0.2Vcc2 / Vcc2)$



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Switching Characteristics

(Vcc1 = Vcc2 = 5V, Vss = 0V, at Topr = -20 to 85° C / -40 to 85° C unless otherwise specified)

Table 23.48	Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area
	access and multiplex bus selection)

Symbol	Parameter		Stan	Standard	
Symbol	Falameter		Min.	Max.	Unit
td(BCLK-AD)	Address Output Delay Time			50	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip Select Output Delay Time			50	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
th(RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			40	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			40	ns
th(BCLK-WR)	WR Signal Output Hold Time	See	0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)	Figure 23.12		50	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns
td(BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		-4		ns
td(AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
th(AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
td(AD-RD)	RD Signal Output Delay From the End of Address		0		ns
td(AD-WR)	WR Signal Output Delay From the End of Address		0		ns
tdz(RD-AD)	Address Output Floating Start Time			8	ns

n is "2" for 2-wait setting, "3" for 3-wait setting.

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

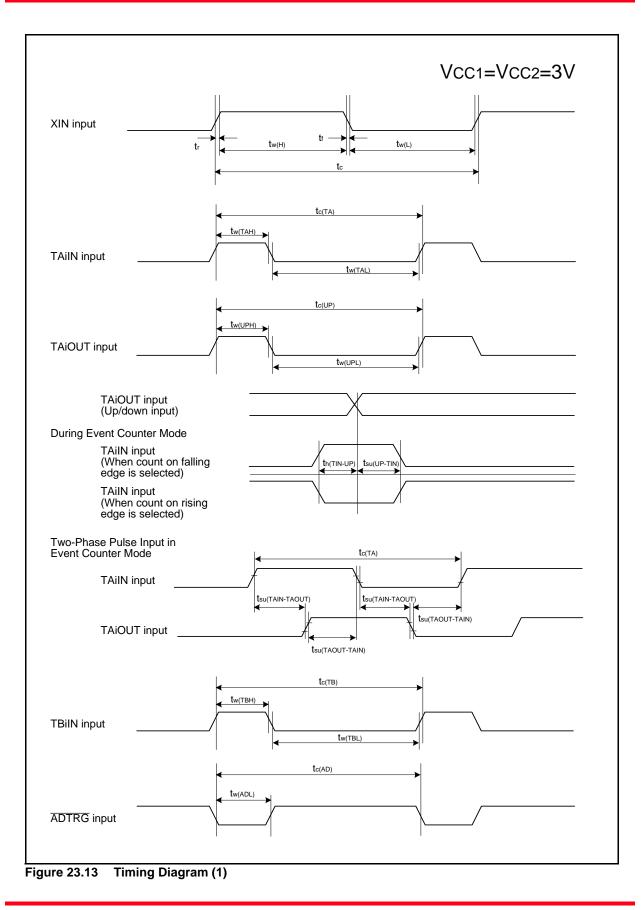
$$\frac{0.5 \times 10^9}{f(BCLK)} - 50[ns]$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40[ns]$$

4. Calculated according to the BCLK frequency as follows:

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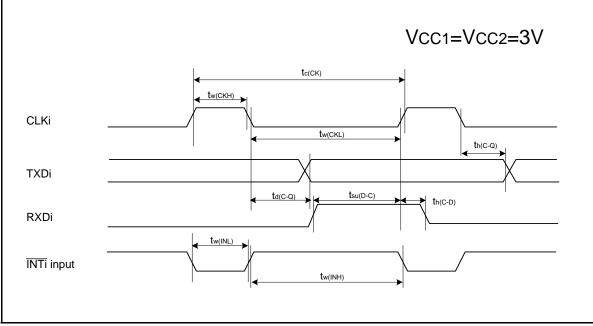
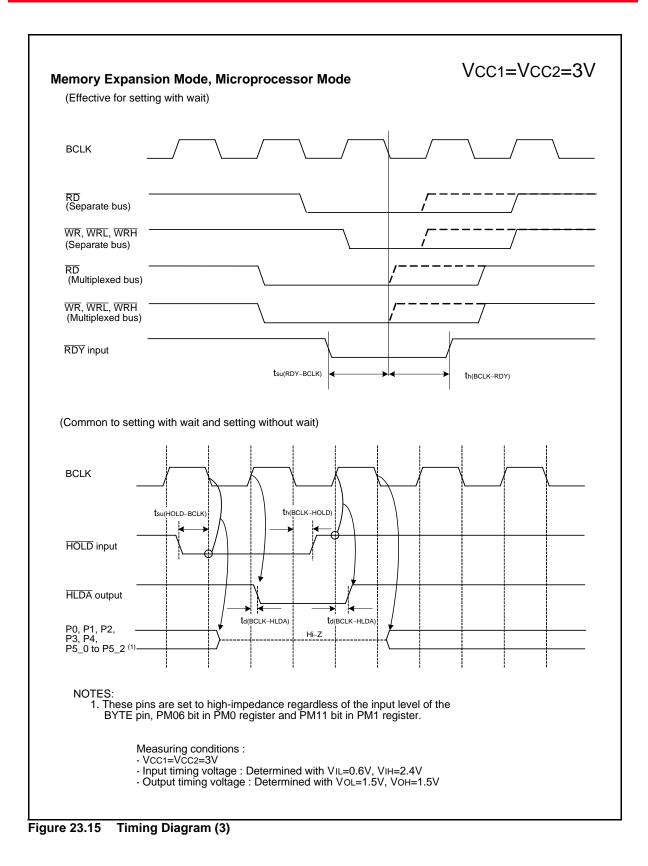
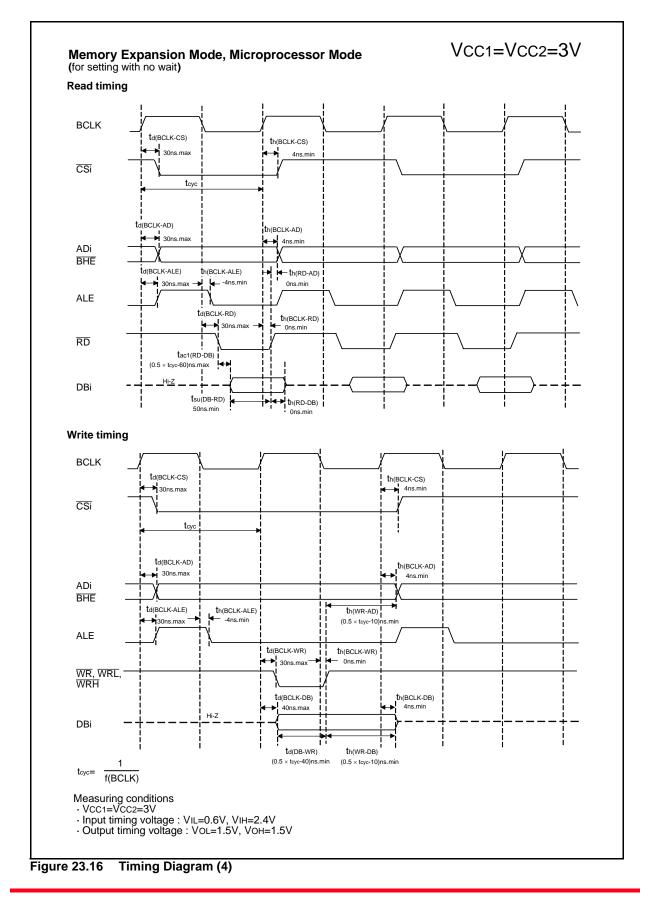


Figure 23.14 Timing Diagram (2)

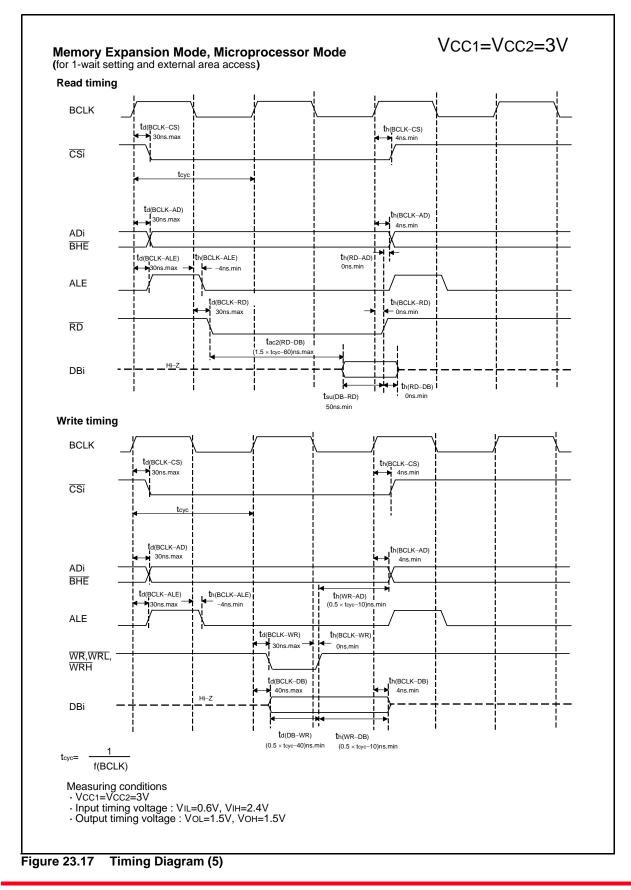
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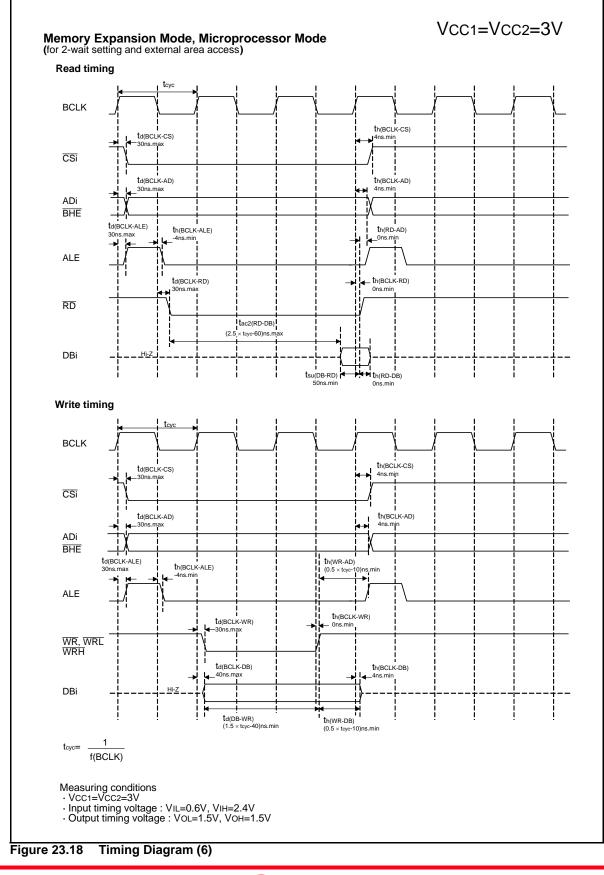
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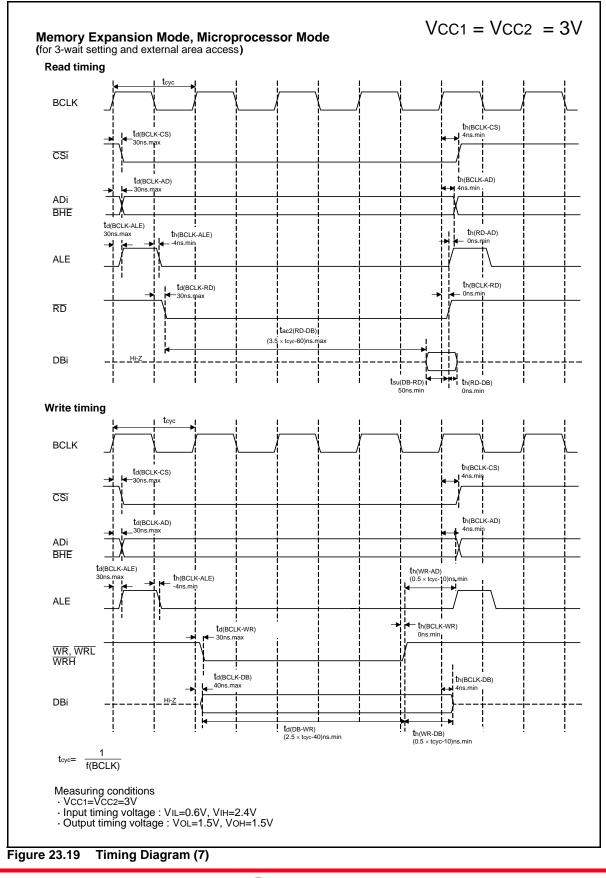
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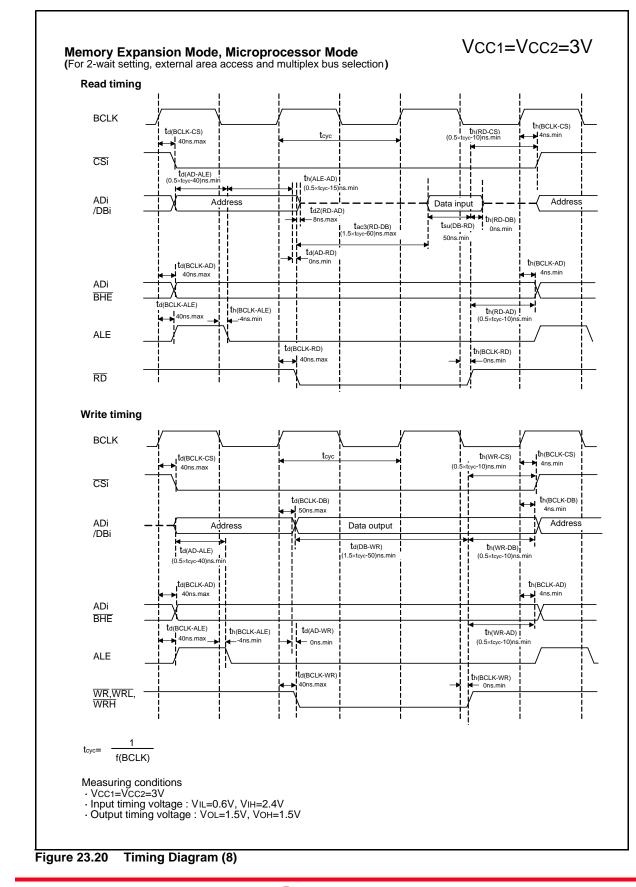
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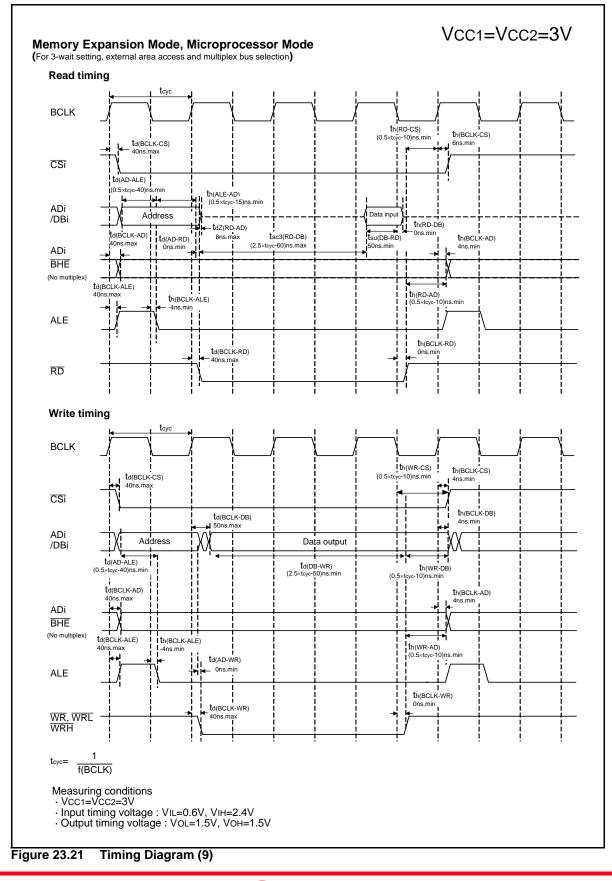
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23.2 Electrical Characteristics (M16C/62PT)

Symbol		Parameter	Condition	Rated Value	Unit
VCC1, VCC2	Supply Voltage		Vcc1=Vcc2=AVcc	-0.3 to 6.5	V
AVcc	Analog Supply \	/oltage	Vcc1=Vcc2=AVcc	-0.3 to 6.5	V
Vı	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		-0.3 to Vcc1+0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	V
	P7_0, P7_1			-0.3 to 6.5	V
Vo	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		-0.3 to Vcc1+0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	V
		P7_0, P7_1		-0.3 to 6.5	V
Pd	Power Dissipation	bn	–40°C <topr≤85°c< td=""><td>300</td><td>mW</td></topr≤85°c<>	300	mW
			85°C <topr≤125°c< td=""><td>200</td><td>mvv</td></topr≤125°c<>	200	mvv
Topr	Operating Ambient	When the Microcomputer is Operating		-40 to 85 / -40 to 125 (2)	°C
	Temperature	Flash Program Erase		0 to 60	
Tstg	Storage Temper	ature		-65 to 150	°C

Table 23.49 Absolute Maximum Ratings

NOTES:

- 1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
- 2. T version = -40 to 85 °C, V version = -40 to 125 °C.

Symbol		Devenuetar		Min. Typ. Max. V 4.0 5.0 5.5 1 VCc1 1 1 1 0 0 1 1 0.8Vcc2 Vcc2 Vcc2 1 0.8Vcc2 Vcc2 1 1	Unit		
Symbol		Parameter		Min.	Тур.	Max.	Unit
VCC1, VCC2	Supply Voltage ((VCC1 = VCC2)		4.0	5.0	5.5	V
AVcc	Analog Supply V	/oltage			Vcc1		V
Vss	Supply Voltage				0		V
AVss	Analog Supply V	/oltage			0		V
Vih	HIGH Input Voltage (4)	P3_1 to P3_7, P4_0 to P4_7, P P12_0 to P12_7, P13_0 to P13	P5_0 to P5_7, 3_7	0.8Vcc2		Vcc2	V
	0	P0_0 to P0_7, P1_0 to P1_7, F (during single-chip mode)	P2_0 to P2_7, P3_0	0.8Vcc2		Vcc2	V
		P6_0 to P6_7, P7_2 to P7_7, P P10_0 to P10_7, P11_0 to P11 XIN, RESET, CNVSS, BYTE		0.8Vcc1		Vcc1	V
		P7_0, P7_1		0.8Vcc1		6.5	V
VIL	LOW Input Voltage (4)	P3_1 to P3_7, P4_0 to P4_7, P P12_0 to P12_7, P13_0 to P13	P5_0 to P5_7, 3_7	0		0.2Vcc2	V
	5	P0_0 to P0_7, P1_0 to P1_7, F (during single-chip mode)	P2_0 to P2_7, P3_0	0		0.2Vcc2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE		0		0.2Vcc	V
IOH(peak)	HIGH Peak Output Current (4)	P4_0 to P4_7, P5_0 to P5_7, P8_0 to P8_4, P8_6, P8_7, P9	IN, RESE1, CNVSS, BYTE 0.0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, 4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, 8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, 11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-10.0	mA
IOH(avg)	HIGH Average Output Current (4)	P0_0 to P0_7, P1_0 to P1_7, F P4_0 to P4_7, P5_0 to P5_7, F P8_0 to P8_4, P8_6, P8_7, P9 P11_0 to P11_7, P12_0 to P12	P6_0 to P6_7, P7_2 to P7_7,			-5.0	mA
IOL(peak)	LOW Peak Output Current (4)	P0_0 to P0_7, P1_0 to P1_7, F P4_0 to P4_7, P5_0 to P5_7, F P8_0 to P8_4, P8_6, P8_7, P9 P11_0 to P11_7, P12_0 to P12	P6_0 to P6_7, P7_0 to P7_7,			10.0	mA
IOL(avg)	LOW Average Output Current (4)	P0_0 to P0_7, P1_0 to P1_7, F P4_0 to P4_7, P5_0 to P5_7, F P8_0 to P8_4, P8_6, P8_7, P9 P11_0 to P11_7, P12_0 to P12	P6_0 to P6_7, P7_0 to P7_7,			5.0	mA
f(XIN)	Main Clock Inpu	t Oscillation Frequency	VCC1=4.0V to 5.5V	0		16	MHz
f(XCIN)	Sub-Clock Oscil	lation Frequency	•		32.768	50	kHz
f(Ring)	On-chip Oscillati	ion Frequency		0.5	1	2	MHz
f(PLL)	PLL Clock Oscill	lation Frequency	VCC1=4.0V to 5.5V	10		24	MHz
f(BCLK)	CPU Operation	Clock		0		24	MHz
ts∪(PLL)	PLL Frequency Wait Time	Synthesizer Stabilization	VCC1=5.5V			20	ms

 Table 23.50
 Recommended Operating Conditions (1) ⁽¹⁾

NOTES:

- 1. Referenced to Vcc1 = Vcc2 = 4.7 to 5.5V at Topr = -40 to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified. T version = -40 to $85^{\circ}C$, V version= -40 to $125^{\circ}C$.
- 2. The Average Output Current is the mean value within 100ms.

3. The total IoL(peak) for ports P0, P1, P2, P8_6, P8_7, P9, P10 P1, P14_0 and P14_1 must be 80mA max. The total IoL(peak) for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total IoH(peak) for ports P0, P1, and P2 must be -40mA max. The total IoH(peak) for ports P3, P4, P5, P12, and P13 must be -40mA max. The total IoH(peak) for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total IOH(peak) for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total IOH(peak) for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total IOH(peak) for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be -40mA max.

As for 80-pin version, the total IOL(peak) for all ports and IOH(peak) must be 80mA. max. due to one Vcc and one Vss.

4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Symbol	Parame	tor		Measuring Condition		Standard	l	Unit		
Symbol	Palame	lei		vieasuring Condition	Min.	Тур.	Max.			
_	Resolution		VREF=VCC1		VREF=VCC1				10	Bits
INL	Integral Non-Linearity Error	10bit	VREF= VCC1= 5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB		
				External operation amp connection mode			±7	LSB		
		8bit	Vref=V	/cc1=5V			±2	LSB		
-	Absolute Accuracy	10bit	VREF= VCC1= 5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB		
			External operation amp connection mode				±7	LSB		
		8bit	VREF=V	/cc1=5V			±2	LSB		
-	Tolerance Level Impeda	ince				3		kΩ		
DNL	Differential Non-Linearit	y Error					±1	LSB		
_	Offset Error						±3	LSB		
_	Gain Error						±3	LSB		
RLADDER	Ladder Resistance		Vref=V	CC1	10		40	kΩ		
tCONV	10-bit Conversion Time, Function Available	10-bit Conversion Time, Sample & Hold Function Available		VREF=VCC1=5V, ϕ AD=12MHz				μS		
tCONV	8-bit Conversion Time, 5 Function Available	Sample & Hold	VREF=Vcc1=5V, φAD=12MHz		2.33			μS		
tSAMP	Sampling Time				0.25			μS		
Vref	Reference Voltage				2.0		Vcc1	V		
VIA	Analog Input Voltage				0		Vref	V		

Table 23.51	A/D Conversion Characteristics (1)
-------------	------------------------------------

NOTES:

1. Referenced to Vcc1=AVcc=VREF=4.0 to 5.5V, Vss=AVss=0V at Topr = -40 to 85°C / -40 to 125°C unless otherwise specified. T version = -40 to 85°C, V version =-40 to 125°C

2. ϕ AD frequency must be 12 MHz or less.

 When sample & hold is disabled, φAD frequency must be 250 kHz or more, in addition to the limitation in Note 2. When sample & hold is enabled, φAD frequency must be 1MHz or more, in addition to the limitation in Note 2.

	Table 23.52	D/A Conversion Characteristics (1)
--	-------------	------------------------------------

Symbol	Parameter	Measuring Condition		Unit		
	Faranielei	Measuring Condition	Min.	Тур.	Max.	Unit
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
ts∪	Setup Time				3	μS
Ro	Output Resistance		4	10	20	kΩ
IVREF	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to Vcc1=VREF=4.0 to 5.5V, Vss=AVss=0V at Topr = -40 to 85° C / -40 to 125° C unless otherwise specified. T version = -40 to 85° C, V version = -40 to 125° C

 This applies when using one D/A converter, with the D/A register for the unused D/A converter set to "00h". The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not "00h", the IVREF will flow even if Vref id disconnected by the A/D control register.

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Symbol	Deremeter	Parameter			Standard			
Symbol	Farameter	Min.	Тур.	Max.	Unit			
-	Program and Erase Endurance ⁽³⁾ Word Program Time (Vcc1=5.0V) Lock Bit Program Time		100			cycle		
_				25	200	μs		
_				25	200	μs		
_	Block Erase Time	4-Kbyte block	4	0.3	4	S		
_	(Vcc1=5.0V)	8-Kbyte block		0.3	4	S		
_	7	32-Kbyte block		0.5	4	S		
_	7	64-Kbyte block		0.8	4	S		
-	Erase All Unlocked Blocks Time (2)				4×n	S		
tPS	Flash Memory Circuit Stabilization Wait Ti	Flash Memory Circuit Stabilization Wait Time			15	μs		
—	Data Hold Time ⁽⁵⁾		20			year		

Table 23.53 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (B, U)

Table 23.54 Flash Memory Version Electrical Characteristics ⁽⁶⁾ for 10,000 cycle products (B7, U7) (Block A and Block 1 ⁽⁷⁾)

Symbol	Parameter		Unit			
Symbol	Faranieler		Min.	Тур.	Max.	Onit
-	Program and Erase Endurance (3, 8, 9)		10,000 (4)			cycle
-	Word Program Time (Vcc1=5.0V)			25		μS
-	Lock Bit Program Time			25		μS
-	Block Erase Time (Vcc1=5.0V)	4-Kbyte block	4	0.3		S
tPS	Flash Memory Circuit Stabilization Wait Time				15	μS
-	Data Hold Time ⁽⁵⁾		20			year

NOTES:

- 1. Referenced to Vcc1=4.5 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.
- 2. n denotes the number of block erases.

(Rewrite prohibited)

- 3. Program and Erase Endurance refers to the number of times a block erase can be performed. If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times. For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block.
- 4. Maximum number of E/W cycles for which operation is guaranteed.
- 5. Ta (ambient temperature)=55 °C. As to the data hold time except Ta=55 °C, please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor.
- 6. Referenced to Vcc1 = 4.5 to 5.5V at Topr = -40 to 85 °C (B7, U7 (T version)) / -40 to 125 °C (B7, U7 (V version)) unless otherwise specified.
- 7. Table 23.54 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 23.53.
- 8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary. Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
- 9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
- 10. Set the PM17 bit in the PM1 register to "1" (wait state) when executing more than 100 times rewrites (B7 and U7).
- 11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 23.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at Topr = 0 to 60 °C(B, U), Topr = -40 to 85 °C (B7, U7 (T version)) / -40 to 125 °C (B7, U7 (V version))

Flash Program, Erase Voltage	Flash Read Operation Voltage
$VCC1 = 5.0 V \pm 0.5 V$	Vcc1=4.0 to 5.5 V

Symbol	Parameter	Measuring Condition		Unit		
Symbol	Falanielei	measuring Condition	Min.	Тур.	Max.	Unit
td(P-R)	Time for Internal Power Supply Stabilization During Powering-On	Vcc1=4.0V to 5.5V			2	ms
td(R-S)	STOP Release Time				150	μS
td(W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	μs

 Table 23.56
 Power Supply Circuit Timing Characteristics

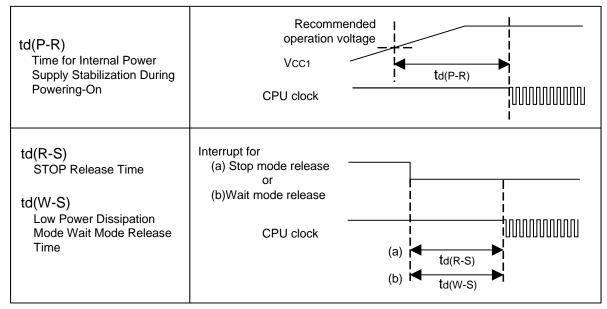


Figure 23.22 Power Supply Circuit Timing Diagram

Symbol		Parameter	r	Measuring Condition	Standard			Unit
,					Min.	Тур.	Max.	Sim
Vон	HIGH Output Voltage ⁽²⁾	P6_0 to P6_7, P7_2 to P7_7 P8_6, P8_7, P9_0 to P9_7, P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	IOH=-5mA	Vcc1-2.0		Vcc1	v
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOH=-5mA	Vcc2-2.0		VCC2	
Vон	HIGH Output Voltage ⁽²⁾	P6_0 to P6_7, P7_2 to P7_7 P8_6, P8_7, P9_0 to P9_7, I P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	ОН=-200μА	Vcc1-0.3		Vcc1	v
				ЮН=-200μА	Vcc2-0.3		Vcc2	v
Vон	HIGH Outpu	t Voltage XOUT	HIGHPOWER	IOH=-1mA	Vcc1-2.0		VCC1	V
			LOWPOWER	IOH=-0.5mA	Vcc1-2.0		Vcc1	v
	HIGH Outpu	t Voltage XCOUT	HIGHPOWER	With no load applied		2.5		
			LOWPOWER	With no load applied		1.6		V
Vol	LOW Output Voltage ⁽²⁾	P6_0 to P6_7, P7_0 to P7_7 P8_6, P8_7, P9_0 to P9_7, P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	IOL=5mA			2.0	v
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOL=5mA			2.0	V
Vol	L LOW P6_0 to P6_7, P7_0 to P7_7 Output P8_6, P8_7, P9_0 to P9_7, Voltage ⁽²⁾ P11_0 to P11_7, P14_0, P1		P10_0 to P10_7,	IOL=200μA			0.45	v
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOL=200μA			0.45	v
Vol	LOW Output	Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	v
			LOWPOWER	IOL=0.5mA			2.0	v
	LOW Output	Voltage XCOUT	HIGHPOWER	With no load applied		0		
			LOWPOWER	With no load applied		0		V
Vt+-Vt-	Hysteresis	HOLD, RDY, TA0IN to TA4II INT0 to INT5, NMI, ADTRG, TA0OUT to TA4OUT, KI0 to SCL0 to SCL2, SDA0 to SD/	CTS0 to CTS2, CLK0 to CLK4, KI3, RXD0 to RXD2,		0.2		1.0	V
Vt+-Vt-	Hysteresis	RESET			0.2		2.5	V
Ін	HIGH Input Current ⁽²⁾	put P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7,		VI=5V			5.0	μΑ
lı.	LOW Input Current ⁽²⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE		VI=0V			-5.0	μΑ
Rpullup	Pull-Up Resistance (2)			VI=0V	30	50	170	kΩ
Rfxin	Feedback R	esistance XIN				1.5		MΩ
Rfxcin	Feedback R	esistance XCIN				15		MΩ
Vram	RAM Retent	ion Voltage		At stop mode	2.0			V

Table 23.57 Electrical Characteristics (1) (1)

NOTES:
1. Referenced to Vcc1=Vcc2=4.0 to 5.5V, Vss = 0V at Topr = -40 to 85°C / -40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = -40 to 85°C, V version =-40 to 125°C.
2. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Symbol	Paramet	or	Moos	Measuring Condition		Standard		
Symbol	Faidillet	ei	Measuring Condition		Min.	Тур.	Max.	Unit
Icc	Power Supply Current (Vcc1=Vcc2=4.0V to 5.5V)	In single-chip mode, the output	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
		pins are open and other pins are Vss		No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
		,	No division, On-chip oscillation		1.8		mA	
			Flash Memory Program	f(BCLK)=10MHz, Vcc1=5.0V		15		mA
			Flash Memory Erase	f(BCLK)=10MHz, Vcc1=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μΑ
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		50		μA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5		μΑ
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		2.0		μΑ
				Stop mode Topr =25°C		2.0	6.0	μΑ
				Stop mode Topr =85°C			20	μΑ
				Stop mode Topr =125°C			TBD	μA

Table 23.58 Electrical Characteristics (2) (1)

NOTES:
1. Referenced to Vcc1=Vcc2=4.0 to 5.5V, Vss = 0V at Topr = -40 to 85°C / -40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = -40 to 85°C, V version = -40 to 125°C.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

Timing Requirements

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -40 to 85°C (T version) / -40 to 125°C (V version) unless otherwise specified)

Table 23.59 External Clock Input (XIN input)

Symbol	Parameter	Stan	ndard Max.	Lloit
	Falametei	Min.	Max.	Unit ns ns ns ns
tc	External Clock Input Cycle Time	62.5		ns
tw(H)	External Clock Input HIGH Pulse Width	25		ns
tw(L)	External Clock Input LOW Pulse Width	25		ns
tr	External Clock Rise Time		15	ns
tf	External Clock Fall Time		15	ns

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Timing Requirements

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -40 to 85°C (T version) / -40 to 125°C (V version) unless otherwise specified)

Table 23.60 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Stan	Max.	Unit
Symbol	Farameter	Min.	Max.	Offic
tc(TA)	TAilN Input Cycle Time	100		ns
tw(TAH)	TAilN Input HIGH Pulse Width	40		ns
tw(TAL)	TAilN Input LOW Pulse Width	40		ns

Table 23.61 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Stan	Max.	Unit ns ns
	Falametei	Min.	Max.	
tc(TA)	TAilN Input Cycle Time	400		ns
tw(TAH)	TAilN Input HIGH Pulse Width	200		ns
tw(TAL)	TAIIN Input LOW Pulse Width	200		ns

Table 23.62 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Stan	ndard Max.	Unit ns ns
	Farameter	Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	200		ns
tw(TAH)	TAilN Input HIGH Pulse Width	100		ns
tw(TAL)	TAIIN Input LOW Pulse Width	100		ns

Table 23.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Stan	dard	- Unit ns
Symbol	Falameter	Min.	Max.	Offic
tw(TAH)	TAIIN Input HIGH Pulse Width	100		ns
tw(TAL)	TAIIN Input LOW Pulse Width	100		ns

Table 23.64 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Stan	dard	Lloit
	Faiallielei	Min.	Max.	Unit
tc(UP)	TAiOUT Input Cycle Time	2000		ns
tw(UPH)	TAiOUT Input HIGH Pulse Width	1000		ns
tw(UPL)	TAiOUT Input LOW Pulse Width	1000		ns
tsu(UP-TIN)	TAiOUT Input Setup Time	400		ns
th(TIN-UP)	TAiOUT Input Hold Time	400		ns

Table 23.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Stan	Max.	Unit
	Farameter	Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	800		ns
tsu(TAIN-TAOUT)	TAiOUT Input Setup Time	200		ns
tsu(TAOUT-TAIN)	TAilN Input Setup Time	200		ns

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Timing Requirements

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -40 to 85°C (T version) / -40 to 125°C (V version) unless otherwise specified)

Table 23.66 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Stan	Idard	Unit ns ns ns
Symbol	Falametei	Min.	Max.	
tc(TB)	TBiIN Input Cycle Time (counted on one edge)	100		ns
tw(TBH)	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
tw(TBL)	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
tc(TB)	TBiIN Input Cycle Time (counted on both edges)	200		ns
tw(TBH)	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
tw(TBL)	TBilN Input LOW Pulse Width (counted on both edges)	80		ns

Table 23.67 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Stan	dard	Unit ns ns
	Farameter	Min.	Max.	
tc(TB)	TBiIN Input Cycle Time	400		ns
tw(TBH)	TBiIN Input HIGH Pulse Width	200		ns
tw(TBL)	TBiIN Input LOW Pulse Width	200		ns

Table 23.68 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Stan	dard	Lloit
	Farameter	Min.	Max.	Unit ns ns
tc(TB)	TBilN Input Cycle Time	400		ns
tw(TBH)	TBiIN Input HIGH Pulse Width	200		ns
tw(TBL)	TBiIN Input LOW Pulse Width	200		ns

Table 23.69 A/D Trigger Input

Symbol	Parameter	Stan	dard	Unit
Symbol	Farameter	Min.	Max.	Onit
tc(AD)	ADTRG Input Cycle Time	1000		ns
tw(ADL)	ADTRG input LOW Pulse Width	125		ns

Table 23.70 Serial Interface

Symbol	Parameter	Stan	Idard	Unit
Symbol	Faiallielei	Min.	Max.	Onit
tc(CK)	CLKi Input Cycle Time	200		ns
tw(CKH)	CLKi Input HIGH Pulse Width	100		ns
tw(CKL)	CLKi Input LOW Pulse Width	100		ns
td(C-Q)	TXDi Output Delay Time		80	ns
th(C-Q)	TXDi Hold Time	0		ns
tsu(D-C)	RXDi Input Setup Time	70		ns
t h(C-D)	RXDi Input Hold Time	90		ns

Table 23.71 External Interrupt INTi Input

Symbol	Parameter	Stan	Unit	
	Farameter	Min.	Max.	Onit
tw(INH)	INTi Input HIGH Pulse Width	250		ns
tw(INL)	INTi Input LOW Pulse Width	250		ns

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Switching Characteristics (Vcc1 = Vcc2 = 5V, Vss = 0V, at Topr = -40 to 85° C (T version) / -40 to 125° C (V version) unless otherwise specified)

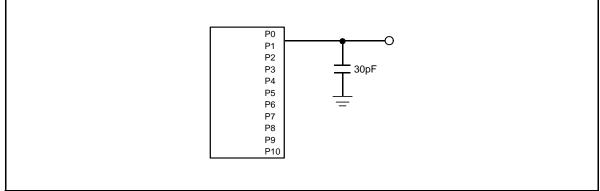
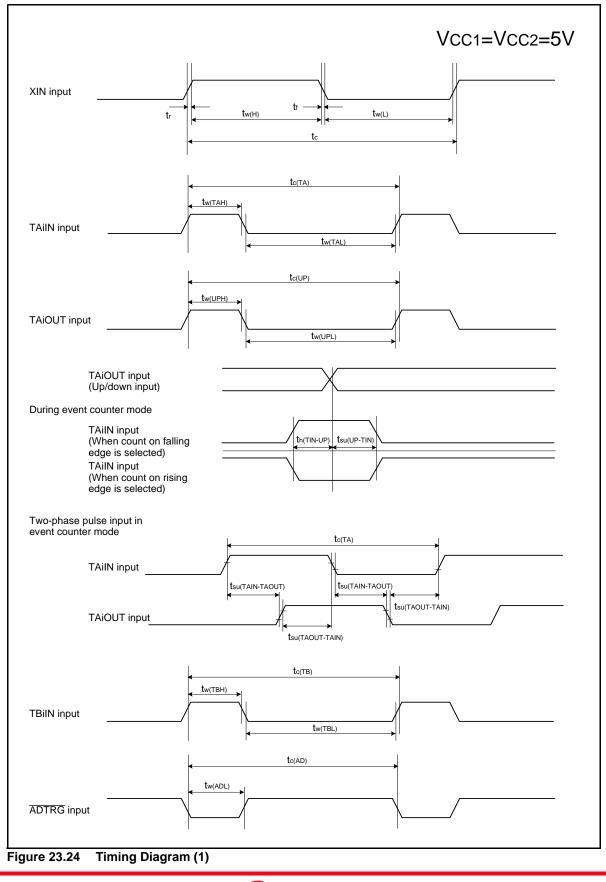


Figure 23.23 Ports P0 to P10 Measurement Circuit



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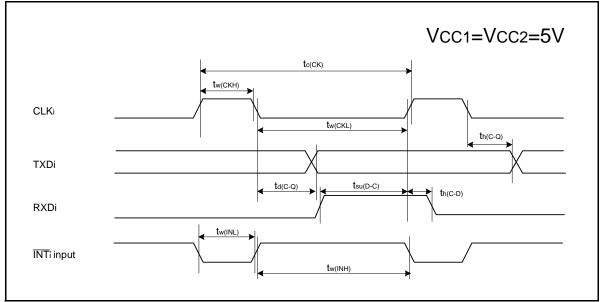


Figure 23.25 Timing Diagram (2)

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24. Precautions

24.1 SFR

24.1.1 Register Settings

Table Table 24.1 Registers with Write-only Bits which can only be written to. Set these registers with immediate values. When establishing the next value by altering the present value, write the present value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

Table 24.1	Registers with Write-only	Bits
------------	---------------------------	------

Register	Symbol	Address
Watchdog timer start register	WDC	000E
Timer A1-1 register	TA11	0343 to 0342
Timer A2-1 register	TA21	0345 to 0344
Timer A4-1 register	TA41	0347 to 0346
Short-circuit preventionTimer	DTT	034C
Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	034D
SI/03 bit rate register	S3BRG	0363
SI/04 bit rateregister	S4BRG	0367
UART0 bit rateregister	U0BRG	03A1
UART1 bit rateregister	U1BRG	03A9
UART2 bit rate register	U2BRG	0379
UART0 Transmit buffer register	U0TB	03A3 to 03A2
UART1 Transmit buffer register	U1TB	03AB to 03AA
UART2 Transmit buffer register	U2TB	037B to 037A
Ups and downs flag	UDF	0384
Timer 0 register	TA0	0387 to 0386
Timer 1 register	TA1	0389 to 0388
Timer 2 register	TA2	038B to 038A
Timer 3 register	TA3	038D to 038C
Timer 4 register	TA4	038F to 038E

24.2 Reset

When supplying power to the microcomputer, the power supply voltage applied to the VCC1 pin must meet the conditions of SVCC.

Svmbol	Parameter		Unit		
Symbol Falameter	Min.	Тур.	Max.	Unit	
SVcc	Power supply rising gradient (VCC1)(Voltage range 0 to 2.0)				V/ms

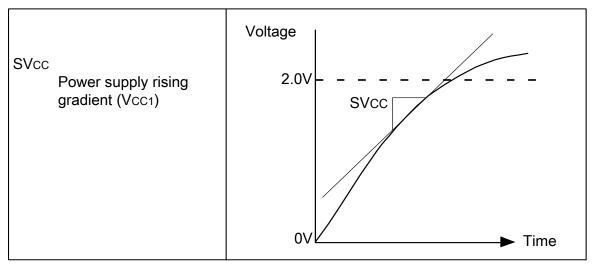


Figure 24.1 Timing of SVcc

24.3 Bus

- The ROMless version can operate only in the microprocessor mode, connect the CNVSS pin to VCC1.
- When resetting CNVss pin with "H" input, contents of internal ROM cannot be read out.

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24.4 PLL Frequency Synthesizer

Stabilize supply voltage so that the standard of the power supply ripple is met.

Symbol	Parameter		Unit			
Symbol Falameter		Min.	Тур.	Max.	Onit	
f(ripple)	Power supply ripple allowable frequency (VCC1)				10	kHz
VP-P(ripple)	Power supply ripple allowable	(VCC1=5V)			0.5	V
	amplitude voltage	(VCC1=3V)			0.3	V
$VCC(\Delta V / \Delta T)$	Power supply ripple rising / falling	(VCC1=5V)			0.3	V/ms
	gradient	(VCC1=3V)			0.3	V/ms

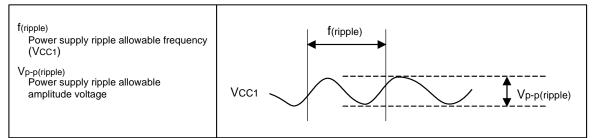


Figure 24.2 Timing of Voltage Fluctuation

24.5 Power Control

- When exiting stop mode by hardware reset, set RESET pin to "L" until a main clock oscillation is stabilized.
- Set the MR0 bit in the TAiMR register (i=0 to 4) to "0" (pulse is not output) to use the timer A to exit stop mode.
- When entering wait mode, insert a JMP.B instruction before a WAIT instruction. Do not execute any instructions which can generate a write to RAM between the JMP.B and WAIT instructions. Disable the DMA transfers, if a DMA transfer may occur between the JMP.B and WAIT instructions. After the WAIT instruction, insert at least 4 NOP instructions. When entering wait mode, the instruction queue roadstead the instructions following WAIT, and depending on timing, some of these may execute before the microcomputer enters wait mode.

Program example when entering wait mode

Program Example:		JMP.B	L1	; Insert JMP.B instruction before WAIT instruction
	L1:			
		FSET	Ι	;
		WAIT		; Enter wait mode
		NOP		; More than 4 NOP instructions
		NOP		
		NOP		
		NOP		

• When entering stop mode, insert a JMP.B instruction immediately after executing an instruction which sets the CM10 bit in the CM1 register to "1", and then insert at least 4 NOP instructions. When entering stop mode, the instruction queue reads ahead the instructions following the instruction which sets the CM10 bit to "1" (all clock stops), and, some of these may execute before the microcomputer enters stop mode or before the interrupt routine for returning from stop mode.

Program example when entering stop mode

Program Example:		FSET	Ι	
		BSET	CM10	; Enter stop mode
		JMP.B	L2	; Insert JMP.B instruction
	L2:			
		NOP		; More than 4 NOP instructions
		NOP		
		NOP		
		NOP		

- Wait until the main clock oscillation stabilizes, before switching the clock source for CPU clock to the main clock.
- Similarly, wait until the sub clock oscillates stably before switching the clock source for CPU clock to the sub clock.

• Suggestions to reduce power consumption

Ports

The processor retains the state of each I/O port even when it goes to wait mode or to stop mode. A current flows in active I/O ports. A pass current flows in input ports that high-impedance state. When entering wait mode or stop mode, set non-used ports to input and stabilize the potential.

A/D converter

When A/D conversion is not performed, set the VCUT bit of ADiCON1 register to "0" (no VREF connection).

When A/D conversion is performed, start the A/D conversion at least 1 µs or longer after setting the VCUT bit to "1" (VREF connection).

D/A converter

When not performing D/A conversion, set the DAiE bit (i=0, 1) of DACON register to "0" (input inhibited) and DAi register to "00h".

Stopping peripheral functions

Use the CM0 register CM02 bit to stop the unnecessary peripheral functions during wait mode.

However, because the peripheral function clock (fC32) generated from the sub-clock does not stop, this measure is not conducive to reducing the power consumption of the chip. If low speed mode or low power dissipation mode is to be changed to wait mode, set the CM02 bit to "0" (do not peripheral function clock stopped when in wait mode), before changing wait mode.

Switching the oscillation-driving capacity

Set the driving capacity to "LOW" when oscillation is stable.

24.6 Protect

Set the PRC2 bit to "1" (write enabled) and then write to any address, and the PRC2 bit will be cleared to "0" (write protected). The registers protected by the PRC2 bit should be changed in the next instruction after setting the PRC2 bit to "1". Make sure no interrupts or DMA transfers will occur between the instruction in which the PRC2 bit is set to "1" and the next instruction.

24.7 Interrupt

24.7.1 Reading address 00000h

Do not read the address 00000h in a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from the address 00000h during the interrupt sequence. At this time, the IR bit for the accepted interrupt is cleared to "0".

If the address 00000h is read in a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is cleared to "0". This factors a problem that the interrupt is canceled, or an unexpected interrupt request is generated.

24.7.2 Setting the SP

Set any value in the SP(USP, ISP) before accepting an interrupt. The SP(USP, ISP) is cleared to "0000h" after reset. Therefore, if an interrupt is accepted before setting any value in the SP(USP, ISP), the program may go out of control.

Especially when using $\overline{\text{NMI}}$ interrupt, set a value in the ISP at the beginning of the program. For the first and only the first instruction after reset, all interrupts including $\overline{\text{NMI}}$ interrupt are disabled.

24.7.3 The NMI Interrupt

- The $\overline{\text{NMI}}$ interrupt cannot be disabled. If this interrupt is unused, connect the $\overline{\text{NMI}}$ pin to VCC1 via a resistor (pull-up).
- The input level of the <u>NMI</u> pin can be read by accessing the P8_5 bit in the P8 register. Note that the P8_5 bit can only be read when determining the pin level in <u>NMI</u> interrupt routine.
- Stop mode cannot be entered into while input on the $\overline{\text{NMI}}$ pin is low. This is because while input on the $\overline{\text{NMI}}$ pin is low the CM10 bit in the CM1 register is fixed to "0".
- Do not go to wait mode while input on the <u>NMI</u> pin is low. This is because when input on the <u>NMI</u> pin goes low, the CPU stops but CPU clock remains active; therefore, the current consumption in the chip does not drop. In this case, normal condition is restored by an interrupt generated thereafter.
- The low and high level durations of the input signal to the $\overline{\text{NMI}}$ pin must each be 2 CPU clock cycles + 300 ns or more.

24.7.4 Changing the Interrupt Generate Factor

If the interrupt generate factor is changed, the IR bit in the interrupt control register for the changed interrupt may inadvertently be set to "1" (interrupt requested). If you changed the interrupt generate factor for an interrupt that needs to be used, be sure to clear the IR bit for that interrupt to "0" (interrupt not requested). Changing the interrupt generate factor refered to here means any act of changing the source, polarity or timing of the interrupt assigned to each software interrupt number. Therefore, if a mode change of any peripheral function involves changing the generate factor, polarity or timing of an interrupt, be sure to clear the IR bit for that interrupt to "0" (interrupt not requested) after making such changes. Refer to the description of each peripheral function for details about the interrupts from peripheral functions. Figure 24.3 shows the Procedure for Changing the Interrupt Generate Factor.

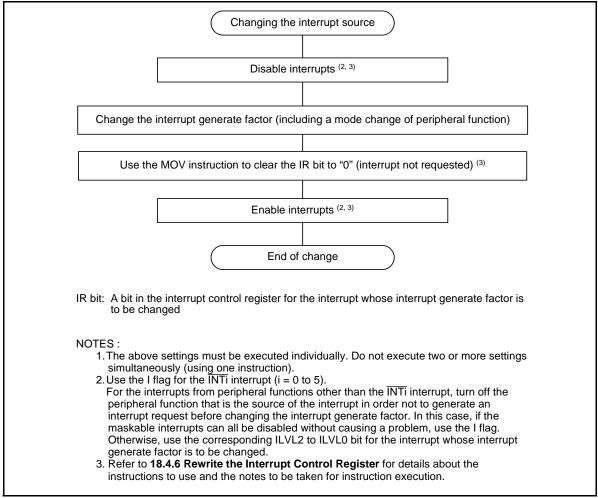


Figure 24.3 Procedure for Changing the Interrupt Generate Factor

24.7.5 INT Interrupt

- Either an "L" level of at least tW(INH) or an "H" level of at least tW(INL) width is necessary for the signal input to pins INT0 through INT5 regardless of the CPU operation clock.
- If the POL bit in the INTOIC to INT5IC registers or the IFSR7 to IFSR0 bits in the IFSR register are changed, the IR bit may inadvertently set to "1" (interrupt requested). Be sure to clear the IR bit to "0" interrupt not requested) after changing any of those register bits.

24.7.6 Rewrite the Interrupt Control Register

- (a) The interrupt control register for any interrupt should be modified in places where no requests for that interrupt may occur. Otherwise, disable the interrupt before rewriting the interrupt control register.
- (b) To rewrite the interrupt control register for any interrupt after disabling that interrupt, be careful with the instruction to be used.
 - Changing any bit other than the IR bit
 - Changing the IR bit

Depending on the instruction used, the IR bit may not always be cleared to "0" (interrupt not requested). Therefore, be sure to use the MOV instruction to clear the IR bit.

(c) When using the I flag to disable an interrupt, refer to the sample program fragments shown below as you set the I flag. (Refer to (b) for details about rewrite the interrupt control registers in the sample program fragments.)

Examples 1 through 3 show how to prevent the I flag from being set to "1" (interrupts enabled) before the interrupt control register is rewrited, owing to the effects of the internal bus and the instruction queue buffer.

Example 1:Using the NOP instruction to keep the program waiting until the interrupt control register is modified

INT_SWITC	H1:	
FCLR	I	; Disable interrupts.
AND.B	#00h, 0055h	; Set the TA0IC register to "00h".
NOP		,
NOP		
FSET	I	; Enable interrupts.

The number of NOP instruction is as follows. PM20=1(1 wait) : 2, PM20=0(2 wait) : 3, when using HOLD function : 4.

Example 2: Using the dummy read to keep the FSET instruction waiting

INT_SWITCH2:

FCLR	I	; Disable interrupts.
AND.B	#00h, 0055h	; Set the TA0IC register to "00h".
MOV.W	MEM, R0	; <u>Dummy read</u> .
FSET	I	; Enable interrupts.

Example 3: Using the POPC instruction to changing the I flag

INT_SWITCH3: PUSHC FLG FCLR I ; Disable interrupts. AND.B #00h, 0055h ; Set the TA0IC register to "00h". POPC FLG ; Enable interrupts.

24.7.7 Watchdog Timer Interrupt

Initialize the watchdog timer after the watchdog timer interrupt occurs.

24.8 DMAC

24.8.1 Write to DMAE Bit in DMiCON Register

When both of the conditions below are met, follow the steps below.

Conditions

• The DMAE bit is set to "1" again while it remains set (DMAi is in an active state).

• A DMA request may occur simultaneously when the DMAE bit is being written.

Steps

- (1) Write "1" to the DMAE bit and DMAS bit in the DMiCON register simultaneously⁽¹⁾.
- (2) Make sure that the DMAi is in an initial state⁽²⁾ in a program.
- If the DMAi is not in an initial state, the above steps should be repeated.

NOTES:

1. The DMAS bit remains unchanged even if "1" is written. However, if "0" is written to this bit, it is set to "0" (DMA not requested). In order to prevent the DMAS bit from being modified to "0", "1" should be written to the DMAS bit when "1" is written to the DMAE bit. In this way the state of the DMAS bit immediately before being written can be maintained.

Similarly, when writing to the DMAE bit with a read-modify-write instruction, "1" should be written to the DMAS bit in order to maintain a DMA request which is generated during execution.

2.Read the TCRi register to verify whether the DMAi is in an initial state. If the read value is equal to a value which was written to the TCRi register before DMA transfer start, the DMAi is in an initial state. (If a DMA request occurs after writing to the DMAE bit, the value written to the TCRi register is "1".) If the read value is a value in the middle of transfer, the DMAi is not in an initial state.

24.9 Timers

24.9.1 Timer A

24.9.1.1 Timer A (Timer Mode)

The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TAiMR (i = 0 to 4) register and the TAi register before setting the TAiS bit in the TABSR register to "1" (count starts). Always make sure the TAiMR register is modified while the TAiS bit remains "0" (count stops) regardless whether after reset or not.

While counting is in progress, the counter value can be read out at any time by reading the TAi register. However, if the counter is read at the same time it is reloaded, the value "FFFFh" is read. Also, if the counter is read before it starts counting after a value is set in the TAi register while not counting, the set value is read.

If a low-level signal is applied to the $\overline{\text{NMI}}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on $\overline{\text{NMI}}$ pin enabled), the TA1OUT, TA2OUT and TA4OUT pins go to a high-impedance state.

24.9.1.2 Timer A (Event Counter Mode)

The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TAiMR (i = 0 to 4) register, the TAi register, the UDF register, the ONSF register TAZIE, TA0TGL and TA0TGH bits and the TRGSR register before setting the TAiS bit in the TABSR register to "1" (count starts).

Always make sure the TAiMR register, the UDF register, the TAZIE, TA0TGL and TA0TGH bits in the ONSF register and the TRGSR register are modified while the TAiS bit remains "0" (count stops) regardless whether after reset or not.

While counting is in progress, the counter value can be read out at any time by reading the TAi register. However, "FFFFh" can be read in underflow, while reloading, and "0000h" in overflow. When setting TAi register to a value during a counter stop, the setting value can be read before a counter starts counting. Also, if the counter is read before it starts counting after a value is set in the TAi register while not counting, the set value is read.

If a low-level signal is applied to the $\overline{\text{NMI}}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on $\overline{\text{NMI}}$ pin enabled), the TA1OUT, TA2OUT and TA4OUT pins go to a high-impedance state.

24.9.1.3 Timer A (One-shot Timer Mode)

The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TAiMR (i = 0 to 4) register, the TAi register, the TA0TGL and TA0TGH bits in the ONSF register and the TRGSR register before setting the TAiS bit in the TABSR register to "1" (count starts).

Always make sure the TAiMR register, the TAOTGL and TAOTGH bits and the TRGSR register are modified while the TAiS bit remains "0" (count stops) regardless whether after reset or not.

When setting TAiS bit to "0" (count stop), the followings occur:

- A counter stops counting and a content of reload register is reloaded.
- TAiOUT pin outputs "L".
- After one cycle of the CPU clock, the IR bit in the TAiIC register is set to "1" (interrupt request).

Output in one-shot timer mode synchronizes with a count source internally generated. When an external trigger has been selected, one-cycle delay of a count source as maximum occurs between a trigger input to TAiIN pin and output in one-shot timer mode.

The IR bit is set to "1" when timer operating mode is set with any of the following procedures:

- Select one-shot timer mode after reset.
- Change an operating mode from timer mode to one-shot timer mode.

• Change an operating mode from event counter mode to one-shot timer mode.

To use the Timer Ai interrupt (the IR bit), set the IR bit to "0" after the changes listed above have been made.

When a trigger occurs, while counting, a counter reloads the reload register to continue counting after generating a re-trigger and counting down once. To generate a trigger while counting, generate a second trigger between occurring the previous trigger and operating longer than one cycle of a timer count source.

If a low-level signal is applied to the $\overline{\text{NMI}}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on $\overline{\text{NMI}}$ pin enabled), the TA1OUT, TA2OUT and TA4OUT pins go to a high-impedance state.

24.9.1.4 Timer A (Pulse Width Modulation Mode)

The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TAiMR (i = 0 to 4) register, the TAi register, the TA0TGL and TA0TGH bits in the ONSF register and the TRGSR register before setting the TAiS bit in the TABSR register to "1" (count starts).

Always make sure the TAiMR register, TA0TGL and TA0TGH bits and the TRGSR register are modified while the TAiS bit remains "0" (count stops) regardless whether after reset or not.

The IR bit is set to "1" when setting a timer operating mode with any of the following procedures:

- · Select the PWM mode after reset.
- Change an operating mode from timer mode to PWM mode.
- Change an operating mode from event counter mode to PWM mode.

To use the Timer Ai interrupt (interrupt request bit), set the IR bit to "0" by program after the above listed changes have been made.

When setting TAiS register to "0" (count stop) during PWM pulse output, the following action occurs:

- Stop counting.
- When TAiOUT pin is output "H", output level is set to "L" and the IR bit is set to "1".
- When TAiOUT pin is output "L", both output level and the IR bit remains unchanged.

If a low-level signal is applied to the $\overline{\text{NMI}}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on $\overline{\text{NMI}}$ pin enabled), the TA1OUT, TA2OUT and TA4OUT pins go to a high-impedance state.

24.9.2 Timer B

24.9.2.1 Timer B (Timer Mode)

The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TBiMR (i = 0 to 5) register and TBi register before setting the TBiS bit in the TABSR or the TBSR register to "1" (count starts). Always make sure the TBiMR register is modified while the TBiS bit remains "0" (count stops) regardless whether after reset or not.

A value of a counter, while counting, can be read in TBi register at any time. "FFFFh" is read while reloading. Setting value is read between setting values in TBi register at count stop and starting a counter.

24.9.2.2 Timer B (Event Counter Mode)

The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TBiMR (i = 0 to 5) register and TBi register before setting the TBiS bit in the TABSR or the TBSR register to "1" (count starts). Always make sure the TBiMR register is modified while the TBiS bit remains "0" (count stops) regardless whether after reset or not.

The counter value can be read out on-the-fly at any time by reading the TBi register. However, if this register is read at the same time the counter is reloaded, the read value is always "FFFFh". If the TBi register is read after setting a value in it while not counting but before the counter starts counting, the read value is the one that has been set in the register.

24.9.2.3 Timer B (Pulse Period/pulse Width Measurement Mode)

The timer remains idle after reset. Set the mode, count source, etc. using the TBiMR (i = 0 to 5) register before setting the TBiS bit in the TABSR or the TBSR register to "1" (count starts).

Always make sure the TBiMR register is modified while the TBiS bit remains "0" (count stops) regardless whether after reset or not. To clear the MR3 bit to "0" by writing to the TBiMR register while the TBiS bit = 1 (count starts), be sure to write the same value as previously written to the TM0D0, TM0D1, MR0, MR1, TCK0 and TCK1 bits and a 0 to the MR2 bit.

The IR bit in the TBiIC register (i=0 to 5) goes to "1" (interrupt request), when an effective edge of a measurement pulse is input or Timer Bi is overflowed. The factor of interrupt request can be determined by use of the MR3 bit in the TBiMR register within the interrupt routine.

If the source of interrupt cannot be identified by the MR3 bit such as when the measurement pulse input and a timer overflow occur at the same time, use another timer to count the number of times Timer B has overflowed.

To set the MR3 bit to "0" (no overflow), set TBiMR register with setting the TBiS bit to "1" and counting the next count source after setting the MR3 bit to "1" (overflow).

Use the IR bit to detect only overflows. Use the MR3 bit only to determine the interrupt factor.

When a count is started and the first effective edge is input, an indeterminate value is transferred to the reload register. At this time, Timer Bi interrupt request is not generated.

A value of the counter is indeterminate at the beginning of a count. MR3 may be set to "1" and Timer Bi interrupt request may be generated between a count start and an effective edge input.

For pulse width measurement, pulse widths are successively measured. Use program to check whether the measurement result is an "H" level width or an "L" level width.

24.10 Serial interface

24.10.1 Clock Synchronous Serial I/O

24.10.1.1 Transmission/reception

With an external clock selected, and choosing the $\overline{\text{RTS}}$ function, the output level of the $\overline{\text{RTS}}$ pin goes to "L" when the data-receivable status becomes ready, which informs the transmission side that the reception has become ready. The output level of the $\overline{\text{RTS}}$ pin goes to "H" when reception starts. So if the $\overline{\text{RTS}}$ pin is connected to the $\overline{\text{CTS}}$ pin on the transmission side, the circuit can transmission and reception data with consistent timing. With the internal clock, the $\overline{\text{RTS}}$ function has no effect.

If a low-level signal is applied to the $\overline{\text{NMI}}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on $\overline{\text{NMI}}$ pin enabled), the $\overline{\text{RTS2}}$ and CLK2 pins go to a high-impedance state.

24.10.1.2 Transmission

When an external clock is selected, the conditions must be met while if the CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the external clock is in the high state; if the CKPOL bit in the UiC0 register = 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the high state; if the CKPOL bit in the UiC0 register = 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the low state.

- The TE bit in the UiC1 register= 1 (transmission enabled)
- The TI bit in the UiC1 register = 0 (data present in UiTB register)
- If $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTSi}}$ pin = L

24.10.1.3 Reception

In operating the clock-synchronous serial I/O, operating a transmitter generates a shift clock. Fix settings for transmission even when using the device only for reception. Dummy data is output to the outside from the TXDi pin when receiving data.

When an internal clock is selected, set the TE bit in the UiC1 register (i = 0 to 2) to 1 (transmission enabled) and write dummy data to the UiTB register, and the shift clock will thereby be generated.

When an external clock is selected, set the TE bit to 1 and write dummy data to the UiTB register, and the shift clock will be generated when the external clock is fed to the CLKi input pin.

When successively receiving data, if all bits of the next receive data are prepared in the UARTi receive register while the RE bit in the UiC1 register (i = 0 to 2) = 1 (data present in the UiRB register), an overrun error occurs and the OER bit in the UiRB register is set to "1" (overrun error occurred). In this case, because the content of the UiRB register is indeterminate, a corrective measure must be taken by programs on the transmit and receive sides so that the valid data before the overrun error occurred will be retransmitted. Note that when an overrun error occurred, the IR bit in the SiRIC register does not change state.

To receive data in succession, set dummy data in the lower-order byte of the UiTB register every time reception is made.

When an external clock is selected, the conditions must be met while if the CKPOL bit = 0, the external clock is in the high state; if the CKPOL bit = 1, the external clock is in the low state.

- The RE bit in the UiC1 register= 1 (reception enabled)
- The TE bit in the UiC1 register= 1 (transmission enabled)
- The TI bit in the UiC1 register= 0 (data present in the UiTB register)

24.10.2 UART

24.10.2.1 Special Mode 1(I²C Mode)

When generating start, stop and restart conditions, set the STSPSEL bit in the UiSMR4 register to "0" and wait for more than half cycle of the transfer clock before setting each condition generate bit (STAREQ, RSTAREQ and STPREQ) from "0" to "1".

24.10.2.2 Special Mode 2

If a low-level signal is applied to the $\overline{\text{NMI}}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on $\overline{\text{NMI}}$ pin enabled), the $\overline{\text{RTS2}}$ and CLK2 pins go to a high-impedance state.

24.10.2.3 Special Mode 4 (SIM Mode)

A transmit interrupt request is generated by setting the U2C1 register U2IRS bit to "1" (transmission complete) and U2ERE bit to "1" (error signal output) after reset is deasserted. Therefore, when using SIM mode, be sure to clear the IR bit to "0" (no interrupt request) after setting these bits.

24.10.3 SI/O3, SI/O4

The SOUTi default value which is set to the SOUTi pin by the SMi7 bit approximately 10ns may be output when changing the SMi3 bit from "0" (I/O port) to "1" (SOUTi output and CLK function) while the SMi2 bit in the SiC (i=3 and 4) to "0" (SOUTi output) and the SMi6 bit is set to "1" (internal clock). And then the SOUTi pin is held high-impedance.

If the level which is output from the SOUTi pin is a problem when changing the SMi3 bit from "0" to "1", set the default value of the SOUTi pin by the SMi7 bit.

24.11 A/D Converter

Set ADCON0 (except bit 6), ADCON1 and ADCON2 registers when A/D conversion is stopped (before a trigger occurs).

When the VCUT bit in the ADCON1 register is changed from "0" (Vref not connected) to "1" (Vref connected), start A/D conversion after passing 1 µs or longer.

To prevent noise-induced device malfunction or latchup, as well as to reduce conversion errors, insert capacitors between the AVCC, VREF, and analog input pins (ANi(i=0 to 7), AN0_i, AN2_i) each and the AVSS pin. Similarly, insert a capacitor between the VCC1 pin and the VSS pin. Figure 24.4 is an example connection of each pin.

Make sure the port direction bits for those pins that are used as analog inputs are set to "0" (input mode). Also, if the TGR bit in the ADCON0 register = 1 (external trigger), make sure the port direction bit for the $\overline{\text{ADTRG}}$ pin is set to "0" (input mode).

When using key input interrupts, do not use any of the four AN4 to AN7 pins as analog inputs. (A key input interrupt request is generated when the A/D input voltage goes low.)

The ϕ AD frequency must be 12MHz or less. Without sample-and-hold function, limit the ϕ AD frequency to 250kHz or more. With the sample and hold function, limit the ϕ AD frequency to 1MHz or more.

When changing an A/D operating mode, select analog input pin again in the CH2 to CH0 bits in the ADCON0 register and the SCAN1 to SCAN0 bits in the ADCON1 register.

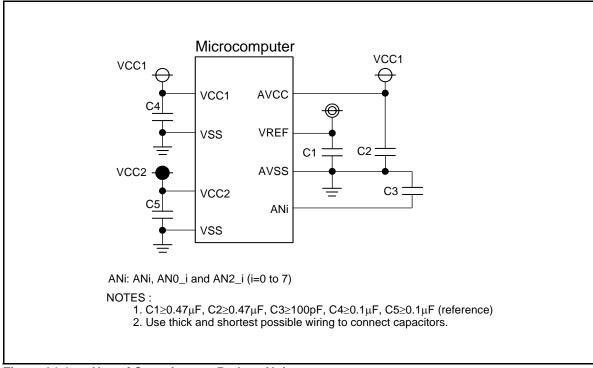


Figure 24.4 Use of Capacitors to Reduce Noise

Rev.2.41 Jan 10, 2006 Page 375 of 390 **RENESAS** REJ09B0185-0241 If VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.

If the CPU reads the ADi register (i = 0 to 7) at the same time the conversion result is stored in the ADi register after completion of A/D conversion, an incorrect value may be stored in the ADi register. This problem occurs when a divide-by-n clock derived from the main clock or a subclock is selected for CPU clock.

• When operating in one-shot or single-sweep mode

Check to see that A/D conversion is completed before reading the target ADi register. (Check the IR bit in the ADIC register to see if A/D conversion is completed.)

• When operating in repeat mode or repeat sweep mode 0 or 1 Use the main clock for CPU clock directly without dividing it.

If A/D conversion is forcibly terminated while in progress by setting the ADST bit in the ADCON0 register to "0" (A/D conversion halted), the conversion result of the A/D converter is indeterminate. The contents of ADi registers irrelevant to A/D conversion may also become indeterminate. If while A/D conversion is underway the ADST bit is cleared to "0" in a program, ignore the values of all ADi registers.

When setting the ADST bit in the ADCON0 register to "0" in single-sweep mode during A/D conversion and suspending A/D conversion, disable the interrupt before setting the ADST bit to "0".

The applied intermediate potential may cause more increase in power consumption than other analog input pins (AN0 to AN3, AN0_0 to AN0_7 and AN2_0 to AN2_7), since the AN4 to AN7 are used with the KI0 to KI3.

24.12 Programmable I/O Ports

If a low-level signal is applied to the $\overline{\text{NMI}}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on $\overline{\text{NMI}}$ pin enabled), the P7_2 to P7_5, P8_0 and P8_1 pins go to a high-impedance state.

Setting the SM32 bit in the S3C register to "1" causes the P9_2 pin to go to a high-impedance state. Similarly, setting the SM42 bit in the S4C register to "1" causes the P9_6 pin to go to a high-impedance state.

The input threshold voltage of pins differs between programmable input/output ports and peripheral functions. Therefore, if any pin is shared by a programmable input/output port and a peripheral function and the input level at this pin is outside the range of recommended operating conditions VIH and VIL (neither "high" nor "low"), the input level may be determined differently depending on which side-the programmable input/output port or the peripheral function-is currently selected.

When changing the PD14_i bit (i=0 to 1) in the PC14 register from "0" (input port) to "1" (output port), follow the procedures below.

•	Setting Procedure	
(1) Set P14_i bit	:MOV.B #00000001b, PC14 ; P14_i bit setting	
(2) Change PD14_i bit to "1" by MOV instruction	:MOV.B #00110001b, PC14 ; Change to output port	

Indeterminate values are read from the P3_7 to P3_4, PD3_7 to PD3_4 bits by reading the P3 and PD3 registers when the PM01 to PM00 bits in the PM0 register are set to "01b" (memory expansion mode) or "11b" (microprocessor mode) and setting the PM11 bit to "1".

Use the MOV instruction when rewriting the P3 and PD3 registers (including the case that the size specifier is ".W" and the P2 and PD2 registers are rewritten).

When the PM01 to PM00 bits are rewritten, "L" is output from the P3_7 to P3_4 pins during 0.5 cycles of the BCLK by setting the PM01 to PM00 bits in the PM0 register to "01b" (memory expansion mode) or "11b" (microprocessor mode) from "00b" (single-chip mode) after setting the PM11 bit to "1".

24.13 Electric Characteristic Differences Between Mask ROM and Flash Memory Version Microcomputers

Flash memory version and mask ROM version may have different characteristics, operating margin, noise tolerated dose, noise width dose in electrical characteristics due to internal ROM, different layout pattern, etc. When switching to the mask ROM version, conduct equivalent tests as system evaluation tests conducted in the flush memory version.

24.14 Mask ROM

When using the masked ROM version, write nothing to internal ROM area.

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24.15 Flash Memory Version

24.15.1 Functions to Inhibit Rewriting Flash Memory Rewrite

ID codes are stored in addresses 0FFFDFh, 0FFFE3h, 0FFFEBh, 0FFFEFh, 0FFFF3h, 0FFFF7h, and 0FFFFBh. If wrong data are written to theses addresses, the flash memory cannot be read or written in standard serial I/O mode.

The ROMCP register is mapped in address 0FFFFFh. If wrong data is written to this address, the flash memory cannot be read or written in parallel I/O mode.

In the flash memory version of microcomputer, these addresses are allocated to the vector addresses (H) of fixed vectors.

24.15.2 Stop mode

When the microcomputer enters stop mode, execute the instruction which sets the CM10 bit to "1" (stop mode) after setting the FMR01 bit to "0" (CPU rewrite mode disabled) and disabling the DMA transfer.

24.15.3 Wait mode

When shifting to wait mode, set the FMR01 bit to "0" (CPU rewrite mode disabled) before executing the WAIT instruction.

24.15.4 Low power dissipation mode, on-chip oscillator low power dissipation mode

If the CM05 bit is set to "1" (main clock stop), the following commands must not be executed.

- Program
- Block erase
- Erase all unlocked blocks
- Lock bit program

24.15.5 Writing command and data

Write the command code and data at even addresses.

24.15.6 Program Command

Write "xx40h" in the first bus cycle and write data to the write address in the second bus cycle, and an auto program operation (data program and verify) will start. Make sure the address value specified in the first bus cycle is the same even address as the write address specified in the second bus cycle.

24.15.7 Lock Bit Program Command

Write "77h" in the first bus cycle and write "xxD0h" to the uppermost address of a block (even address, however) in the second bus cycle, and the lock bit for the specified block is cleared to "0". Make sure then address value specified in the first bus cycle is the same uppermost block address that is specified in the second bus cycle.

24.15.8 Operation speed

Before entering CPU rewrite mode (EW0 or EW1 mode), set the CM11 bit in the CM1 register to "0" (main clock), select 10 MHz or less for CPU clock using the CM06 bit in the CM0 register and CM17 to CM16 bits in the CM1 register. Also, set the PM17 bit in the PM1 register to "1" (with wait state).

24.15.9 Instructions inhibited against use

The following instructions cannot be used in EW0 mode because the flash memory's internal data is referenced: UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

24.15.10 Interrupts

EW0 Mode

- Any interrupt which has a vector in the relocatable vector table can be used providing that its vector is transferred into the RAM area.
- The NMI and watchdog timer interrupts can be used because the FMR0 register and FMR1 register are initialized when one of those interrupts occurs. The jump addresses for those interrupt service routines should be set in the fixed vector table.

Because the rewrite operation is halted when a $\overline{\text{NMI}}$ or watchdog timer interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.

• The address match interrupt cannot be used because the flash memory's internal data is referenced.

EW1 Mode

- Make sure that any interrupt which has a vector in the variable vector table or address match interrupt will not be accepted during the auto program or auto erase period.
- Avoid using watchdog timer interrupts.
- The $\overline{\text{NMI}}$ interrupt can be used because the FMR0 register and FMR1 register are initialized when this interrupt occurs. The jump address for the interrupt service routine should be set in the fixed vector table. Because the rewrite operation is halted when a $\overline{\text{NMI}}$ interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.

24.15.11 How to access

To set the FMR01, FMR02, or FMR11 bit to "1", write "0" and then "1" in succession. This is necessary to ensure that no interrupts or DMA transfers will occur before writing "1" after writing "0". Also only when $\overline{\text{NMI}}$ pin is "H" level.

24.15.12 Writing in the user ROM area

EW0 Mode

• If the power supply voltage drops while rewriting any block in which the rewrite control program is stored, a problem may occur that the rewrite control program is not correctly rewritten and, consequently, the flash memory becomes unable to be rewritten thereafter. In this case, standard serial I/O or parallel I/O mode should be used.

EW1 Mode

• Avoid rewriting any block in which the rewrite control program is stored.

24.15.13 DMA transfer

In EW1 mode, make sure that no DMA transfers will occur while the FMR00 bit in the FMR0 register = 0 (during the auto program or auto erase period).

24.15.14 Regarding Programming/Erasing Endurance and Execution Time

As the number of programming/erasure times increases, so does the execution time for software commands (Program, Block Erase, Erase All Unlock Blocks, and Lock Bit Program). Especially when the number of programming/erasure times exceeds 1,000, the software command execution time is noticeably extended. Therefore, the software command wait time that is set must be greater than the maximum rated value of electrical characteristics.

The software commands are suspended by hardware reset 1, hardware reset 2, $\overline{\text{NMI}}$ interrupt, and watchdog timer interrupt. If a software command is suspended by such reset or interrupt, the block that was in process must be erased before reexecuting the suspended command.

24.16 Noise

Connect a bypass capacitor (approximately 0.1 μ F) across the VCC1 and XSS pins, and VCC2 and VSS pins using the shortest and thicker possible wiring. Figure 24.5 shows the Bypass Capacitor Connection.

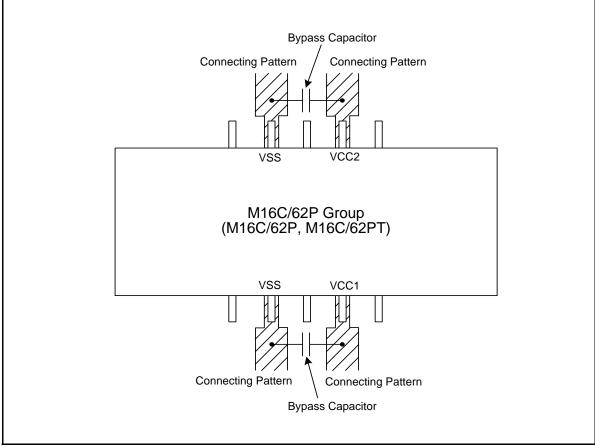


Figure 24.5 Bypass Capacitor Connection

25. Differences Depending on Manufacturing Period

Table 25.1 and Table 25.2 list the precautions are applicable or not applicable every chip version of M16C/62P flash and ROM external versions. Contact separately about the mask ROM version.

Table 25.1	Technical Update Applicable Table of M16C/62P Flash and ROM External Versions (1)
------------	---

Procession	Precaution Chip Version		TECHNICAL UPDATE	
	Α	В	С	TECHNICAL OFDATE
Ensure that RESET must hold valid-low state during power-on.				
When using a reset IC, use a CMOS type IC. When using an				
open-drain type reset IC, insert a capacitor between the reset		_	_	
input and VSS. Adjust the R-C time constant between the	•			
capacitor and pull-up resistor at least 10 times longer than the				
VCC rising time.				
If UART0 or UART1 are used as a slave in the I ² C mode, P6_1				
or P6_5 are placed in a high-impedance state. P6_1 or P6_5	,			
cannot be used as an output port even if the PD6_1 or PD6_5 bits	\checkmark	-	-	TN-M16C-100-0309
in the PD6 register are set to "1" (output mode). Therefore, set				
the PD6_1 or PD6_5 bits to "0" (Input mode).				
Do not enter wait mode when the main clock or on-chip oscillator				
clock is selected as the CPU clock of which division is set by the	\checkmark	_	_	TN-M16C-108-0309
CM06 bit in the CM0 register, and the CM16 and CM17 bits in the				Precaution 1.1
CM1 register.				
The CM05 bit in the CM0 register is set to "0" (main clock	,			TN-M16C-108-0309
oscillation) and the CM02 bit is set to "1" (peripheral function	\checkmark	-	-	Precaution 1.2
clock stops in wait mode).				
Do not generate an NMI interrupt after entering mode.	\checkmark	_	_	TN-M16C-108-0309
Do not concrete a valtage dataction intervine ofter entering				Precaution 1.3 TN-M16C-108-0309
Do not generate a voltage detection interrupt after entering mode.	\checkmark	-	-	Precaution 1.4
I/O ports (P0 to P5) will be indeterminate until internal power				FIECaulion 1.4
supply is stable, such as when the power is turned on, if "H" is				TN-M16C-114-0310
applied to the CNVSS pin and "L" to the RESET pin while internal	\checkmark			Precaution 1.1
power supply is unstable.				
I/O ports (P6 to P14) will be indeterminate until internal power				
supply is stable, such as when the power is turned on, if "H" is	,			TN-M16C-114-0310
applied to the CNVSS pin and "L" to the RESET pin while internal	\checkmark	-	-	Precaution 1.1
power supply is unstable.				
When the RESET pin is "L" in boot mode (apply "H" to the				
CNVSS pin and P5_0 (CE), and "L" to the P5_5 (EPM)), internal				
pull-up is enabled for P10_0 to P10_3, P11_0 to P11_7, P12_5		_	_	TN-M16C-114-0310
to P12_7, P13_0 to P13_7, P14_0 and P14_1 and so become "H"				Precaution 1.2
P0_0 to P0_7 and P1_0 to P1_7 may become indeterminate				
when P8_4 is "H" and the RESET pin is "L" in boot mode (apply				
"H" to the CNVSS pin and P5_0 (CE), and "L" to P5_5 (EPM)).	\checkmark	\checkmark		TN-M16C-114-0310
$P0_0$ to $P0_7$ and $P1_0$ to $P1_7$ are in a high impedance state	v	v	v	Precaution 1.3
when the RESET pin and P8_4 are "L".				

 $\sqrt{1}$: Applies

- : Dose not apply

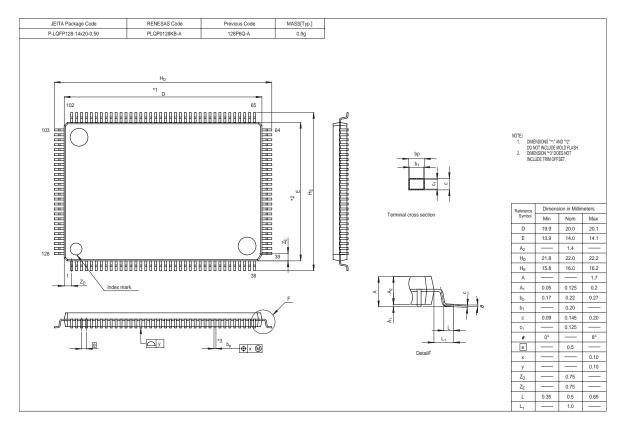
Precaution		p Ver	sion	TECHNICAL UPDATE	
	Α	В	С	TECHNICAL OF DATE	
When supplying power to the microcomputer, the power supply voltage applied to the VCC1 pin must meet the conditions of SVCC.	÷	-	-	TN-M16C-116-0311	
 Do not set the CM10 bit in the CM1 register to 1 (stop mode) with setting the VC13 bit in the VCR1 register to 1 (VCC1≥Vdet 4) when a low voltage detection interrupt in the voltage detection circuit is used under the following settings: the VC27 bit in the VCR2 register to 1 (low voltage detection circuit enabled) the D40 bit in the D4INT register to 1 (low voltage detection interrupt enabled) the D41 bit to 1 (use low voltage detection interrupt to exit stop mode) 	÷	-	-	TN-M16C-107-0309 Precaution 1.1	
Do not generate the NMI interrupt after setting the CM10 bit in the CM1 register to "1" (stop mode) and entering stop mode.	÷	-	-	TN-M16C-107-0309 Precaution 1.2	
 Do not set the CM10 bit in the CM1 register to "1" (stop mode) when the microcomputer is in low-speed mode under the following settings: the CM04 bit in the CM0 register is set to "1" (sub clock oscillation) the CM07 bit in the CM0 register is set to "1" (sub clock) 	÷	-	-	TN-M16C-107-0309 Precaution 1.3	
When using the sub clock (XCIN-XCOUT) as the CPU clock (BCLK) or as the timer count source, DO NOT leave the CM03 bit set to "1" (XCINXCOUT drive capacity "HIGH").	÷	÷	-	TN-M16C-119A/EA	

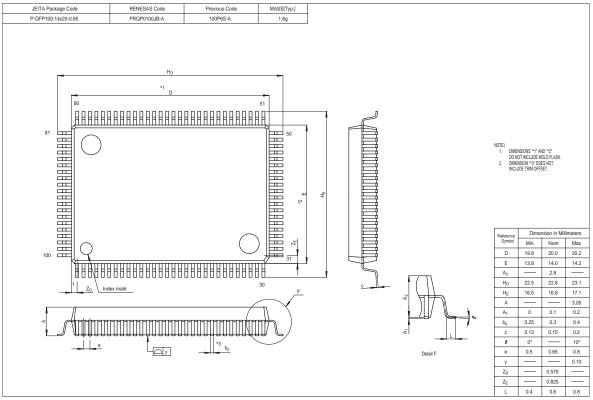
Table 25.2	Technical Update Applicable Table of M16C/62P Flash and ROM External Versions (2)

 $\sqrt{1}$: Applies

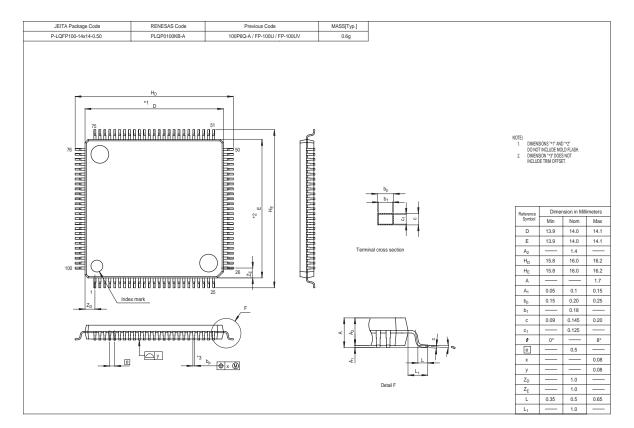
- : Dose not apply

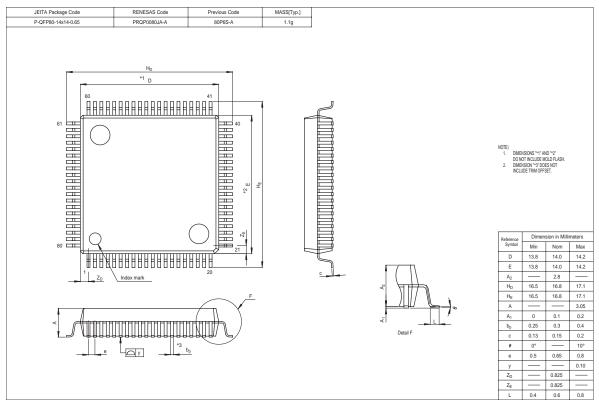
Appendix 1.Package Dimensions





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Appendix 2. Difference between M16C/62P and M16C/30P

Appendix Table 2.1	Function Difference (1) ⁽¹⁾	
Item	M16C/62P	M16C/62A
Shortest instruction	41.7ns (f(BCLK)=24MHz, VCC1=3.0 to 5.5V)	62.5ns (f(XIN)=16MHz, VCC=4.2V to 5.5V)
execution time	100ns (f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	100ns (f(XIN)=10MHz, VCC=2.7V to 5.5V
		with software one-wait)
Supply voltage	VCC1=3.0 to 5.5V, VCC2=3.0V to VCC1	VCC=4.2V to 5.5V (f(XIN)=16MHz,
	(f(BCLK)=24MHz)	without software wait)
	VCC1=VCC2=2.7 to 5.5V	VCC=2.7V to 5.5V (f(XIN)=10MHz,
	(f(BCLK)=10MHz)	with software one-wait)
I/O power supply	Double (VCC1, VCC2)	Single (VCC)
Package	80-pin, 100-pin, 128-pin plastic mold QFP	80-pin, 100-pin plastic mold QFP
Voltage detection	Built-in	None
circuit	Vdet3, Vdet4 detect	
	Voltage down detect interrupt	
	Hardware reset 2	
Clock Generating	PLL, XIN, XCIN, on-chip oscillator	XIN, XCIN
Circuit	When placed in low power mode, a divide-	When placed in low power mode, the
	by-8 value is used for these clocks. The XIN	divide-by-n value for the main clock
	drive capability is set to HIGH.	does not change. Nor does the XIN
		drive capability change.
System clock	Built-in	None
protective function	Duit in	(protected by protect register)
Oscillation Stop,	Built-in	None
Re-oscillation	Duit in	
Detection		
Function		
Low power	18mA (VCC1=VCC2=5V, f(BCLK)=24MHz)	32.5mA (VCC=5V, f(XIN)=16MHz)
consumption	8mA (VCC1=VCC2=3V, f(BCLK)=10MHz)	8.5mA (VCC=3V, f(XCIN)=10MHz with
consumption	$1.8\mu A (VCC1=VCC2=3V, f(XCIN)=32kHz,$	software one-wait)
		,
	when wait mode)	0.9μA (VCC=3V, f(XCIN)=32kHz,
Mamani	Mamany area avpandabla	when wait mode)
Memory Area	Memory area expandable	1 Mbytes fixed
External Device	(4 Mbytes) 04000h to 07FFFh(PM13=0)	
External Device		04000h to 05FFFh(PM13=0)
Connect	08000h to 0FFFh(PM10=0)	06000h to CFFFh
Area	10000h to 26FFFh	D0000h to FFFFh(Microprocessor mode)
	28000h to 7FFFh	
	80000h to CFFFFh(PM13=0)	
<u></u>	D0000h to FFFFh(Microprocessor mode)	
Upper address in	P4_0 to P4_3 (A16 to A19), P3_4 to P3_7	P4_0 to P4_3 (A16 to A19) : Switchable
memory expansion	(A12 to A15) : Switchable between	between address bus and I/O port
mode and	address bus and I/O port	A12 to A15 : No switchable
microprocessor mode		
Access to SFR	Variable (1 to 2 waits)	1 wait fixed
Software wait to	Variable (0 to 3 waits)	Variable (0 to 1 wait)
external area		
Protect	Can be set for PM0, PM1, PM2, CM0,	Can be set for PM0, PM1, CM0, CM1,
	CM1, CM2, PLC0, INVC0, INVC1, PD9,	PD9, S3C, S4C registers
	S3C, S4C, TB2SC, PCLKR, VCR2, D4INT	
	registers	
Watchdog timer	Watchdog timer interrupt or watchdog	Watchdog timer interrupt
	timer reset is selected	No count source protective mode
	Count source protective mode is available	
Address match	Count source protective mode is available 4	2

Appendix Table 2.1 Function Difference (1)⁽¹⁾

NOTES:

1. About the details and the electric characteristics, refer to hardware manual.

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ltem	M16C/62P	M16C/62A
Timers A, B count	Selectable: f1, f2, f8, f32, fC32	Selectable: f1, f8, f32, fC32
source		
Timer A two-phase	Function Z-phase (counter reset) input	No function Z-phase (counter reset) input
pulse signal		
processing		
Timer functions for	Function protect by protect register	Function protect by protect register
three-phase motor	Count source is selected:	Count source is selected:
control	f1, f2, f8, f32, fC32	f1, f8, f32, fC32
	Dead time timer count source is selected:	Dead time timer count source is fixed at f1
	f1, f1 divided by 2, f2, f2 divided by 2	divided by 2
	Three-phase output forcible shutoff function	
	based on NMI input is available, output	
	polarity change, carrier wave phase	
	detection.	
Serial I/O	(UART, clock synchronous, I ² C bus, IEBus)	(UART, clock synchronous) x 2
(UART0 to UART2)	x 3	(UART, clock synchronous, I ² C bus, IEBus)
		x 1
UART0 to UART2,	Select from f1SIO, f2SIO, f8SIO, f32SIO	Select from f1, f8, f32
SI/O3, SI/O4 count		
source		
Serial I/O RTS timing	Assert low when receive buffer is read	Assert low when reception is completed
UART0 to UART2	This error occurs if the serial I/O started	This error occurs when the next data is
Overrun Error	receiving the next data before reading the	ready before contents of UARTi receive
Generation Timing	UiRB register (i=0 to 2) and received the 7	buffer register are read out
	th bit of the next data (clock synchronous)	
	This error occurs if the serial I/O started	
	receiving the next data before reading the	
	UiRB register and received the bit one	
	before the last stop bit of the next data	
	(UART)	
CTS/RTS separate	Have	None
function		
UART2 data transmit	After data was written, transfer starts at the	After data was written, transfer starts at the
UART2 data transmit timing	After data was written, transfer starts at the 2nd BRG overflow timing	After data was written, transfer starts at the 1st BRG overflow timing
		1st BRG overflow timing (Output starts one cycle of BRG overflow
timing	2nd BRG overflow timing	1st BRG overflow timing
	2nd BRG overflow timing	1st BRG overflow timing (Output starts one cycle of BRG overflow
timing Serial I/O sleep function	2nd BRG overflow timing (same as UART0 and UART1) None	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have
timing Serial I/O sleep	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition:	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition:
timing Serial I/O sleep function Serial I/O I ² C mode	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable
timing Serial I/O sleep function Serial I/O I ² C mode Serial I/O I ² C mode	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable Only digital delay is selected as SDA delay	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA
timing Serial I/O sleep function Serial I/O I ² C mode	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA delay
timing Serial I/O sleep function Serial I/O I ² C mode Serial I/O I ² C mode SDA delay	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable Only digital delay is selected as SDA delay SDA digital delay count source: BRG	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA delay SDA digital delay count source: 1/ f(XIN)
timing Serial I/O sleep function Serial I/O I ² C mode SDA delay SI/O3, SI/O4 clock	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable Only digital delay is selected as SDA delay	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA delay
timing Serial I/O sleep function Serial I/O I ² C mode SDA delay SI/O3, SI/O4 clock polarity	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable Only digital delay is selected as SDA delay SDA digital delay count source: BRG Selectable	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA delay SDA digital delay count source: 1/ f(XIN) Fixed
timing Serial I/O sleep function Serial I/O I ² C mode SDA delay SI/O3, SI/O4 clock	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable Only digital delay is selected as SDA delay SDA digital delay count source: BRG Selectable 10 bits X 8 channels	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA delay SDA digital delay count source: 1/ f(XIN) Fixed 10 bits X 8 channels
timing Serial I/O sleep function Serial I/O I ² C mode Serial I/O I ² C mode SDA delay SI/O3, SI/O4 clock polarity A/D Converter	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable Only digital delay is selected as SDA delay SDA digital delay count source: BRG Selectable 10 bits X 8 channels Expandable up to 26 channels	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA delay SDA digital delay count source: 1/ f(XIN) Fixed 10 bits X 8 channels Expandable up to 10 channels
timing Serial I/O sleep function Serial I/O I ² C mode SDA delay SI/O3, SI/O4 clock polarity	2nd BRG overflow timing (same as UART0 and UART1) None Start condition, stop condition: Auto-generationable Only digital delay is selected as SDA delay SDA digital delay count source: BRG Selectable 10 bits X 8 channels	1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1) Have Start condition, stop condition: Not auto-generationable Analog or digital delay is selected as SDA delay SDA digital delay count source: 1/ f(XIN) Fixed 10 bits X 8 channels

Appendix Table 2.2 Function Difference (1)⁽¹⁾

NOTES:

1. About the details and the electric characteristics, refer to hardware manual.

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ltem	M16C/62P	M16C/62A
User ROM blocks	14 blocks: 4 Kbytes x 3, 8 Kbytes x 3,	7 blocks: 8 Kbytes x 2, 16 Kbytes x1,
	32 Kbytes x1, 64 Kbytes x 7	32 Kbytes x 1, 64 Kbytes x 3
	(Flash memory: max. 512 Kbytes)	(Flash memory: max. 256 Kbytes)
Program manner	Word	Page
Program command	Page program command: none	Page program command: have
(software command)	Program command: have	Program command: none
	(program method: in units of word, in units of byte)	(program method: in units of page)
Block status after	None	Have
program function		
CPU rewrite	EW1 mode is available	No EW1 mode
mode		

Appendix Table 2.3	Function Difference	(1)	(1))
--------------------	---------------------	-----	-----	---

NOTES:

1. About the details and the electric characteristics, refer to hardware manual.

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U0C1 to U2C1185
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U0RB to U2RB181
U0SMR to U2SMR186
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U0SMR3 to U2SMR3187
U0SMR4 to U2SMR4188
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Pov	Dete		Description
Rev.	Date	Page	Summary
1.0	Jan 31, 2003	1	Applications are partly revised.
		2	Table 1.1.1 is partly revised.
		5	Table 1.1.3 is partly revised.
			Figure 1.1.2 is partly revised.
		11	Explanation of "Memory" is partly revised.
		20	Explanation of "Hardware Reset 1" is partly revised.
		21	Figure 1.5.1 is partly revised.
		22	Figure 1.5.2 is partly revised.
		24	Figure 1.5.4 is partly revised.
		25	VCR2 Register in Figure 1.5.6 is partly revised.
		26	Figure 1.5.6 is partly revised.
		27	Explanation of "Power Supply Down Detection Interrupt" is partly revised.
		30	Figure 1.6.1 is partly revised.
		31	Figure 1.6.2 is partly revised.
		39	Table 1.7.5 is partly revised.
		41	Table 1.7.7 is partly revised.
		43	Figure 1.7.8 is partly revised.
		44	Explanation of "4 Mbyte Mode" is partly revised.
		53	Notes 12 and 13 in Figure 1.9.2 is partly revised.
		54	Notes 2 and 5 in Figure 1.9.3 is partly revised.
		55	Figure 1.9.4 is partly revised.
		57	Note 4 in Figure 1.9.6 is partly revised.
		60	Explanation of "PLL Clock" is partly revised.
		61	Figure 1.9.9 is partly revised.
		62	Explanation of "CPU Clock and BCLK" is partly revised.
		63	Explanation of "Low-speed Mode" is partly revised.
			Explanation of "Low Power Dissipation Mode" is partly revised.
		64	Explanation of "Low Power Dissipation Mode" is partly revised.
			Explanation of "On-chip Oscillator Low Power Dissipation Mode" is partly revised.
			Table 1.9.3 is partly revised.
		65	Table 1.9.5 is partly revised.
		68	Figure 1.9.10 is partly revised.
		69	Figure 1.9.11 is partly revised.
		70	Table 1.9.7 is added.
		71	Explanation of "System Clock Protective Function" is partly revised.
		77	Explanation of "Power Supply Down Detection Interrupt" is partly revised.
		78	Table 1.11.1 is partly revised.

Rev. Date	Dut	Description	
Rev.	Date	Page	Summary
		88	Figure 1.11.9 is partly revised.
		96	WDTS Register in Figure 1.12.2 is partly revised.
		99	Figure 1.13.2 is partly revised.
		100	Figure 1.13.3 is partly revised.
		103	Figure 1.13.5 is partly revised.
		104	Table 1.13.3 is partly revised.
		105	Explanation of "DMA Enable" is partly revised.
		109	Figure 1.14.3 is partly revised.
		115	Table 1.14.5 is partly revised.
		117	Explanation of "Counter Initialization by Two-Phase Pulse Signal Processing" is partly revised.
		117	Figure 1.14.10 is partly revised.
		122	Figure 1.14.14 is partly revised.
			Figure 1.14.15 is partly revised.
		124	Figure 1.15.3 is partly revised.
		128	Figure 1.15.7 is partly revised.
		128	Figure 1.15.8 is partly revised.
		130	Figure 1.16.1 is partly revised.
		132	Figure 1.16.3 is partly revised.
		134	Note 7 is added to TAi, TAi1 Register in Figure 1.16.5.
		137	Figure 1.16.8 is partly revised.
		146	UiSMR2 Register in Figure 1.17.7 is partly revised.
		163	Figure 1.20.1 is partly revised.
		164, 165	Table 1.20.2 and Table 1.20.3 are partly revised.
		169	Figure 1.20.4 is partly revised.
			Explanation of "Arbitration" is partly revised.
		170	Explanation of "Transfer Clock" is partly revised.
		171	Explanation of "ACK and NACK" is partly revised.
		179	Explanation of "Special Mode 4 (SIM Mode)" is partly revised.
			Table 1.20.9 is partly revised.
		184	Figure 1.21.1 is partly revised.
		187	Figure 1.21.4 is partly revised.
		203	Explanation of "External Operation Amp Connection Mode" is partly revised.
		205	Explanation of "Caution of Using A/D Converter" is partly revised.
			Figure 1.22.11 is partly revised
		206	Table 1.23.1 is partly revised.
		207	Figure 1.23.3 is partly revised.

Rev.	Date		Description
Rev.	Date	Page	Summary
		218	Figure 1.25.9 is partly revised.
		223	Table 1.26.1 is partly revised.
		224	Table 1.26.2 is partly revised.
		225	Note 1 of Table 1.26.3 is partly revised.
			Note 1 of Table 1.26.4 is partly revised.
			Table 1.26.6 is partly revised.
		227	Note 1 of Table 1.26.9 is partly revised.
		228	Note 1 of Table 1.26.10 is partly revised.
		229	Measurement conditions of timing requirements are partly revised.
			Table 1.26.11 is partly revised.
		230	Measurement conditions of timing requirements are partly revised.
		230	Table 1.26.18 is added.
		231	Measurement conditions of timing requirements are partly revised.
		232	Measurement conditions of switching characteristics are partly revised.
		233	Measurement conditions of switching characteristics are partly revised.
		234	Measurement conditions of switching characteristics are partly revised.
		235	Figure 1.26.2 is partly revised.
		242	Figure 1.26.9 is partly revised.
		244	Note of Table 1.26.28 is partly revised.
		245	Figure 1.26.29 is partly revised.
		246	Measurement conditions of timing requirements are partly revised.
			Table 1.26.30 is partly revised.
		247	Measurement conditions of timing requirements are partly revised.
		247	Table 1.26.37 is added.
		248	Measurement conditions of timing requirements are partly revised.
		249	Measurement conditions of switching characteristics are partly revised.
		250	Measurement conditions of switching characteristics are partly revised.
		251	Measurement conditions of switching characteristics are partly revised.
		252	Figure 1.26.12 is partly revised.
		255	Figure 1.26.15 is partly revised.
		256	Figure 1.26.16 is partly revised.
		257	Figure 1.26.17 is partly revised.
		258	Figure 1.26.18 is partly revised.
		259	Figure 1.26.19 is partly revised.
		260	Figure 1.26.20 is partly revised.
		262	Explanation of "Memory Map" is partly revised.
		263	Explanation of "Boot Mode" is partly revised.
		264	Figure 1.27.3 is partly revised.
		268	Note of FIDR Register in Figure 1.27.4 is partly revised.

Rev.	Date		Description
Rev.	Dale	Page	Summary
		271	Figure 1.27.7 is partly revised.
		272	Explanation of "Interrupts" is partly revised.
			Explanation of "Writing in the User ROM Space" is partly revised.
		274	Table 1.27.4 is partly revised.
			Explanation of "Read Array Command" is partly revised.
		278	Explanation of "Program Command" is partly revised.
		287	Figure 1.27.15 is partly revised.
		293	Partly revised.
1.10	May 28, 2003	2	Table 1.1.1 is partly revised.
		4-5	Table 1.1.2 and 1.1.3 is partly revised.
		14-19	SFR is partly revised.
			Note 1 is partly revised.
		20	Explanation of "Hardware Reset 1" is partly revised.
		23	Note 1 is added.
		24	Figure 1.5.4 is partly revised.
			Note 1 of Figure 1.5.5 is partly revised.
		26	Figure 1.5.7 is partly revised.
		27	Table 1.5.2 is partly revised.
			Table 1.5.3 is partly revised.
			Explanation of "1. Limitations on Stop Mode" is partly revised.
		28	Explanation of "1. Limitations on WAIT instruction" is partly revised.
			Figure 1.5.8 is partly revised.
		31	Note is added.
		33	Explanation of "Multiplexed Bus" is revised.
		34	Explanation of "(2) Data Bus" is revised.
		38	Explanation of "(7) Hold Signal" is revised.
			Note 3 of Table 1.7.4 is added.
		39	Note 4 of Table 1.7.5 is added.
		40	Explanation of "(10) Software Wait" is revised.
		41	Table 1.7.7 is revised.
		46	Table of Figure 1.8.5 is revised.
		47	Explanation is revised.
		48-50	Figures 1.8.7 to 1.8.9 is partly revised.
		51	Explanation of "Clock Generation Circuit" is revised.
		52	Figure 1.9.1 is revised.
		53	Note of Figure 1.9.2 is revised.
		55	Note 12 is added.
		58	Explanation of "(1) Main clock" is partly revised.
		60	Explanation of "(4) PLL Clock" is partly revised.

Davi	Data		Description
Rev.	Date	Page	Summary
		63	Explanation of "Low power Dissipation Mode" is partly revised.
		64	Explanation of "Entering Wait mode" is partly revised.
		66	Explanation of "(3) Stop Mode" is partly revised.
		69	Note 9 is added.
		70	Table 1.9.7 is revised.
		75	Figure 1.11.1 is revised.
		79	Note 6 is added.
		83	Note 2 is added to Figure 1.11.4.
		84	Table 1.11.5 is partly revised.
		85	Figure 1.11.6 is partly revised.
		86	Figure 1.11.8 is partly revised.
		89	Notes 1 to 2 is added to IFSR register of Figure 1.11.4.
		91	Explanation of "Address Match Interrupt" is partly revised.
			Figure 1. 11.12 is changed into Table 1.11.6.
		93-94	Notes are deleted. (All notes are indicated in "M16C/62 GROUP (M16C/ 62P) USAGE NOTES").
		93	Explanation of "Watchdog Timer" is partly revised.
		94	A formula is added.
		104	Explanation of "Channel Priority Transfer Timing" is partly revised.
		109	TRGSR register of Figure 1.14.6 is partly revised.
		116	Table 1.14.4 is partly revised.
		117	Figure 1.14.12 is partly revised.
		129	Figure 1.16.2 is partly revised.
		130	Figure 1.16.3 is partly revised.
		143	U0SMR to U2SMR of Figure 1.17.6 is partly revised.
		144	U0SMR2 to U2SMR2 of Figure 1.17.7 is partly revised.
		154,162, 175	"-" of UiBRG of Tables 1.19.2, 1.20.2 and 1.20.8 is changed into "0 to 7".
		161	Figure 1.20.1 is partly revised.
		164	Table 1.20.4 is partly revised. Notes 5 to 7 is added.
		166	Explanation of "Output of Start and Stop Condition" is partly revised.
		177	Note 2 is added to Table 1.20.9.
		178	"-" of U2BRG of Table 1.20.10 is changed into "0 to 7".
		179	Figure 1.20.10 is revised.
		183	Note of SiC register of Figure 1.21.2 is partly revised.
		187	Note 2 of Table 1.22.1 is revised.
		188	Figure 1.22.1 is partly revised.
		190	Table of ADCON2 register of Figure 1.22.3 is partly revised.
		202	The value of a capacitor of Figure 1.22.10 is changed.

Dav	Data		Description
Rev.	Date	Page	Summary
		202	Notes are deleted. (All notes are indicated in "M16C/62 GROUP (M16C/ 62P) USAGE NOTES").
		208- 212	Note 1 of Figures 1.25.1 to 1.25.5 is partly revised.
		218	Table 1.25.1 and 1.25.2 is revised.
		219	Figure 1.25.12 is partly revised.
		222	Table 1.26.3 is partly revised.
		223	Table 1.26.5 is partly revised.
			Table 1.26.6 is added.
		224	Table 1.26.9 is partly revised.
		230	Notes 1 and 2 in Table 1.26.26 is partly revised.
		231	Notes 1 in Table 1.26.27 is partly revised.
		230- 231	Note 3 is added to "Data output hold time (refers to BCLK)" in Table 1.26.26 and 1.26.27.
		232	Note 4 is added to "th(ALE-AD)" in Table 1.26.28.
		230- 232	Switching Characteristics is partly revised.
		236- 239	th(WR-AD) and th(WR-DB) in Figure 1.26.5 to 1.5.8 is partly revised.
		240- 241	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.26.9 to 1.5.10 is partly revised.
		242	Note 2 is added to Table 1.26.29.
		247	Notes 1 and 2 in Table 1.26.45 is partly revised.
		248	Notes 1 in Table 1.26.46 is partly revised.
		247- 248	Note 3 is added to "Data output hold time(refers to BCLK)" in Table 1.26.45 and 1.26.46
		249	Note 4 is added to "th(ALE-AD)" in Table 1.26.47.
		247- 249	Switching Characteristics is partly revised.
		253- 256	th(WR-AD) and th(WR-DB) in Figure 1.26.15 to 1.5.18 is partly revised.
		257- 258	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.26.19 to 1.5.20 is partly revised.
		259	Table 1.27.1 is partly revised. Notes 3 and 4 is added.
		260	Notes 1 and 2 is added to Table 1.27.2.
		264	Note 2 is added to Table 1.27.3.
		267	Notes 1 and 3 of FMR0 register of Table 1.27.4 is partly revised.
		268	Figure 1.27.5 is partly revised. Note 2 is added.
		270	Figure 1.27.7 is partly revised.
		277	Figure 1.27.11 is partly revised.
		281	Figure 1.27.12 is partly revised.

Boy	Data		Description
Rev.	Date	Page	Summary
		283	Table 1.27.7 is partly revised.
		284- 286	Figures 1.27.13 to 1.27.15 is partly revised.
		287- 288	Figures 1.27.16 and 1.27.17 is partly revised.
		292- 293	Difference in Mask ROM Version and Flash Memory Version is revised.
		294	Difference in Flash Memory Version is revised.
1.11	Jun 20, 2003	259	Number of program and erasure in Table 1.26.27 is partly revised.
1.20	Sep 11, 2003	94	Figure 1.12.2 is revised.
2.30	Sep 01, 2004	_	Since high reliability version is added, a group name is revised. M16C/62P Group (M16C/62P) M16C/62P Group (M16C/62P, M16C/ 62PT)
		2-4	Table 1.1 to 1.3 are revised.
			Note 3 is partly revised.
		6	Figure 1.2 Note5 is deleted.
		7-9	Table 1.4 to 1.7 Product List is partly revised.
		11	Table 1.8 and Figure 1.4 are added.
		12	Table 1.9 and Figure 1.5 are added.
		13-16	Figure 1.6 to 1.9 ZP is added.
		17	Table 1.10 and 1.13 ZP is added to timer A.
		18, 20	Table 1.11 to 1.13 are revised.
		19, 21	Table 1.12 to 1.14 are revised.
		24	Figure 3.1 is partly revised.
			Note 3 is added.
		25	Note 6 is added.
		30	After Reset of D/A register 0, 1 are revised.
		31	5.2 Voltage Down Detection Reset (Hardware Reset 2) is revised.
		32	Figure 5.1 is partly revised.
		35	Figure 6.1 is partly revised.
		36	Figure 6.2 is revised.
		37	Figure 6.3 is revised.
		39	Figure 6.4 is revised.
		40	6.2 Limitations on Exiting Stop Mode and 6.3 Limitations on Exiting Wait Mode are revised.
		41	Note in 7. Processor is added.
		44	Figure 7.2 is partly revised.
		46	Note in 8. Bus is added.
			8.1.2.2 When the input level on BYTE pin is low (16-bit data bus) is revised.

Rev.	Dete		Description
Rev.	Date	Page	Summary
		46	Table 8.1 is added.
		47	Note 2 in Figure 8.1 is revised.
		50	Figure 8.4 is revised.
		54	Table 8.8 is partly revised.
			Note 5 is added.
		57	Note in 9 Memory Space Expansion Function is added.
		62-64	Figure 9.7 to 9.9 are revised.
		79	Table 10.4 is partly revised.
		81	Table 10.6 is partly revised.
		82	Figure 10.10 is partly revised.
		83	Note 6 in figure 10.11 is added.
		88	Note in 11. Protect is added.
		89	Note in 12. Interrupt is added.
		108	Note 1 and 2 in figure 13.2 is revised.
		109	13.2 Cold start / Warm start is added.
		120	Note in 15. Timer is added.
		121	Note in 15.1 Timer A is added.
		126	Table 15.1 is partly revised.
		127	Table 15.2 is partly revised.
		131	15.1.2.1 Counter Initialization by Two-Phase Pulse Signal Processing is partly revised.
		137	Note in 15.2 Timer B is added.
		140	Table 15.6 is partly revised.
		144	Note in 16. Three-Phase Motor Control Timer Function is added.
		146- 153	Figure 16.2 to 16.9 is revised.
		154	Note in 17. Serial I/O is added.
			Note in 17.1 UART1 is added.
		155- 156	Figure 17.1 to 17.3 are revised.
		160	Figure 17.7 is partly revised.
		168	17.1.1.1 Counter Measure for Communication Error Occurs is added.
		169	17.1.1.4 Continuous Receive Mode is revised.
		171	17.1.1.7 CTS/RTS Function is added.
		172	Note 3 in Table 17.5 is added.
		176	17.1.2.1 Bit Rates is added.
		177	17.1.2.2 Counter Measure for Communication Error Occurs is added.
		179	17.1.2.6 CTS/RTS Function is added.
		182	Note 2 in Table 17.11 is revised.

Rev.	Data		Description
Rev.	Date	Page	Summary
		192	Note 2 in Table 17.16 is revised.
		195	Note 2 in Table 17.17 is revised.
		197	Note 3 in Table 17.18 is added.
		202	Note in 17.2 SI/O3, SIO4 is added.
		207	Table 18.1 is revised.
		210	Figure 18.3 is partly revised.
		222	18.2.6 Output Impedance of Sensor under A/D Conversion is added.
		228	Note in 21. Programmable I/O Ports is added.
			Table 21.1 is added.
		229	21.3 Pull-up Control Register 0 to Pull-up Control Register 3 (PUR0 to PUR3 Registers) is partly revised.
		235	Note 3 in Figure 21.7 is partly revised.
		236	Note 3 in Figure 21.8 is partly revised.
		237	Note 2 in Figure 21.9 is partly revised.
		240	Note 5 in Table 21.2 is added.
			Note 7 in Table 21.3 is revised.
		242- 273	Almost all pages are revised (22. Flash Memory Version).
		274	Table 23.1 is revised.
		275	Table 23.2 is revised.
		276	Table 23.3 is revised.
			Note 2 in Table 23.4 is added.
		277	Table 23.5 to 23.6 is partly revised.
		278	Table 23.8 is revised.
			Table 23.9 is revised.
		279	Table 23.10 is revised.
		280	Table 23.11 is revised.
		281	Table 23.13 is partly revised.
		283	Table 23.24 is partly revised.
		284	Figure 23.2 is partly revised.
			Table 23.26 is partly revised.
		285	Table 23.27 is partly revised.
		286	Table 23.28 is partly revised.
		287	Figure 23.3 is partly revised.
		290- 291	Figure 23.6 to 23.7 is partly revised.
		292- 293	Figure 23.8 to 23.9 is partly revised.
		295	Figure 23.11 is Figure 23.6 to 23.7 is partly revised.
		296	Table 23.29 is revised.

Rev.	Dete	Description		
Rev.	Date	Page	Summary	
		297	Table 23.30 is revised.	
		298	Table 23.32 is partly revised.	
		300	Table 23.43 is partly revised.	
		301	Figure 23.12 is partly revised.	
			Table 23.45 is partly revised.	
		302	Table 23.46 is partly revised.	
		303	Table 23.47 is partly revised.	
		304	Figure 23.13 is partly revised.	
		307- 308	Figure 23.16 to 23.17 is partly revised.	
		309- 310	Figure 23.18 to 23.19 is partly revised.	
		313- 339	23.2 Electrical Characteristics (M16C/62PT) is added.	
		340	24.1 Reset is added.	
		341	24.2 External Bus is partly revised.	
		342	Figure 24.2 is added.	
		343	24.4 Power Control is partly revised.	
		346	24.9.2.1 Special Mode (I2C mode) is added.	
		347	24.9.3 SI/O3, SI/O4 is added.	
		348- 349	24.10 A/D Converter is partly revised.	
		352	24.13 Mask ROM Version is added.	
		356	24.15 Noise is added.	
		357	25. Differences Depending on Manufacturing Period is a	
2.40	Dec 15, 2005	-	voltage down detection reset -> brown-out detection Reset	
		2-4	Tables 1.1 to 1.3 Performance outline of M16C/62P group are partly revised.	
		7	Table 1.4 Product List (1) is partly revised. Note 1 is added.	
		8	Table 1.5 Product List (2) is partly revised. Note 1 and 2 are added.	
		9	Table 1.6 Product List (3) is partly revised. Note 1 and 2 are added.	
		10	Table 1.7 Product List (4) is partly revised. Note 1 and 2 are added.	
		11	Figure 1.3 Type No., Memory Size, and Package is partly revised	
		12	Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P is partly revised.	
		13	Table 1.9 Product Code of Flash Memory version for M16C/62P is partly revised.	

Rev.	Date		Description
Rev.	Dale	Page	Summary
		14	Figure 1.6 Pin Configuration (Top View) is partly revised.
		15-17	Tables 1.10 to 1.12 Pin Characteristics for 128-Pin Package are added.
		18-19	Figure 1.7 and 1.8 Pin Configuration (Top View) are partly revised.
		20-21	Tables 1.13 to 1.14 Pin Characteristics for 100-Pin Package are added.
		22	Figure 1.9 Pin Configuration (Top View) is partly revised.
		23-24	Tables 1.15 to 1.16 Pin Characteristics for 80-Pin Package are added.
		25-29	Tables 1.17 to 1.21 are partly revised.
		34	Note 4 of Table 4.1 SFR Information is partly revised.
		40-44	Change sections in Chapter 5.
		42	5.2 Brown-out Detection Reset (Hardware Reset 2) is partly revised.
		45	6. Voltage Detection Circuit is partly revised.
			Figure 6.1 Voltage Detection Circuit Block is partly revised.
		48	Figure 6.4 Typical Operation of Brown-out Detection Reset (Hardware Reset 2) is partly revised.
		49	Table 6.2 Sampling Periods is partly revised.
		52-53	6.4 Cold Start-up / Warm Start-up Determine Function is added.
		57	Note 7 of Figure 7.2 PM1 Register is partly revised.
		64	8.2.6 RDY Signal is partly revised.
		69	Table 8.8 Bit and Bus Cycle Related to Software
		80	Figure 9.8 Relationship Between Address on 4-Mbyte ROM and Those on Microcomputer (2) is partly revised.
		89	Figure 10.7 Examples of Main Clock Connection Circuit is partly revised.
		90	Figure 10.8 Examples of Sub Clock Connection Circuit is partly revised.
		91	10.1.4 PLL Clock is partly revised.
		94	10.4.1.6 On-chip Oscillator Mode is partly revised.
		95	10.4.1.7 On-chip Oscillator Low Power Dissipation Mode is partly revised
		96	Table 10.4 Pin Status During Wait Mode is partly revised.
		97	10.4.2.4 Exiting Wait Mode is partly revised.
		98	10.4.3 Stop Mode is partly revised.
			Table 10.6 Interrupts to Stop Mode and Use Conditions is added.
		99	10.4.3.3 Exiting Stop Mode is partly revised.
		100	Figure 10.11 State Transition in Normal Operating Mode is partly revised
		104	10.6.3 How to Use Oscillation Stop and Re-oscillation Detect Function is partly revised.
		107	12.2.2 Overflow Interrupt is partly revised.
		118	12.5.8 Returning from an Interrupt Routine is partly revised.
			12.5.9 Interrupt Priority is partly revised.
		119	12.5.10 Interrupt Priority Level Select Circuit is partly revised.
		120	Figure 12.11 IFSR and IFSR2A Registers (Interrupt Factor Select
			Register) is partly revised.

Devi	Data		Description
Rev.	Date	Page	Summary
		125	13.1 Cold Start / Warm Start moved to 5. Reset.
		127	Table 14.1 DMAC Specifications is partly revised.
		132	14.1.3 Effect of Software Wait is partly revised.
		165	Table 16.1 Three-phase Motor Control Timer Functions Specifications is partly revised.
		167	Notes 5 and 7 of Figure 16.2 INVC0 Register are partly revised.
		177- 179	Figures 17.1 to 17.3 UART Block Diagram are partly revised.
		181	Note 3 of Figure 17.5 UiRB Register is added.
		186	Figure 17.10 UCON and UiSMR Registers Notes 3 is revised.
		188	Table 17.1 Clock Synchronous Serial I/O Mode Specifications is partly revised. Note 2 is partly revised.
		192	Figure 17.13 Transmit and Receive Operation is revised.
		193	17.1.1.1 Counter Measure for Communication Error Occurs is partly revised.
		197	Table 17.5 UART Mode Specifications is partly revised. Note 1 is partly revised
		200	Figure 17.19 Transmit Operation is revised.
		201	17.1.2.1 Bit Rate is partly revised.
			Table 17.9 Example of Bit Rates and Settings is partly revised.
		202	17.1.2.2 Counter Measure for Communication Error Occurs is partly revised.
		205	Table 17.10 I ² C Mode Specifications is partly revised.
		207	Note 4 of Table 17.11 Registers to Be Used and Settings in I ² C Mode (1) is added.
		215	Table 17.15 Special Mode Specifications is partly revised.
		222	Table 17.18 SIM Mode Specifications is partly revised.
		224	Figure 17.34 Transmit and Receive Timing in SIM Mode is partly revised.
		226	17.1.6.2 Format is partly revised.
		230	Table 17.20 SI/O3 and SI/O4 Specifications is partly revised.
		231	Figure 17.41 SI/Oi Operation Timing is partly revised.
			Figure 17.42 Polarity of Transfer Clock is partly revised.
		232	17.2.3 Functions for Settings an SOUTi Internal Value is partly revised.
		249	18.2.6 Output Impedance of Sensor under A/D Conversion is partly revised.
		250	Figure 18.11 Analog Input Pin and External Sensor Equivalent Circuit is partly revised.
		251	Table 19.1 D/A Converter Performance is partly revised.

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		252	Figure 19.2 DA0 and DA1 Register is partly revised.
			Note 2 of Figure 19.3 D/A Converter is added.
		254	Figure 20.3 CRC Calculation is partly revised.
		261	Note 2 of Figure 21.6 I/O Pin is deleted.
		270	Table 22.1 Flash Memory Version Specifications is partly revised.
		274	Figure 22.2 ROMCP Register is partly revised.
		275	Note 1 of Table 22.3 EM0 Mode and EW1 Mode is partly revised.
		276	22.3.2 EW1 Mode is partly revised.
		279	22.3.3.4 FMSTP Bit is partly revised.
		283	Figure 22.9 Processing Before and After Low Power Dissipation mode is partly revised.
		285	22.3.4.12 Low-Power Consumption Mode and On-chip Oscillator Low- power Consumption Mode is partly revised.
		288	22.3.5.5 Block Erase Command is partly revised.
			Figure 22.11 Block Erase Command is partly revised.
		292	Table 22.5 Status Register is partly revised.
		294	Figure 22.14 Full Status Check and Handling Procedure for Each Error is partly revised.
		297	Table 22.7 Pin Functions (Flash Memory Standard Serial I/O Mode) is partly revised. Note 2 is partly revised. Note 3 is added.
		297- 300	Figures 22.15 to 22.18 are partly revised.
		301	Figure 22.19 Circuit Application in Standard I/O Mode 1 is partly revised.
		302	Figure 22.20 Circuit Application in Standard I/O Mode 2 is partly revised.
		307	Table 23.4 A/D Conversion Characteristics is partly revised.
		309	Table 23.6 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised.
			Table 23.7 Flash Memory Version Electrical Characteristics for 10,000cycle products is partly revised.
			Table 23.8 Flash Memory Version Program / Erase Voltage and ReadOperation Voltage Characteristics is partly revised.
		310	Table 23.9 Low Voltage Detection Circuit Electrical Characteristics is partly revised.
		311	Figure 23.1 Power Supply Circuit Timing Diagram is partly revised.
		313	Table 23.12 Electrical Characteristics (2) is partly revised.
		314	Note 1 of Table 23.13 External Clock Input (XIN input) is added.
		331	Notes 1 to 4 of Table 23.32 External Clock Input (XIN input) are added.
		349	Table 23.53 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised. Standard (Min.) is partly revised.

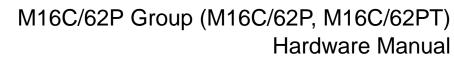
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		349	Table 23.54 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised. Standard (Min.) is partly revised. Note 5 is revised.
			Table 23.55 Flash Memory Version Program / Erase Voltage and ReadOperation Voltage Characteristics is partly revised.
		352 359	Table 23.58 Electrical Characteristics is partly revised. 24.1 SFR and 24.1.1 Register Settings, Table 24.1 Registers with Write- only Bits are added.
		360 363	Figure 24.1 Timing of SVcc is revised. 24.5 Power Control is revised.
		375	Figure 24.4 Use of Capacitors to Reduce Noise is partly revised.
		375	24.11 A/D Converter is partly revised.
		377	24.12 Programable I/O Ports is partly revised.
		379	24.15.2 Stop mode is partly revised.
		380	24.15.8 Operation speed is partly revised.
		381	24.15.14 Regarding Programming/Erasing Endurance and Execution Time is partly revised. (Title change.)
		383	Table 25.1 Technical Update Applicable of M16C/62P Flash and ROM External Versions is partly revised.
2.41	Jan 10, 2006	-	voltage down detection -> low voltage detection
		99	Figure 10.10 State Transition to Stop Mode and Wait Mode is partly revised.
		100	Figure 10.11 State Transition in Normal Operating Mode is partly revised.
		132	14.1.3 Effect of Software Wait is partly revised.
		186	Figure 17.10 UCON and UiSMR Registers Notes 4 is added. Bit3(LSYN) is added.
		252	Figure 19.3 D/A Converter Equivalent Circuit is partly revised.

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