National Semiconductor

LP3990
150mA Linear Voltage Regulator for Digital Applications

General Description

The LP3990 regulator is designed to meet the requirements of portable, battery-powered systems providing an accurate output voltage, low noise, and low quiescent current. The LP3990 will provide a 0.8V output from the low input voltage of 2V at up to 150mA load current. When switched into shutdown mode via a logic signal at the enable pin, the power consumption is reduced to virtually zero.

The LP3990 is designed to be stable with space saving ceramic capacitors as small as 1.0µF.

Performance is specified for a -40˚C to 125˚C junction temperature range.

For output voltages other than 0.8V, 1.2, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, or 3.3V please contact your local NSC sales office.

Features

- 1% Voltage Accuracy at Room Temperature
- Stable with Ceramic Capacitor
- Logic Controlled Enable
- No Noise Bypass Capacitor Required
- Thermal-Overload and Short-Circuit Protection

Key Specifications

Input Voltage Range	2.0 to 6.0V
Output Voltage Range	0.8 to 3.3V
Output Current	150mA
Output Stable - Capacitors	1.0uF
Virtually Zero I_Q (Disabled)	<10nA
Very Low I_Q (Enabled)	43uA
Low Output Noise	150uV$_{RMS}$
PSRR	55dB at 1kHz
Fast Start Up	105us

Package

All available in Lead Free option.

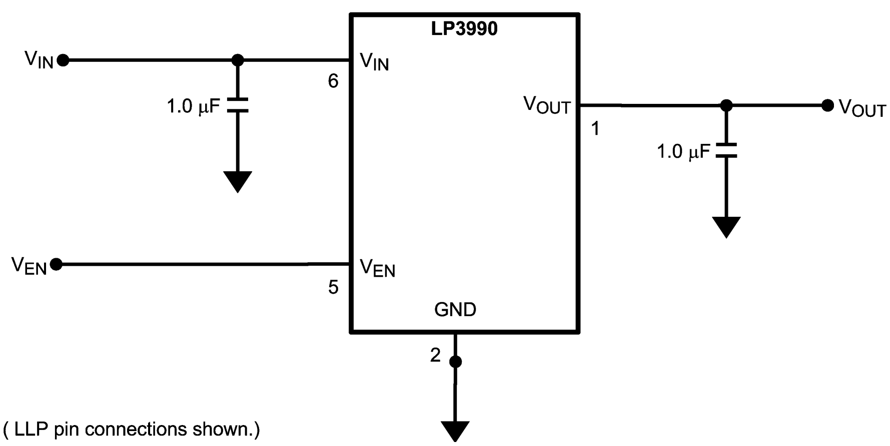
4 Pin micro SMD	1 mm x 1.3 mm
6 pin LLP (SOT23 footprint)	
SOT23 - 5	

For other package options contact your NSC sales office.

Applications

- Cellular Handsets
- Hand-Held Information Appliances

Typical Application Circuit



(LLP pin connections shown.)

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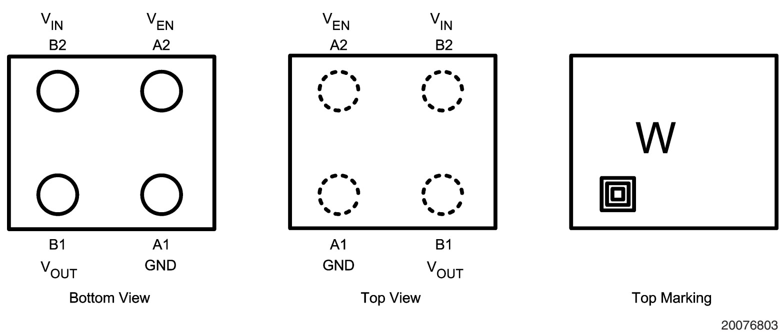
Pin Descriptions

Packages

Pin No			Symbol	Name and Function
LLP	micro SMD	SOT23-5		
5	A2	3	V_{EN}	Enable Input; Enables the Regulator when ≥ 0.95V. Disables the Regulator when ≤ 0.4V. Enable Input has 1MΩ pulldown resistor to GND.
2	A1	2	GND	Common Ground. Connect to Pad.
1	B1	5	V_{OUT}	Voltage output. A 1.0µF Low ESR Capacitor should be connected to this Pin. Connect this output to the load circuit.
6	B2	1	V_{IN}	Voltage Supply Input. A 1.0µF capacitor should be connected at this input.
3		4	N/C	No Connection. Do not connect to any other pin.
4			N/C	No Connection. Do not connect to any other pin.
Pad			GND	Common Ground. Connect to Pin 2.

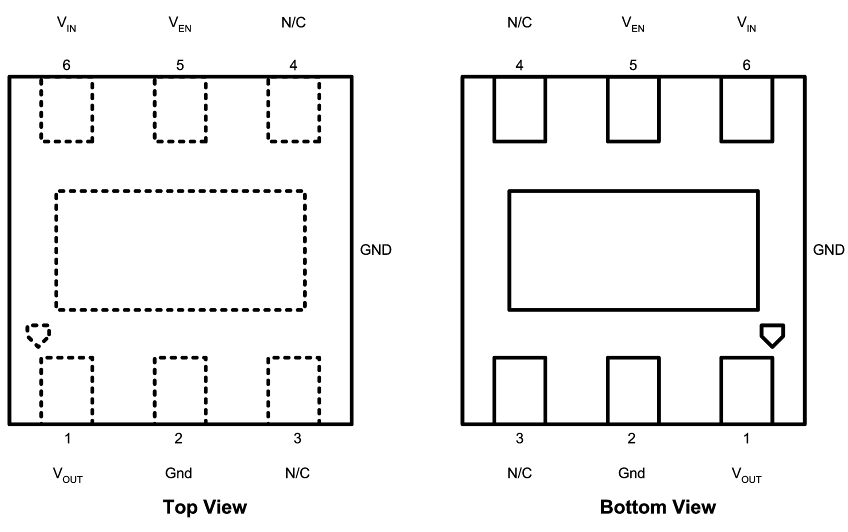
Connection Diagrams

Micro SMD, 4 Bump Package



See NS package number TLA04

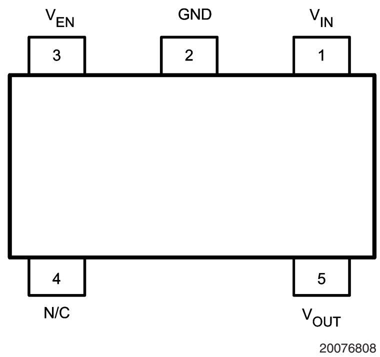
LLP-6 Package



See NS package number SDE06A

Connection Diagrams (Continued)

SOT23 - 5 Package (MF)



See NS package number MF05A

Ordering Information

For micro SMD Package

Output Voltage (V)	Grade	LP3990 Supplied as 250 Units, Tape and Reel	LP3990 Supplied as 3000 Units, Tape and Reel	Package Marking
0.8	STD	LP3990TL-0.8	LP3990TLX-0.8	
1.2	STD	LP3990TL-1.2	LP3990TLX-1.2	
1.35	STD	LP3990TL-1.35	LP3990TLX-1.35	
1.5	STD	LP3990TL-1.5	LP3990TLX-1.5	
1.8	STD	LP3990TL-1.8	LP3990TLX-1.8	
2.5	STD	LP3990TL-2.5	LP3990TLX-2.5	
2.8	STD	LP3990TL-2.8	LP3990TLX-2.8	

For LLP-6 Package

Output Voltage (V)	Grade	LP3990 Supplied as 1000 Units, Tape and Reel	LP3990 Supplied as 3000 Units, Tape and Reel	Package Marking
0.8	STD	LP3990SD-0.8	LP3990SDX-0.8	L085B
1.2	STD	LP3990SD-1.2	LP3990SDX-1.2	L086B
1.35	STD	LP3990SD-1.35	LP3990SDX-1.35	L150B
1.5	STD	LP3990SD-1.5	LP3990SDX-1.5	L087B
1.8	STD	LP3990SD-1.8	LP3990SDX-1.8	L088B
2.5	STD	LP3990SD-2.5	LP3990SDX-2.5	L090B
2.8	STD	LP3990SD-2.8	LP3990SDX-2.8	L091B

For SOT23 - 5 Package

Output Voltage (V)	Grade	LP3990 Supplied as 1000 Units, Tape and Reel	LP3990 Supplied as 3000 Units, Tape and Reel	Package Marking
1.2	STD	LP3990MF-1.2	LP3990MFX-1.2	SCDB
1.5	STD	LP3990MF-1.5	LP3990MFX-1.5	SCEB
1.8	STD	LP3990MF-1.8	LP3990MFX-1.8	SCFB
2.5	STD	LP3990MF-2.5	LP3990MFX-2.5	SCJB
2.8	STD	LP3990MF-2.8	LP3990MFX-2.8	SCKB
3.3	STD	LP3990MF-3.3	LP3990MFX-3.3	SCLB

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	-0.3 to 6.5V
Output Voltage	-0.3 to (V_{IN} + 0.3V) with 6.5V (max)
Enable Input Voltage	-0.3 to (V_{IN} + 0.3V) with 6.5V (max)
Junction Temperature	150˚C
Lead/Pad Temp. (Note 3)	
LLP/SOT23	235˚C
micro SMD	260˚C
Storage Temperature	-65 to 150˚C
Continuous Power Dissipation	
Internally Limited(Note 4)	

ESD (Note 5)	
Human Body Model	2KV
Machine Model	200V

Operating Ratings(Note 1)

Input Voltage	2V to 6V
Enable Input Voltage	0 to (V_{IN} + 0.3V) with 6.0V (max)
Junction Temperature	-40˚C to 125˚C
Ambient Temperature T_ARange (Note 6)	-40˚C to 85˚C

Thermal Properties(Note 1)

Junction To Ambient Thermal Resistance(Note 8)	
θ_{JA}(LLP-6)	88˚C/W
θ_{JA}(microSMD)	220˚C/W
θ_{JA}SOT23-5	220˚C/W

Electrical Characteristics

Unless otherwise noted, V_{EN} =950mV, V_{IN} = V_{OUT} + 1.0V, or 2.0V, whichever is higher. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} =0.47 µF. Typical values and limits appearing in normal type apply for T_J = 27˚C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, –40 to +125˚C. (Note 13)

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
V_{IN}	Input Voltage	(Note 14)			2	6	V
ΔV_{OUT}	Output Voltage Tolerance	I_{LOAD} = 1 mA	Micro SMD		-1	+1	%
			LLP		-1.5	+1.5	
			SOT-23		-1.5	+1.5	
		Over full line and load regulation.	Micro SMD		**-2.5**	**+2.5**	
			LLP		**-3**	**+3**	
			SOT-23		**-4**	**+4**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 6.0V,		0.02	**-0.1**	**0.1**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 150mA	V_{OUT} = 0.8 to 1.95V MicroSMD	0.002	**-0.005**	**0.005**	%/mA
			V_{OUT} = 0.8 to 1.95V LLP, SOT-23	0.003	**-0.008**	**0.008**	
			V_{OUT} = 2.0 to 3.3V MicroSMD	0.0005	**-0.002**	**0.002**	
			V_{OUT} = 2.0 to 3.3V LLP, SOT-23	0.002	**-0.005**	**0.005**	
V_{DO}	Dropout Voltage	I_{OUT} = 150mA (Note 7)		120			mV
I_{LOAD}	Load Current	(Notes 9, 10)			0		µA
I_Q	Quiescent Current	V_{EN} = 950mV, I_{OUT} = 0mA		43		**80**	µA
		V_{EN} = 950mV, I_{OUT} = 150mA		65		**120**	
		V_{EN} = 0.4V		0.002		0.2	
I_{SC}	Short Circuit Current Limit	(Note 11)		550		**1000**	mA
I_{OUT}	Maximum Output Current				**150**		mA
PSRR	Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 1mA to 150mA		55			dB
		f = 10kHz, I_{OUT} = 150mA		35			

Electrical Characteristics (Continued)

Unless otherwise noted, V_{EN} =950mV, V_{IN} = V_{OUT} + 1.0V, or 2.0V, whichever is higher. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} =0.47 µF. Typical values and limits appearing in normal type apply for T_J = 27˚C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125˚C. (Note 13)

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
e_n	Output noise Voltage (Note 10)	BW = 10Hz to 100kHz,	V_{OUT} = 0.8	60			μV_{RMS}
			V_{OUT} = 1.5	125			
			V_{OUT} = 3.3	180			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		155			˚C
		Hysteresis		15			
Enable Control Characteristics							
I_{EN} (Note 12)	Maximum Input Current at V_{EN} Input	V_{EN} = 0.0V		0.001		0.1	µA
		V_{EN} = 6V		6	**2.5**	**10**	
V_{IL}	Low Input Threshold	V_{IN} = 2V to 6V				**0.4**	V
V_{IH}	High Input Threshold	V_{IN} = 2V to 6V			**0.95**		V
Timing Characteristics							
T_{ON}	Turn On Time (Note 10)	To 95% Level $V_{IN(MIN)}$ to 6.0V	V_{OUT} = 0.8	80		**150**	µs
			V_{OUT} = 1.5	105		**200**	
			V_{OUT} = 3.3	175		**250**	
Transient Response	Line Transient Response $\|\delta V_{OUT}\|$	T_{rise} = T_{fall} = 30µs (Note 10) δV_{IN} = 600mV		8		**16**	mV (pk - pk)
	Load Transient Response $\|\delta V_{OUT}\|$	T_{rise} = T_{fall} = 1µs (Note 10)I_{OUT} = 1mA to 150mA C_{OUT} = 1µF		55		**100**	mV

Note 1: Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All Voltages are with respect to the potential at the GND pin.

Note 3: For further information on these packages please refer to the following application notes;AN-1112 Micro SMD Package Wafer Level Chip Scale Package,AN-1187 Leadless Leadframe Package.

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage.

Note 5: The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 6: The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125˚C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Note 7: Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter only for output voltages above 2.0V.

Note 8: Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Note 9: The device maintains the regulated output voltage without the load.

Note 10: This electrical specification is guaranteed by design.

Note 11: Short circuit current is measured with V_{OUT} pulled to 0V and V_{IN} worst case = 6.0V.

Note 12: Enable Pin has 1MΩ typical, resistor connected to GND.

Note 13: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at T_J = 25˚C or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 14: $V_{IN(MIN)} = V_{OUT(NOM)}$ + 0.5V, or 2.0V, whichever is higher.

Electrical Characteristics (Continued)

Output Capacitor, Recommended Specifications

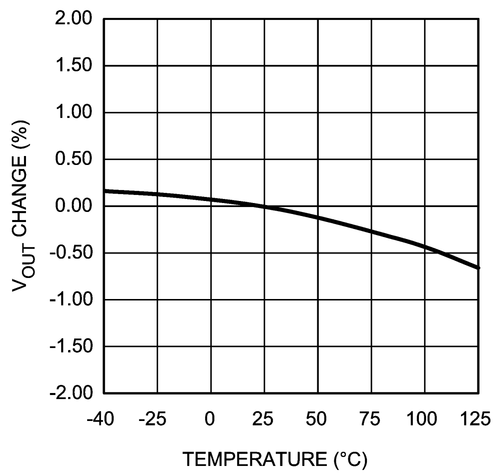
Symbol	Parameter	Conditions	Nom	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance (Note 15)	1.0	**0.7**		µF
		ESR		5	500	mΩ

Note 15: The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. (See capacitor section in Applications Hints)

Typical Performance Characteristics.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT} = 0.47 µF Ceramic, $V_{IN} = V_{OUT(NOM)}$ + 1.0V, T_A = 25˚C, $V_{OUT(NOM)}$ = 1.5V , Shutdown pin is tied to V_{IN}.

Output Voltage Change vs Temperature



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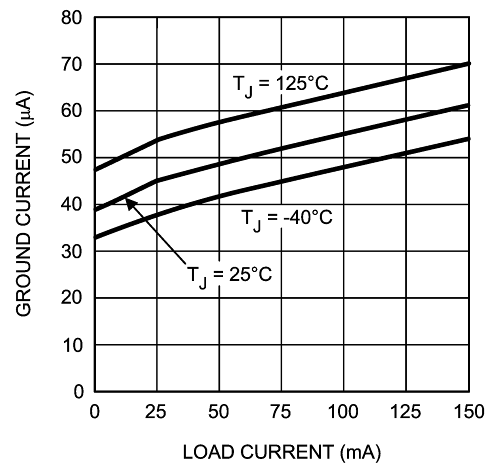
Ground Current vs Load Current



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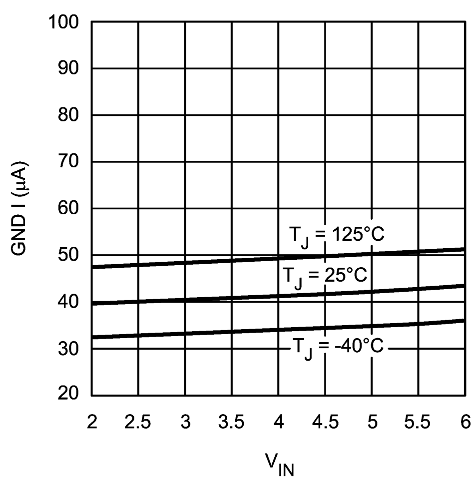
Ground Current vs V_{IN}. I_{LOAD} = 0mA



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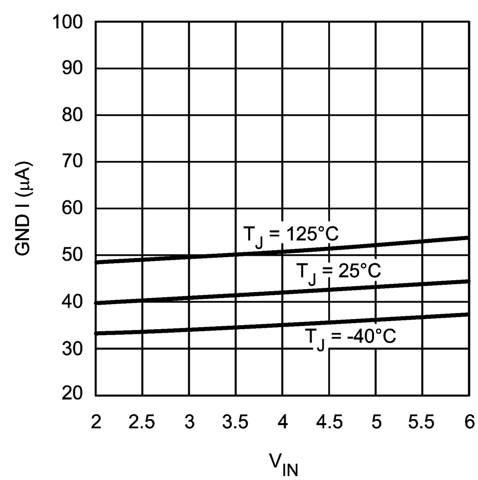
Ground Current vs V_{IN}. I_{LOAD} = 1mA



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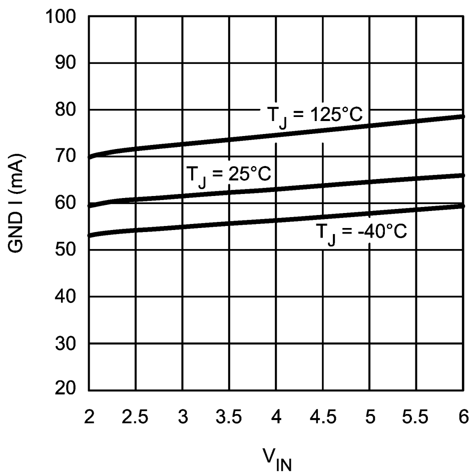
Typical Performance Characteristics.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT} = 0.47 µF Ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1.0V, T_A = 25˚C, $V_{OUT(NOM)}$ = 1.5V , Shutdown pin is tied to V_{IN}. (Continued)

Ground Current vs V_{IN}. I_{LOAD} = 150mA



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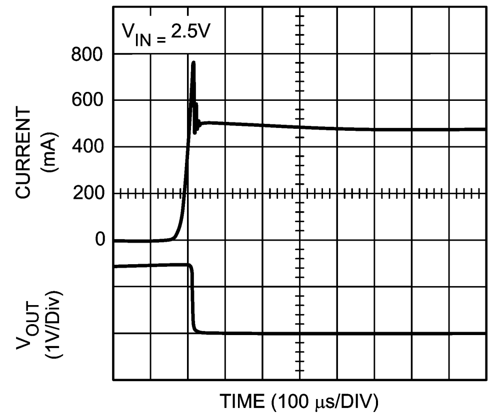
Short Circuit Current



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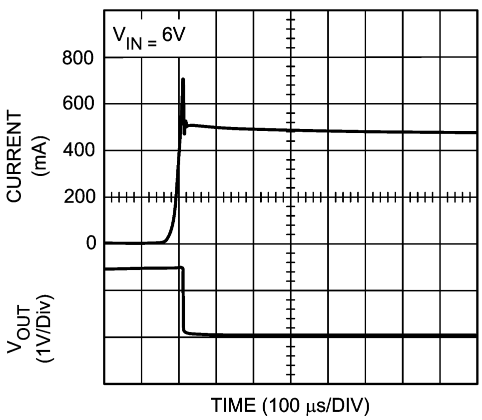
Short Circuit Current



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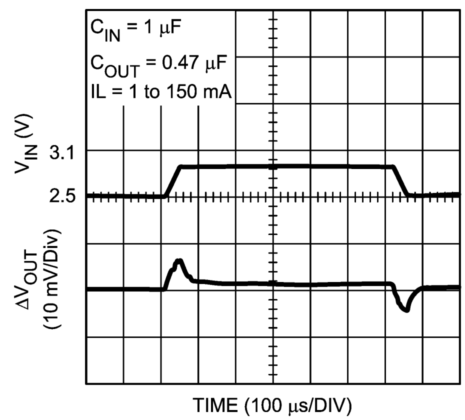
Line transient



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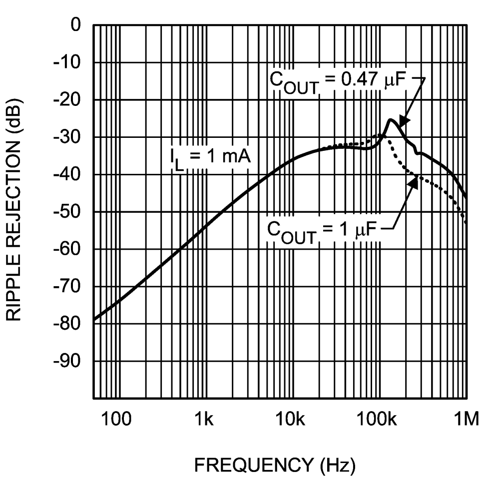
Power Supply Rejection Ratio



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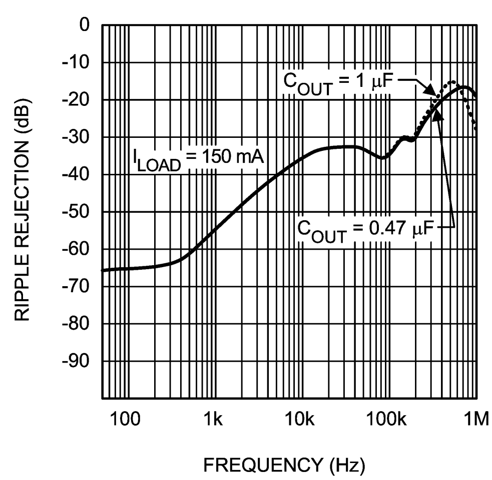
Power Supply Rejection Ratio



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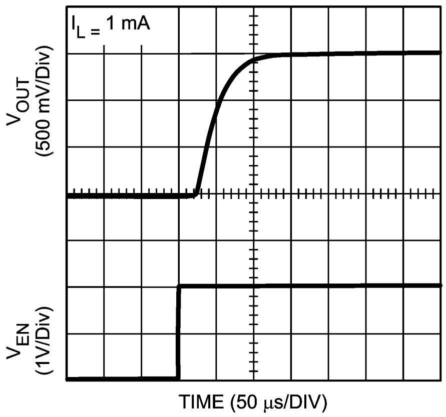
Typical Performance Characteristics.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT} = 0.47 µF Ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1.0V, T_A = 25˚C, $V_{OUT(NOM)}$ = 1.5V , Shutdown pin is tied to V_{IN}. (Continued)

Enable Start-up Time



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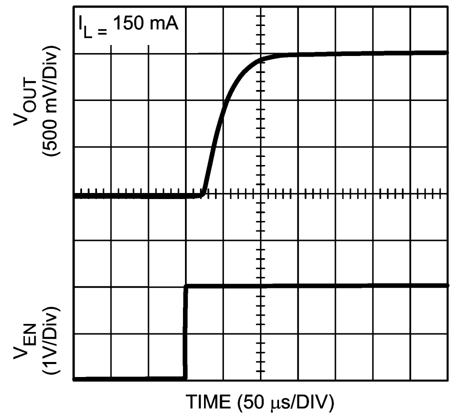
Enable Start-up Time



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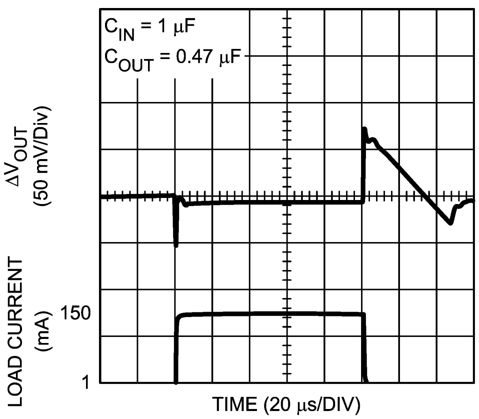
Load Transient



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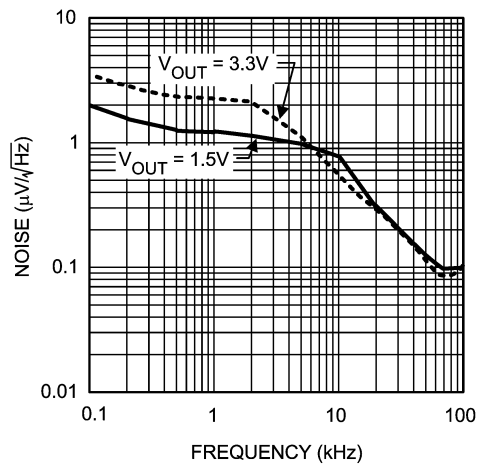
Noise Density



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Application Hints

EXTERNAL CAPACITORS

In common with most regulators, the LP3990 requires external capacitors for regulator stability. The LP3990 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP3990 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB design practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are used to connect the battery or other power sorce to the LP3990, then it is recommended that the input capacitor is increased. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3990 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5mΩ to 500mΩ, is suitable in the LP3990 application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5mΩ to 500mΩ for stability.

NO-LOAD STABILITY

The LP3990 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3990 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP3990.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, *Figure 1* shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

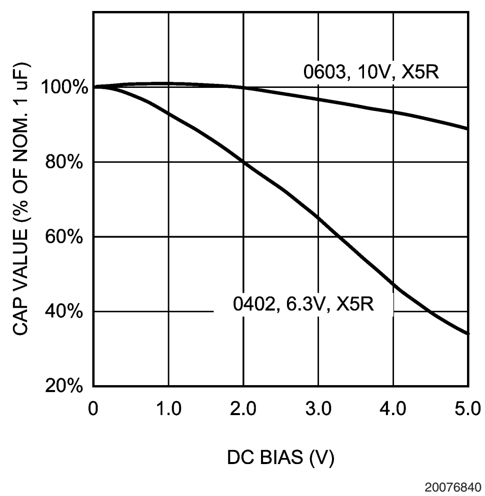


FIGURE 1. Graph Showing a Typical Variation in Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55˚C to +125˚C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55˚C to +85˚C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25˚C to 85˚C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25˚C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47µF to 4.7µF range.

Application Hints (Continued)

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to -40˚C, so some guard band must be allowed.

ENABLE CONTROL

The LP3990 features an active high Enable pin, V_{EN}, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 2nA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Micro SMD MOUNTING

The micro SMD package requires specific mounting techniques, which are detailed in National Semiconductor Application Note AN-1112.

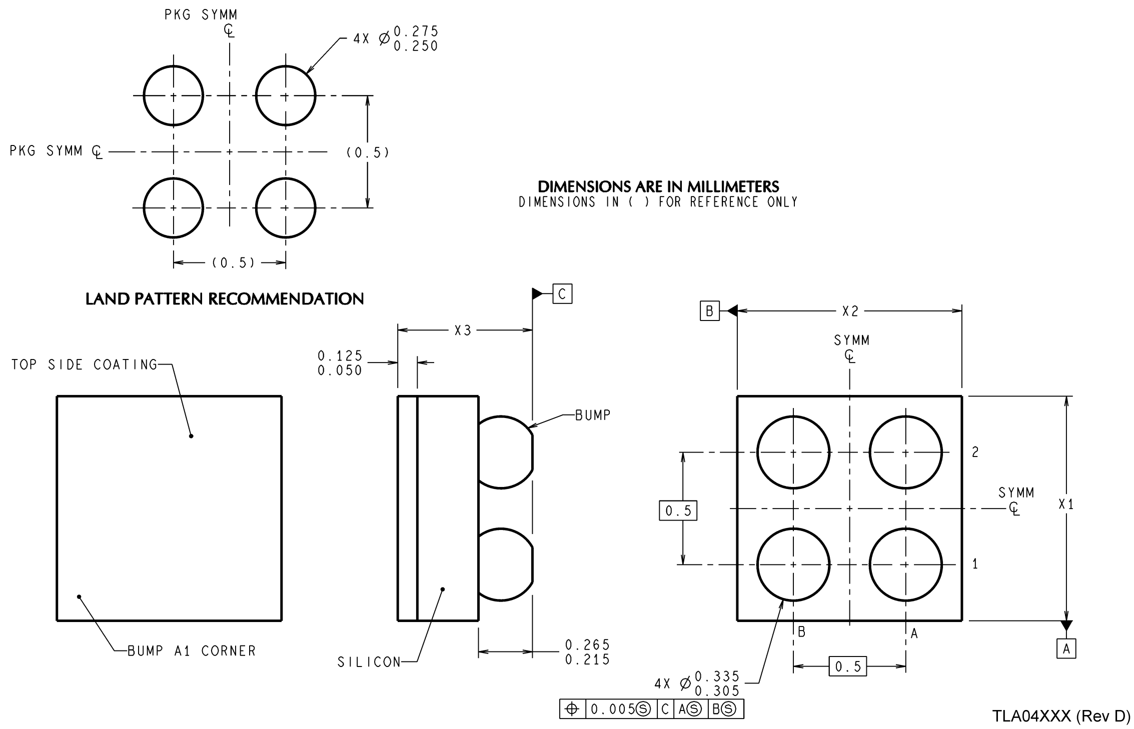
For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

Micro SMD LIGHT SENSITIVITY

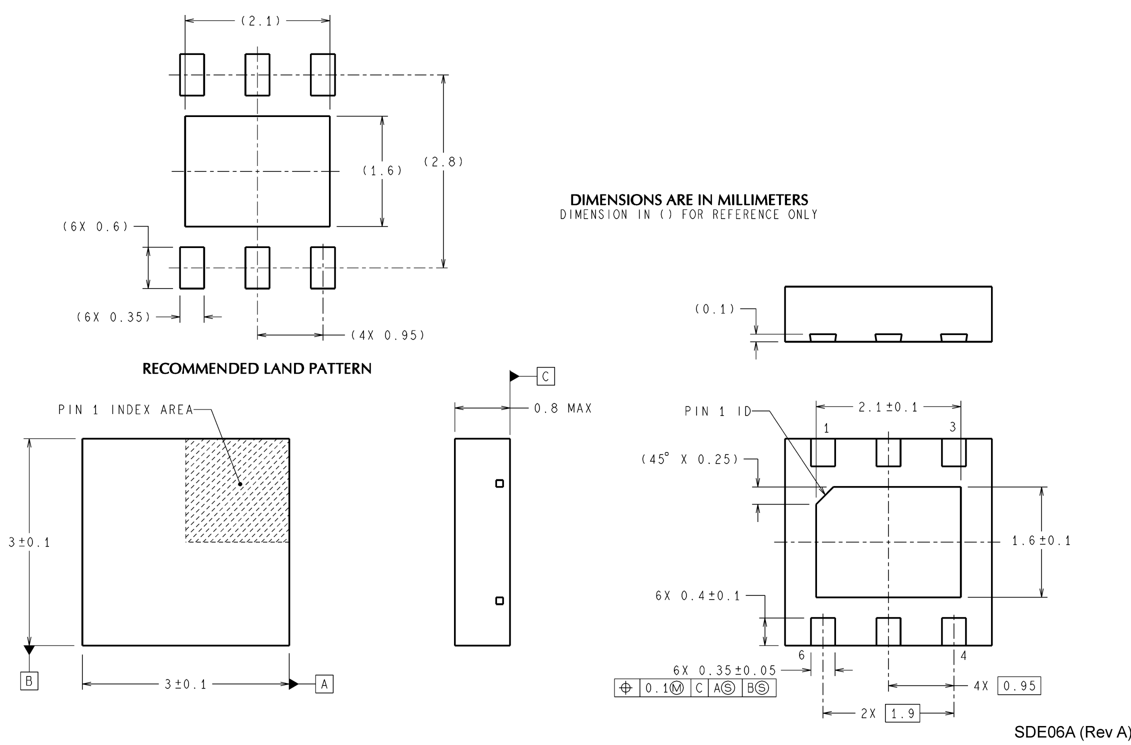
Exposing the micro SMD device to direct light may affect the operation of the device. Light sources, such as halogen lamps, can affect electrical performance, if placed in close proximity to the device.

Light with wavelengths in the infra-red portion of the spectrum is the most detrimental, and so, fluorescent lighting used inside most buildings, has little or no effect on performance.

Physical Dimensions inches (millimeters) unless otherwise noted

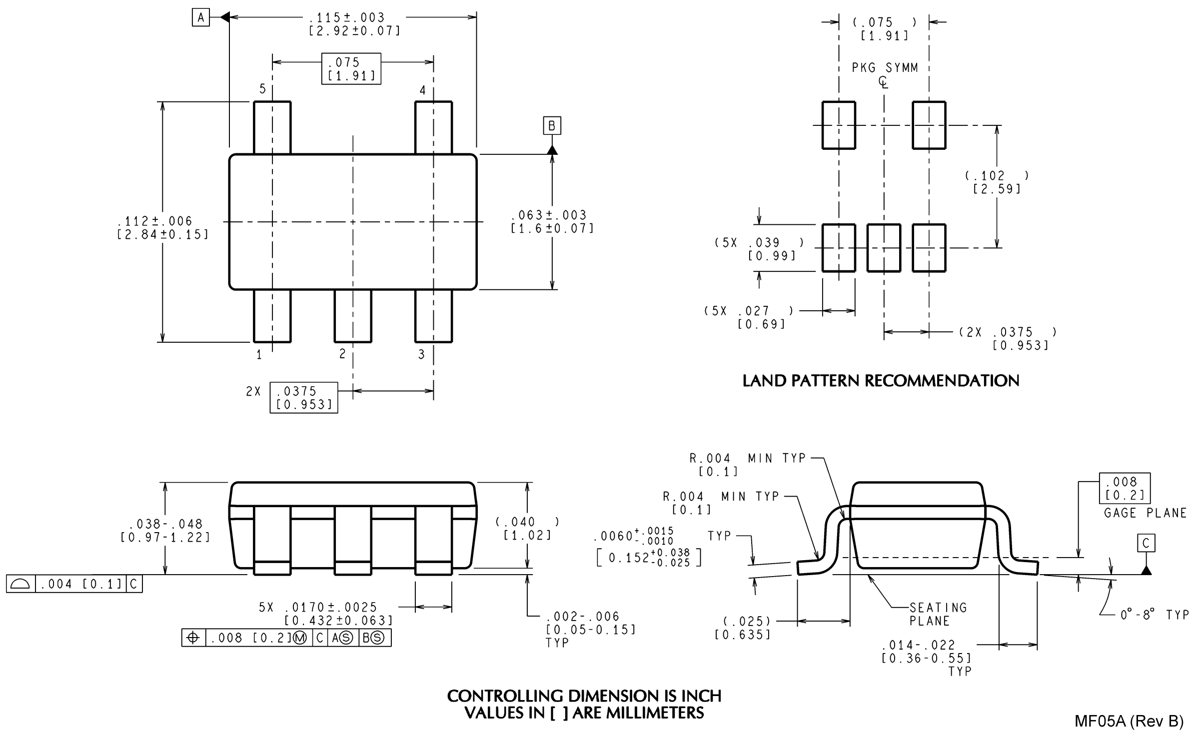


micro SMD, 4 Bump, Package (TLA04)
NS Package Number TLA04AMA
The dimensions for X1, X2 and X3 are given as:
X1 = 1.014 +/– 0.03mm
X2 = 1.294 +/– 0.03mm
X3 = 0.600 +/– 0.075mm



LLP, 6 Lead, Package (SOT23 Land)
NS Package Number SDE06A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



SOT23 - 5 Package
NS Package Number MF05A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no ''Banned Substances'' as defined in CSP-9-111S2.

Leadfree products are RoHS compliant.

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