National Semiconductor

August 2003

LM4849 Boomer® Audio Power Amplifier Series
Stereo 2W Audio Power Amplifiers with DC Volume Control and Input Mux

General Description

The LM4849 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD+N, or 2.2W into 3Ω (Note 2) with less than 1.0% THD+N.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4849 incorporates a DC volume control, stereo bridged audio power amplifiers, and an input mux making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4849 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note 1: When properly mounted to the circuit board, the LM4849MH will deliver 2W into 4Ω. See the Application Information section for LM4849MH usage information.

Note 2: An LM4849MH that has been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Key Specifications

- P_O at 1% THD+N
  - into 3Ω (Note2) 2.2W (typ)
  - into 4Ω (Note1) 2.0W (typ)
  - into 8Ω 1.1W (typ)
- Single-ended mode - THD+N at 85mW into 32Ω 1.0% (typ)
- Shutdown Current 0.2µA (typ)

Features

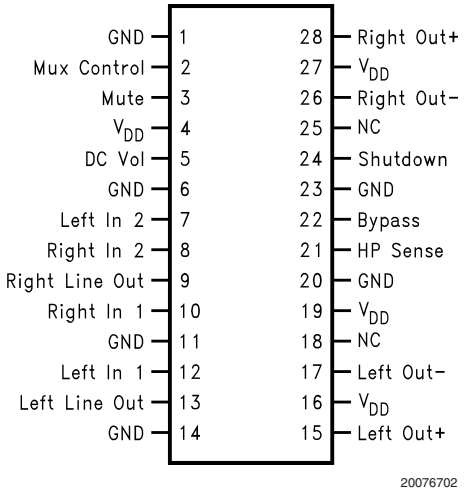
- DC Volume Control Interface
- Input mux
- Stereo switchable bridged/single-ended power amplifiers
- “Click and pop” suppression circuitry
- Thermal shutdown protection circuitry

Applications

- Portable and Desktop Computers
- Multimedia, LCD Monitors/TV
- Portable Radios, PDAs, and Portable TVs

Connection Diagram

TSSOP Package



Top View
Order Number LM4849MH
See NS Package Number MXA28A for Exposed-DAP TSSOP

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Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65˚C to +150˚C
Input Voltage	–0.3V to V_{DD} +0.3V
Power Dissipation	Internally limited
ESD Susceptibility (Note 12)	2500V
ESD Susceptibility (Note 13)	250V
Junction Temperature	150˚C
Soldering Information	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 “Surface Mounting and their Effects on Product Reliability” for other methods of soldering surface mount devices.

θ_{JA} (typ)—MXA28A (exposed DAP) (Note 3)	41˚C/W
θ_{JA} (typ)—MXA28A (exposed DAP) (Note 4)	54˚C/W
θ_{JA} (typ)—MXA28A (exposed DAP) (Note 5)	59˚C/W
θ_{JA} (typ)—MXA28A (exposed DAP) (Note 6)	93˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	–40˚C ≤TA ≤ 85˚C
Supply Voltage	2.7V≤ V_{DD} ≤ 5.5V

Electrical Characteristics for Entire IC

(Notes 7, 10) The following specifications apply for V_{DD} = 5V and T_A = 25˚C unless otherwise noted.

Symbol	Parameter	Conditions	LM4849		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
V_{DD}	Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	15	30	mA (max)
I_{SD}	Shutdown Current	$V_{shutdown}$ = V_{DD}	0.7	2.0	µA (max)
V_{IH}	VIN High on all Logic Inputs			0.8 x VDD	V (min)
V_{IL}	VIN Low on all Logic Inputs			0.2 x VDD	V (max)

Electrical Characteristics for Volume Attenuators

(Notes 7, 10) The following specifications apply for V_{DD} = 5V and T_A = 25˚C unless otherwise noted.

Symbol	Parameter	Conditions	LM4849		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
C_{RANGE}	Attenuator Range	Gain with V_{DCVol} = 5.0V, No Load		±0.75	dB (max)
C_{RANGE}	Attenuator Range	Attenuation with V_{DCVol} = 0V (BM & SE)		-75	dB (min)
A_M	Mute Attenuation	V_{mute} = 5V, Bridged Mode (BM)		-78	dB (min)
		V_{mute} = 5V, Single-Ended Mode (SE)		-78	dB (min)

Electrical Characteristics for Single-Ended Mode Operation

(Notes 7, 10) The following specifications apply for V_{DD} = 5V and T_A = 25˚C unless otherwise noted.

Symbol	Parameter	Conditions	LM4849		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
P_O	Output Power	THD+N = 1.0%; f = 1kHz; R_L = 32Ω	85		mW
		THD+N = 10%; f = 1 kHz; R_L = 32Ω	95		mW
THD+N	Total Harmonic Distortion+Noise	V_{OUT} = 1V_{RMS}, f=1kHz, R_L = 10kΩ, A_{VD} = 1	0.065		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f =120 Hz, V_{RIPPLE} = 200 mVrms	58		dB
SNR	Signal to Noise Ratio	P_{OUT} =75 mW, R_L = 32Ω, A-Wtd Filter	102		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	65		dB

Electrical Characteristics for Bridged Mode Operation

(Notes 7, 10) The following specifications apply for V_{DD} = 5V and T_A = 25˚C unless otherwise noted.

Symbol	Parameter	Conditions	LM4849		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V, No Load		±50	mV (max)
P_O	Output Power	THD + N = 1.0%; f=1kHz; R_L = 3Ω (Note 8)	2.2		W
		THD + N = 1.0%; f=1kHz; R_L = 4Ω (Note 9)	2		W
		THD = 1.5% (max);f = 1 kHz; R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%;f = 1 kHz; R_L = 8Ω	1.5		W
THD+N	Total Harmonic Distortion+Noise	P_O = 1W, f = 1kHz, R_L = 8Ω, A_{VD} = 2	0.2		%
		P_O = 340 mW, R_L = 32Ω	1.0		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f = 120 Hz, V_{RIPPLE} = 200 mVrms; R_L = 8Ω	74		dB
SNR	Signal to Noise Ratio	V_{DD} = 5V, P_{OUT} = 1.1W, R_L = 8Ω, A-Wtd Filter	93		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	70		dB

Note 3: The θ_{JA} given is for an MXA28A package whose exposed-DAP is soldered to an exposed 2in^2 piece of 1 ounce printed circuit board copper.

Note 4: The θ_{JA} given is for an MXA28A package whose exposed-DAP is soldered to a 2in^2 piece of 1 ounce printed circuit board copper on a bottom side layer through 21 8mil vias.

Note 5: The θ_{JA} given is for an MXA28A package whose exposed-DAP is soldered to an exposed 1in^2 piece of 1 ounce printed circuit board copper.

Note 6: The θ_{JA} given is for an MXA28A package whose exposed-DAP is not soldered to any copper.

Note 7: All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 2.

Note 8: When driving 3Ω loads from a 5V supply the LM4849MH exposed DAP must be soldered to the circuit board and forced-air cooled.

Note 9: When driving 4Ω loads from a 5V supply the LM4849MH exposed DAP must be soldered to the circuit board.

Note 10: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 11: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$.

Note 12: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 13: Machine Model, 220pF–240pF discharged through all pins.

Note 14: Typicals are measured at 25˚C and represent the parametric norm.

Note 15: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Typical Application

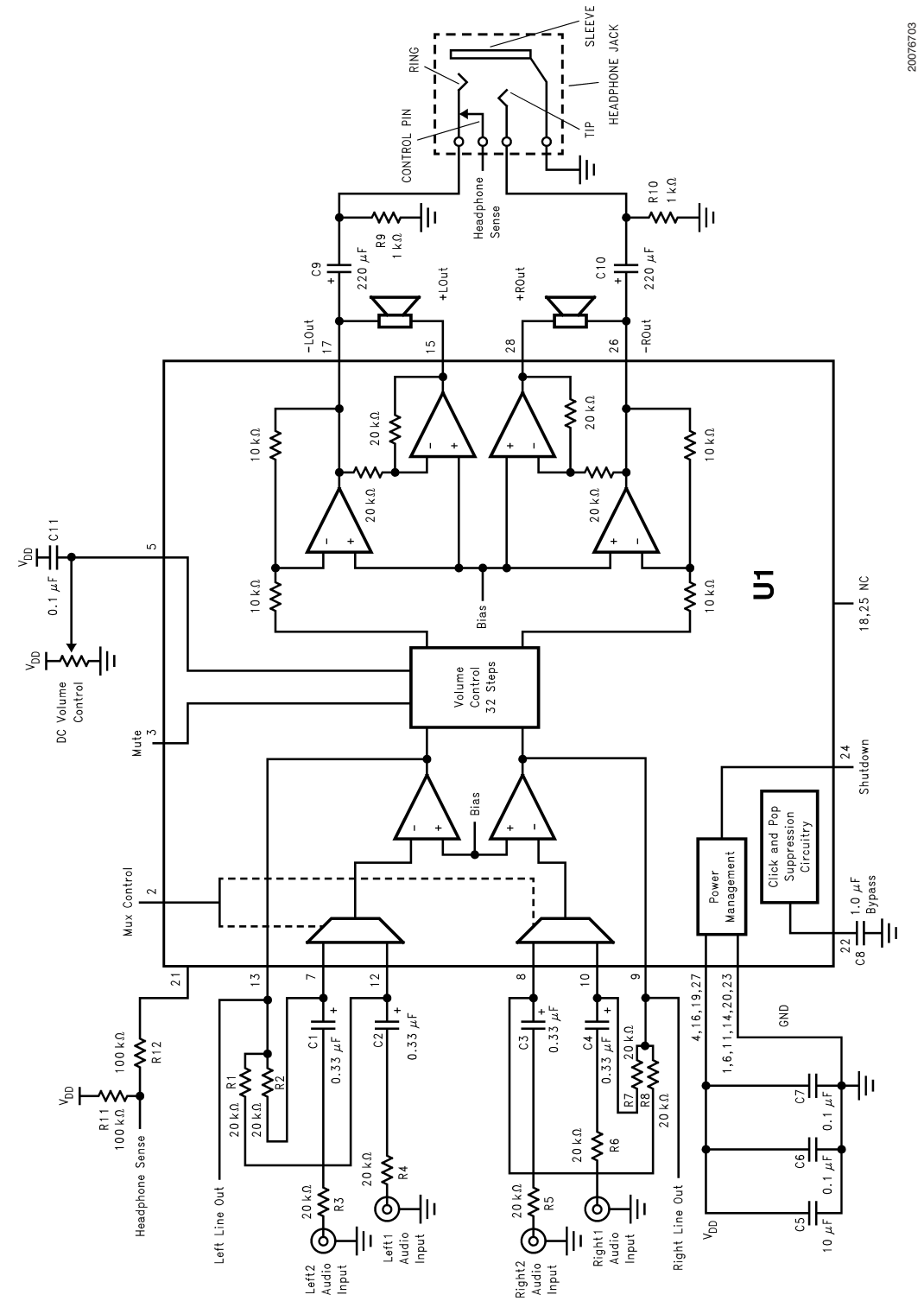


FIGURE 1. Typical Application Circuit (MH pinout)

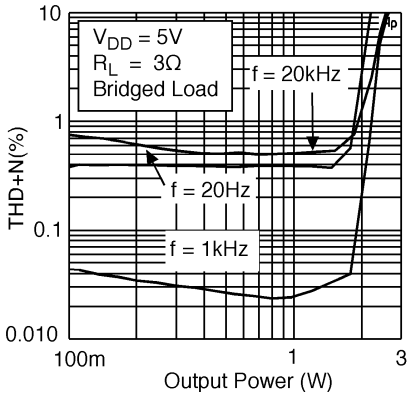
Truth Table for Logic Inputs (Note 16)

Mute	Mux Control	HP Sense	Inputs Selected	Bridged Output	Single-Ended Output
0	0	0	Left In 1, Right In 1	Vol. Adjustable	-
0	0	1	Left In 1, Right In 1	Muted	Vol. Adjustable
0	1	0	Left In 2, Right In 2	Vol. Adjustable	-
0	1	1	Left In 2, Right In 2	Muted	Vol. Adjustable
1	X	X	-	Muted	Muted

Note 16: If system beep is detected on the Beep in pin (pin 11) and beep is fed to inputs, the system beep will be passed through the bridged amplifier regardless of the logic of the Mute, HP sense, or DC Volume Control pins.

Typical Performance Characteristics

LM4849MH
THD+N vs Output Power



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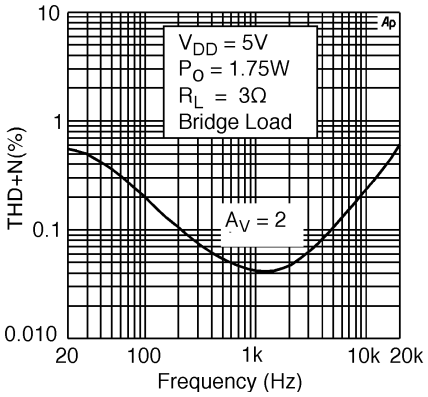
LM4849MH
THD+N vs Frequency



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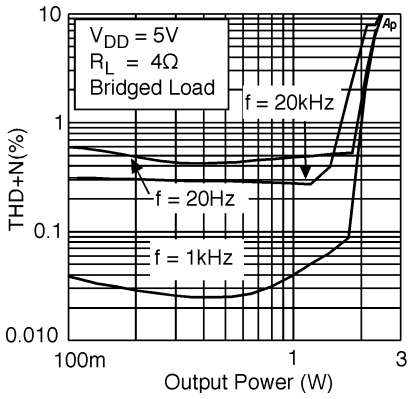
LM4849MH
THD+N vs Output Power



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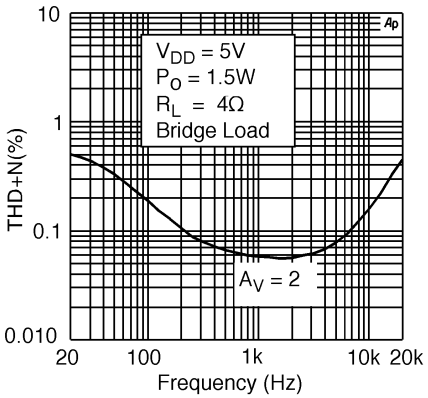
LM4849MH
THD+N vs Frequency



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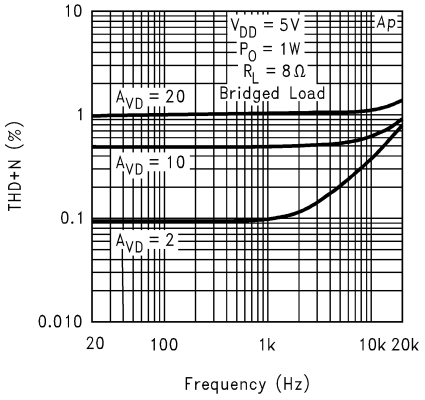
Typical Performance Characteristics (Continued)

THD+N vs Frequency



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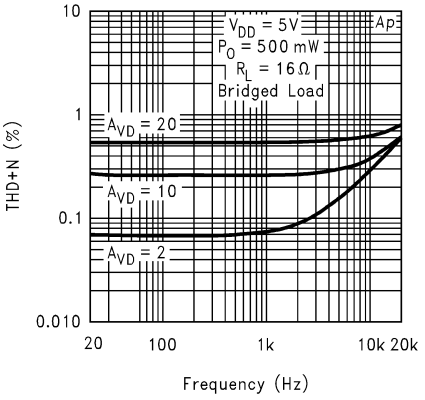
THD+N vs Frequency



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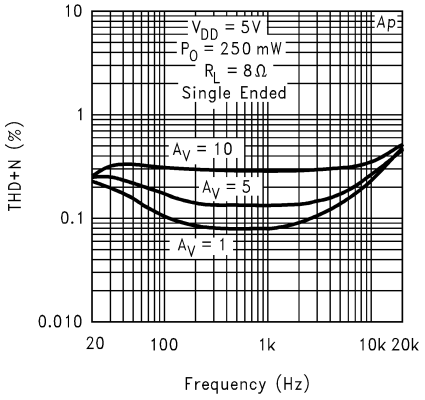
THD+N vs Frequency



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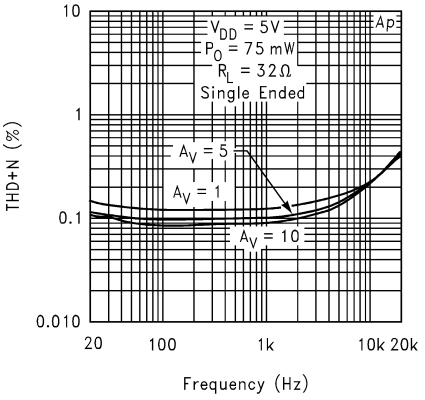
THD+N vs Frequency



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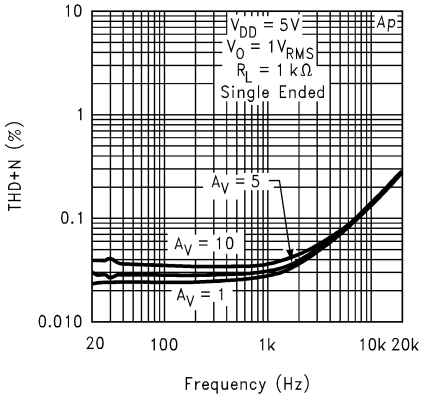
THD+N vs Frequency



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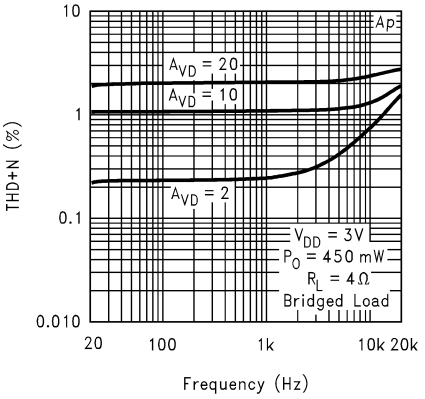
THD+N vs Frequency



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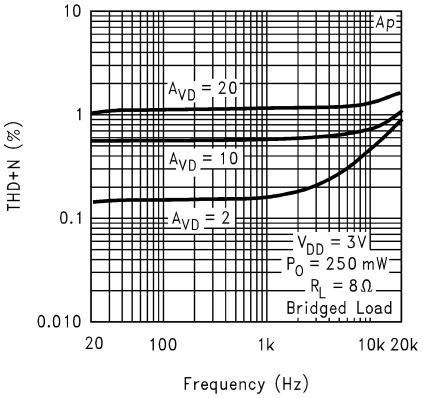
Typical Performance Characteristics (Continued)

THD+N vs Frequency



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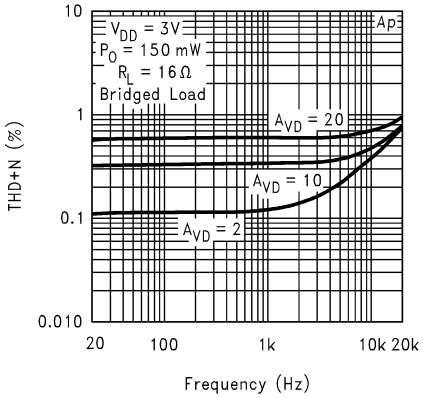
THD+N vs Frequency



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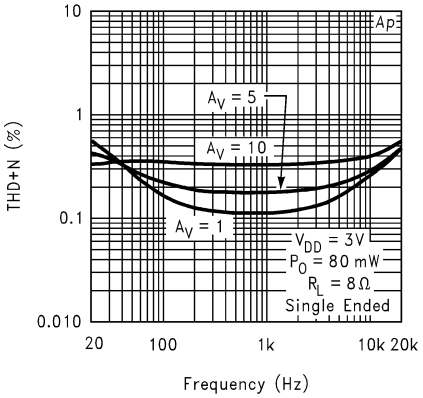
THD+N vs Frequency



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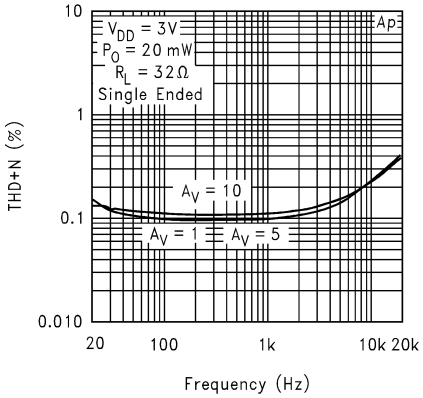
THD+N vs Frequency



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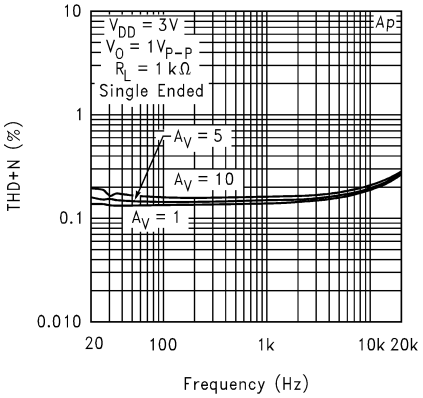
THD+N vs Frequency



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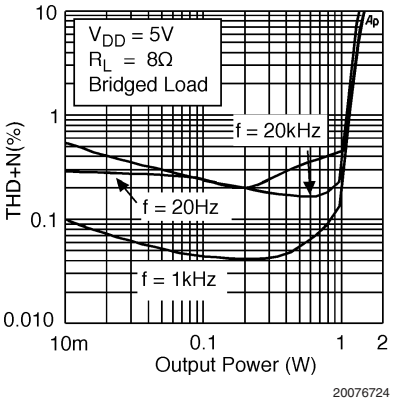
THD+N vs Output Power



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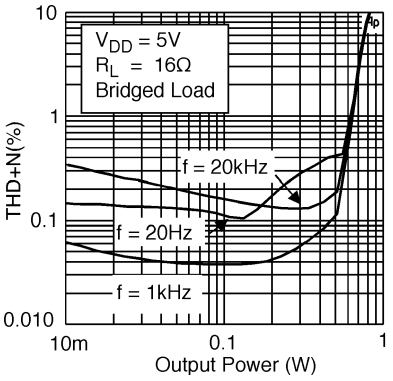
Typical Performance Characteristics (Continued)

THD+N vs Output Power



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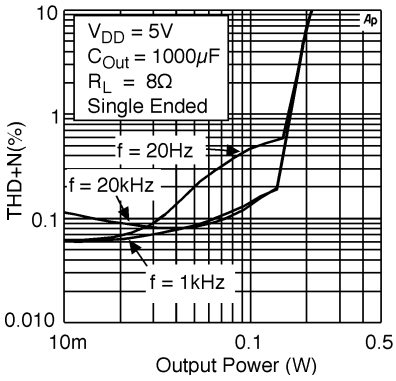
THD+N vs Output Power



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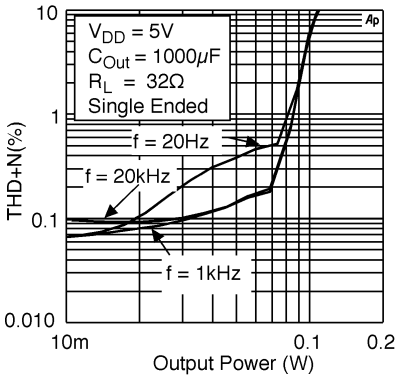
THD+N vs Output Power



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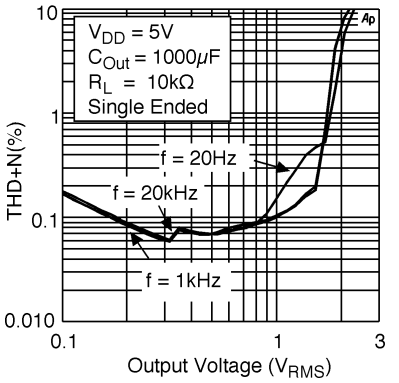
THD+N vs Output Power



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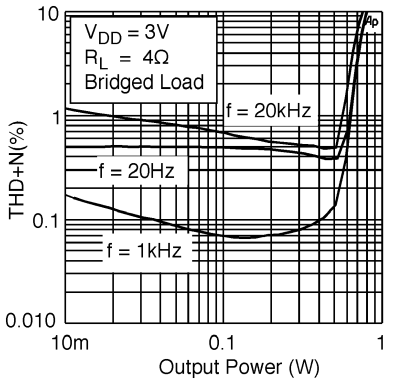
THD+N vs Output Power



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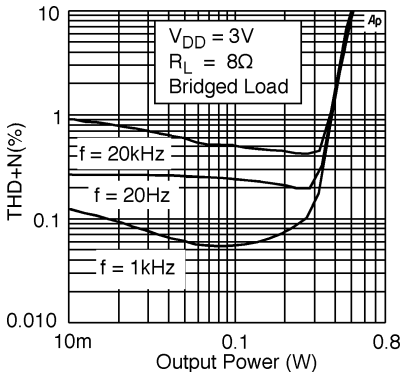
THD+N vs Output Power



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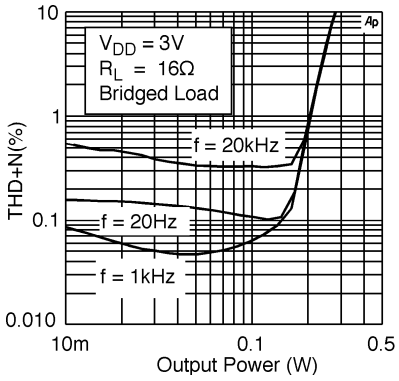
Typical Performance Characteristics (Continued)

THD+N vs Output Power



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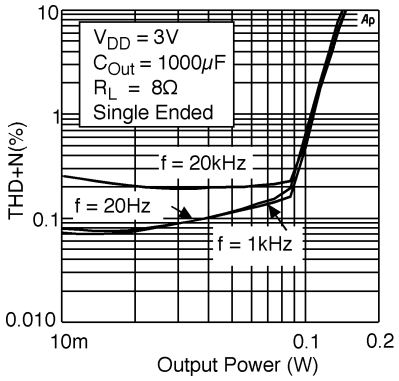
THD+N vs Output Power



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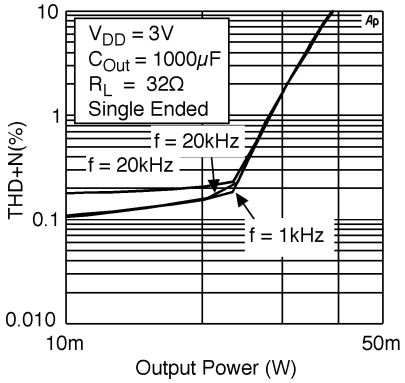
THD+N vs Output Power



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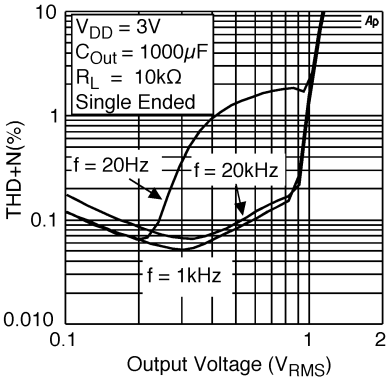
THD+N vs Output Power



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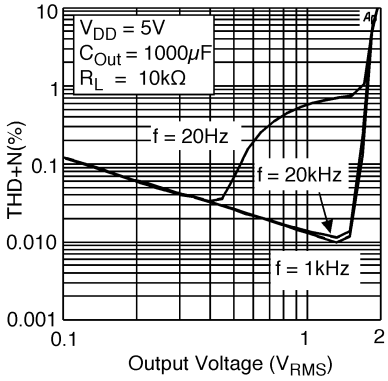
THD+N vs Output Voltage Line Out Pins



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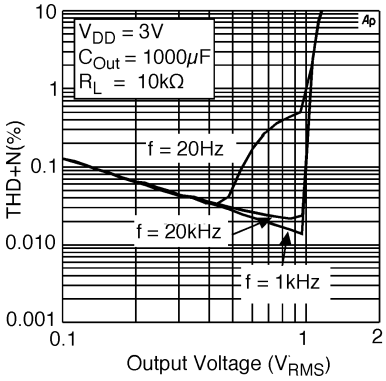
THD+N vs Output Voltage Line Out Pins



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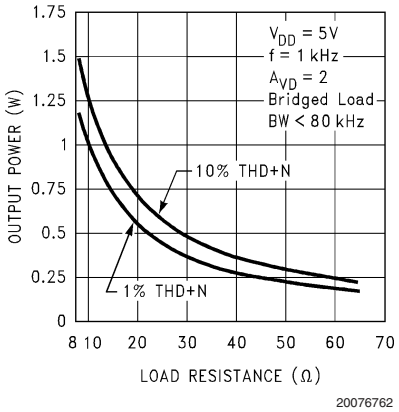
Typical Performance Characteristics (Continued)

Output Power vs Load Resistance



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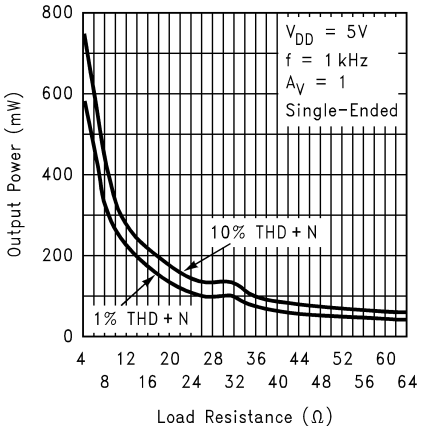
Output Power vs Load Resistance



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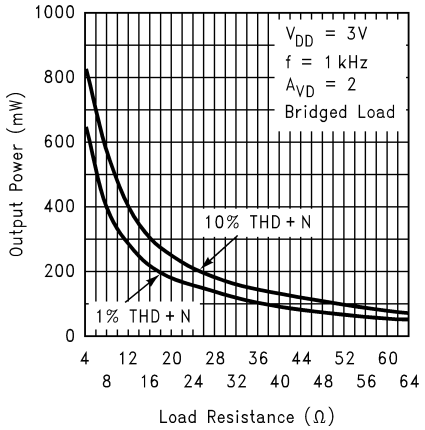
Output Power vs Load Resistance



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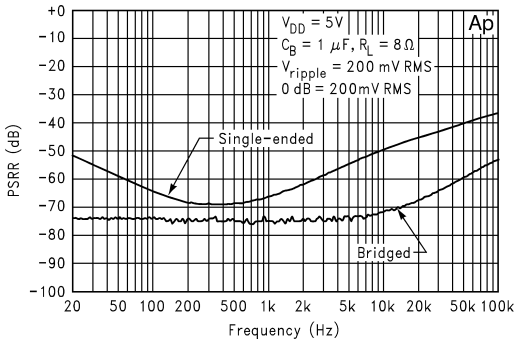
Power Supply Rejection Ratio



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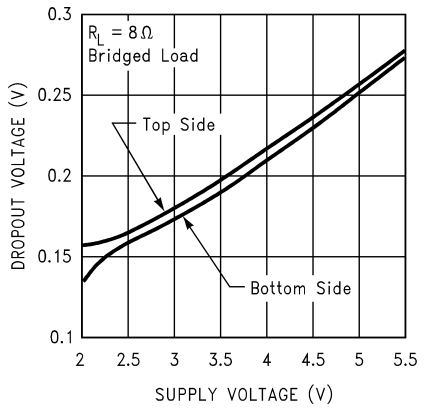
Dropout Voltage



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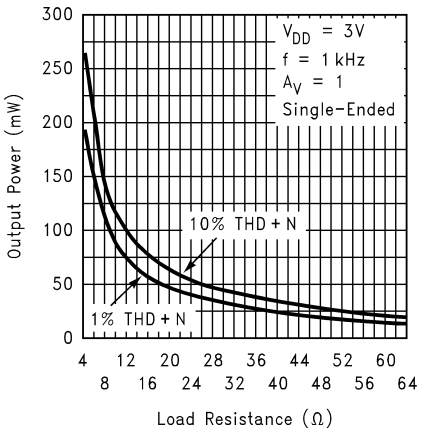
Output Power vs Load Resistance



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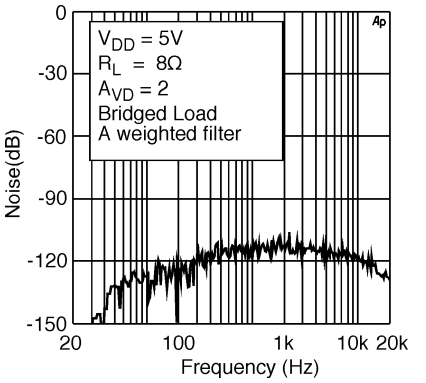
Typical Performance Characteristics (Continued)

Noise Floor



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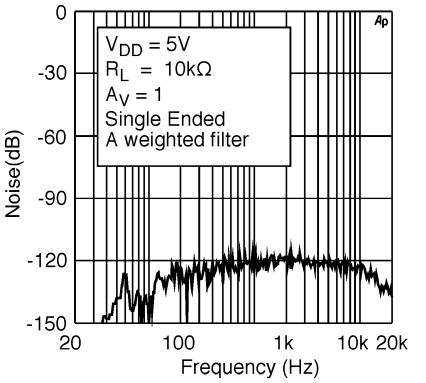
Noise Floor



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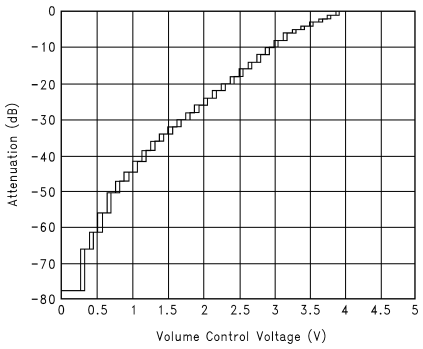
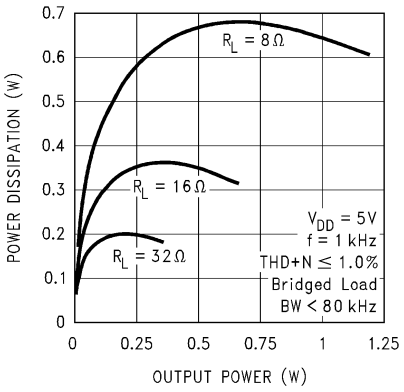
Volume Control Characteristics



20076736

Power Dissipation vs Output Power



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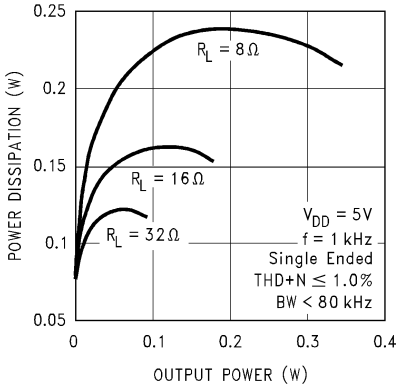
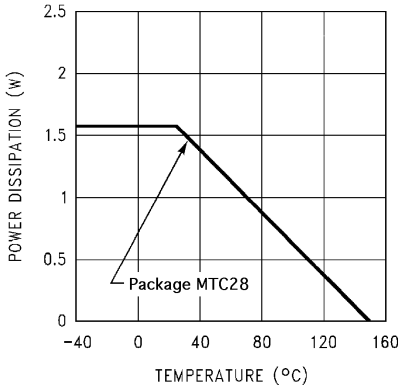
Power Dissipation vs Output Power



20076752

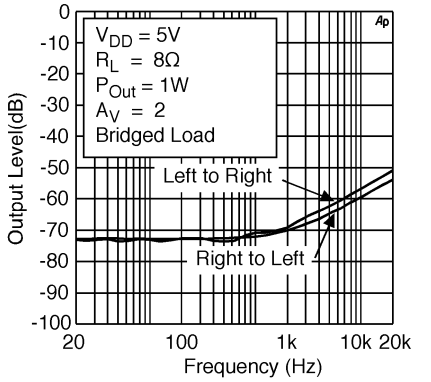
Power Derating Curve



20076763

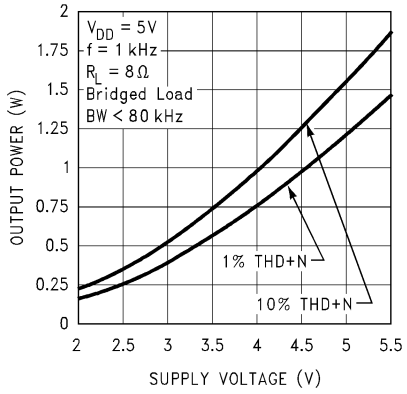
Typical Performance Characteristics (Continued)

Crosstalk



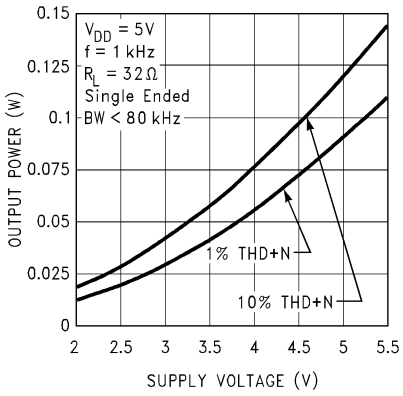
20076749

Output Power vs Supply voltage



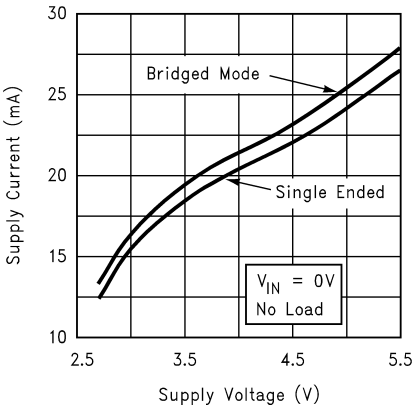
20076754

Output Power vs Supply Voltage



20076756

Supply Current vs Supply Voltage



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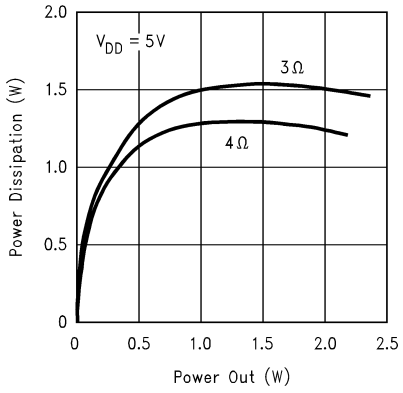
LM4849MH Power Dissipation vs Output Power



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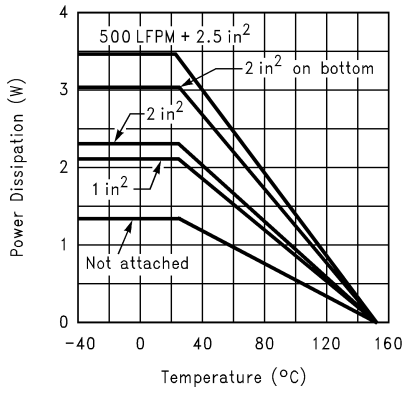
LM4849MH Power Derating Curve



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Note 17: These curves show the thermal dissipation ability of the LM4849MH at different ambient temperatures given these conditions:

500LFPM + 2in^2: The part is soldered to a 2in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it.

2in^{2}on bottom: The part is soldered to a 2in^2, 1oz. copper plane that is on the bottom side of the PC board through 21 8 mil vias.

2in^2: The part is soldered to a 2in^2, 1oz. copper plane.

1in^2: The part is soldered to a 1in^2, 1oz. copper plane.

Not Attached: The part is not soldered down and is not forced-air cooled.

Application Information

EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4849's exposed-DAP (die attach paddle) package (MH) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.1W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4849's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The MH package must have its exposed DAP soldered to a grounded copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 32(4x8) (MH) vias. The via diameter should be 0.012in–0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4849 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25˚C ambient temperature. Increase the area to compensate for ambient temperatures above 25˚C. In systems using cooling fans, the LM4849MH can take advantage of forced air cooling. With an air flow rate of 450 linear-feet per minute and a 2.5in^2 exposed copper or 5.0in^2 inner layer copper plane heatsink, the LM4849MH can continuously drive a 3Ω load to full power. The LM4849's power de-rating curve in the **Typical Performance Characteristics** shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-DAP TSSOP package is shown in the **Demonstration Board Layout** section.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4849 output stage consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.)

Figure 1 shows that the first amplifier's negative (-) output serves as the second amplifier's input. This results in both amplifiers producing signals identical in magnitude, but 180˚ out of phase. Taking advantage of this phase difference, a load is placed between –OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: **its differential output doubles the voltage swing across the load.** This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the **Audio Power Amplifier Design** section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4849 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 * (V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \quad (3)$$

Application Information (Continued)

The LM4849's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

The LM4849's T_{JMAX} = 150˚C. In the MH package soldered to a DAP pad that expands to a copper area of 2in^2 on a PCB, the LM4849's θ_{JA} is 41˚C/W. At any given ambient temperature T_A, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting P_{DMAX} for P_{DMAX}' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4849's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX}\,\theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 45˚C for the MH package.

$$T_{JMAX} = P_{DMAX}\,\theta_{JA} + T_A \quad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the LM4849's T_{JMAX} of 150˚C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If twice the value given by Equation (3) is greater than that of Equation (4), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the **Typical Performance Characteristics** curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 µF in parallel with a 0.1 µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0 µF tantalum bypass capacitance connected between the LM4849's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4849's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large a capacitor, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

PROPER SELECTION OF EXTERNAL COMPONENTS

Optimizing the LM4849's performance requires properly selecting external components. Though the LM4849 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4849 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain circuits demand input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of 1V_{RMS} (2.83V_{P-P}). Please refer to the **Audio Power Amplifier Design** section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires a high value input coupling capacitor (0.33µF in *Figure 1*). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using a large input capacitor.

Besides affecting system cost and size, the input coupling capacitor has an effect on the LM4849's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually V_{DD}/2) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistors, (R1, 2, 7, 8). Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired –3dB frequency.

As shown in *Figure 1*, the input resistors (R3, 4, 5, 6) and the input capacitors (CIN = 0.33µF) produce a –6dB high pass filter cutoff frequency that is found using Equation (7).

Application Information (Continued)

$$f_{-6\,dB} = \frac{1}{2\pi R_{IN} C_1} \quad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, the input coupling capacitor using Equation (7), is 0.063µF. The 0.33µF input coupling capacitor shown in *Figure 1* allows the LM4849 to drive high efficiency, full range speaker whose response extends below 30Hz.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4849 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pops”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4849’s internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD} . As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C_{Bypass} alters the device’s turn-on time and the magnitude of “clicks and pops”. Increasing the value of C_{Bypass} reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_{Bypass} increases, the turn-on time increases. There is a linear relationship between the size of C_{Bypass} and the turn-on time. Here are some typical turn-on times for various values of C_{Bypass}:

C_{Bypass}	T_{ON}
0.01µF	2ms
0.1µF	20ms
0.22µF	44ms
0.47µF	94ms
1.0µF	200ms

RIGHT AND LEFT LINE OUT

Applications such as notebook computers can take advantage of a line output signal to connect to external devices such as monitors or audio/visual equipment that sends or receives line level signals. The LM4849 has two outputs which connect to the outputs of the internal input amplifiers that drive the volume control inputs. These input amplifiers can drive loads of >1kΩ (such as powered speakers) with a rail-to-rail signal. Since the output signal present on the RIGHT Line Out and LEFT Line Out pins is biased to $V_{DD}/2$, coupling capacitors need to be connected in series with the load. Typical values for the coupling capacitors are 0.33µF to 1.0µF. If polarized coupling capacitors are used, connect their "+" terminals to the respective output pin.

Since the Line Out outputs precede the internal volume control, the signal amplitude will be equal to the input signal’s magnitude and cannot be adjusted. However, the input amplifier’s closed-loop gain can be adjusted using external resistors. These 20K resistors are shown in Figure 1 (R1 - R8) and they set each input amplifier’s gain to -1. Use Equation 8 to determine the input and feedback resistor values for a desired gain.

$$-A_v = R_2 / R_3 \quad (8)$$

Adjusting the input amplifier’s gain sets the minimum gain for that channel. Although the single ended outputs of the Bridge Output Amplifiers can be used to drive line level outputs, it is recommended that the Right & Left Line Outputs simpler signal path be used for better performance.

STEREO-INPUT MULTIPLEXER (STEREO MUX)

The LM4849 has two stereo inputs. The MUX CONTROL pin controls which stereo input is active. Applying 0V to the MUX CONTROL pin selects stereo input 1. Applying V_{DD} to the MUX CONTROL pin selects stereo input 2.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4849’s shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the LM4849’s micro-power shutdown feature turns off the amplifier’s bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.7 µA typical shutdown current is achieved by applying a voltage that is as near as V_{DD} as possible, to the SHUTDOWN pin. A voltage that is less than V_{DD} may increase the shutdown current. The Logic Level Truth Table shows the logic signal levels that activate and deactivate micro-power shutdown and headphone amplifier operation.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to V_{DD} through the pull-up resistor, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the need for a pull up resistor.

Application Information (Continued)

TABLE 1. Logic Level Truth Table for SHUTDOWN, HP-IN, and MUX Operation

SHUTDOWN PIN	HP-IN PIN	MUX CHANNEL SELECT PIN	OPERATIONAL MODE (MUX INPUT CHANNEL #)
Logic Low	Logic Low	Logic Low	Bridged Amplifiers (1)
Logic Low	Logic Low	Logic High	Bridged Amplifiers (2)
Logic Low	Logic High	Logic Low	Single-Ended Amplifiers (1)
Logic Low	Logic High	Logic High	Single-Ended Amplifiers (2)
Logic High	X	X	Micro-Power Shutdown

MUTE FUNCTION

The LM4849 mutes the amplifier and DOCK outputs when V_{DD} is applied to the MUTE pin. Applying 0V to the MUTE pin returns the LM4849 to normal, unmated operation. Prevent unanticipated mute behavior by connecting the MUTE pin to V_{DD} or ground. Do not let the mute pin float.

HP SENSE FUNCTION (Head Phone In)

Applying a voltage between 4V and V_{DD} to the LM4849's HP-IN headphone control pin turns off the amps that drive the left out "+" and right out "+" pins. This action mutes a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 2 shows the implementation of the LM4849's headphone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP Sense pin at approximately 50mV. This 50mV puts the LM4849 into bridged mode operation. The output coupling capacitor blocks the amplifier's half supply DC voltage, protecting the headphones. (The HP-IN threshold is set at 4V). While the LM4849 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from R2 and allows R1 to pull the HP Sense pin up to V_{DD} through R4. This enables the headphone function, turns off both of the "+" output amplifiers and mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistors R2 and R3. These resistors have negligible effect on the LM4849's output drive capability since the typical impedance of headphones is 32Ω.

Figure 2 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP-IN pin when connecting headphones.

A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP-IN pin, a bridge-connected speaker is muted and the single ended output amplifiers will drive a pair of headphones.

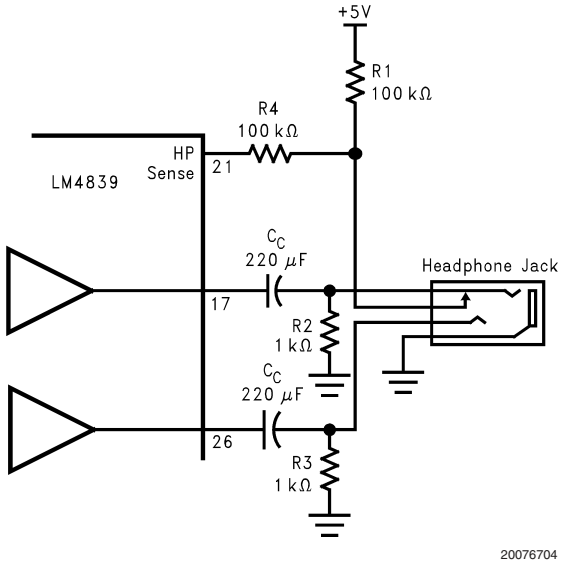


FIGURE 2. Headphone Sensing Circuit (MH Pinout)

DC VOLUME CONTROL

The LM4849 has an internal stereo volume control whose setting is a function of the DC voltage applied to the DC VOL CONTROL pin.

The LM4849 volume control consists of 31 steps that are individually selected by a variable DC voltage level on the volume control pin. The range of the steps, controlled by the DC voltage, are from 0dB - 78dB. Each gain step corresponds to a specific input voltage range, as shown in table 2.

To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis has been implemented. The amount of hysteresis corresponds to half of the step width, as shown in Volume Control Characterization Graph (DS200133-40).

For highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions to the next highest or next lowest gain levels.

The gain levels are 1dB/step from 0dB to -6dB, 2dB/step from -6dB to -36dB, 3dB/step from -36dB to -47dB, 4dB/step from -47db to -51dB, 5dB/step from -51dB to -66dB, and 12dB to the last step at -78dB.

Application Information (Continued)

VOLUME CONTROL (Table 2)

Gain (dB)	Voltage Range (% of Vdd)			Voltage Range (Vdd = 5)			Voltage Range (Vdd = 3)		
	Low	High	Recommended	Low	High	Recommended	Low	High	Recommended
0	77.5%	100.00%	100.000%	3.875	5.000	5.000	2.325	3.000	3.000
-1	75.0%	78.5%	76.875%	3.750	3.938	3.844	2.250	2.363	2.306
-2	72.5%	76.25%	74.375%	3.625	3.813	3.719	2.175	2.288	2.231
-3	70.0%	73.75%	71.875%	3.500	3.688	3.594	2.100	2.213	2.156
-4	67.5%	71.25%	69.375%	3.375	3.563	3.469	2.025	2.138	2.081
-5	65.0%	68.75%	66.875%	3.250	3.438	3.344	1.950	2.063	2.006
-6	62.5%	66.25%	64.375%	3.125	3.313	3.219	1.875	1.988	1.931
-8	60.0%	63.75%	61.875%	3.000	3.188	3.094	1.800	1.913	1.856
-10	57.5%	61.25%	59.375%	2.875	3.063	2.969	1.725	1.838	1.781
-12	55.0%	58.75%	56.875%	2.750	2.938	2.844	1.650	1.763	1.706
-14	52.5%	56.25%	54.375%	2.625	2.813	2.719	1.575	1.688	1.631
-16	50.0%	53.75%	51.875%	2.500	2.688	2.594	1.500	1.613	1.556
-18	47.5%	51.25%	49.375%	2.375	2.563	2.469	1.425	1.538	1.481
-20	45.0%	48.75%	46.875%	2.250	2.438	2.344	1.350	1.463	1.406
-22	42.5%	46.25%	44.375%	2.125	2.313	2.219	1.275	1.388	1.331
-24	40.0%	43.75%	41.875%	2.000	2.188	2.094	1.200	1.313	1.256
-26	37.5%	41.25%	39.375%	1.875	2.063	1.969	1.125	1.238	1.181
-28	35.0%	38.75%	36.875%	1.750	1.938	1.844	1.050	1.163	1.106
-30	32.5%	36.25%	34.375%	1.625	1.813	1.719	0.975	1.088	1.031
-32	30.0%	33.75%	31.875%	1.500	1.688	1.594	0.900	1.013	0.956
-34	27.5%	31.25%	29.375%	1.375	1.563	1.469	0.825	0.937	0.881
-36	25.0%	28.75%	26.875%	1.250	1.438	1.344	0.750	0.862	0.806
-39	22.5%	26.25%	24.375%	1.125	1.313	1.219	0.675	0.787	0.731
-42	20.0%	23.75%	21.875%	1.000	1.188	1.094	0.600	0.712	0.656
-45	17.5%	21.25%	19.375%	0.875	1.063	0.969	0.525	0.637	0.581
-47	15.0%	18.75%	16.875%	0.750	0.937	0.844	0.450	0.562	0.506
-51	12.5%	16.25%	14.375%	0.625	0.812	0.719	0.375	0.487	0.431
-56	10.0%	13.75%	11.875%	0.500	0.687	0.594	0.300	0.412	0.356
-61	7.5%	11.25%	9.375%	0.375	0.562	0.469	0.225	0.337	0.281
-66	5.0%	8.75%	6.875%	0.250	0.437	0.344	0.150	0.262	0.206
-78	0.0%	6.25%	0.000%	0.000	0.312	0.000	0.000	0.187	0.000

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	1 W_{RMS}
Load Impedance:	8Ω
Input Level:	1 V_{RMS}
Input Impedance:	20 kΩ
Bandwidth:	100 Hz–20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the **Typical Performance Characteristics** section. Another way, using Equation (11), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (11). The result is Equation (12).

$$V_{outpeak} = \sqrt{(2R_L P_O)} \quad (9)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{OD_{TOP}} + V_{OD_{BOT}})) \quad (10)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4849 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of

Application Information (Continued)

supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the **Power Dissipation** section.

After satisfying the LM4849's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation (13).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (11)$$

Thus, a minimum overall gain of 2.83 allows the LM4849's to reach full output swing and maintain low noise and THD+N performance.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (12)$$

and an

$$f_H = 20kHz \times 5 = 100kHz \quad (13)$$

As mentioned in the **Selecting Proper External Components** section, R_i (Right & Left) and C_i (Right & Left) create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (17).

$$C_i \geq 1/(2\pi R_i f_L) \quad (14)$$

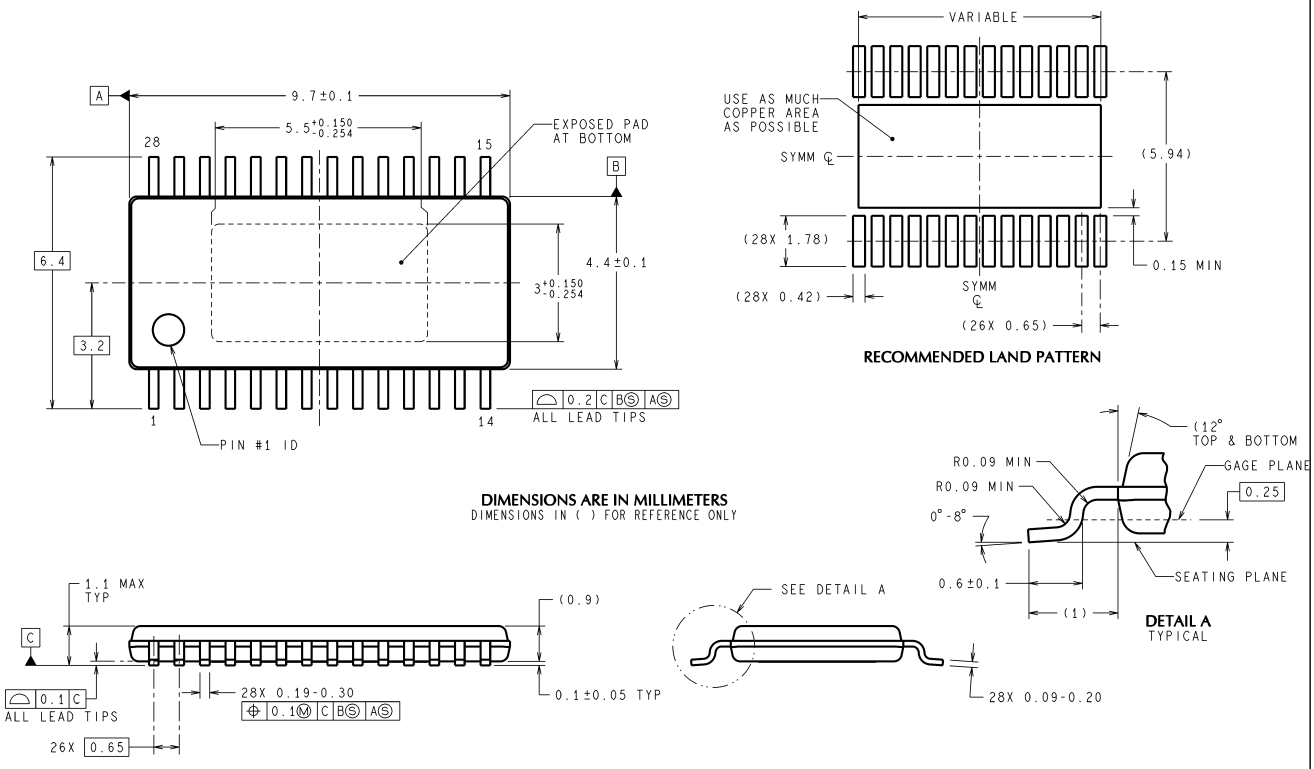
The result is

$$1/(2\pi * 20k\Omega * 20Hz) = 0.397\mu F \quad (15)$$

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_{VD}, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4849's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance,restricting bandwidth limitations.

Physical Dimensions inches (millimeters) unless otherwise noted



MXA28A (Rev C)

Exposed-DAP TSSOP Package
Order Number LM4849MH
NS Package Number MXA28A for Exposed-DAP TSSOP

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