Ordering number : EN3356A

SANYO Semiconductors
DATA SHEET

CMOS IC

LC7185-8750 — CB Transceiver PLL Frequency Synthesizer and Controller

Overview

This 27 MHz band, PLL frequency synthesizer LSI chip is designed specifically for CB transceivers.
The specifications are suited for use in U.S.A.(FCC).

Functions

The LC7185-8750 incorporates PLL circuitry and a controller for CB applications on a single CMOS chip. The controller handles the PLL circuitry, frequency data ROM, channel preset/recall RAM, and LED display driver. It also supports channel scan, channel preset/recall, and emergency channel call.

Features

1. A built-in programmable divider for the 16 MHz VCO
2. Transmission is inhibited when the PLL is unlocked (digital lock monitor).
3. Direct channel 9 or 19 selection (sliding switch)
4. A 7-segment, 2-character LED display
5. "PA" is displayed in public announcement mode.
6. Output beep-tone control circuitry
7. Up to 5 channel settings can be stored in memory.
8. 4 × 3 key matrix implementation

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Pin V_{DD}	–0.3 to +9.0	V
Input voltage	$V_{IN}1$ max	Pins $\overline{HOLD}$, $\overline{TX}$	–0.3 to +15	V
	$V_{IN}2$ max	Input pins other than $V_{IN}1$ max	–0.3 to V_{DD} +0.3	V
Output voltage	V_O1 max	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2	–0.3 to +15	V
	V_O2 max	Pins $\overline{UL}$, BEEP	–0.3 to +15	V
	V_O3 max	Pin PD	–0.3 to V_{DD} +0.3	V
	V_O4 max	Output pins other than mentioned above	–0.3 to V_{DD} +0.3	V
Output Current	I_O1 max	Pins SA, SB, SC, SD, SE, SF, SG	0 to +30	mA
	I_O2 max	Pins D1, D2	0 to +10	mA
	I_O3 max	Pins $\overline{UL}$	0 to +20	mA
	I_O4 max	Pin BEEP	0 to +10	mA
Allowable power dissipation	Pd max	(Ta ≤ 85°C)	350	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

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Allowable Operating Conditions at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		5.0		8.0	V
Input high-level voltage	$V_{IH}1$	Pins $\overline{HOLD}$, $\overline{TX}$	$0.7V_{DD}$		12	V
	$V_{IH}2$	Pin $\overline{INIT}$	3.2		V_{DD}	V
	$V_{IH}3$	Pins KI1, KI2, KI3, KI4	$0.6V_{DD}$		V_{DD}	V
Input low-level voltage	$V_{IL}1$	Pins $\overline{HOLD}$, $\overline{TX}$	0		$0.3V_{DD}$	V
	$V_{IL}2$	Pin $\overline{INIT}$	0		1.3	V
	$V_{IL}3$	Pins KI1, KI2, KI3, KI4	0		$0.4V_{DD}$	V
Output voltage	$V_{OUT}1$	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2	0		13	V
	$V_{OUT}2$	Pins $\overline{UL}$, BEEP	0		8	V
Input frequency	$f_{IN}1$	Pin XIN (sine wave, capacitor coupled)	1.0	10.24	15	MHz
	$f_{IN}2$	Pin PIN (sine wave, capacitor coupled)	10		30	MHz
Input amplitude	$V_{IN}1$	Pin XIN (sine wave, capacitor coupled)	0.5		1.5	Vrms
	$V_{IN}2$	Pin PIN (sine wave, capacitor coupled)	0.15		1.5	Vrms
Required oscillating frequency	X'tal	Pins XIN, XOUT (CI ≦ 50 Ω)	5.0	10.24	15	MHz

Electrical Characteristics at under allowable operating conditions

Parameter	Symbol	Conditions	min	typ	max	Unit
Internal feedback resistance	Rf1	Pin XIN		1.0		MΩ
	Rf2	Pin PIN		500		kΩ
Pull-down resistor	RpdN	Pins KI1, KI2, KI3, KI4, TEST	30	50	70	kΩ
Input high-level current	$I_{IH}1$	Pins $\overline{HOLD}$, $\overline{TX}$ V_I = 12 V			5.0	μA
	$I_{IH}2$	Pin $\overline{INIT}$ $V_I = V_{DD}$			5.0	μA
	$I_{IH}3$	Pin XIN $V_I = V_{DD}$			25	μA
	$I_{IH}4$	Pin PIN $V_I = V_{DD}$			50	μA
Input low-level current	$I_{IL}1$	Pins $\overline{HOLD}$, $\overline{TX}$ $V_I = V_{SS}$			5.0	μA
	$I_{IL}2$	Pin $\overline{INIT}$ $V_I = V_{SS}$			5.0	μA
	$I_{IL}3$	Pin XIN $V_I = V_{SS}$			25	μA
	$I_{IL}4$	Pin PIN $V_I = V_{SS}$			50	μA
Output high-level voltage	$V_{OH}1$	Pins KO1, KO2, KO3 I_O = 1 mA	V_{DD}–2.0	V_{DD}–1.0	V_{DD}–0.5	V
	$V_{OH}2$	Pin PD I_O = 0.5 mA	V_{DD}–1.0			V
Output low-level voltage	$V_{OL}1$	Pins KO1, KO2, KO3 I_O = 20 μA	0.6	1.0	1.4	V
	$V_{OL}2$	Pin PD I_O = 0.5 mA			1.0	V
	$V_{OL}3$	Pin BEEP I_O = 2 mA			1.0	V
	$V_{OL}4$	Pins SA, SB, SC, SD, SE, SF, SG I_O = 20 mA			1.0	V
	$V_{OL}5$	Pins D1, D2 I_O = 5 mA			1.0	V
	$V_{OL}6$	Pin $\overline{UL}$ I_O = 10 mA			1.0	V
Output leakage current	$I_{OFF}1$	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2 V_O = 13 V			5.0	μA
	$I_{OFF}2$	Pins $\overline{UL}$, BEEP V_O = 8 V			5.0	μA
High-level tristate leakage current	I_{OFFH}	Pin PD $V_O = V_{DD}$		0.01	10.0	nA
Low-level tristate leakage current	I_{OFFL}	Pin PD $V_O = V_{SS}$		0.01	10.0	nA
Supply current	$I_{DD}1$	Normal mode *1 (PLL operates)		5	10	mA
	$I_{DD}2$	Hold mode V_{DD} = 3.2 V *2 (memory backup) V_{DD} = 8.0 V			5 15	μA μA

*1: $f_{IN}2$ = 20 MHz (PIN)
$V_{IN}2$ = 0.15 Vrms
X'tal = 10.240 MHz
$\overline{TX}$ = $\overline{HOLD}$ = $\overline{INIT}$ = V_{DD}
Other inputs = V_{SS}
Other outputs = open

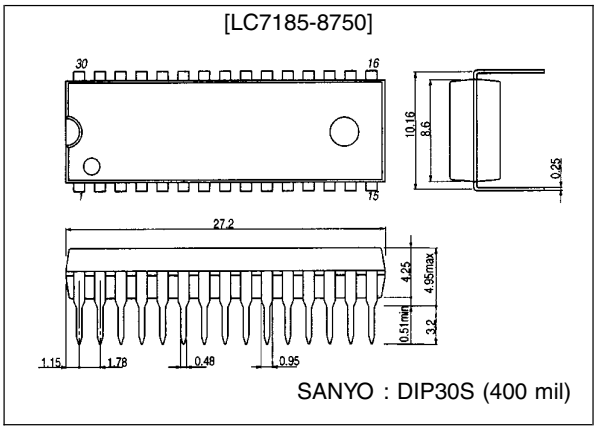
*2: $\overline{HOLD}$ = V_{SS}
$\overline{TX}$ = $\overline{INIT}$ = V_{DD}
Other inputs = V_{SS}
Other outputs = open

Note: Be careful that the dielectric strength of pins SA, SB, SC, SD, SE, SF, D1, D2, UL, BEEP are weak.

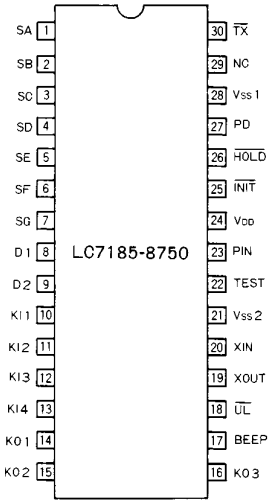
Package Dimensions

unit : mm

3061-DIP30S

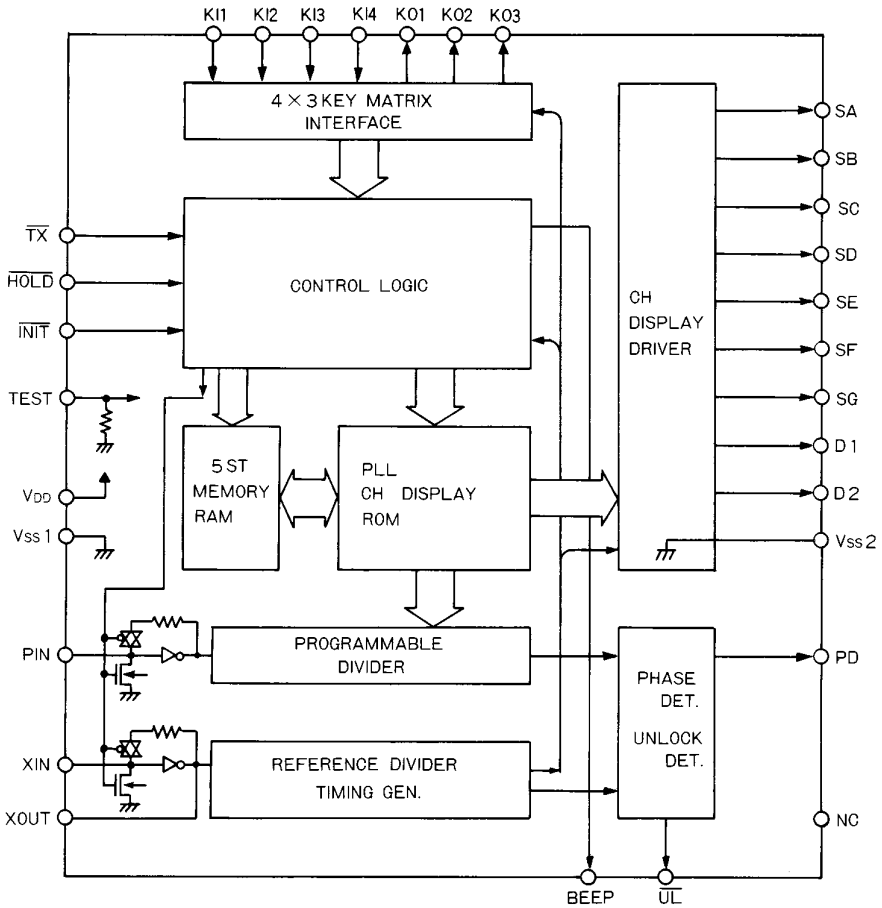


Pin Assignment



Top view

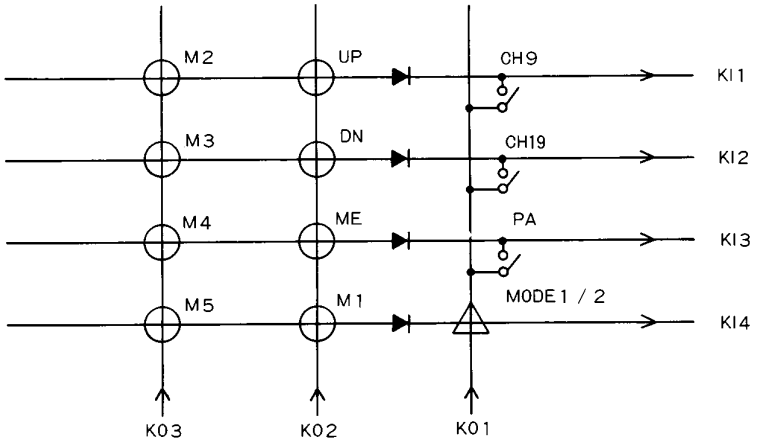
Block Diagram



Pin Descriptions

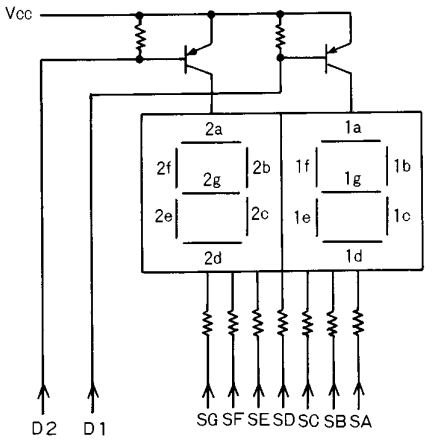
$\overline{TX}$	Transmit/receive select	PD	Charge pump output
$\overline{HOLD}$	Hold mode select	NC	NC pin
$\overline{INIT}$	Initial input	SA to SG	Segment driver (for display)
TEST	Test point (input)	D1, D2	Digit output (for display)
V_{DD}, $V_{SS}1$, $V_{SS}2$	Power supply	KI1 to KI4	Key inputs
PIN	Programmable divider input	KO1 to KO3	Key scan outputs
XIN, XOUT	Crystal oscillator input, output (10.240 MHz)	BEEP	Beep-tone control output
$\overline{UL}$	Unlock detection signal output		

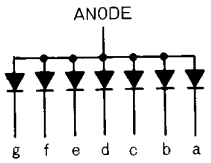
Key Matrix



CH9	Emergency CH9 recall	ME	Station Memory Enable
CH19	Emergency CH19 recall	M1 to M5	Station Memory recall
PA	Public announcement display	UP/DN/ME/M1 to 5	Momentary SW
MODE 1/2	Display Mode	CH9/CH19/PA	Slide SW
UP	CH up/scan	MODE 1/2	Diode
DN	CH down/scan		

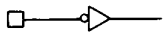
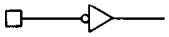
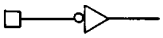
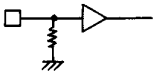
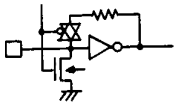
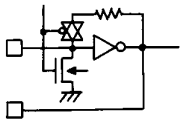
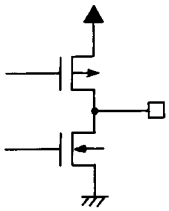
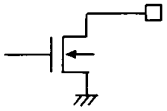
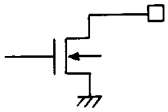
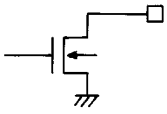
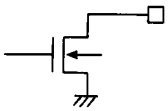
LED Display Configuration (Common anode/7 segment)





	SG	SF	SE	SD	SC	SB	SA
D1	1g	1f	1e	1d	1c	1b	1a
D2	2g	2f	2e	2d	2c	2b	2a

Pin Description

Pin Name	Pin No.	Type	Description
$\overline{TX}$	30		• Transmit/receive select $\overline{TX}$ = "0"...Transmit, TX = "1"...Receive
$\overline{HOLD}$	26		• Hold mode select $\overline{HOLD}$ = "0"...Hold mode select = "1"...Normal mode select
$\overline{INIT}$	25		• Reset line $\overline{INIT}$ = "0"...Reset
TEST	22		• Test point (input) Tie to ground or leave floating
V_{DD}	24		• Power supply (+) Normal mode: 5.0 to 8.0 V Hold mode: ≧ 3.2 V
$V_{SS}2$	21		• Channel display LED driver ground
PIN	23		• Programmable divider input 150 mVrms min Hold mode: Programmable divider is disabled.
XIN XOUT	20 19		• Crystal oscillator Frequency: 10.24 MHz Hold mode: Oscillator is disabled.
PD	27		• Charge pump output from the phase comparator. If the frequency of fV (the signal obtained by dividing the PIN input by N) is higher than that of fR (the reference signal), or if the phase of fV leads that of fR, positive pulses are output on this pin. If the frequency is lower or the phase lags, negative pulses are output on this pin. If they match, the pin goes to high impedance. • fV > fR OR leading: Positive Pulses • fV < fR OR leading: Negative Pulses • fV = fR and phase muched: High impedance Hold mode: High impedance
$V_{SS}1$	28		• PLL circuit and controller ground
NC	29		• No-connection
$\overline{UL}$	18		• Unlock detected output Fixed to low level when unlocked, when changing channels, in PA mode, or in hold mode. Open: Locked
BEEP	17		• Beep-tone control output During station memory operation During I/O on emergency channel When changing channels During reset During hold mode recovery Fixed to low level in hold mode — Transistor: Off (50 ms cycle) → Open
SA to SG	1 to 7		• Segment drivers for the display (Common anode/7 segments)
D1 D2	8 9		• Digit output (150 Hz) for the display (common anode/7 segments) Hold mode: Transistor goes off.

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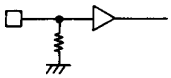
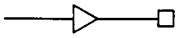
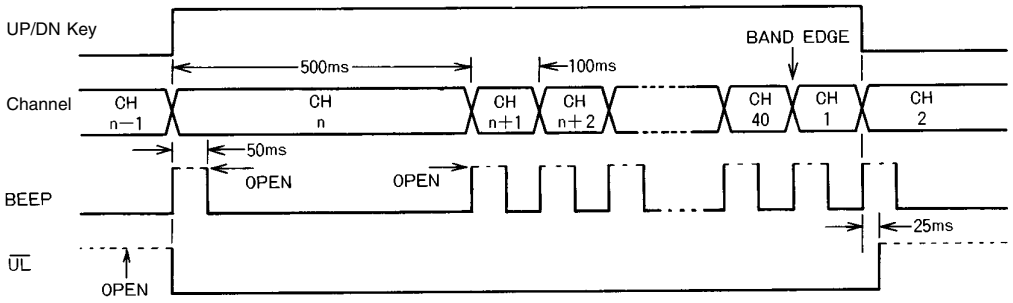
Pin Name	Pin No.	Type	Description
KI1 to KI4	10 to 13		• Key inputs Input from the key matrix
KO1 to KO3	14 to 16		• Key scan output (75 Hz) Output to the key matrix Hold mode: Low (scanning stops)

Operation

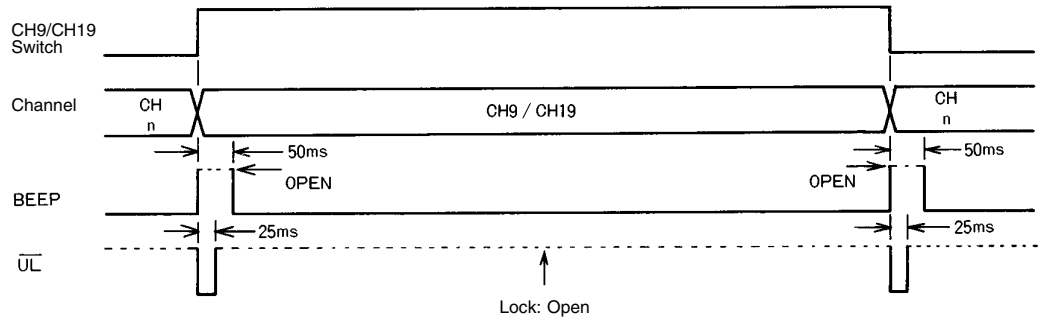
(1) Channel Selection (up/down)

1. Manual scanning (up/down)
   Pressing the UP key increments by one channel and pressing the DN key decrements by channel.
   When scanning reaches the end of the band, it automatically wraps around to the beginning.
2. Auto scanning (up/down)
   Holding the UP (or DN) key down for 500 ms or longer starts auto scanning. For both up and down scanning, each channel takes 100 ms to scan.
3. The unlock detected line ($\overline{UL}$) is asserted (low) when the UP (or DN) key is pressed and deactivated 25 ms after the key is released.
4. The beep-tone control line (BEEP) is asserted (open) for 50 ms after each new channel is selected.



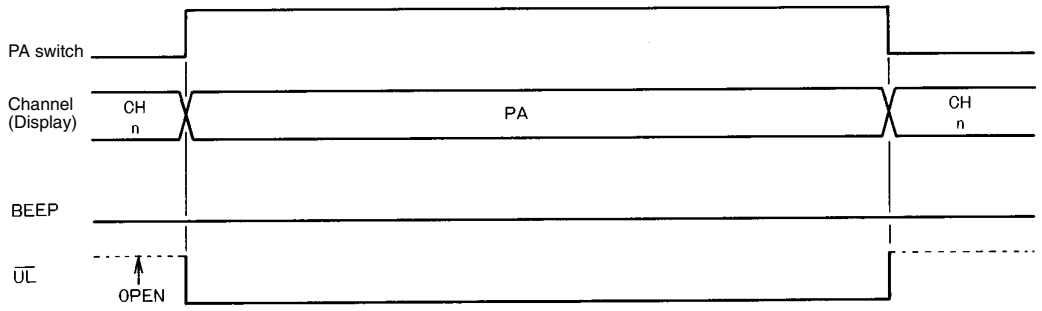
(2) Selecting an Emergency Channel (CH9/CH19)

1. If the CH9 or CH19 switch is turned on, the LC7185 stores the value of the previous channel and asserts the beep-tone control line for 50 ms.
2. While the CH9 or CH19 switch is turned on, the LC7185 disables all keys except $\overline{TX}$ and PA (UP/DN, ME, and M1 to M5 switches).
3. Even if the CH9 or CH19 switch is turned off while transmitting using the CH9 or CH19 switch, keep the emergency channel open until the LC7185 is in the receive mode.
4. After the CH9 or CH19 switch is turned back off, the beep-tone control line is asserted for 50 ms and the LC7185 reopens the previous channel.
5. Note the CH9 has a higher priority over CH19. As a result, if both switches are turned on, CH9 will be opened.
6. The $\overline{UL}$ line is asserted for 25 ms after the CH9 or CH19 switch is turned off or on.
7. Causes either "9" or "19" to blink on the display.



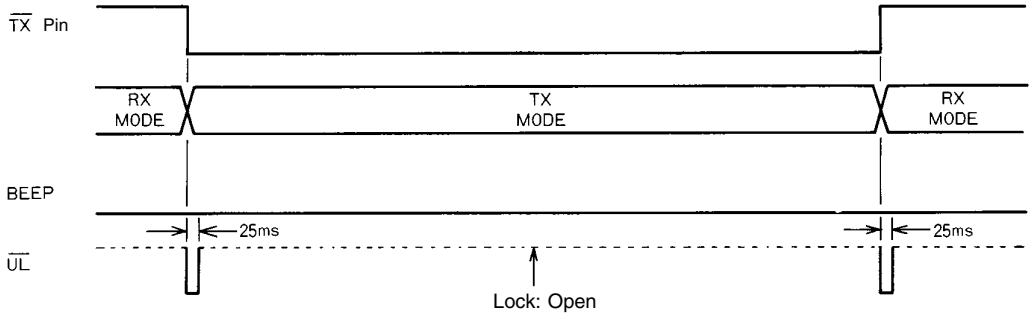
(3) Public Announcement (PA) Mode

1. When the PA switch is turned on, the LC7185 stores the value of the previous channel and enters the PA mode.
2. While the PA switch is turned on, the LC7185 disables all keys ($\overline{TX}$, CH9/CH19, UP/DN, ME, M1 to M5)
3. "PA" is displayed on the channel display.
4. When the PA switch is turned back off, the LC7185 enters the CB mode and reopens the previous channel.
5. The $\overline{UL}$ line is asserted while the PA switch is turned on.



(4) Transmit/Receive Selection

1. When the $\overline{TX}$ line is asserted, the LC7185 enters TX mode.
2. If the PA switch is turned on while the LC7185 is in TX mode, the device enters PA mode. However, if any other switch (other than the PA switch) or key (UP/DN, ME, M1 through M5, CH9, CH19) is pressed while the LC7185 is in TX mode, that switch or key has no effect.
3. The unlock detected signal is output each time the device switches between transmitting and receiving.



(5) Channel Preset/Recall Facility

1. The LC7185 allows up to 5 channels to be preset (assigned to M1 to M5).
   • After a reset (when the power is turned on, etc.), M1 to M5 are assigned to CH33.
2. Recalling preset channels
   • A preset channel is recalled by pressing one of the preset memory keys (M1 to M5) to which the channel was previously assigned.
   • There are two different display modes as shown below.

   Mode 1 (without diode)

   Each time a key is pressed (M1 to M5), the new channel is displayed.

   Example: Display 21 → 15

   key M1

   Mode 2 (with diode)

   Each time a key is pressed (M1 to M5), a key mnemonic ("P1" to "P5") is displayed for 400 ms, then the new channel is displayed.

   Example: Display 21 → P1 → 15

   400 ms

   Key M1

3. Presetting channels
   - First select the channel to be preset, then hold down the ME key and press the preset memory key (M1 to M5) to which you would like to assign the current channel.
     In the following cases, a channel will not be preset:
     - M1 to M5 is pressed and in the memory preset mode.
     - Emergency channels CH9 or CH19 are currently selected.
     - The $\overline{TX}$ line is asserted.
     - The PA switch is turned on (PA mode).
     - The $\overline{HOLD}$ line is asserted (hold mode).

     Even if the above key operations are not performed, the preset mode will be canceled automatically after 9 seconds.

   - There are two different display modes as shown below.

     Mode 1 (without diode)

     The current channel is displayed throughout the preset process.

     Example: Display 15 ⟶ 15
     Key ME M1

     Mode 2 (with diode)

     When the ME key is held down, "PE" is flashed on the display, indicating that presetting is possible. Once a preset memory key (M1 to M5) is pressed, the key mnemonic ("P1" to "P5") is displayed for 400 ms before the current channel is redisplayed.

     Example: Display 15 → PE → P1 → 15
     400 ms
     Key ME M1

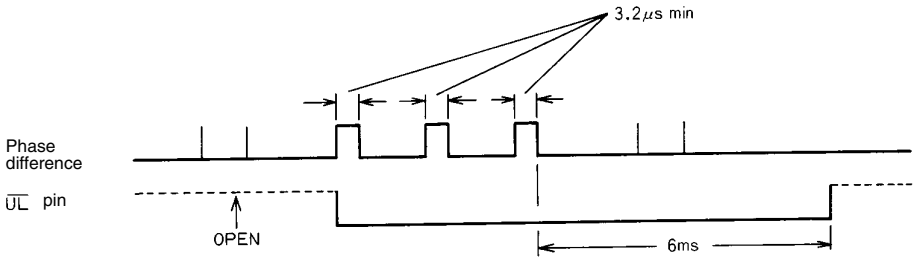
   - Note that if two or more keys are pressed at the same time, priority is assigned as follows:
     M1 > M2 > M3 > M4 > M5

(6) Beep-tone Control Output (BEEP pin)

After each of the following events, the BEEP line is asserted for 50 ms:
- A reset, such as a battery replacement ($\overline{INIT}$ = 0)
- Any key press associated with the channel memory
- Any emergency channel switch activation
- A new channel is selected
- Leaving hold mode

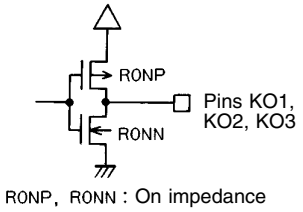
(7) Unlock Detected Output ($\overline{UL}$ pin)

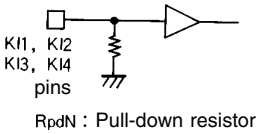
In the following cases, the $\overline{UL}$ line is asserted.
- When the phase difference between the programmable and reference divider outputs exceeds 3.2 µs, the $\overline{UL}$ line is held low for 6 ms after the last out-of-range phase sample is detected, as shown below.



- After a new transmit/receive or channel selection, the $\overline{UL}$ line is asserted for 25 ms.
- While the PA switch is turned on, the $\overline{UL}$ line is asserted during PA mode.
- The $\overline{UL}$ pin is open while the device is in the PLL LOCK state (when the phase difference is < 3.2 µs).

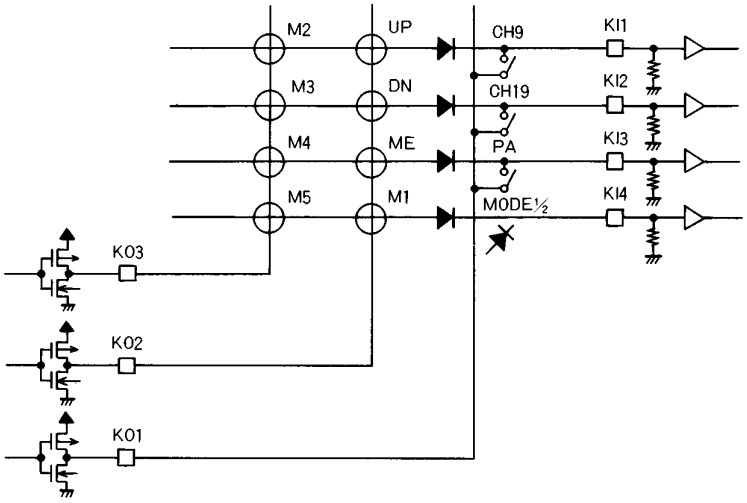
(8) Key Matrix
It is normal to put diodes in series with the key scanning lines to avoid creating a short with the output lines. But KO1, KO2 and KO3 lines (key scan signal output) do not need diodes.





unit : kΩ

Item	min	typ	max
RONP	0.5	1.0	2.0
RONN	30	50	70
RpdN	30	50	70

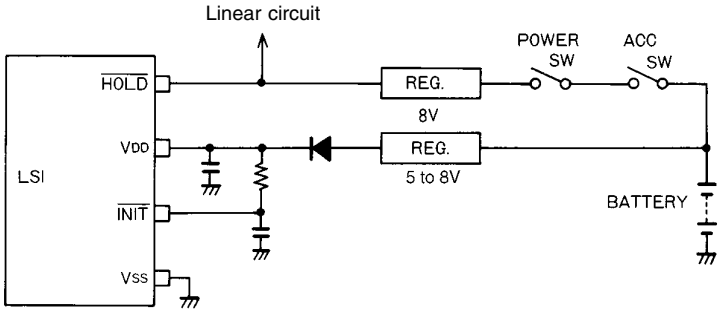


Explanation Regarding Power On and Hold Mode

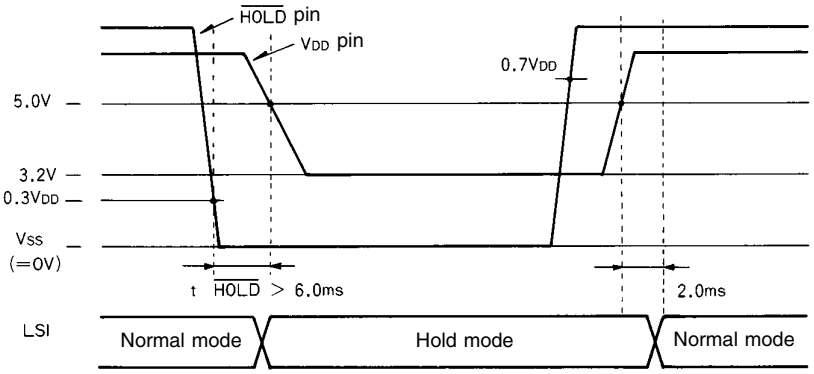
(1) Operation in hold mode
When in hold mode ($\overline{HOLD}$ = 0), the LC7185-8750 does not accept any operation other than the $\overline{INIT}$ pin being asserted (reset). The primary function of hold mode is to maintain the contents of station memory.
- In hold mode, the programmable divider, crystal oscillator and reference divider are all stopped. The PD pin (charge pump output) goes to high impedance. The $\overline{UL}$ pin goes to V_{SS}.
- The channel display pins D1 and D2 go to high impedance.
- The BEEP pin goes to V_{SS}.
- The key scan signal outputs (KO1 to KO3) go to V_{SS}.

When the LC7185-8750 leaves hold mode, the previously selected channel is reopened.

(2) Initial state settings
The LC7185-8750 can be reset to its initial state settings (reset) after the battery has been replaced, etc., by setting $\overline{INIT}$ = 0. The initial state that is established by an initial reset is as follows:
- When the V_{DD} pin turned on, CH9 or CH33 is selected.
- When the V_{DD} pin operate voltage already, CH9 is selected.
- All of station memory is set to CH33.



(3) Timing Requirements for Hold Mode

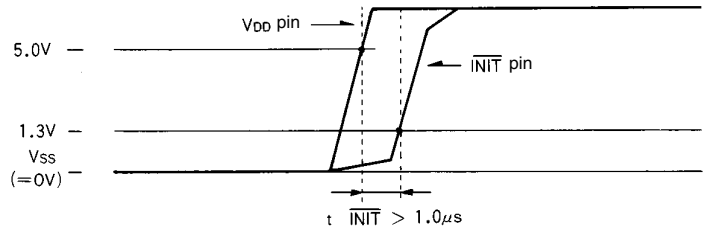


V_{DD} must remain at 5.0 V or higher (crystal oscillator requirement) for 6.0 ms (t $\overline{HOLD}$) after the $\overline{HOLD}$ line is asserted ($\overline{HOLD}$ = 0 (< 0.3 V_{DD}). After this, V_{DD} may go as low as 3.2 V.
There are no constraints on timing for the $\overline{HOLD}$ and V_{DD} pins when the chip is leaving hold mode.
The signal can be activated in one of two orders.

If $\overline{HOLD}$ is already deactivated (> 0.7 V_{DD}), the LC7185-8750 leaves hold mode within 2.0 ms after V_{DD} rises to >5.0 V.
If V_{DD} is > 5.0 V, the LC7185-8750 enters normal mode within 2.0 ms after $\overline{HOLD}$ is deactivated.

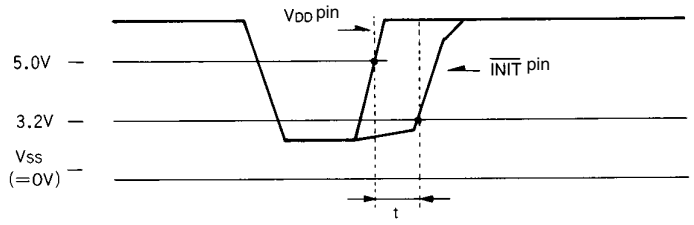
(4) Reset Timing

1. Reset timing (e.g. battery replacement)



Note: t$\overline{INIT}$ should be greater than 1.0 µs.

2. Reset caused by a sudden voltage (V_{DD}) drop



If V_{DD} drops momentarily down to less than 3.2 V and rises up to more than 5.0 V t > t$\overline{INIT}$ (t > 1.0 µs), a reset may be generated.

Frequency Table (U.S.A.: LC7185-8750)

CHANNEL	FREQUENCY (MHz)	RX ($\overline{TX}$ = 1)		TX ($\overline{TX}$ = 0)	
		N	Fvco	N	Fvco
1	26.965	6508	16.27	5393	13.4825
2	26.975	6512	16.28	5395	13.4875
3	26.985	6516	16.29	5397	13.4925
4	27.005	6524	16.31	5401	13.5025
5	27.015	6528	16.32	5403	13.5075
6	27.025	6532	16.33	5405	13.5125
7	27.035	6536	16.34	5407	13.5175
8	27.055	6544	16.36	5411	13.5275
9	27.065	6548	16.37	5413	13.5325
10	27.075	6552	16.38	5415	13.5375
11	27.085	6556	16.39	5417	13.5425
12	27.105	6564	16.41	5421	13.5525
13	27.115	6568	16.42	5423	13.5575
14	27.125	6572	16.43	5425	13.5625
15	27.135	6576	16.44	5427	13.5675
16	27.155	6584	16.46	5431	13.5775
17	27.165	6588	16.47	5433	13.5825
18	27.175	6592	16.48	5435	13.5875
19	27.185	6596	16.49	5437	13.5925
20	27.205	6604	16.51	5441	13.6025
21	27.215	6608	16.52	5443	13.6075
22	27.225	6612	16.53	5445	13.6125
23	27.255	6624	16.56	5451	13.6275
24	27.235	6616	16.54	5447	13.6175
25	27.245	6620	16.55	5449	13.6225
26	27.265	6628	16.57	5453	13.6325
27	27.275	6632	16.58	5455	13.6375
28	27.285	6636	16.59	5457	13.6425
29	27.295	6640	16.60	5459	13.6475
30	27.305	6644	16.61	5461	13.6525
31	27.315	6648	16.62	5463	13.6575
32	27.325	6652	16.63	5465	13.6625
33	27.335	6656	16.64	5467	13.6675
34	27.345	6660	16.65	5469	13.6725
35	27.355	6664	16.66	5471	13.6775
36	27.365	6668	16.67	5473	13.6825
37	27.375	6672	16.68	5475	13.6875
38	27.385	6676	16.69	5477	13.6925
39	27.395	6680	16.70	5479	13.6975
40	27.405	6684	16.71	5481	13.7025

V_{CO} (TX) = RF ÷ 2
V_{CO} (RX) = RF – 10.695 MHz (IF)
CH1: V_{CO} (TX) = 26.965 ÷ 2 = 13.4825
V_{CO} (RX) = 26.965 – 10.965 = 16.27

Sample Application Circuit