International **IOR** Rectifier

AUTOMOTIVE MOSFET

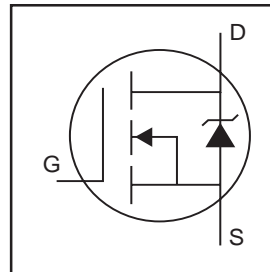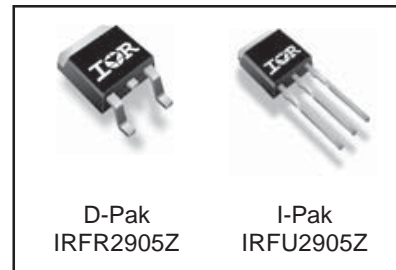# IRFR2905Z
IRFU2905Z

HEXFET® Power MOSFET

Features
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

$V_{DSS} = 55V$

$R_{DS(on)} = 14.5m\Omega$

$I_D = 42A$

Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

D-Pak
IRFR2905Z

I-Pak
IRFU2905Z

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	59	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	42	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	42	
I_{DM}	Pulsed Drain Current ①	240	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.72	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS (Thermally limited)}$	Single Pulse Avalanche Energy②	55	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	82	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

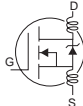|	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	1.38	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ⑦ ⑧	——	40	
$R_{\theta JA}$	Junction-to-Ambient ⑧	——	110	

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IRFR/U2905Z

Electrical Characteristics @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V$_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔV$_{(BR)DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.053	——	V/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	11.1	14.5	mΩ	V$_{GS}$ = 10V, I$_D$ = 36A ③
V$_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA
gfs	Forward Transconductance	20	——	——	S	V$_{DS}$ = 25V, I$_D$ = 36A
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	20	µA	V$_{DS}$ = 55V, V$_{GS}$ = 0V
		——	——	250		V$_{DS}$ = 55V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	200	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V$_{GS}$ = -20V
Q$_g$	Total Gate Charge	——	29	44		I$_D$ = 36A
Q$_{gs}$	Gate-to-Source Charge	——	7.7	——	nC	V$_{DS}$ = 44V
Q$_{gd}$	Gate-to-Drain ("Miller") Charge	——	12	——		V$_{GS}$ = 10V ③
R$_G$	Gate Input Resistance	——	1.3	——	Ω	f = 1MHz, open drain
t$_{d(on)}$	Turn-On Delay Time	——	14	——		V$_{DD}$ = 28V
t$_r$	Rise Time	——	66	——		I$_D$ = 36A
t$_{d(off)}$	Turn-Off Delay Time	——	31	——	ns	R$_G$ = 15 Ω
t$_f$	Fall Time	——	35	——		V$_{GS}$ = 10V ③
L$_D$	Internal Drain Inductance	——	4.5	——		Between lead,
					nH	6mm (0.25in.)
L$_S$	Internal Source Inductance	——	7.5	——		from package
						and center of die contact
C$_{iss}$	Input Capacitance	——	1380	——		V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	240	——		V$_{DS}$ = 25V
C$_{rss}$	Reverse Transfer Capacitance	——	120	——	pF	f = 1.0MHz
C$_{oss}$	Output Capacitance	——	820	——		V$_{GS}$ = 0V, V$_{DS}$ = 1.0V, f = 1.0MHz
C$_{oss}$	Output Capacitance	——	190	——		V$_{GS}$ = 0V, V$_{DS}$ = 44V, f = 1.0MHz
C$_{oss}$ eff.	Effective Output Capacitance	——	300	——		V$_{GS}$ = 0V, V$_{DS}$ = 0V to 44V ④

Source-Drain Ratings and Characteristics

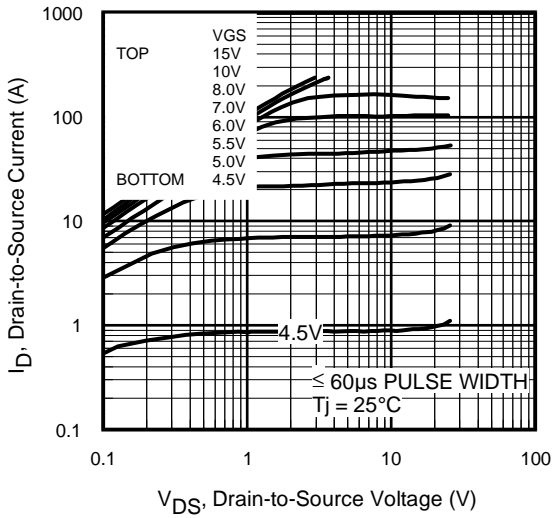|	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	36	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	240		
V$_{SD}$	Diode Forward Voltage	——	——	1.3	V	T$_J$ = 25°C, I$_S$ = 36A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	——	23	35	ns	T$_J$ = 25°C, I$_F$ = 36A, V$_{DD}$ = 28V
Q$_{rr}$	Reverse Recovery Charge	——	16	24	nC	di/dt = 100A/µs ③
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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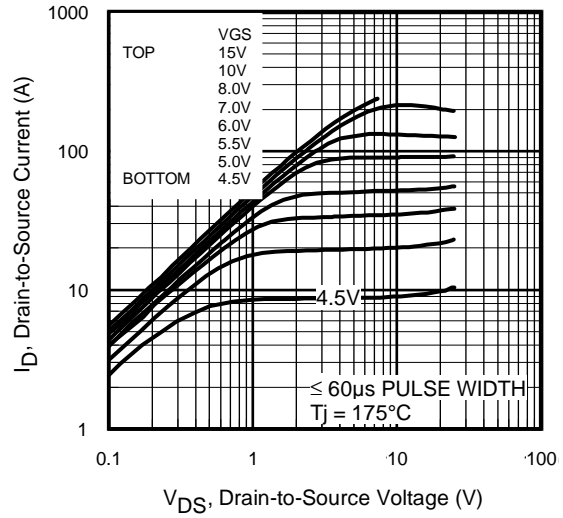
Fig 1. Typical Output Characteristics

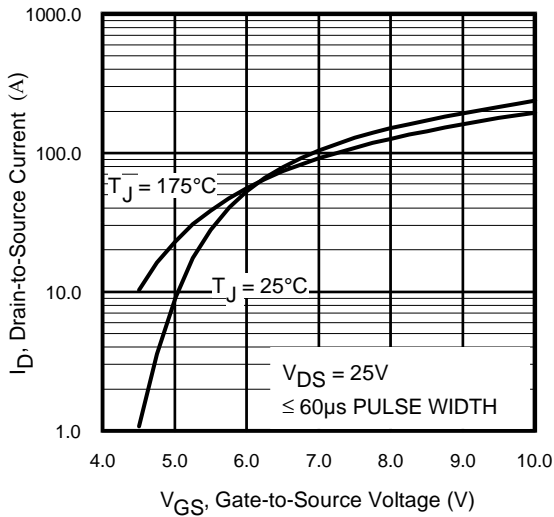**Fig 2.** Typical Output Characteristics

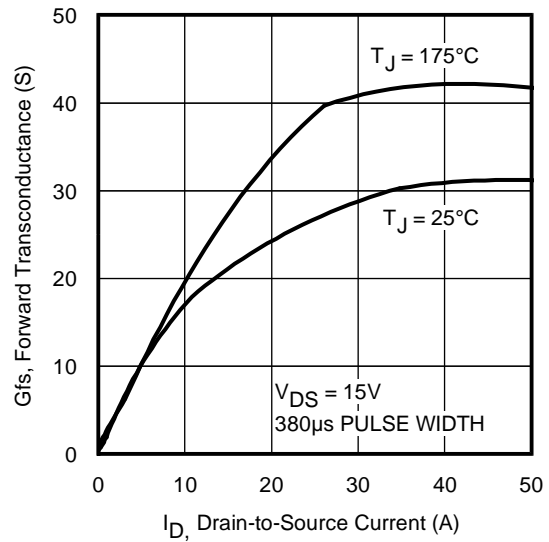**Fig 3.** Typical Transfer Characteristics

Fig 4. Typical Forward Transconductance Vs. Drain Current
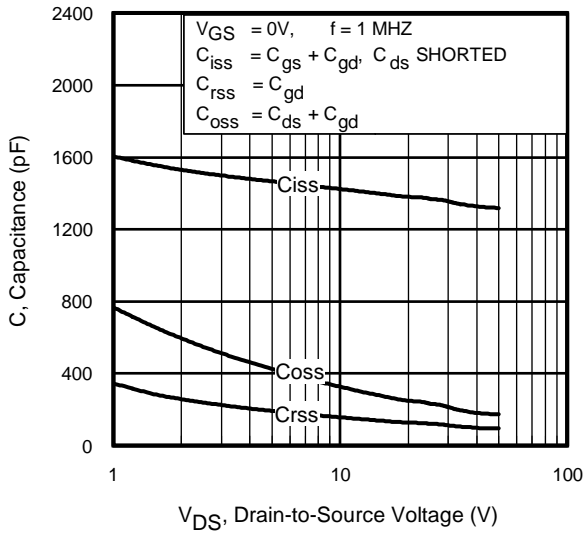
IRFR/U2905Z

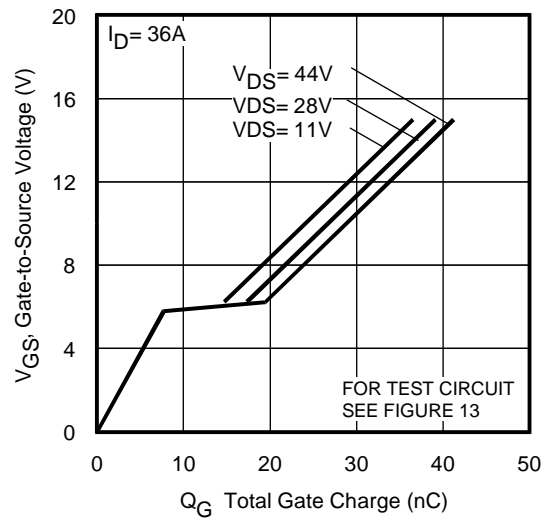**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

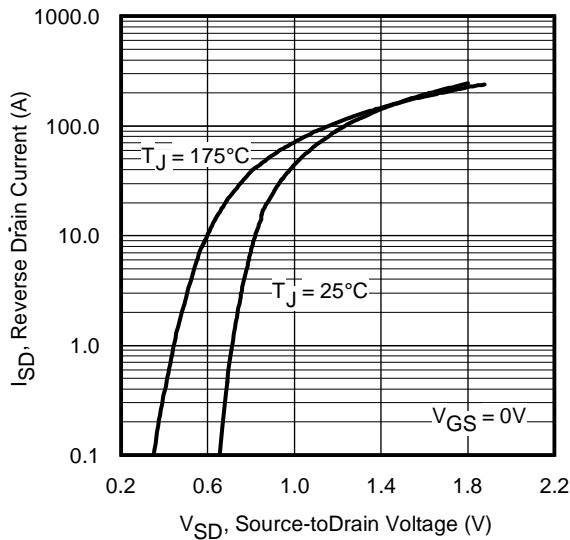**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

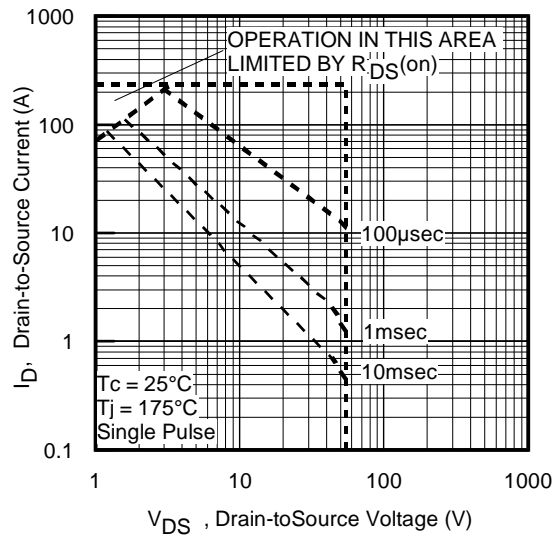**Fig 7.** Typical Source-Drain Diode Forward Voltage
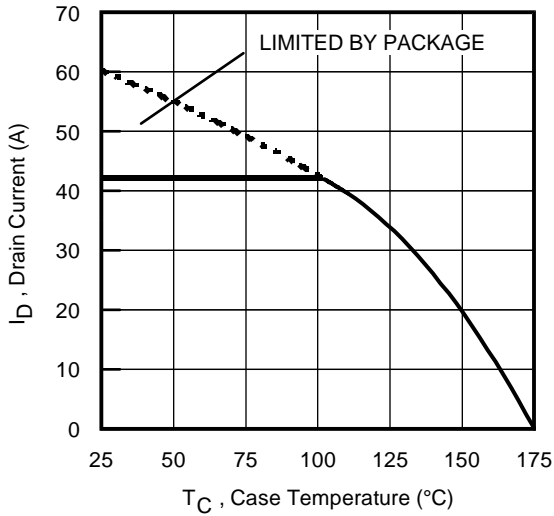

Fig 8. Maximum Safe Operating Area

4

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Fig 9. Maximum Drain Current Vs.
Case Temperature

Fig 10. Normalized On-Resistance
Vs. Temperature

Ri (°C/W)	τi (sec)
0.3962	0.00012
0.5693	0.00045
0.4129	0.0015

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

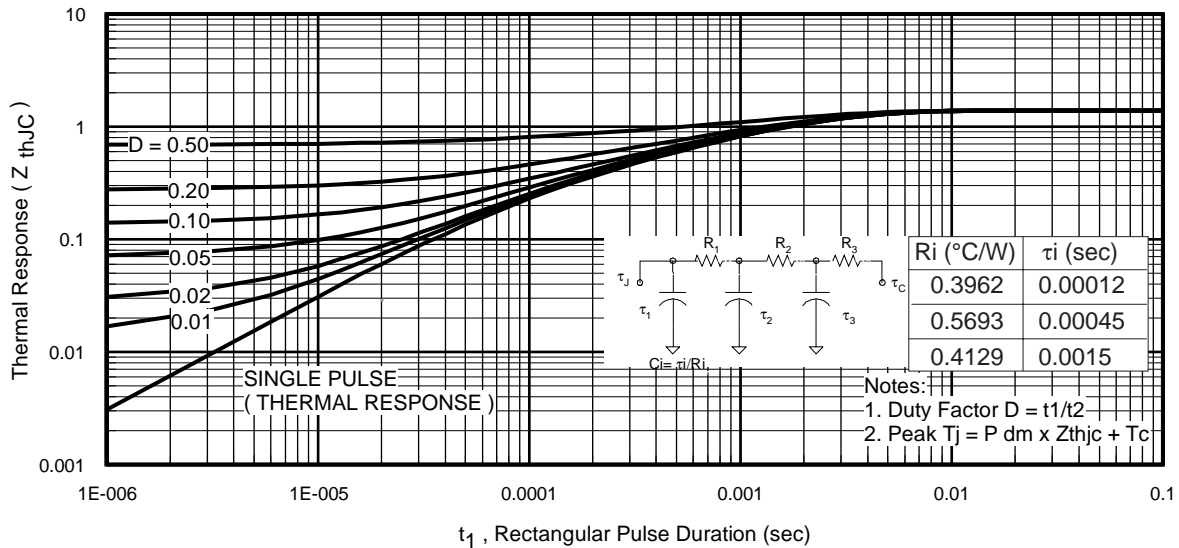**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

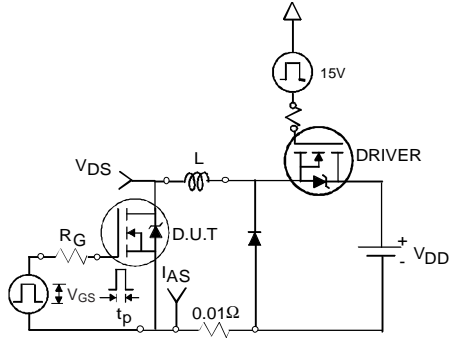# IRFR/U2905Z

Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

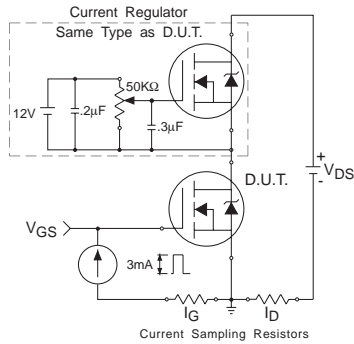**Fig 13a.** Basic Gate Charge Waveform

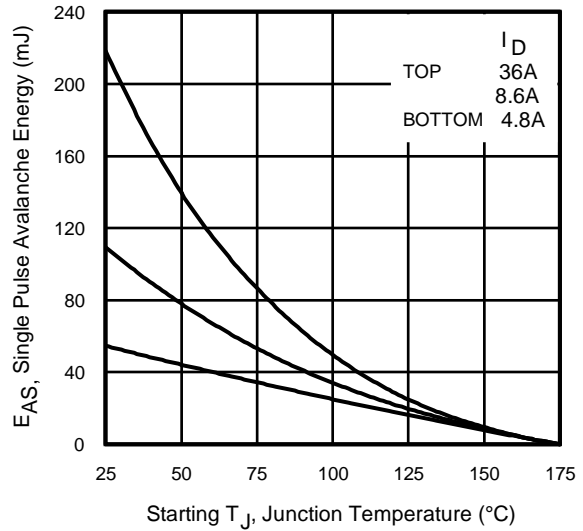**Fig 13b.** Gate Charge Test Circuit

6

Fig 12c. Maximum Avalanche Energy
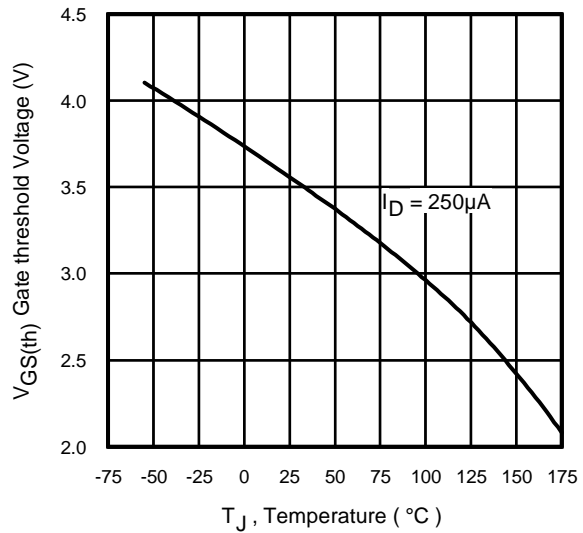Vs. Drain Current

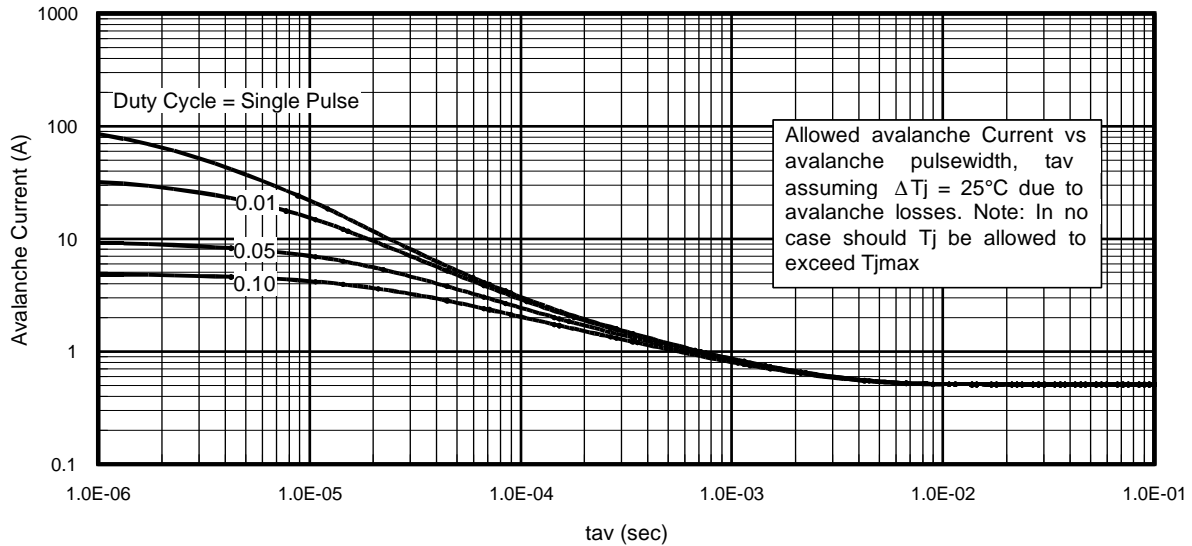**Fig 14.** Threshold Voltage Vs. Temperature
www.irf.com

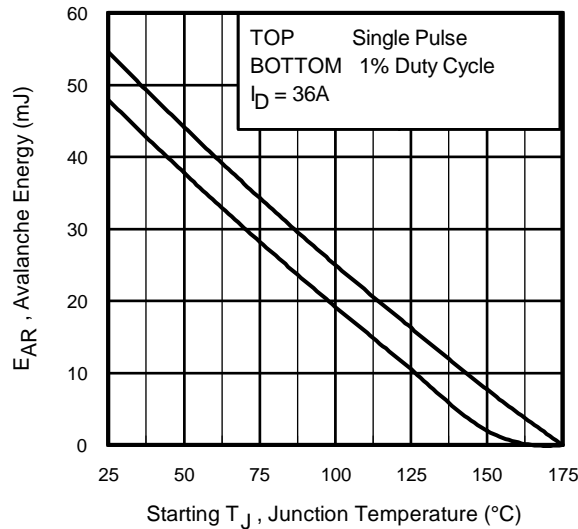**Fig 15.** Typical Avalanche Current Vs.Pulsewidth

Fig 16. Maximum Avalanche Energy
Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

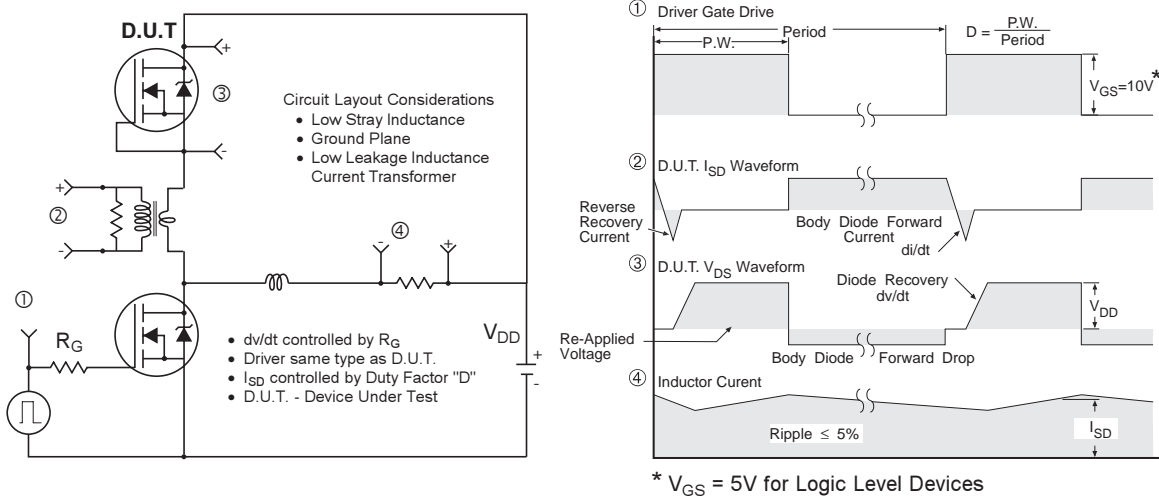# IRFR/U2905Z

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET® Power MOSFETs
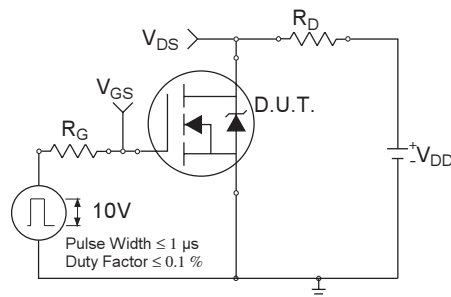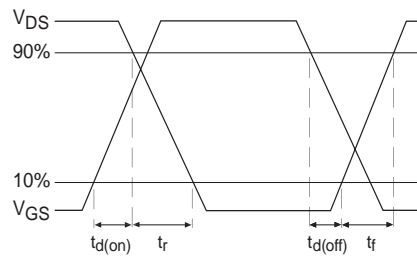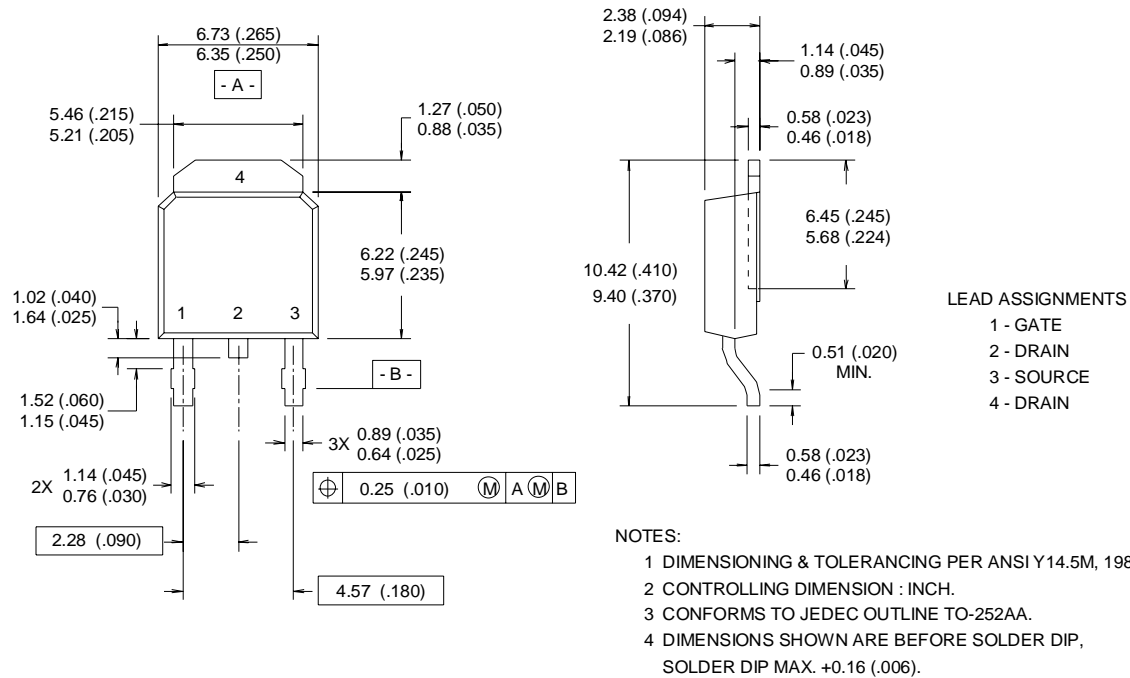

Fig 18a. Switching Time Test Circuit

Fig 18b. Switching Time Waveforms

8

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

6.73 (.265)
6.35 (.250)

- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

6.22 (.245)
5.97 (.235)

1.02 (.040)
1.64 (.025)

1   2   3

- B -

1.52 (.060)
1.15 (.045)

3X 0.89 (.035)
0.64 (.025)

2X 1.14 (.045)
0.76 (.030)

⊕ 0.25 (.010) Ⓜ A Ⓜ B

2.28 (.090)

4.57 (.180)

2.38 (.094)
2.19 (.086)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

10.42 (.410)
9.40 (.370)

0.51 (.020)
MIN.

0.58 (.023)
0.46 (.018)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
  SOLDER DIP MAX. +0.16 (.006).

D-Pak (TO-252AA) Part Marking Information

Notes : This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 9U1P

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
IGR 016
9U   1P

DATE CODE
YEAR = 0
WEEK = 16

ASSEMBLY
LOT CODE

Notes : This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 1234
          ASSEMBLED ON WW 16, 1999
          IN THE ASSEMBLY LINE "A"

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

IRFU120
IGR 916A
12   34

DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A

ASSEMBLY
LOT CODE

IRFR/U2905Z

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

6.73 (.265)
6.35 (.250)
- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

1.52 (.060)
1.15 (.045)

6.22 (.245)
5.97 (.235)

1   2   3

- B -

2.28 (.090)
1.91 (.075)

9.65 (.380)
8.89 (.350)

3X 1.14 (.045)
    0.76 (.030)

3X 0.89 (.035)
    0.64 (.025)

2.28 (.090)
2X

⊕ 0.25 (.010) Ⓜ A Ⓜ B

2.38 (.094)
2.19 (.086)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
   SOLDER DIP MAX. +0.16 (.006).

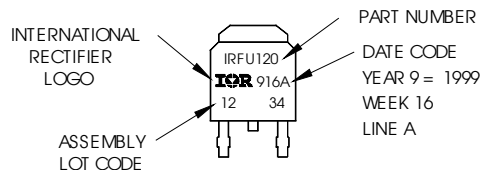## I-Pak (TO-251AA) Part Marking Information

Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 9U1P

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
IOR 016
9U   1P

DATE CODE
YEAR = 0
WEEK = 16

ASSEMBLY
LOT CODE

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 5678
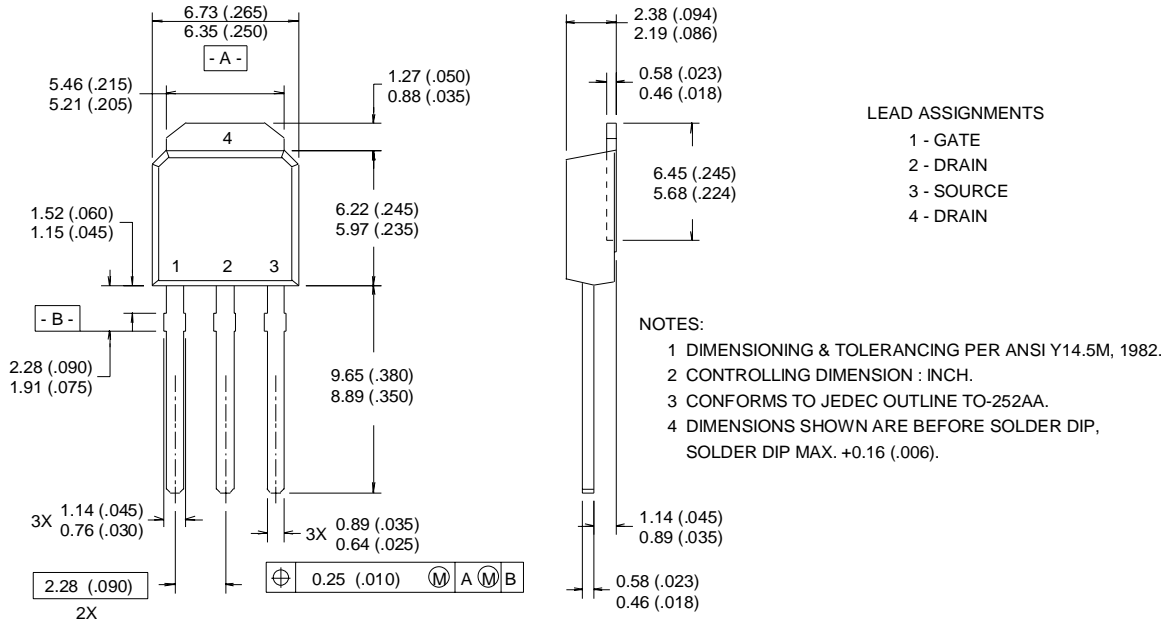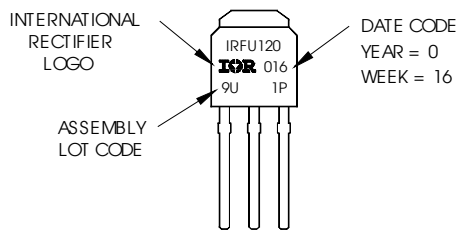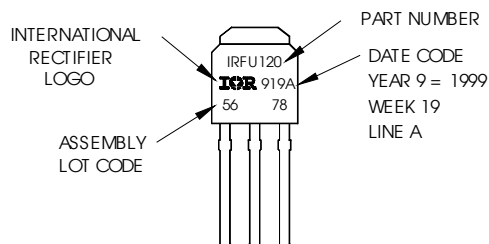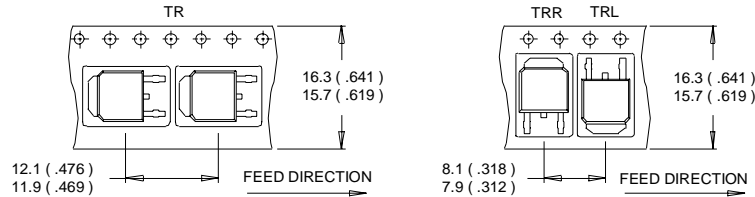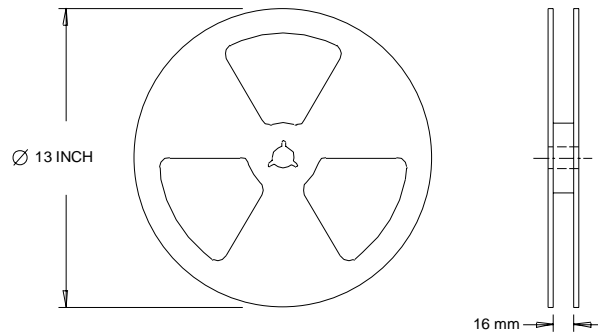   ASSEMBLED ON WW 19, 1999
          IN THE ASSEMBLY LINE "A"

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

IRFU120
IOR 919A
56   78

DATE CODE
YEAR 9 = 1999
WEEK 19
LINE A

ASSEMBLY
LOT CODE

10

www.irf.com

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)

TR

16.3 (.641)
15.7 (.619)

12.1 (.476)
11.9 (.469)

FEED DIRECTION

TRR   TRL

16.3 (.641)
15.7 (.619)

8.1 (.318)
7.9 (.312)

FEED DIRECTION

NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

⌀ 13 INCH

16 mm

NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting $T_J = 25°C$, L = 0.08mH $R_G = 25\Omega$, $I_{AS} = 36A$, $V_{GS} = 10V$. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994

⑧ R_θ is measured at T_J approximately 90°C

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International IΩR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.11/03

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/