

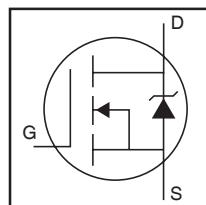
**IRFB4310**  
**IRFS4310**  
**IRFSL4310**

### Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

### Benefits

- Worldwide Best  $R_{DS(on)}$  in TO-220
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and di/dt Capability



HEXFET® Power MOSFET

$V_{DSS}$	<b>100V</b>
$R_{DS(on)}$ typ.	<b>5.6mΩ</b>
max.	<b>7.0mΩ</b>
$I_D$	<b>140A</b>



### Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	140①	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	97 ①	
$I_{DM}$	Pulsed Drain Current ②	550	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	330	W
	Linear Derating Factor	2.2	W/ $^\circ C$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
dV/dt	Peak Diode Recovery ④	14	V/ns
$T_J$	Operating Junction and	-55 to + 175	$^\circ C$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb-in (1.1N·m)	

### Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	980	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		

### Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	—	0.45	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface , TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑨	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D <sup>2</sup> Pak ⑧⑨	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.064	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$ ②
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	5.6	7.0	$\text{m}\Omega$	$V_{GS} = 10V, I_D = 75\text{A}$ ⑤
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{DS} = 100\text{V}, V_{GS} = 0V$
		—	—	250	—	$V_{DS} = 100\text{V}, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200	—	$V_{GS} = -20V$
$R_G$	Gate Input Resistance	—	1.4	—	$\Omega$	$f = 1\text{MHz}$ , open drain

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

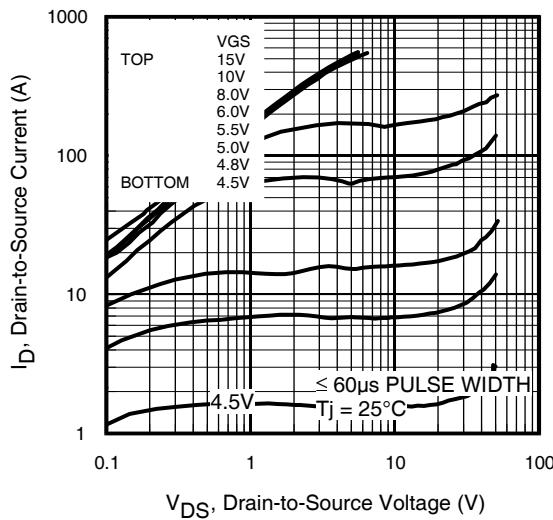
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	160	—	—	S	$V_{DS} = 50\text{V}, I_D = 75\text{A}$
$Q_g$	Total Gate Charge	—	170	250	nC	$I_D = 75\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	46	—	—	$V_{DS} = 80\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	62	—	—	$V_{GS} = 10V$ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	$V_{DD} = 65\text{V}$
$t_r$	Rise Time	—	110	—	—	$I_D = 75\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	68	—	—	$R_G = 2.6\Omega$
$t_f$	Fall Time	—	78	—	—	$V_{GS} = 10V$ ⑤
$C_{iss}$	Input Capacitance	—	7670	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	540	—	—	$V_{DS} = 50\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	280	—	—	$f = 1.0\text{MHz}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)⑦	—	650	—	—	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80\text{V}$ ⑧, See Fig.11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑥	—	720.1	—	—	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80\text{V}$ ⑥, See Fig. 5

**Diode Characteristics**

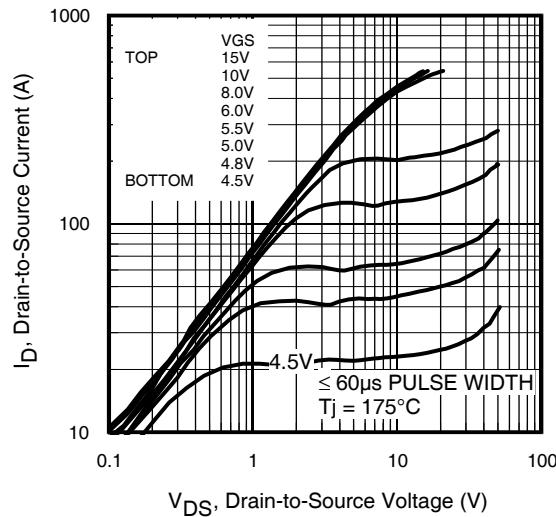
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current (Body Diode)	—	—	140①	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ②⑦	—	—	550	—	—
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_s = 75\text{A}, V_{GS} = 0V$ ⑤
$t_{rr}$	Reverse Recovery Time	—	45	68	ns	$T_J = 25^\circ\text{C} \quad V_R = 85\text{V},$
		—	55	83	—	$T_J = 125^\circ\text{C} \quad I_F = 75\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	82	120	nC	$T_J = 25^\circ\text{C} \quad \text{di/dt} = 100\text{A}/\mu\text{s}$ ⑤
		—	120	180	—	$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	3.3	—	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

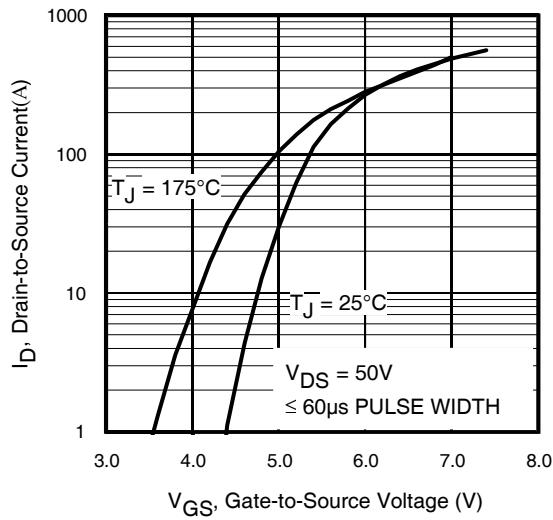
- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{J\text{max}}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.35\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 75\text{A}$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ④  $I_{SD} \leq 75\text{A}$ ,  $\text{di/dt} \leq 550\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss \text{ eff. (TR)}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$



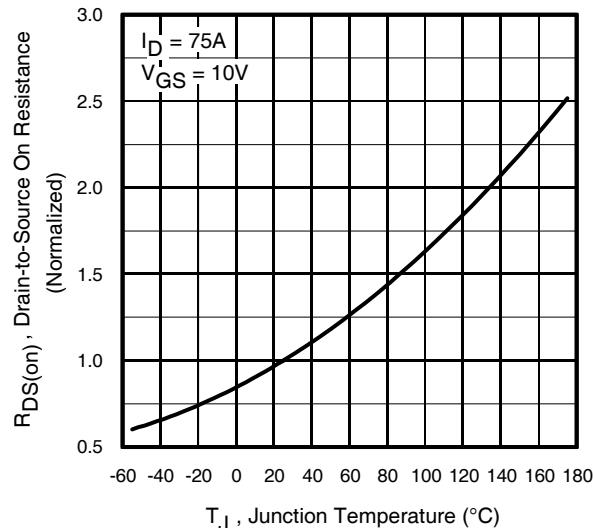
**Fig 1.** Typical Output Characteristics



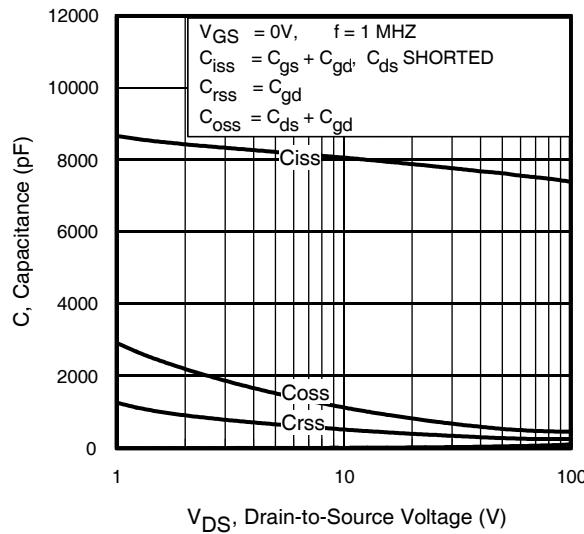
**Fig 2.** Typical Output Characteristics



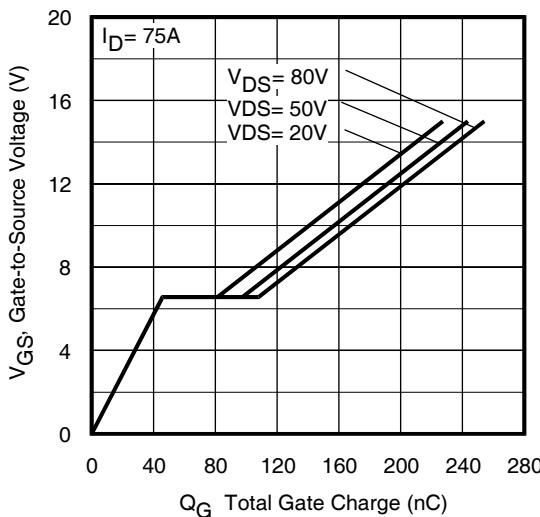
**Fig 3.** Typical Transfer Characteristics



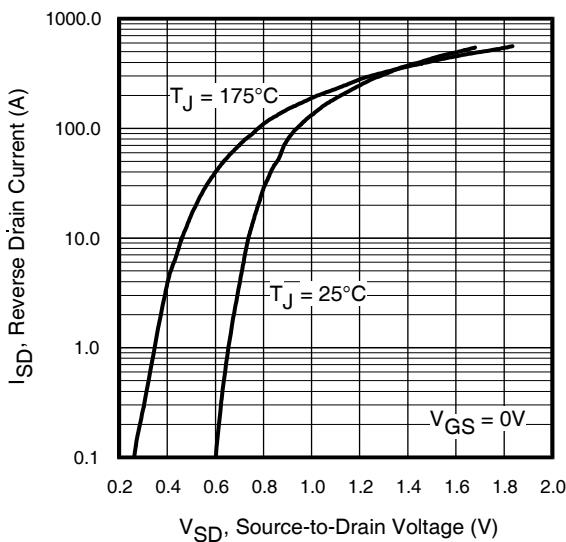
**Fig 4.** Normalized On-Resistance vs. Temperature



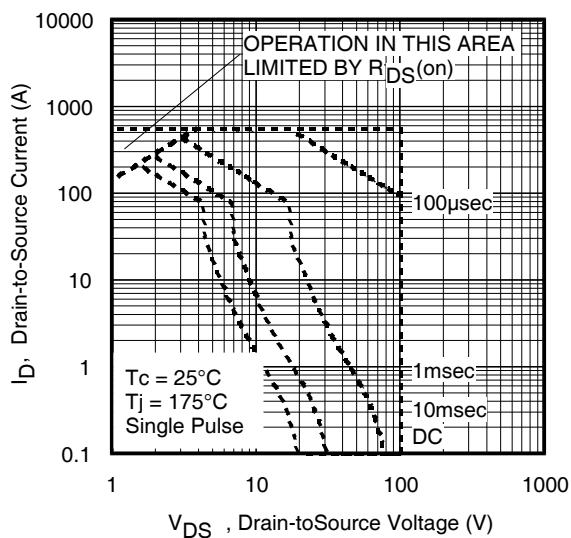
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



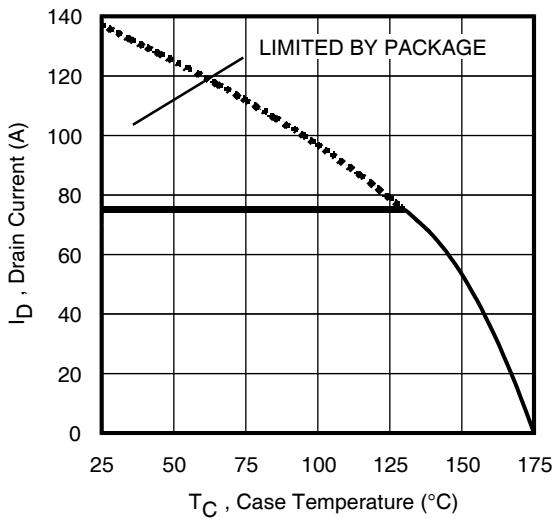
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



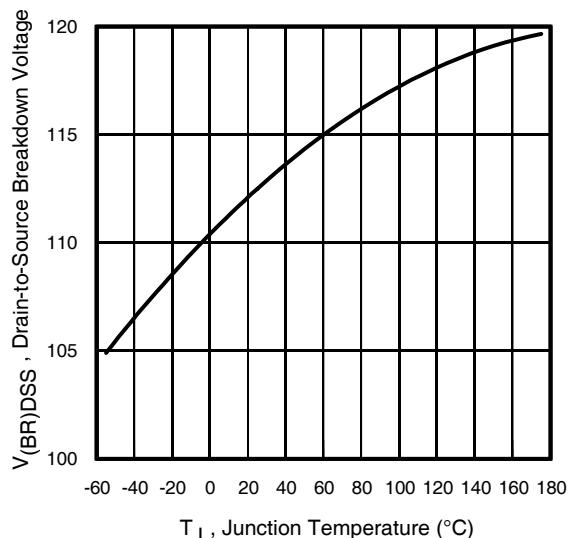
**Fig 7.** Typical Source-Drain Diode Forward Voltage



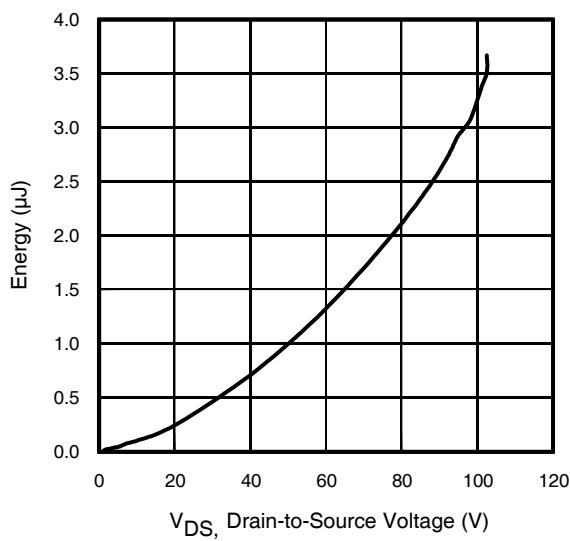
**Fig 8.** Maximum Safe Operating Area



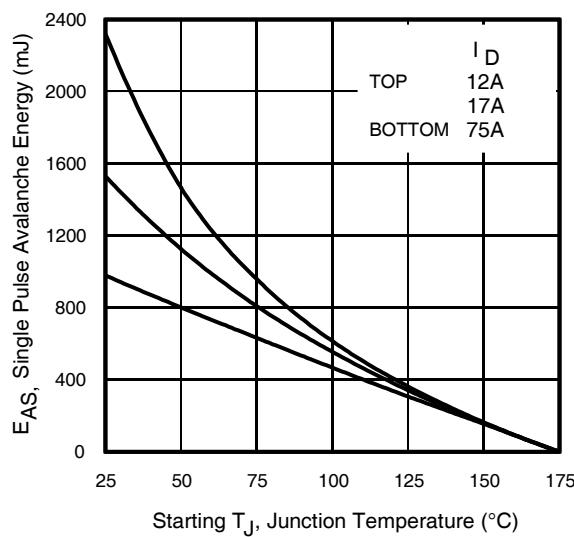
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{oss}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy Vs. DrainCurrent

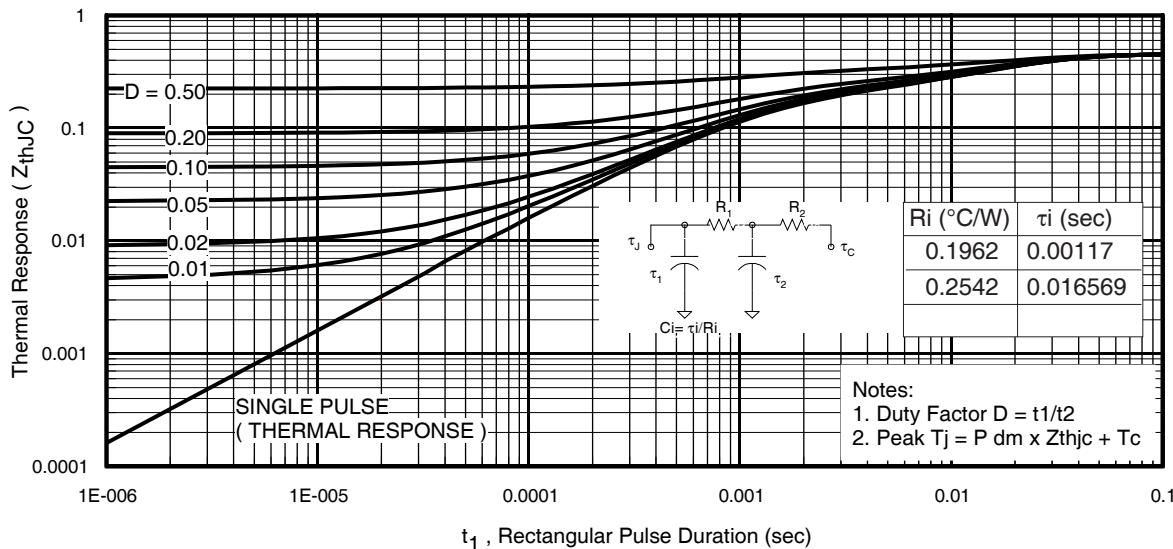


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

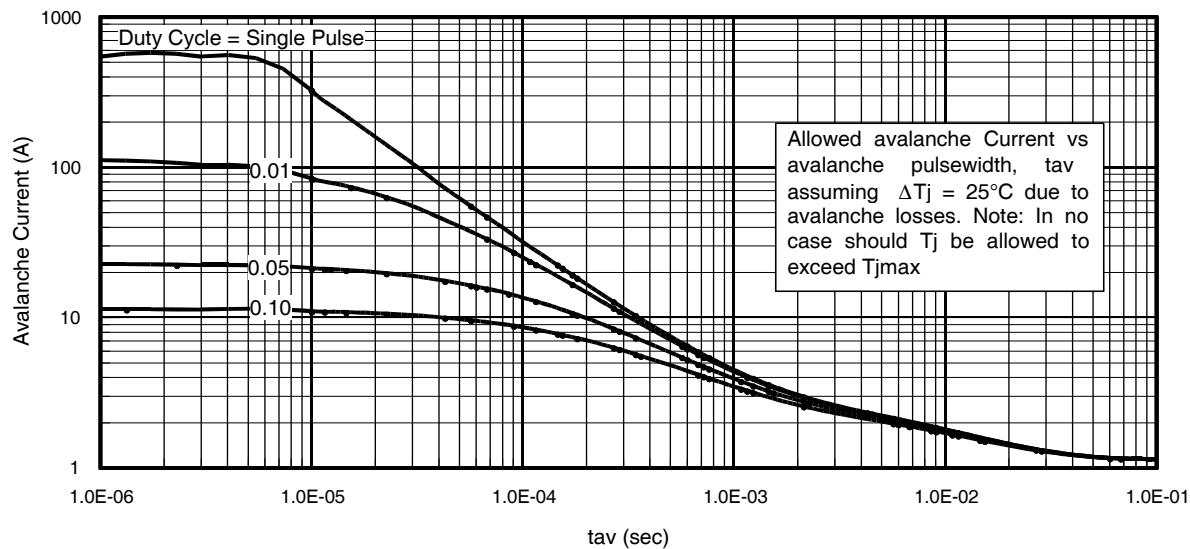


Fig 14. Typical Avalanche Current vs.Pulsewidth

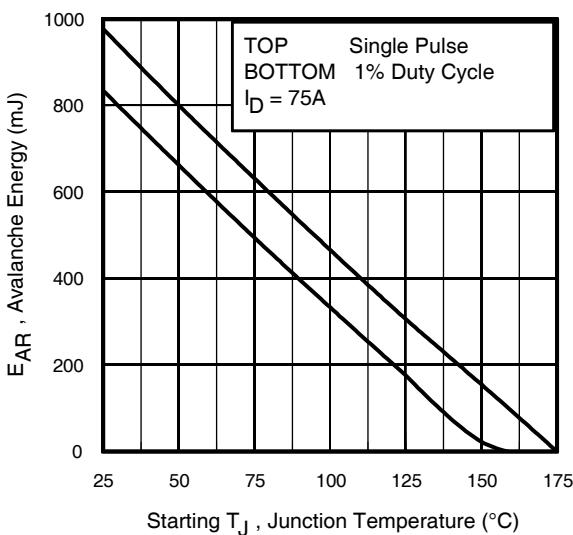


Fig 15. Maximum Avalanche Energy vs. Temperature

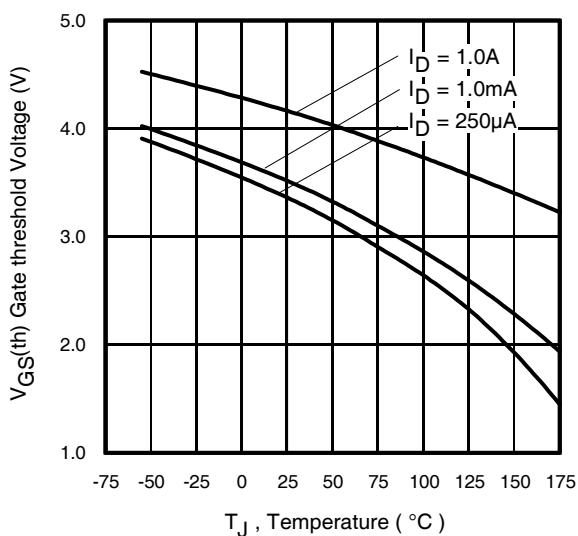
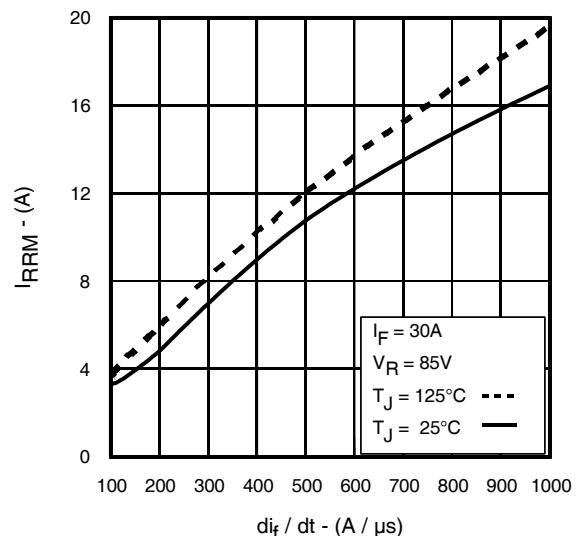
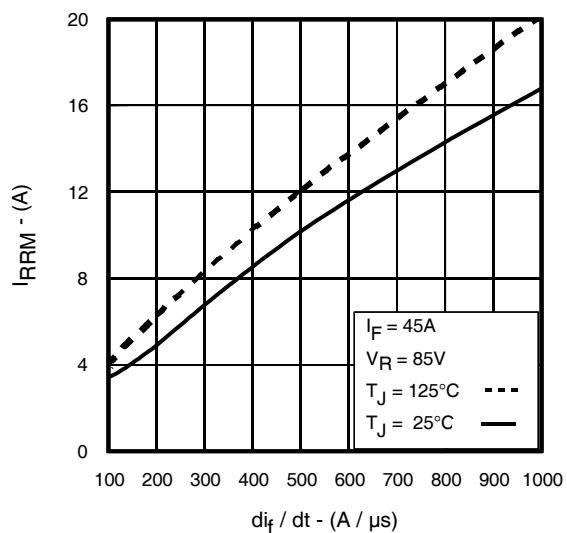
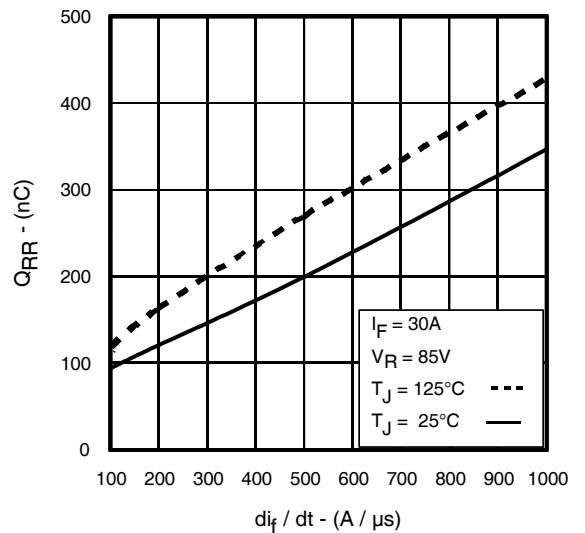
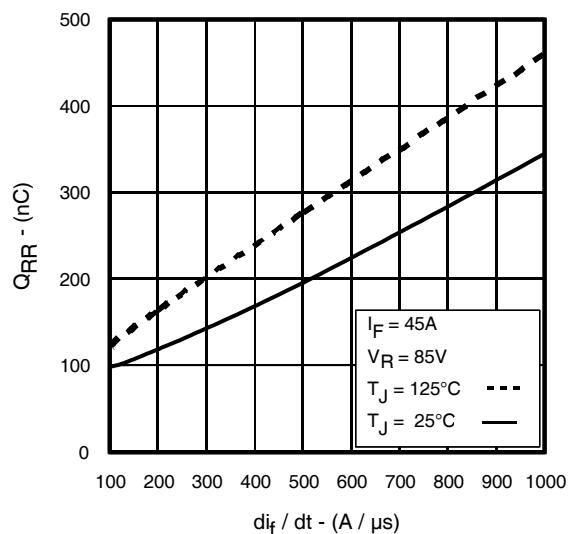
Notes on Repetitive Avalanche Curves , Figures 14, 15:  
 (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

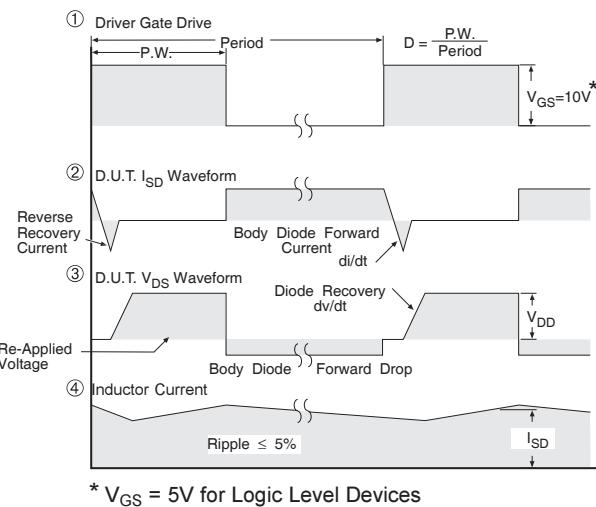
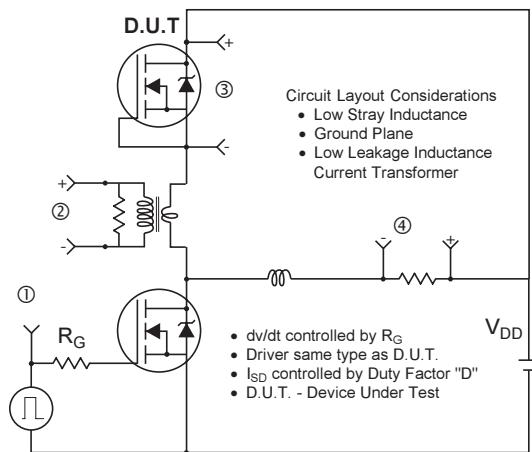
1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
  2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
  3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
  4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
  5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
  6.  $I_{av}$  = Allowable avalanche current.
  7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ C$  in Figure 14, 15).
- $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

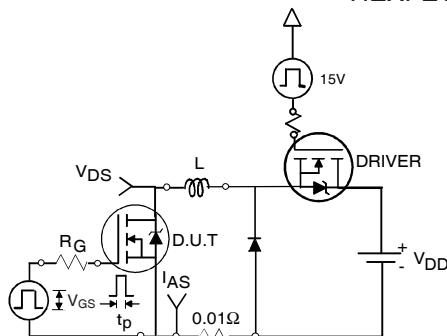
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

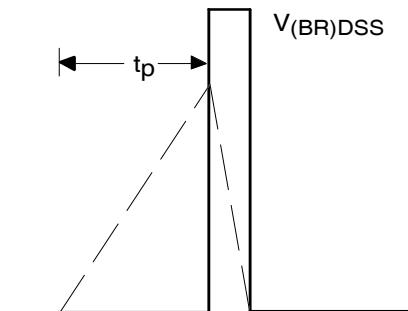
**Fig. 16.** Threshold Voltage Vs. Temperature**Fig. 17 -** Typical Recovery Current vs.  $di_f/dt$ **Fig. 18 -** Typical Recovery Current vs.  $di_f/dt$ **Fig. 19 -** Typical Stored Charge vs.  $di_f/dt$ **Fig. 20 -** Typical Stored Charge vs.  $di_f/dt$



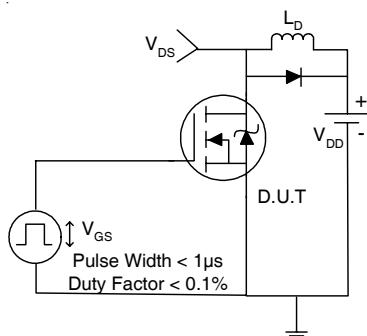
**Fig 21.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



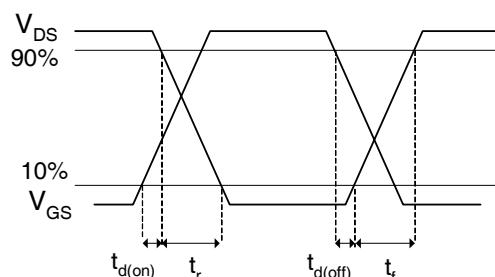
**Fig 22a.** Unclamped Inductive Test Circuit



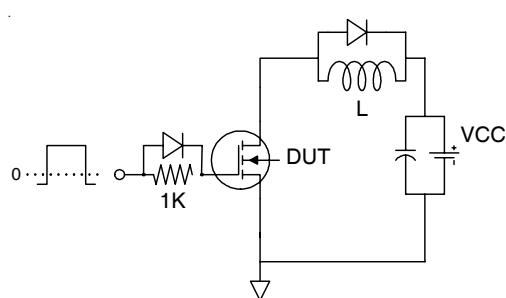
**Fig 22b.** Unclamped Inductive Waveforms



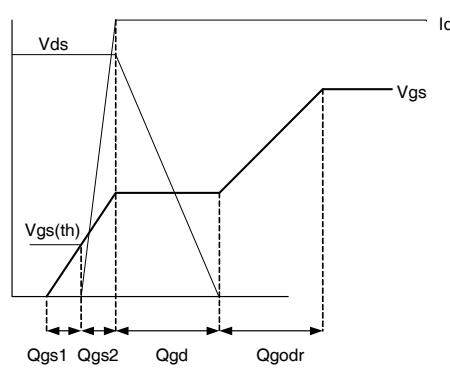
**Fig 23a.** Switching Time Test Circuit



**Fig 23b.** Switching Time Waveforms



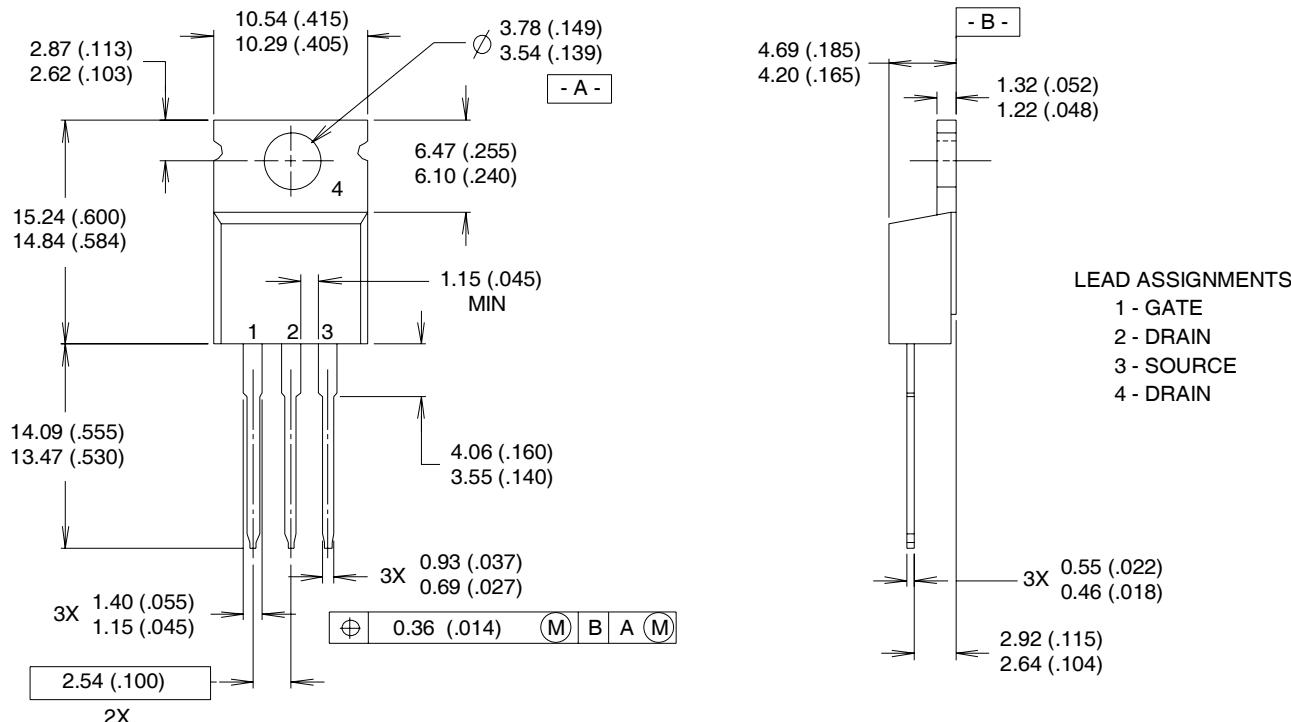
**Fig 24a.** Gate Charge Test Circuit  
[www.irf.com](http://www.irf.com)



**Fig 24b.** Gate Charge Waveform

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



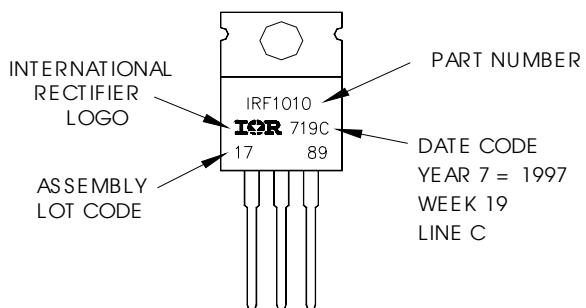
## NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

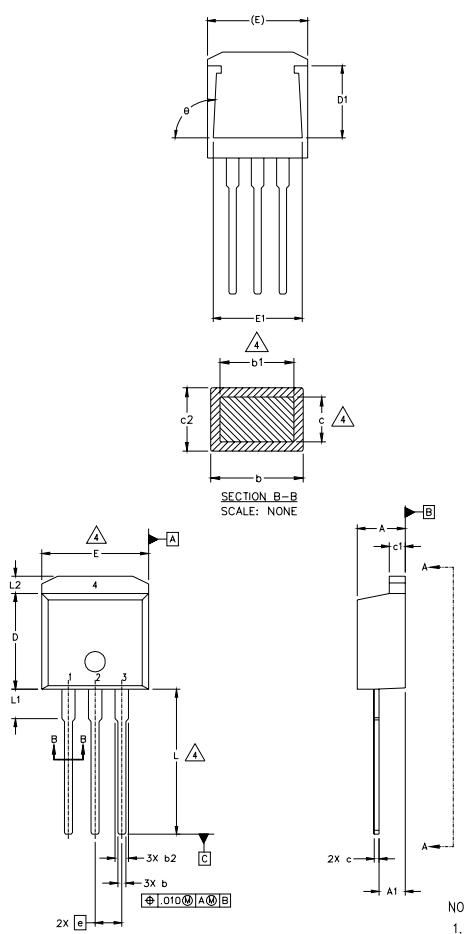
## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



TO-220AB packages are not recommended for Surface Mount Application.

## TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	2.03	2.92	.080	.115		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035	4	
b2	1.14	1.40	.045	.055		
c	0.38	0.63	.015	.025	4	
c1	1.14	1.40	.045	.055		
c2	0.43	.063	.017	.029		
D	8.51	9.65	.335	.380	3	
D1	5.33		.210			
E	9.65	10.67	.380	.420	3	
E1	6.22		.245			
e	2.54	BSC	.100	BSC		
L	13.46	14.09	.530	.555		
L1	3.56	3.71	.140	.146		
L2		1.65		.065		

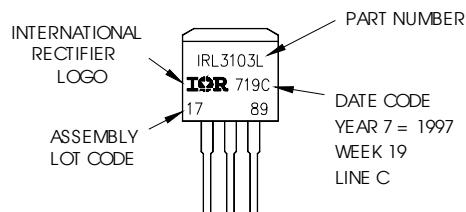
### LEAD ASSIGNMENTS

HEXFET	IGBT
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- Emitter
4- DRAIN	4- COLLECTOR

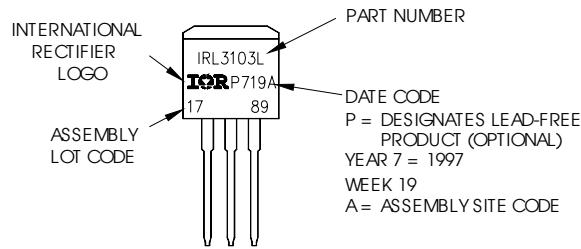
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

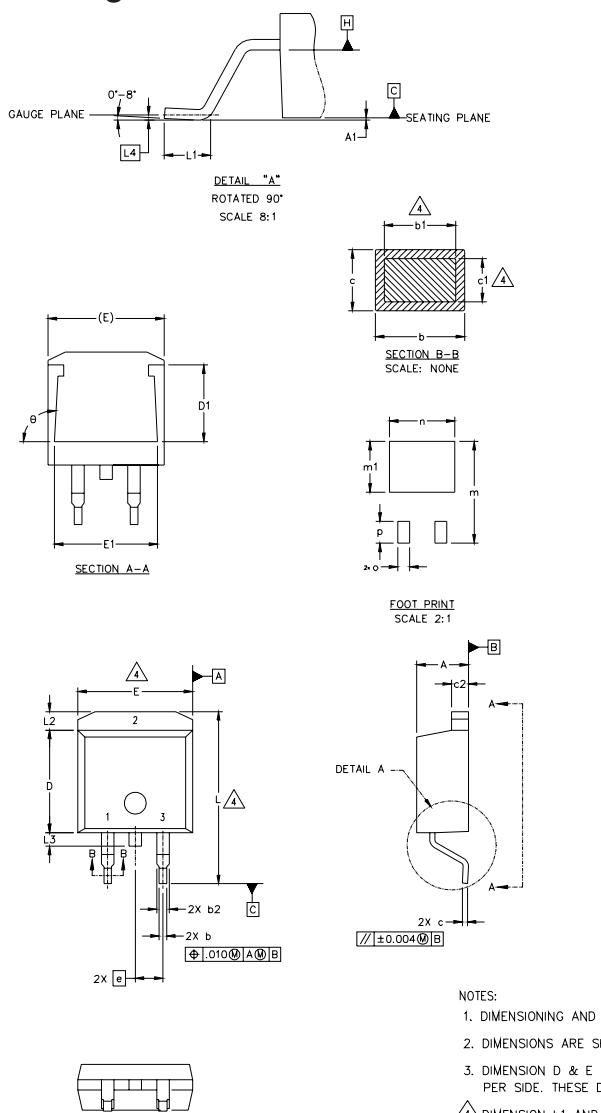
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
 Note: "P" in assembly line position indicates "Lead-Free"



OR



D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1		0.127		.005		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035	4	
b2	1.14	1.40	.045	.055		
c	0.43	0.63	.017	.025		
c1	0.38	0.74	.015	.029	4	
c2	1.14	1.40	.045	.055		
D	8.51	9.65	.335	.380	3	
D1	5.33		.210			
E	9.65	10.67	.380	.420	3	
E1	6.22		.245			
e	2.54	BSC	.100	BSC		
L	14.61	15.88	.575	.625		
L1	1.78	2.79	.070	.110		
L2		1.65		.065		
L3	1.27	1.78	.050	.070		
L4	0.25	BSC	.010	BSC		
m	17.78		.700			
m1	8.89		.350			
n	11.43		.450			
o	2.08		.082			
p	3.81		.150			
θ	90°	93°	90°	93°		

## LEAD ASSIGNMENTS

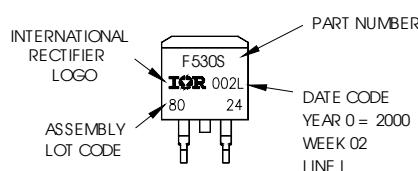
HEXFET	IGBTs_CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- Emitter	3.- ANODE

\* PART DEPENDENT.

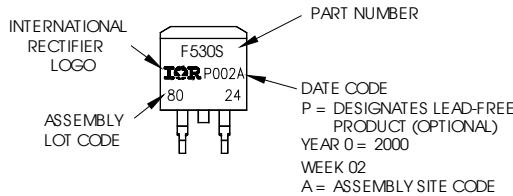
D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

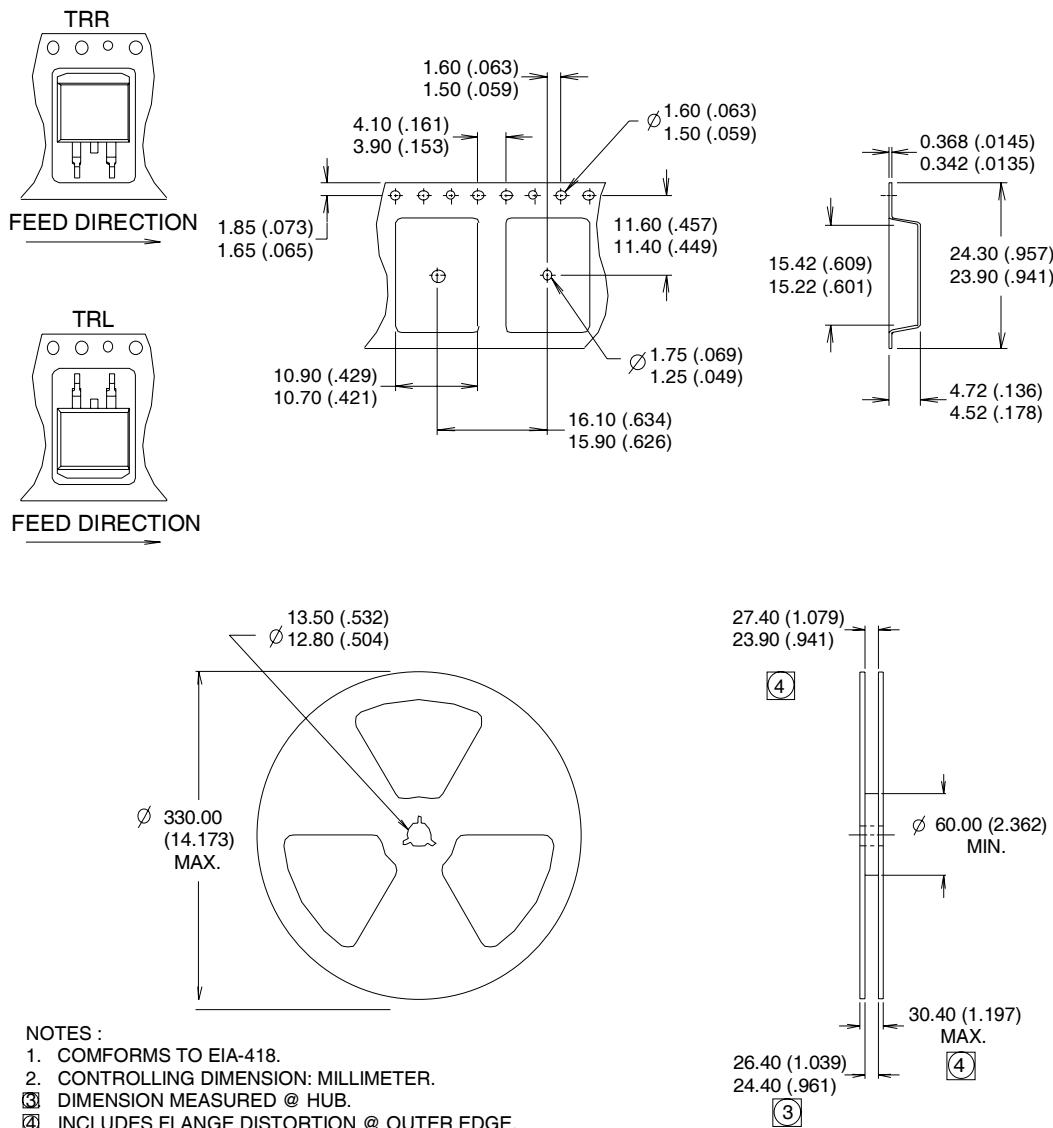
Note: "P" in assembly line  
position indicates "Lead-Free"



OR



## D<sup>2</sup>Pak Tape & Reel Information



Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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