

# FAN7310

## LCD Backlight Inverter Drive Integrated Circuit

### Features

- High-Efficiency, Single-Stage Power Conversion
- Wide Input Voltage Range: 5V to 24V
- Backlight Lamp Ballast and Soft Dimming
- Reduce External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS full-bridge topology
- Soft-Start Feature
- PWM Control at Fixed Frequency
- Analog and Burst Dimming Function
- Synchronizable Switching Frequency with External Signal
- Open-Lamp Protection
- Open-Lamp Regulation
- 20-Pin SSOP

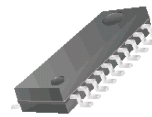
### Applications

- LCD TV
- LCD Monitor

### Description

The FAN7310 provides all the control functions for a series parallel resonant converter and contains a pulse width modulation (PWM) controller to develop a supply voltage. Typical operating frequency range is between 30kHz and 250kHz, depending on the CCFL and the transformer's characteristics. The FAN7310 has a patent-pending on phase-shift control.

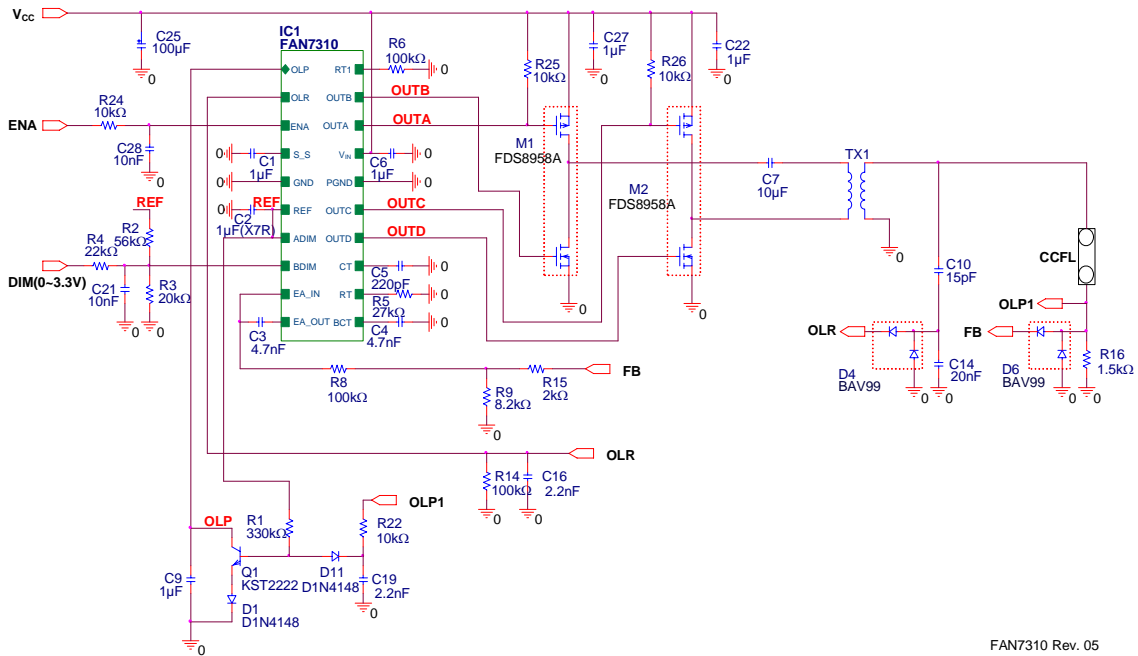
20-SSOP



### Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7310G	20-SSOP	Yes	-25°C ~ 85°C	Rail
FAN7310GX	20-SSOP	Yes		Tape & Reel

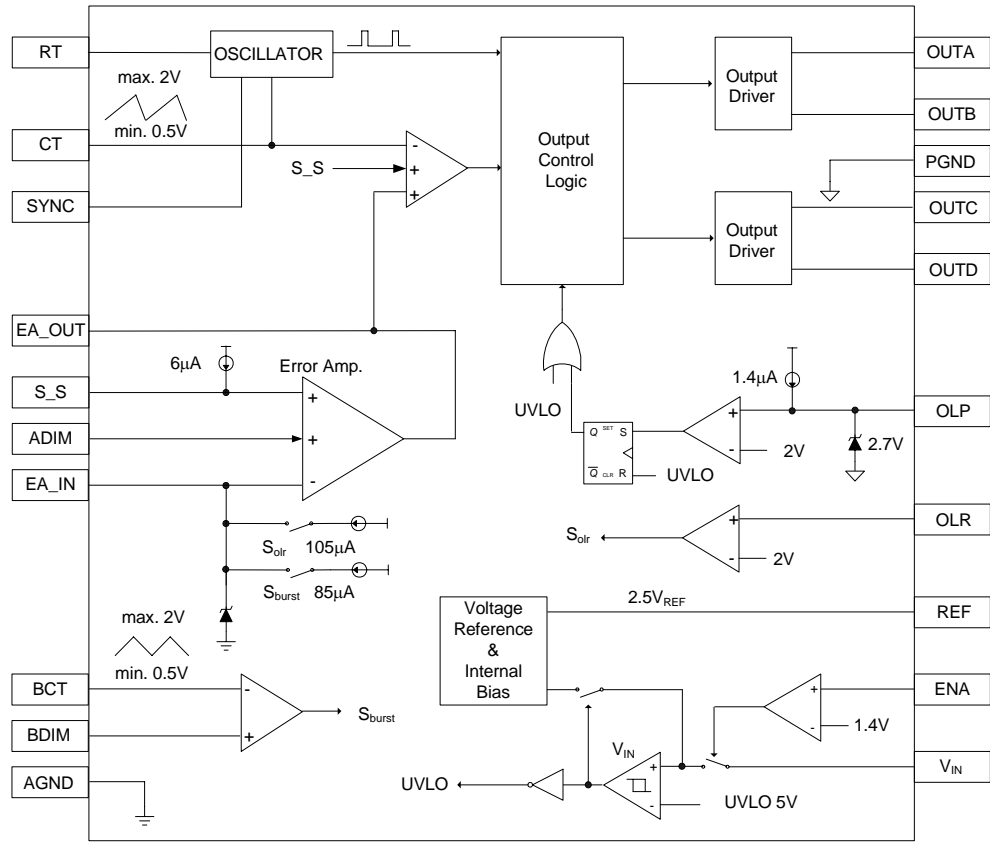
### Typical Application



FAN7310 Rev. 05

Figure 1. Application Circuit for CCFL

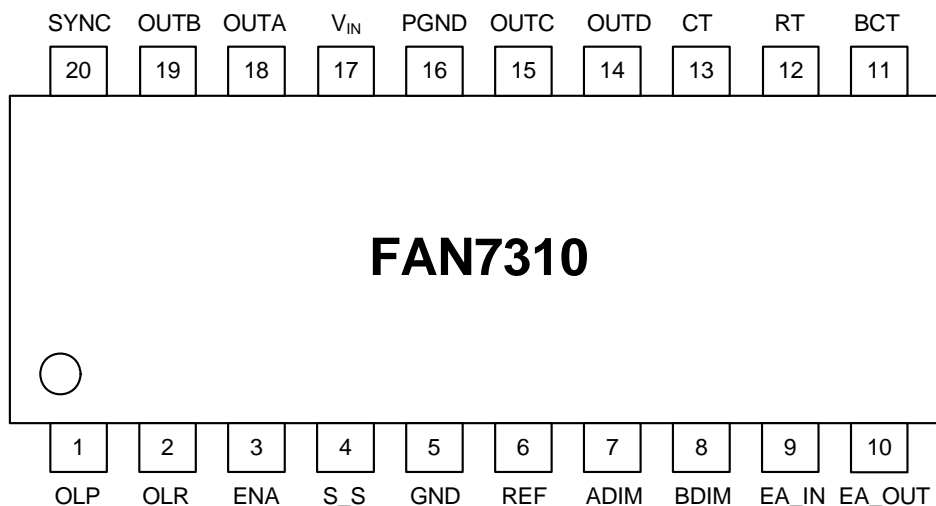
### Internal Block Diagram



FAN7310 Rev.03

Figure 2. Functional Block Diagram

## Pin Assignments



FAN7310 Rev. 03

Figure 3. Pin Configuration (Top View)

## Pin Definitions

Pin #	Name	Description	Pin #	Name	Description
1	OLP	Open-Lamp Protection	11	BCT	Burst Dimming Timing Capacitor
2	OLR	Open-Lamp Regulation	12	RT	Timing Resistor
3	ENA	Enable Input	13	CT	Timing Capacitor
4	S_S	Soft-Start	14	OUTD	NMOSFET Drive Output D
5	GND	Analog Ground	15	OUTC	PMOSFET Drive Output C
6	REF	2.5V Reference Voltage	16	PGND	Power Ground
7	ADIM	Analog Dimming Input	17	V <sub>IN</sub>	Supply Voltage
8	BDIM	Burst Dimming Input	18	OUTA	PMOSFET Drive Output A
9	EA_IN	Error Amplifier Input	19	OUTB	NMOSFET Drive Output B
10	EA_OUT	Error Amplifier Output	20	SYNC	Synchronization Input/Output

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Characteristics	Value	Unit
$V_{CC}$	Supply Voltage	5 ~ 24	V
$T_A$	Operating Temperature Range	-25 ~ 85	°C
$T_{STG}$	Storage Temperature Range	-65 ~ 150	°C
$\theta_{JA}$	Thermal Resistance Junction-Air <sup>(1)(2)</sup>	112	°C/W
$P_D$	Power Dissipation	1.1	W

### Notes:

1. Thermal resistance test board size: 76.2 \* 114.3 \* 1.6mm (1S0P). JEDEC standards: JESD51-3, JESD51-7.
2. Assume no ambient airflow.

## Electrical Characteristics

For typical values,  $T_A=25^\circ\text{C}$ ,  $V_{CC}=12\text{V}$  and for min./max. values,  $T_A$  is the operating ambient temperature range with  $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$  and  $5\text{V} \leq V_{CC} \leq 24\text{V}$ , unless otherwise specified.

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
<b>REFERENCE SECTION (Recommend X7R Capacitor)</b>						
$\Delta V_{\text{ref}}$	Line Regulation	$5 \leq V_{CC} \leq 24\text{V}$		2	25	mV
$V_{25}$	2.5V Regulation Voltage		2.45	2.50	2.55	V
<b>OSCILLATOR SECTION (MAIN)</b>						
$f_{\text{OSC}}$	Oscillation Frequency	$T_A = 25^\circ\text{C}$ , $C_T = 270\text{pF}$ $R_T = 18\text{k}\Omega$	108	115	122	kHz
		$C_T = 270\text{pF}$ , $R_T = 18\text{k}\Omega$	106	115	124	
$V_{\text{CTH}}$	CT High-Voltage			2.0		V
$V_{\text{CTL}}$	CT Low-Voltage			0.5		V
	SYNC Threshold Voltage			1		V
	Recommended SYNC Input Pulse Width			10		%
<b>OSCILLATOR SECTION (BURST)</b>						
$f_{\text{oscb}}$	Oscillation Frequency	$C_{\text{TB}} = 10\text{nF}$ , $R_T = 18\text{k}\Omega$	195	225	255	Hz
$V_{\text{bcth}}$	BCT High-Voltage			2		V
$V_{\text{bctl}}$	BCT Low-Voltage			0.5		V
<b>ERROR AMPLIFIER SECTION</b>						
	Open-Loop Gain			80		dB
	Unit Gain Bandwidth			1.5		MHz
$V_{\text{eh}}$	Feedback Output High Voltage	$\text{EA\_IN} = 0\text{V}$		2.5		V
$I_{\text{sin}}$	Output Sink Current	$\text{EA\_OUT} = 1.5\text{V}$			-1	mA
$I_{\text{sur}}$	Output Source Current	$\text{EA\_OUT} = 1.5\text{V}$	1			mA
$I_{\text{olr}}$	EA_IN Driving Current On OLR		75	105	135	$\mu\text{A}$
$I_{\text{burst}}$	EA_IN Driving Current On Burst Dimming		61	85	109	$\mu\text{A}$
$V_{\text{fbh}}$	Feedback High Voltage On Burst Dimming	$R(\text{EA\_IN}) = 60\text{k}\Omega$	$V_a+0.1$	$V_a+0.4$	$V_a+0.7$	V
<b>SOFT-START SECTION</b>						
$I_{\text{SS}}$	Soft-Start Current	$S\_S=2\text{V}$	4	6	8	$\mu\text{A}$
$V_{\text{ssh}}$	Soft-Start Clamping Voltage			5		V
<b>PROTECTION SECTION</b>						
$V_{\text{olp}}$	Open-Lamp Protection Voltage		1.75	2.00	2.25	V
$V_{\text{olr}}$	Open-Lamp Regulation Voltage		1.75	2.00	2.25	V
$I_{\text{olp}}$	Open-Lamp Protection Charging Current		0.7	1.4	2.1	
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>						
$V_{\text{th}}$	Start Threshold Voltage				5	V
$I_{\text{st}}$	Start-up Current	$V_{CC} = V_{\text{th}}-0.2$		130		$\mu\text{A}$
$I_{\text{op}}$	Operating Supply Current	$V_{CC} = 12\text{V}$		1.5		mA
$I_{\text{sb}}$	Stand-by Current	$V_{CC} = 12\text{V}$		200		$\mu\text{A}$
<b>ON/OFF SECTION</b>						
$V_{\text{on}}$	On State Input Voltage		2		5	V
$V_{\text{off}}$	Off Stage Input Voltage				0.7	

**Electrical Characteristics** (Continued)

For typical values,  $T_A=25^{\circ}\text{C}$ ,  $V_{CC}=12\text{V}$  and for min./max. values,  $T_A$  is the operating ambient temperature range with  $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  and  $5\text{V} \leq V_{CC} \leq 24\text{V}$ , unless otherwise specified.

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
<b>OUTPUT SECTION</b>						
$V_{pdhv}$	PMOS Gate High-Voltage	$V_{CC} = 12\text{V}$		$V_{CC}$		V
$V_{phlv}$	PMOS Gate Low-Voltage	$V_{CC} = 12\text{V}$	$V_{CC}-10.5$	$V_{CC}-8.5$	$V_{CC}-6.0$	
$V_{ndhv}$	NMOS Gate Drive Voltage	$V_{CC} = 12\text{V}$	6	8.5	10.5	V
$V_{ndhv}$	NMOS Gate Drive Voltage	$V_{CC} = 12\text{V}$		0		
$V_{puv}$	PMOS Gate Voltage With UVLO Activated	$V_{CC} = V_{th}-0.2$	$V_{CC}-0.3$			V
$V_{nuv}$	NMOS Gate Voltage With UVLO Activated	$V_{CC} = V_{th}-0.2$			0.3	V
$t_r$	Rising Time	$V_{CC} = 12\text{V}$ , $C_L=2\text{nF}$		200	500	ns
$t_f$	Falling Time	$V_{CC} = 12\text{V}$ , $C_L=2\text{nF}$		200	500	ns
<b>MAX./MIN. OVERLAP</b>						
	Min. Overlap Between Diagonal Switches	$f_{osc}=100\text{KHz}$		0		%
	Max. Overlap Between Diagonal Switches	$f_{osc}=100\text{KHz}$		100		%
<b>DELAY TIME</b>						
	PDR_A/NDR_B	$R_T=18\text{k}\Omega$		450		ns
	PDR_C/NDR_D	$R_T=18\text{k}\Omega$		450		ns

## Function Description

**UVLO:** The under-voltage lockout circuit guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the  $V_{IN}$  value. The UVLO circuit turns on the control circuit when  $V_{IN}$  exceeds 5V. When  $V_{IN}$  is lower than 5V, the IC's standby current is less than 200 $\mu$ A.

**ENA:** Applying the voltage higher than 2V to ENA pin enables the operation of the IC. Applying to the voltage lower than 0.7V to ENA pin disables the operation of the inverter.

**Soft-Start:** The soft-start functions provided that S\_S pin is connected through a capacitor to GND. A soft-start circuit ensures a gradual increase in the input and output power. The capacitor connected to S\_S pin determines the rate of rise of the duty ratio. It is charged by a current source of 6 $\mu$ A.

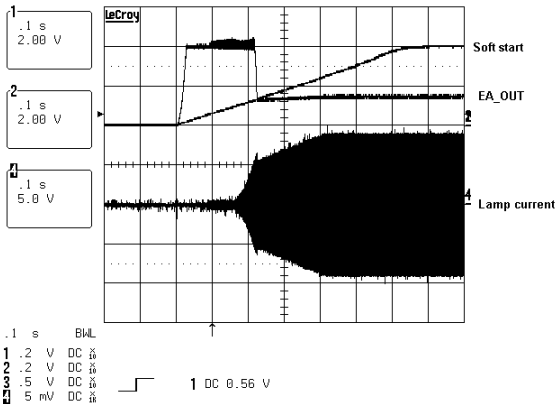


Figure 4. Soft-Start During Initial Operation

**Main Oscillator:** Timing capacitors  $C_T$  are charged by the reference current source, formed by the timing resistor  $R_T$  whose voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once reached, capacitors begin discharging down to 0.5V. Next timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed with adjusting the values of  $R_T$  and  $C_T$ . The main frequency can be calculated as shown in Equation 1:

$$f_{op} = \frac{19}{32 R_T C_T} \quad \text{EQ. 1}$$

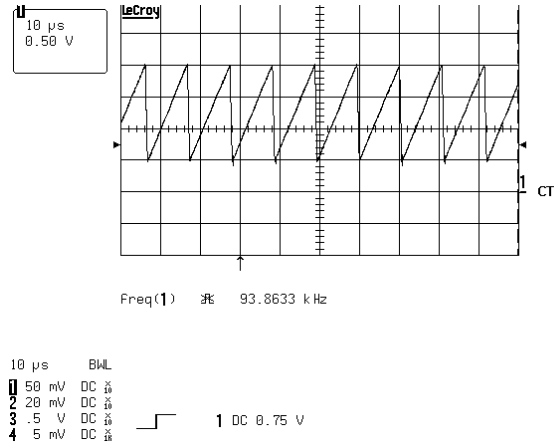


Figure 5. Main Oscillator Waveform

**Burst Oscillator & Burst Dimming:** Timing capacitor BCT are charged by the reference current source, formed by the timing resistor  $R_T$  whose voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once reached, capacitors begin discharging down to 0.5V. Next timing capacitors start charging again and a new switching cycle begins. The burst dimming frequency can be programmed by adjusting the values of  $R_T$  and  $BC_T$ . The burst dimming frequency can be calculated as shown in Equation 2:

$$f_{burst} = \frac{3.75}{96 R_T BC_T} \quad \text{EQ. 2}$$

The burst dimming frequency should be greater than 120Hz to avoid visible flicker.

Comparing the input of BDIM pin with the 0.5~2V triangular wave of burst oscillator makes the PWM pulse for burst dimming. The PWM pulse controls EA\_OUT's voltage by summing 85 $\mu$ A into EA\_IN pin.

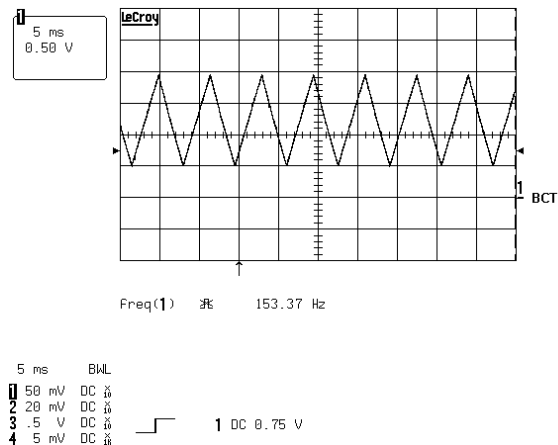


Figure 6. Burst Oscillator Waveform

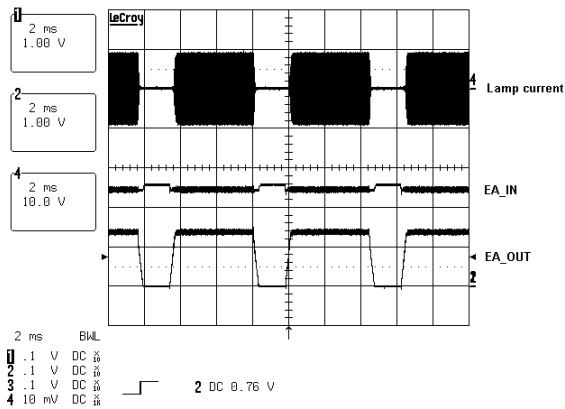


Figure 7. Burst Dimming

**Open-Lamp Regulation & Open Lamp Protection:** It is necessary to suspend power stage operation if an open lamp occurs because the power stage has high gain. When a voltage higher than 2V is applied to the OLR pin, the part enters the regulation mode and controls EA\_OUT voltage to limit the lamp voltage by summing 105 $\mu$ A into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 1.4 $\mu$ A internal current source. Once reached to 2V, IC enters shutdown where all the output is high.

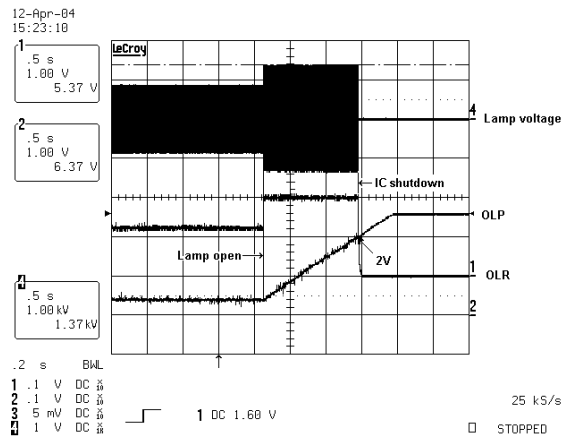


Figure 8. OLR Voltage During Striking Mode

**SYNC:** This pin is used as the frequency synchronization. The switching frequency can be synchronized with an external control signal. The threshold voltage of this pin is 1V. A resistor should be connected between this pin and GND for safe operation.

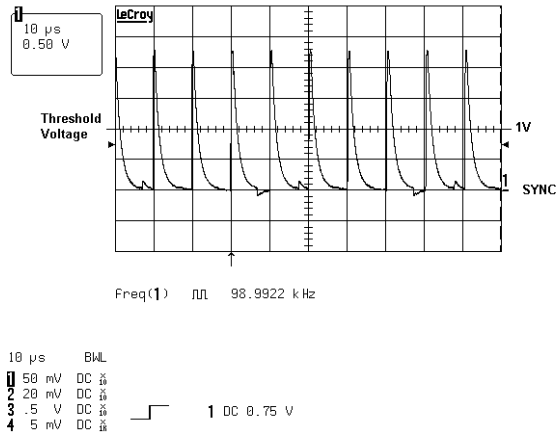


Figure 9. SYNC Waveform

**Output Drives:** The four output drives are designed so that switches A and B, C and D never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair drives the other half-bridge.

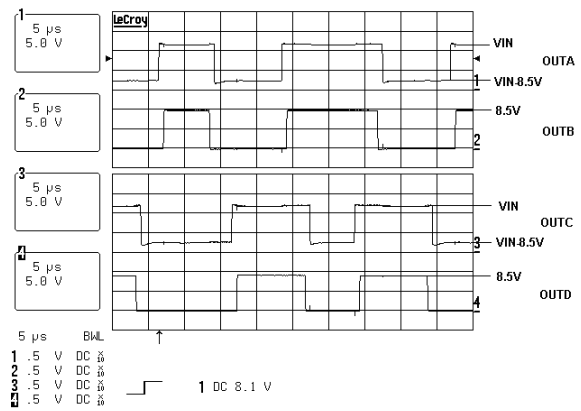
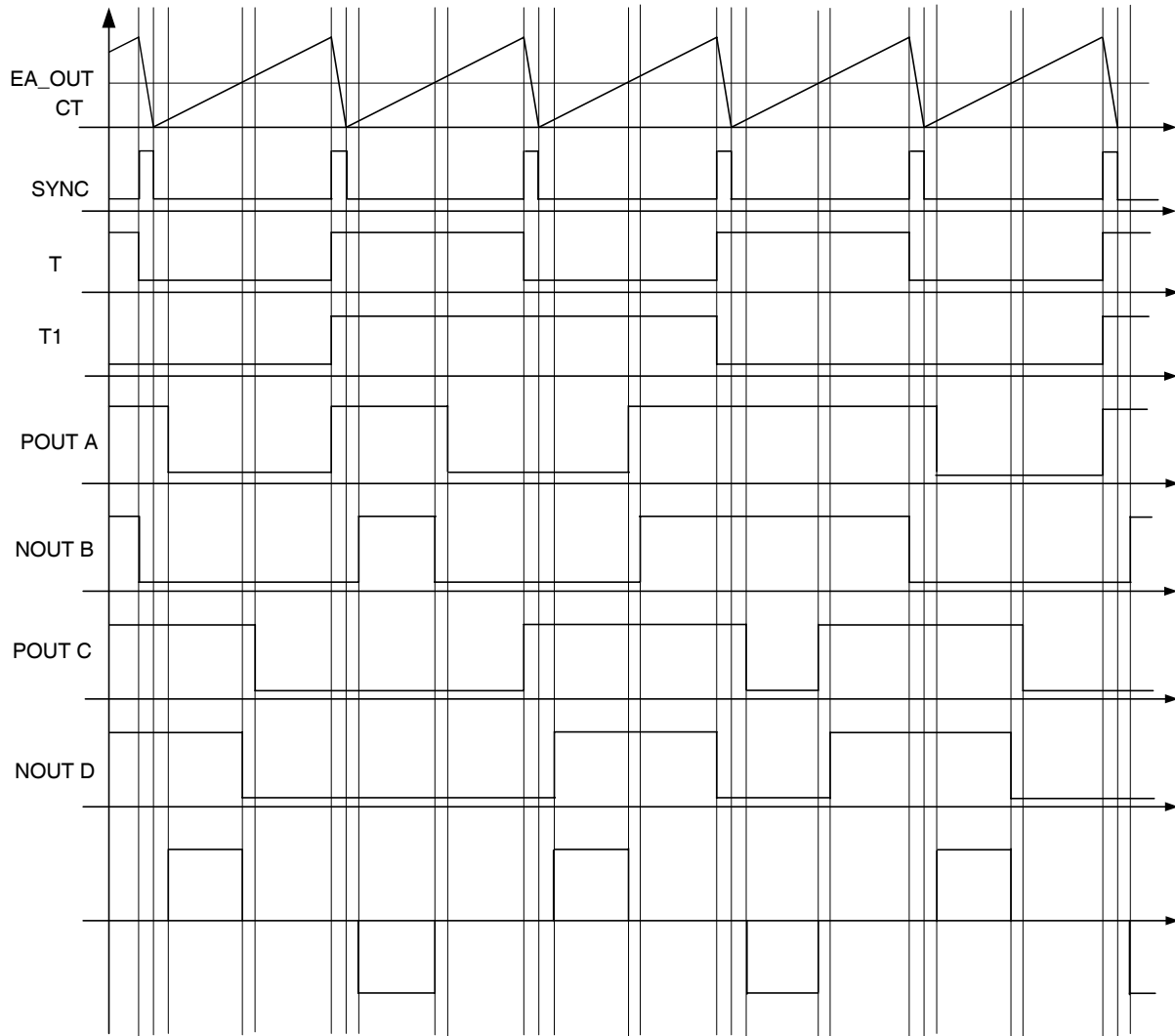


Figure 10. Phase-Shift Control Waveforms



### Timing Diagram

FAN7310 use the improved phase-shift control full-bridge to drive CCFL. As a result, the temperature difference between the left leg and the right legs is almost zero. The detail timing is shown as bellow.



FAN7310 Rev.03

Figure 10. Phase-Shift Control Waveforms

## Package Dimensions

### 20-SSOP

Dimensions are in millimeters unless otherwise noted.

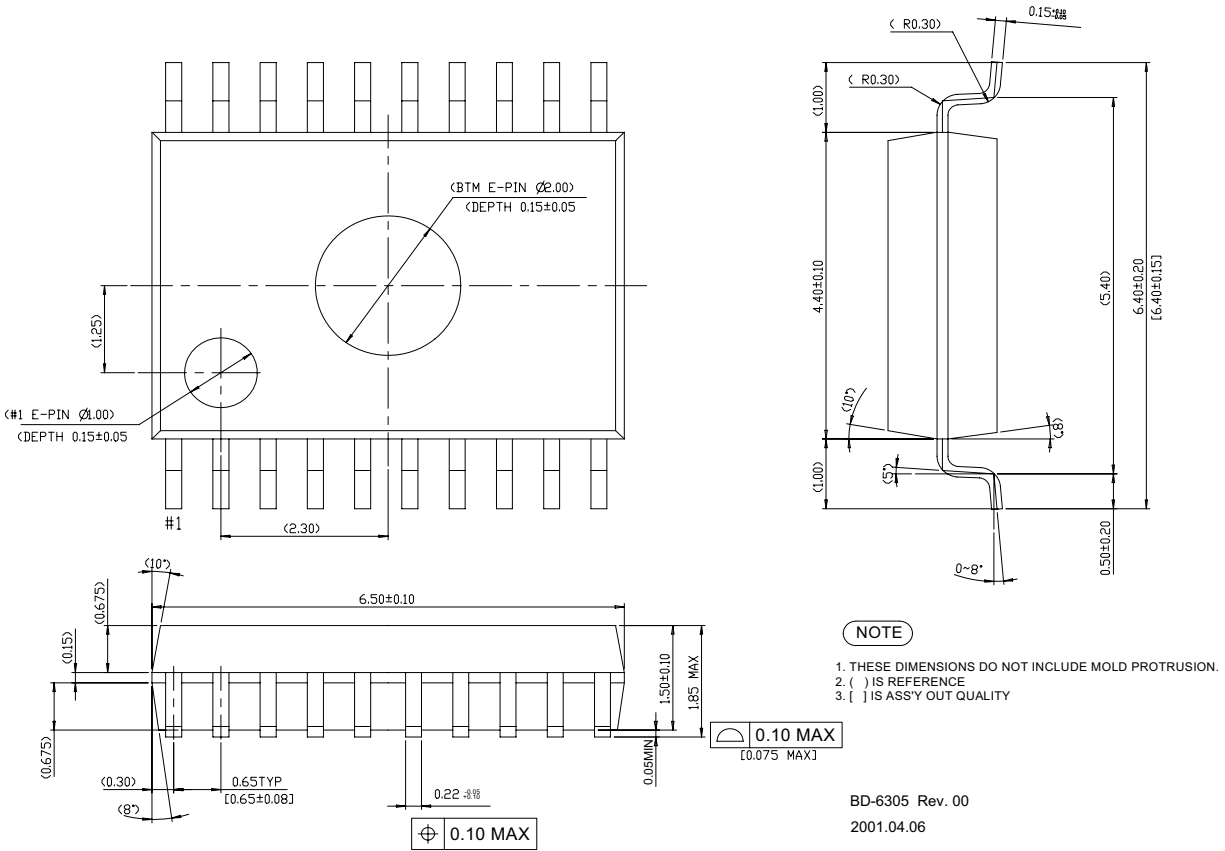



Figure 12. 20-Lead Shrink Small Outline Package (SSOP)



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Rev. I28