

2N7002L

Preferred Device

Small Signal MOSFET 60 V, 115 mA

N-Channel SOT-23

Features

- Pb-Free Package May be Available. The G-Suffix Denotes a Pb-Free Lead Finish

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 M\Omega$)	V_{DGR}	60	Vdc
Drain Current - Continuous $T_C = 25^\circ C$ (Note 1) - Pulsed (Note 2) $T_C = 100^\circ C$ (Note 1)	I_D I_{DM}	± 115 ± 75 ± 800	mAdc
Gate-Source Voltage - Continuous - Non-repetitive ($t_p \leq 50 \mu s$)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 3) $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	225 1.8	mW mW/ $^\circ C$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ C/W$
Total Device Dissipation Alumina Substrate, (Note 4) $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	300 2.4	mW mW/ $^\circ C$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ C/W$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ C$

- The Power Dissipation of the package may result in a lower continuous drain current.
- Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2.0\%$.
- FR-5 = $1.0 \times 0.75 \times 0.062$ in.
- Alumina = $0.4 \times 0.3 \times 0.025$ in 99.5% alumina.

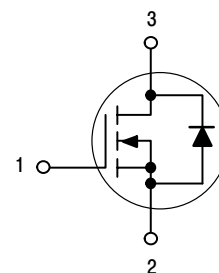


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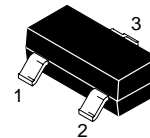
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$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
60 V	7.5 m Ω @ 10 V, 500 mA	115 mA

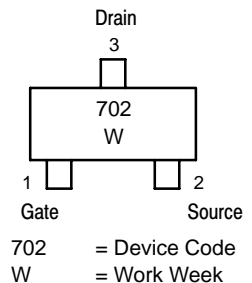
N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23
CASE 318
STYLE 21



ORDERING INFORMATION

Device	Package	Shipping†
2N7002LT1	SOT-23	3000 Tape & Reel
2N7002LT3		10,000 Tape & Reel
2N7002LT1G	SOT-23 (Pb-free)	3000 Tape & Reel
2N7002LT3G		10,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0, I _D = 10 μAdc)	V _{(BR)DSS}	60	–	–	Vdc
Zero Gate Voltage Drain Current (V _{GS} = 0, V _{DS} = 60 Vdc)	I _{DSS}	T _J = 25°C	–	–	1.0
		T _J = 125°C	–	–	500
Gate–Body Leakage Current, Forward (V _{GS} = 20 Vdc)	I _{GSSF}	–	–	100	nAdc
Gate–Body Leakage Current, Reverse (V _{GS} = –20 Vdc)	I _{GSSR}	–	–	–100	nAdc

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc)	V _{GS(th)}	1.0	–	2.5	Vdc
On–State Drain Current (V _{DS} ≥ 2.0 V _{DS(on)} , V _{GS} = 10 Vdc)	I _{D(on)}	500	–	–	mA
Static Drain–Source On–State Voltage (V _{GS} = 10 Vdc, I _D = 500 mAdc) (V _{GS} = 5.0 Vdc, I _D = 50 mAdc)	V _{DS(on)}	–	–	3.75	Vdc
		–	–	0.375	
Static Drain–Source On–State Resistance (V _{GS} = 10 V, I _D = 500 mAdc) (V _{GS} = 5.0 Vdc, I _D = 50 mAdc)	r _{DS(on)}	T _C = 25°C	–	–	7.5
		T _C = 125°C	–	–	13.5
		T _C = 25°C	–	–	7.5
		T _C = 125°C	–	–	13.5
Forward Transconductance (V _{DS} ≥ 2.0 V _{DS(on)} , I _D = 200 mAdc)	g _{FS}	80	–	–	mmhos

DYNAMIC CHARACTERISTICS

Input Capacitance (V _{DS} = 25 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	–	–	50	pF
Output Capacitance (V _{DS} = 25 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{oss}	–	–	25	pF
Reverse Transfer Capacitance (V _{DS} = 25 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	–	–	5.0	pF

SWITCHING CHARACTERISTICS (Note 5)

Turn–On Delay Time	(V _{DD} = 25 Vdc, I _D ≅ 500 mAdc, R _G = 25 Ω, R _L = 50 Ω, V _{gen} = 10 V)	t _{d(on)}	–	–	20	ns
Turn–Off Delay Time		t _{d(off)}	–	–	40	ns

BODY–DRAIN DIODE RATINGS

Diode Forward On–Voltage (I _S = 11.5 mAdc, V _{GS} = 0 V)	V _{SD}	–	–	–1.5	Vdc
Source Current Continuous (Body Diode)	I _S	–	–	–115	mAdc
Source Current Pulsed	I _{SM}	–	–	–800	mAdc

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

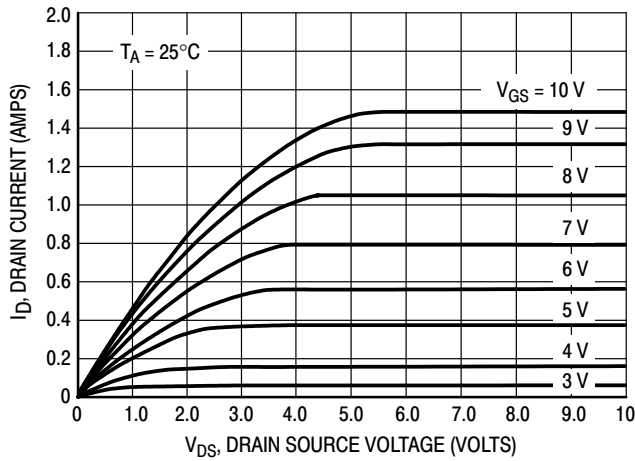


Figure 1. Ohmic Region

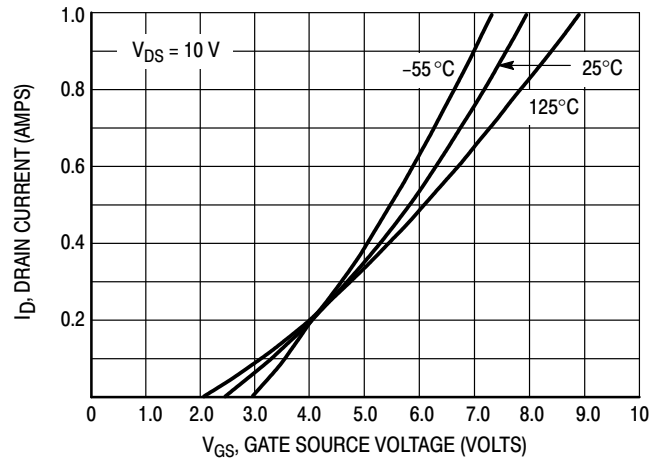


Figure 2. Transfer Characteristics

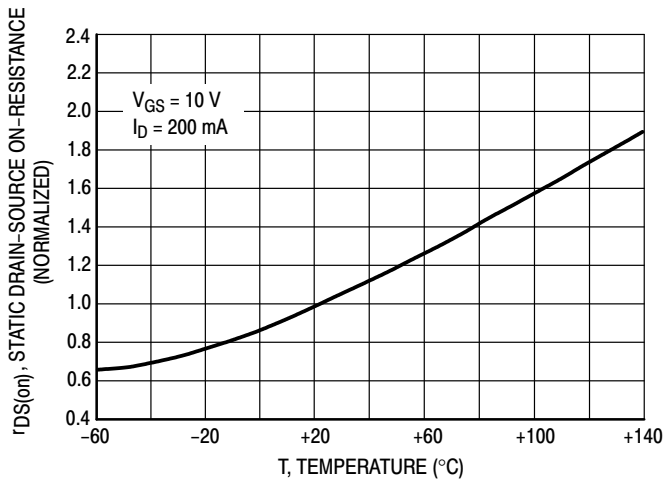


Figure 3. Temperature versus Static Drain-Source On-Resistance

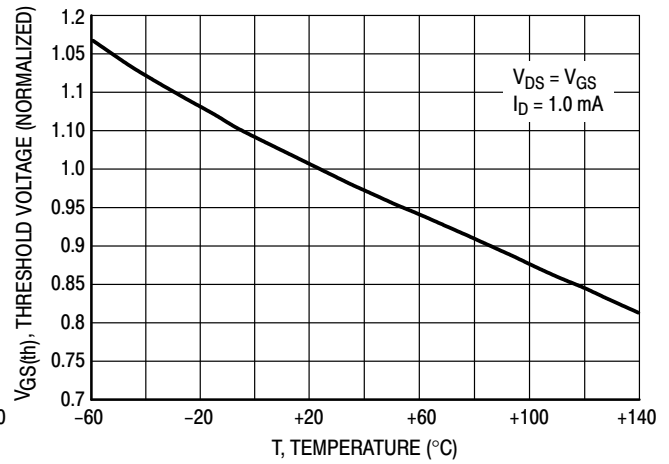


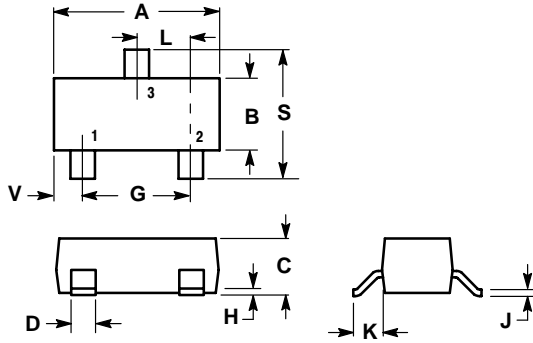
Figure 4. Temperature versus Gate Threshold Voltage

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PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AH

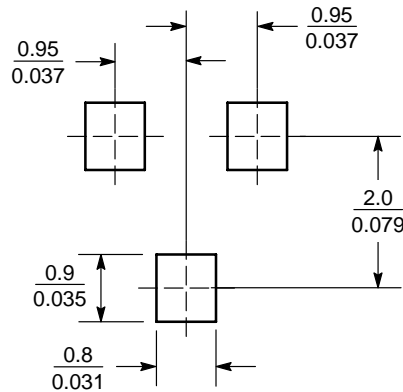
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. 318-03 AND -07 OBSOLETE, NEW STANDARD 318-08.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

- STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Figure 5. SOT-23

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