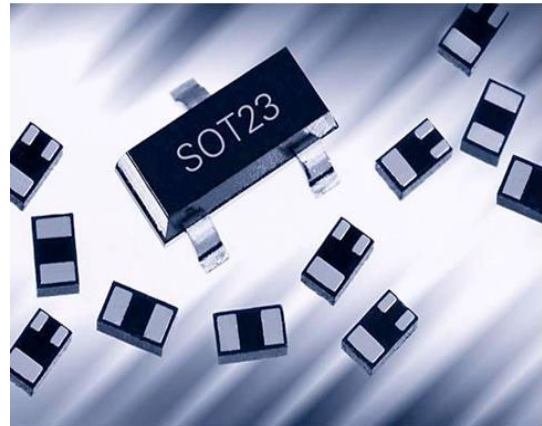


Ultra-Low Capacitance ESD Diode Array

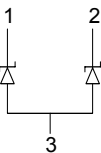
- ESD / transient protection of high-speed data lines exceeding IEC61000-4-2 (ESD): 20 kV (air / contact)
IEC61000-4-4 (EFT): 40 A (5/50 ns)
IEC61000-4-5 (surge): 3 A (8/20 μ s)
- Max. working voltage: 5.3 V
- Extremely low capacitance: down to 0.2 pF
- Very low clamping voltage: 12 V typ.
- Extremely low forward clamping voltage: 4 V typ.
- Very low reverse current: < 1 nA typ.
- Pb-free (RoHS compliant) package


Applications

- USB 2.0, 10/100/1000 Ethernet, FireWire, DVI
HDMI, S-ATA
- Mobile communication
- Consumer products (STB, MP3; DVD, DSC...)
- LCD displays, camera
- Notebooks and desktop computers, peripherals



ESD5V3U2U-03F
ESD5V3U2U-03LRH



Type	Package	Configuration	Marking
ESD5V3U2U-03F	TSFP-3	2 lines, uni-directional*	Z1
ESD5V3U2U-03LRH	TSLP-3-7	2 lines, uni-directional*	Z1

* or 1 line, bi-directional between pins 1 and 2, if pin 3 is not connected

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
ESD contact/ air discharge ¹⁾	V_{ESD}	20	kV
Peak pulse current ($t_p = 8 / 20 \mu\text{s}$) ²⁾	I_{pp}	3	A
Operating temperature range	T_{op}	-40...125	°C
Storage temperature	T_{stg}	-65...150	

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics -					
Reverse working voltage	V_{RWM}	-	-	5.3	V
Breakdown voltage $I_{\text{(BR)}} = 1 \text{ mA}$, from pin 1 to 3	$V_{\text{(BR)}}$	6	-	-	
Reverse current $V_{\text{R}} = 5.3 \text{ V}$, from pin 1 to 3	I_{R}	-	< 1	50	nA
Clamping voltage $I_{\text{PP}} = 1 \text{ A}$, $t_p = 8/20\mu\text{s}$ ²⁾ , from 1/2 to 3 $I_{\text{PP}} = 3 \text{ A}$, $t_p = 8/20\mu\text{s}$ ²⁾ , from 1/2 to 3	V_{CL}	-	10	13	V
		-	12	15	
Forward clamping voltage $I_{\text{PP}} = 1 \text{ A}$, $t_p = 8/20\mu\text{s}$ ²⁾ , from 3 to 1/2 $I_{\text{PP}} = 3 \text{ A}$, $t_p = 8/20\mu\text{s}$ ²⁾ , from 3 to 1/2	V_{FC}	-	2	4	
		-	4	6	
Line capacitance, $V_{\text{R}} = 0 \text{ V}$, $f = 1 \text{ MHz}$ from pin 1/2 to 3 ³⁾ from pin 1 to 2, pin 3 not connected	C_{T}	-	0.4	0.6	pF
		-	0.2	0.4	

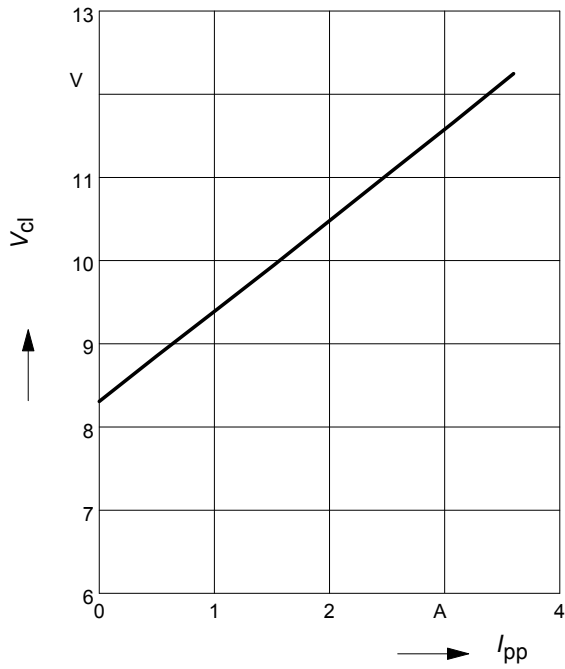
¹⁾ V_{ESD} according to IEC61000-4-2

²⁾ I_{pp} according to IEC61000-4-5

³⁾Total capacitance line to ground

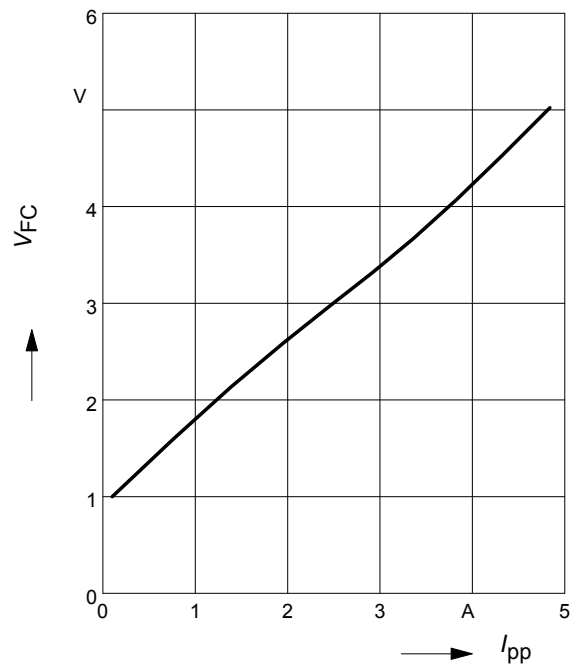
Clamping voltage, $V_{cl} = f(I_{pp})$

$t_p = 8 / 20 \mu s$, from pin 1/2 to 3



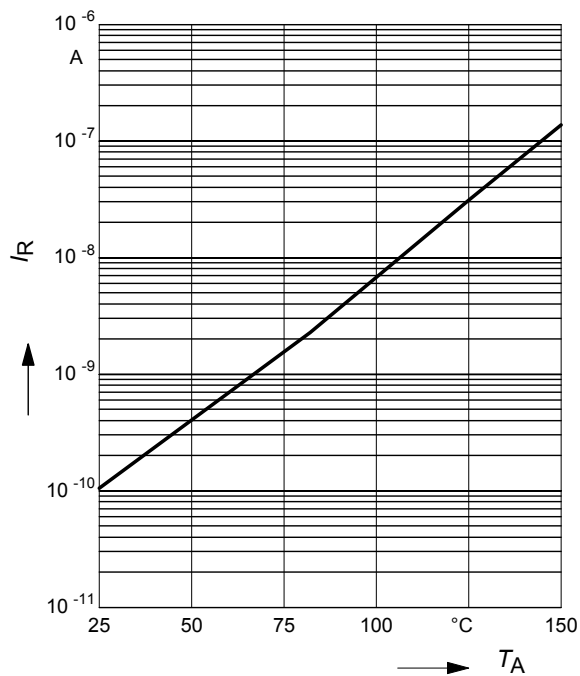
Forward clamping voltage $V_{FC} = f(I_{PP})$

$t_p = 8 / 20 \mu s$, from pin 3 to 1/2



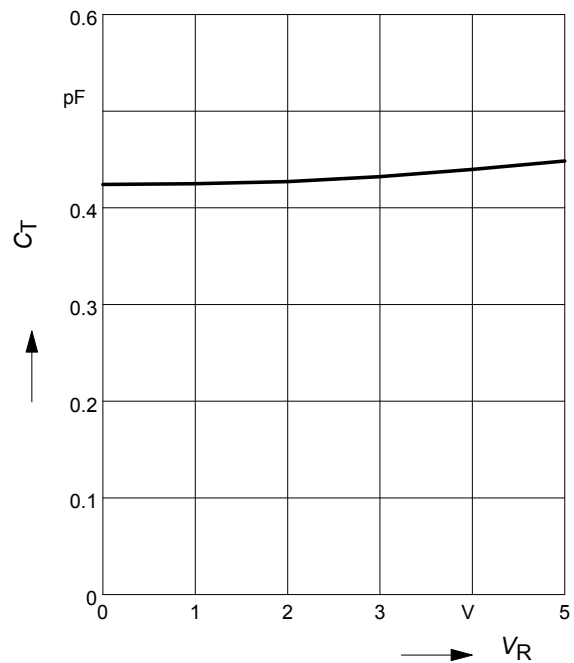
Reverse current $I_R = f(T_A)$

$V_R =$ Parameter, from pin 1/2 to 3



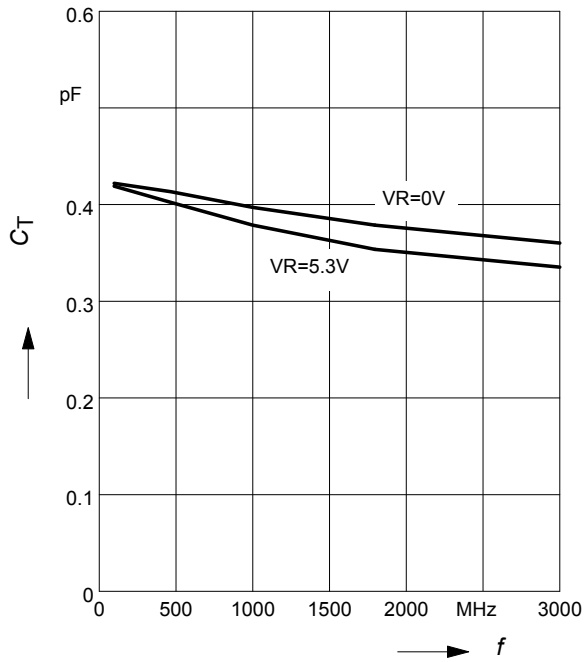
Diode capacitance $C_T = f(V_R)$

$f = 1 MHz$, from pin 1/2 to 3



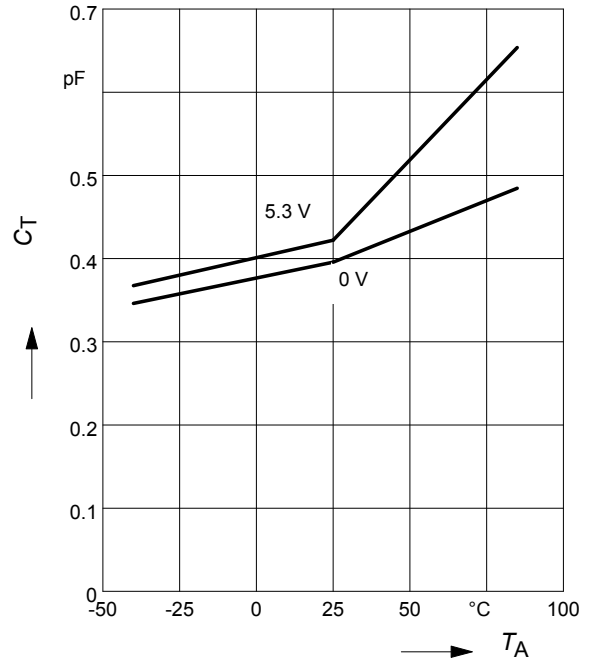
Line capacitance $C_T = f(f)$

$V_R =$ parameter, from pin 1/2 to 3



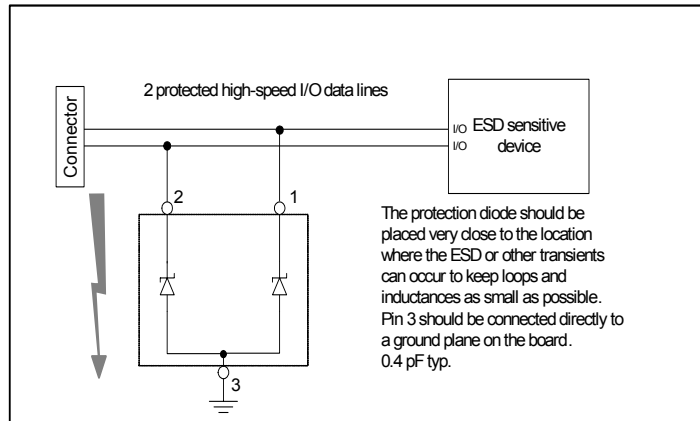
Line capacitance $C_T = f(T_A)$

$V_R = 0 V, f = 1 MHz$



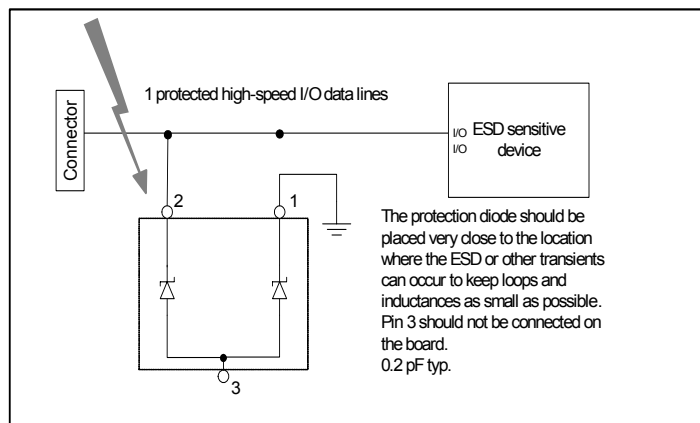
Application example ESD5V3U2U...

2 lines, uni-directional

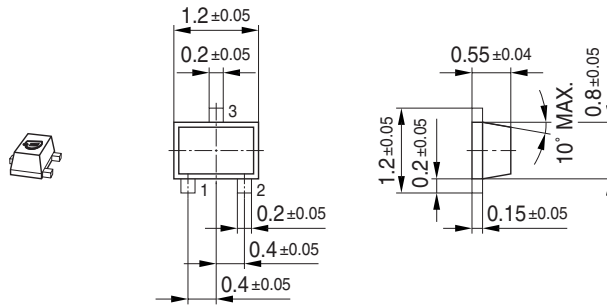


Application example ESD5V3U2U...

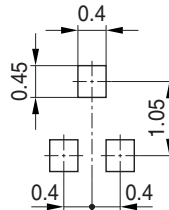
1 line, bi-directional



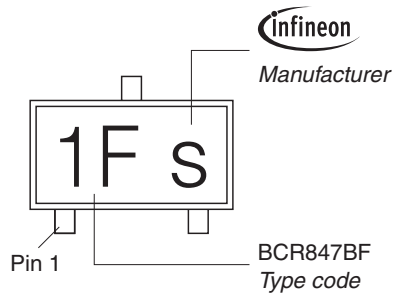
Package Outline



Foot Print

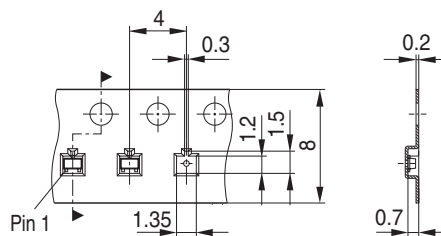


Marking Layout (Example)

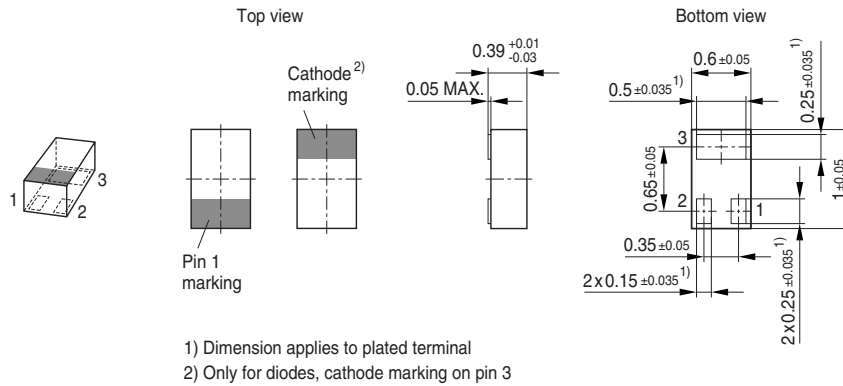


Standard Packing

Reel $\varnothing 180 \text{ mm} = 3.000 \text{ Pieces/Reel}$
 Reel $\varnothing 330 \text{ mm} = 10.000 \text{ Pieces/Reel}$

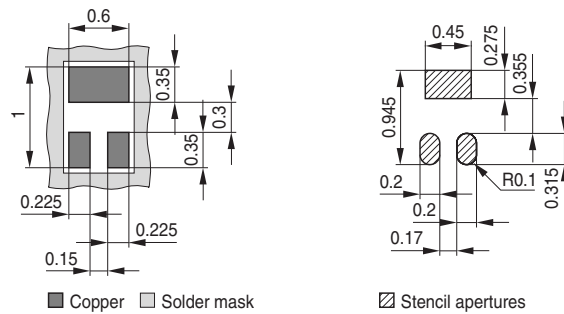


Package Outline

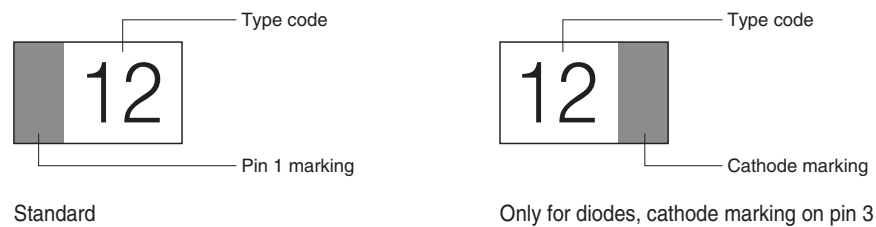


Foot Print

For board assembly information please refer to Infineon website "Packages"

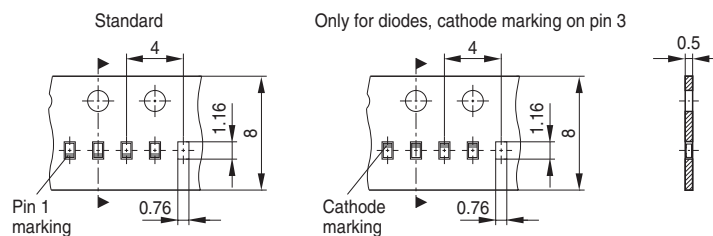


Marking Layout



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



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