LED Controller IC
ICLS8082G

Offline LED Controller For PFC And Dimming With Integrated 800 V CoolMOS®

Data Sheet for LED Controller IC

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Page or Item	Subjects (major changes since previous revision)
Rev1.0, 2011-03-01	
1.0	**DataSheet,Version 1.0, March 1st 2011**

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Product Highlights

- Quasi-resonant control for highly efficient LED driving solutions
- Primary-side flyback control with integrated PFC and phase-cut dimming
- High-voltage **CoolMOS®** and startup cell for short "time to light"
- Best-in-class system BOM for dimmable LED bulbs with the integrated **CoolMOS®**
- Miniatuarization with the integrated **CoolMOS®**

Features

- High, stable efficiency over a wide operating range
- Optimized for trailing- and leading-edge dimmers
- Precise PWM for primary PFC and dimming control
- Startup cell for Vcc precharging with constant current
- Built-in digital soft start
- Foldback correction and cycle-by-cycle peak current limitation
- VCC over/undervoltage lockout
- Auto restart mode for short-circuit protection
- Adjustable latch-off mode for output overvoltage protection

Description

The ICLS8082G employs a quasi-resonant operation mode optimized for off-line LED lighting, especially for dimmable LED bulbs for replacement of incandescent lamps.

Precise PWM generation enables primary control for phase-cut dimming and high power factors (PF) > 98 %. It offers significantly improved driver efficiency, up to 90 %, compared to other conventional solutions. The product has a wide operation range (up to 26 V) of IC voltage supply and lower power consumption. Multiple safety functions ensure full system protection in failure situations.

With its full feature set and simple application, the ICLS8082G represents an outstanding choice for quasi-resonant flyback LED bulb designs combining the feature set and performance at minimum BOM cost.

Application Circuit for Primary Control

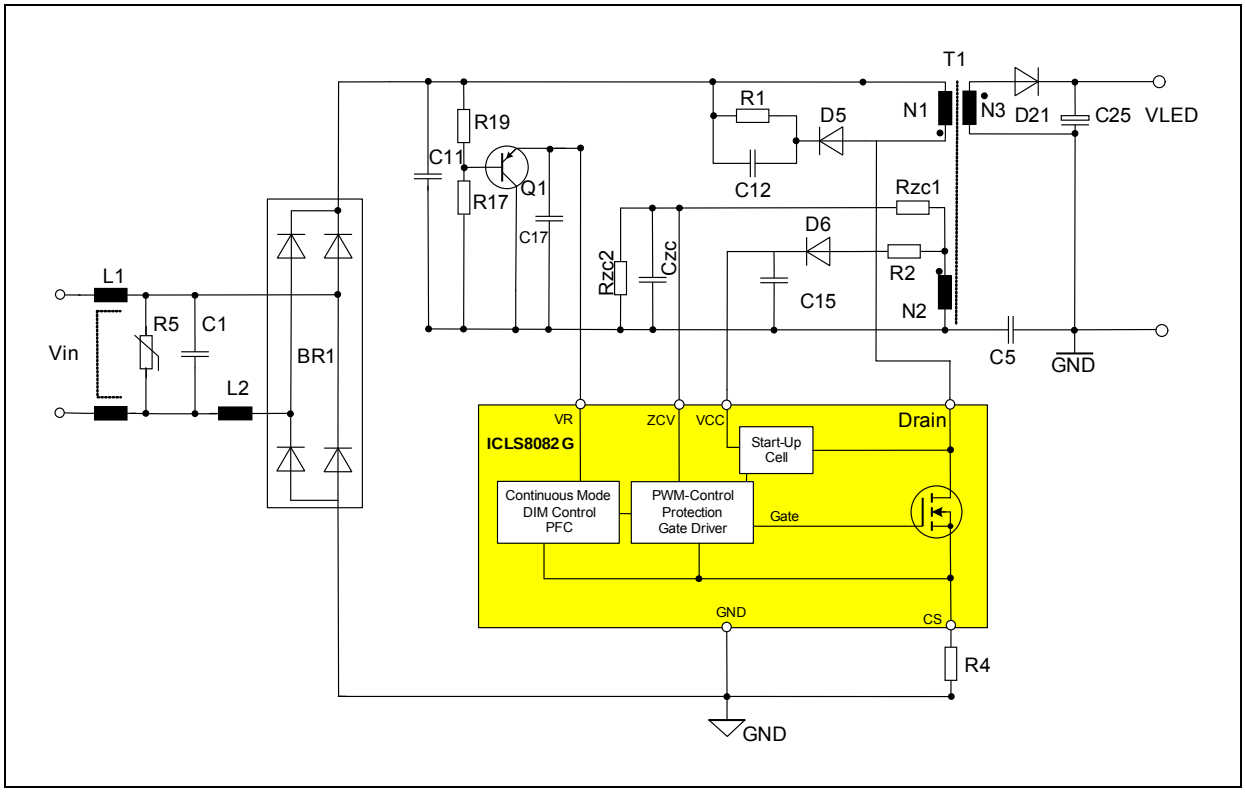


Figure 1 Application Circuit for Primary Control

Type	Package	V_{DS}	R_{DSon} [1]	230VAC±15% [2]	110VAC±15% [2]
ICLS8082G	PG-DSO-12	800 V	2.26	28 W	14 W

1) Typical @ T_j=25 °C

2) Calculated maximum input power rating at Ta = 50 °C,Tj = 125 °C and with 232 mm², 2-oz. copper area on the drain pin as the heat sink

Table of Contents

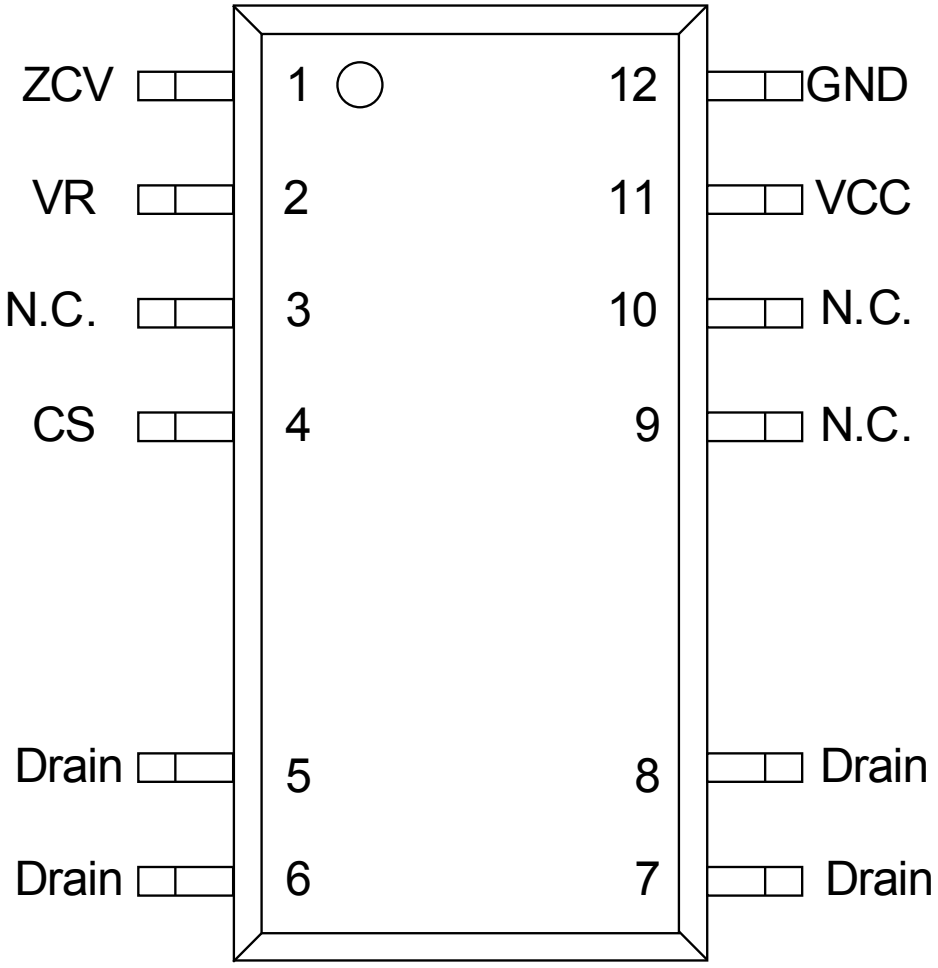
1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DSO-12/10

Table 1 Pin Description

Ball No.	Name	Function
1	ZCV	**Zero Crossing**
2	VR	**Voltage Sense**
3	N.C.	**Not Connected**
4	CS	**Current Sense**
5	Drain	**800V Depletion CoolMOS® Drain**
6	Drain.	**800V Depletion CoolMOS® Drain**
7	Drain	**800V Depletion CoolMOS® Drain**
8	Drain	**800V Depletion CoolMOS® Drain**
9	N.C.	**Not Connected**
10	N.C.	**Not Connected**
11	VCC	**Controller Supply Voltage**
12	GND	**Controller Ground**

1.2 Package PG-DSO-12



Pin Configuration PG-DSO-12 (Top View)
Note: Pins 5,6,7,8 are shorted within the package

Figure 1 Pin Configuration PG-DSO-12 (top view)

1.3 Pin Functionality

ZCV (Zero Crossing)

At this pin, the voltage from the auxiliary winding is applied after a time delay circuit. Internally, this pin is connected to the zero-crossing detector for switch-on determination. Additionally, the output overvoltage detection is realized by comparing the voltage Vzc with an internal preset threshold.

VR (Voltage Sense)

The rectified input mains voltage is sensed at this pin. The signal is used to set the peak current of the peak-current control and therefore allow the PFC and phase-cut dimming functionality.

CS (Current Sense)

This pin is connected to the shunt resistor for the primary current sensing (externally), and the PWM signal generator for switch-off determination (together with the feedback voltage), internally. Moreover, short-winding protection is realized by monitoring the voltage Vcs during the on-time of the main power switch.

Drain (Drain of the integrated depletion CoolMOS®)

The drain pin is the connection to the drain of the internal depletion CoolMOS®.

VCC (Power supply)

Positive power is supplied to the IC at the VCC pin. The operating range is between V_{VCCoff} and V_{VCCOVP}.

GND (Ground)

This is the common ground of the controller.

2 Representative Block Diagram

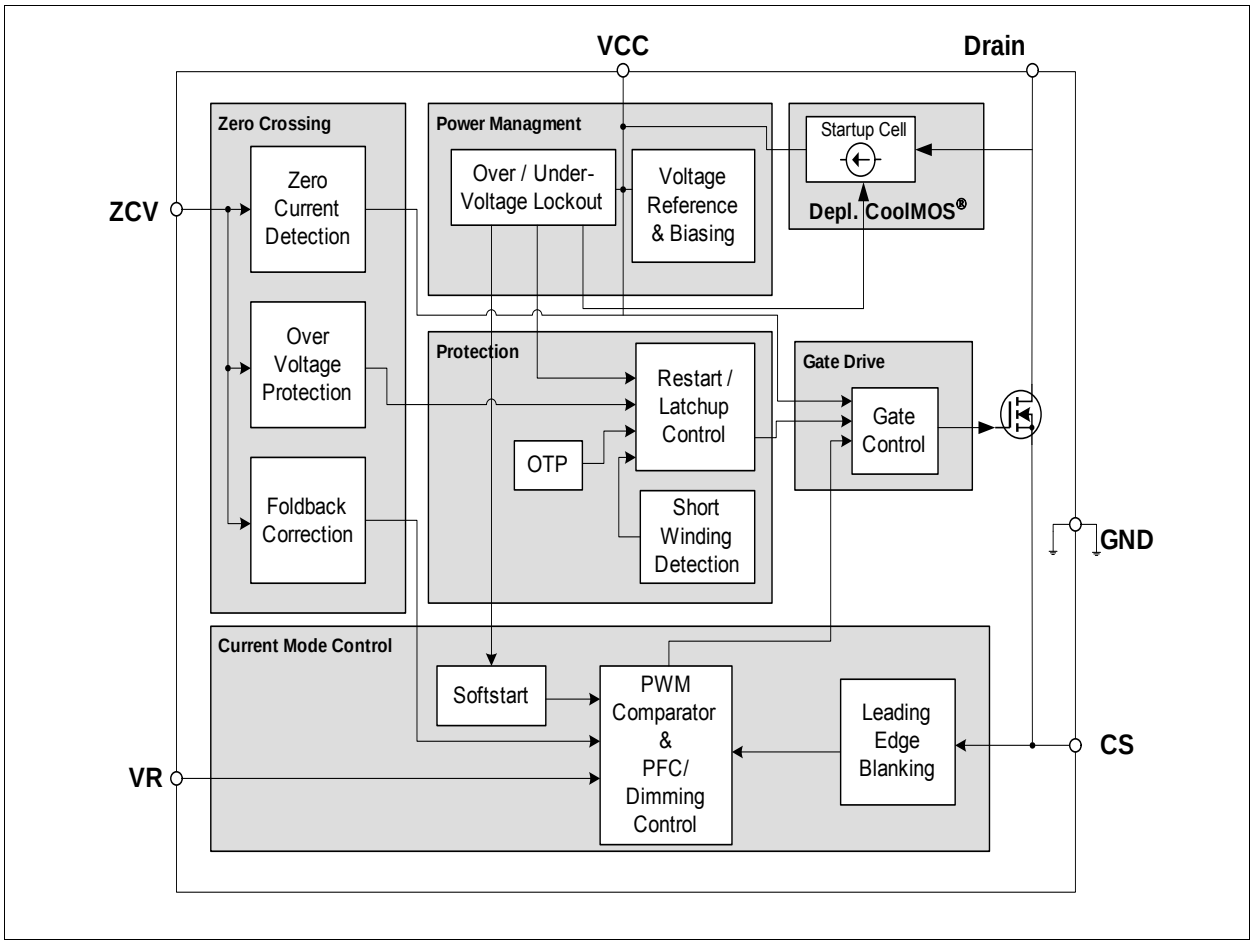


Figure 2 Representative Block Diagram

3 Functional Description

3.1 VCC Precharging and Typical VCC Voltage During Startup

A high-voltage startup cell is integrated into the ICLS8082G. As shown in Figure 2, the start cell is integrated into the depletion **CoolMOS®**. The startup cell consists of a high-voltage device and a controller, whereby the high-voltage device is controlled by the controller. The startup cell provides precharging of the VCC capacitor until the VCC voltage reaches the VCC turned-on threshold V_{VCCon} and the IC begins to operate.

Once the mains input voltage is applied, a rectified voltage occurs across the capacitor Cbus. The high-voltage device provides a current to charge the VCC capacitor Cvcc. Before the VCC voltage reaches a certain value, the amplitude of the current through the high voltage device is determined only by its channel resistance and can be as high as several mA. Once the VCC voltage is high enough, the controller controls the high-voltage device so that a constant current of about 1 mA is provided to further charge the VCC capacitor until the VCC voltage exceeds the turned-on threshold V_{VCCon}. As shown by the time phase I in Figure 3, the VCC voltage increases almost linearly and the charging speed is independent of the mains voltage level.

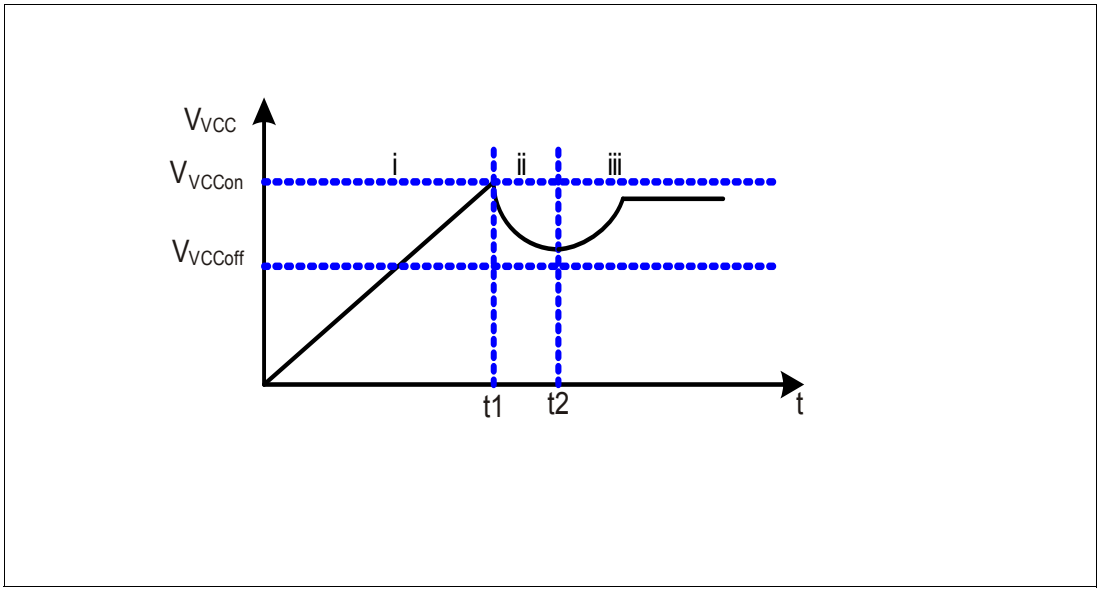


Figure 3 VCC voltage at startup

The time required for VCC precharging can then be approximately calculated as:

$$t_1 = \frac{V_{VCCon} \cdot C_{VCC}}{I_{VCCcharge2}} \quad (1)$$

where $I_{VCCcharge2}$ is the charging current from the startup cell, which is typically 1.05 mA.

If the VCC voltage exceeds the turned-on threshold V_{VCCon} at time t1, the startup cell is switched off, and the IC begins to operate with a soft start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the VCC capacitor before the output voltage, the VCC voltage drops (Phase II). Once the output voltage is high enough, the VCC capacitor then receives energy from the auxiliary winding from the time point t_2 on. The VCC will then reach a constant value dependent on the output load.

3.2 Soft Start

At the time t_{on}, the IC begins to operate with a soft start. With this soft start, the switching stresses for the switch, diode and transformer are minimized. The soft start implemented in ICLS8082G is a digital time-based function. The preset soft start time is 12 ms in 4 steps. If not limited by other functions, the peak voltage at the CS pin will increase step by step from 0.32 V finally to 1 V.

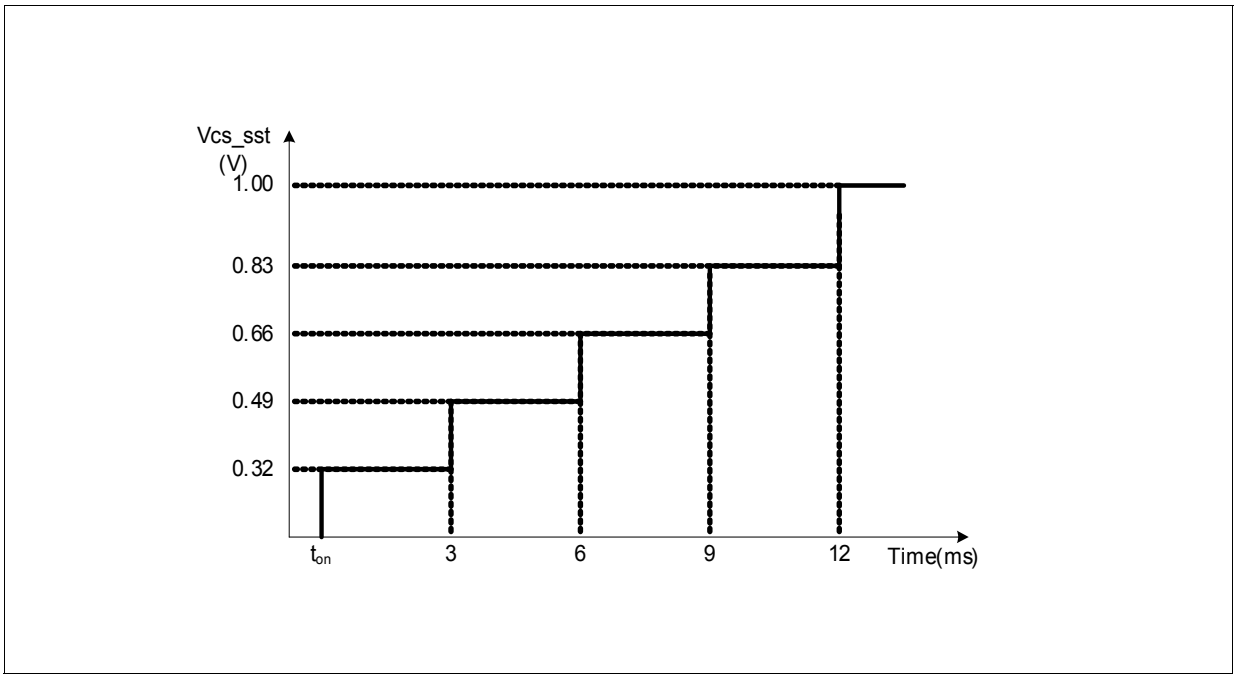


Figure 4 Maximum current sense voltage during soft start

3.3 Normal Operation

The PWM controller during normal operation consists of a digital signal processing circuit, including a comparator and an analog circuit that includes a current measurement unit and a comparator. The switch on and off times are each determined by the digital circuit and the analog circuit, respectively. As input information for the switch-on determination, the zero-crossing input signal is needed, while the voltage sense signal at the pin VR and the current sensing signal V_{CS} are necessary for determination of switch-off. Details on full operation of the PWM controller in normal operation are provided in the following paragraphs.

3.4 Zero Crossing

In the system, the voltage from the auxiliary winding is applied to the zero-crossing pin through an RC network, which provides a time delay to the voltage from the auxiliary winding. Internally, this pin is connected to a clamping network, a zero-crossing detector, an output overvoltage detector and a ringing suppression time controller.

During the on-state of the power switch a negative voltage applies to the ZCV pin. Through the internal clamping network, the voltage at the pin is clamped to a certain level.

The voltage Vzc is also used for the output overvoltage protection. Once the voltage at this pin is higher than the threshold V_{ZCOVP} during off-time of the main switch, the IC is latched off after a fixed blanking time.

To achieve the switch-on during the voltage valley, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of Rzc1, Rzc2 and Czc as shown in typical application circuit) before it is applied to the zero-crossing detector through the ZC pin. The time delay needed for the main oscillation signal Dt should be approximately one fourth of the oscillation period (by means of the transformer primary inductor and drain-

source capacitor) minus the propagation delay from the detected zero-crossing to switch-on of the main switch t_{delay}. This is theoretically:

$$\Delta t = \frac{T_{OSC}}{4} - t_{delay} \tag{2}$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{ZC} \cdot \frac{R_{ZC1} \cdot R_{ZC2}}{R_{ZC1} + R_{ZC2}}$$

3.5 Ringing Suppression Time

After the MOSFET is turned off, there will be some oscillation on VDS, which will also appear on the voltage at the ZC pin. To prevent the MOSFET from being mistriggered by oscillations of this kind, a ringing suppression timer is implemented. The timer is dependent on the voltage Vzc. If the voltage Vzc is lower than the threshold V_{ZCRS} a longer preset time applies, while a shorter time is set when the voltage Vzc is higher than the threshold.

3.6 Switch-on Determination

After the gate drive goes to low, it cannot be changed to high during the ring suppression time.

After the ring suppression time, the gate drive can be turned on when zero crossing is detected.

However, it is also possible that the oscillation between the primary inductor and drain-source capacitor is dampened very quickly and that the IC cannot detect zero crossing. In this case, a maximum off-time is implemented. After the gate drive has remained off for the period of T_{OffMax}, the gate drive will be turned on again regardless of the counter values and Vzc. This function can effectively prevent the switching frequency from falling below 20 kHz, otherwise this will cause audible noise during start-up.

3.7 Switch-off Determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between the low-side terminal of the main power switch and the common ground. The sensed voltage across the shunt resistor V_{CS} is applied to an internal current measurement unit, and its output voltage V1 is compared with the voltage at the pin VR. Once the voltage V1 exceeds the voltage V_{VR}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V1 and the Vcs is described by:

$$V_1 = 3.3 \cdot V_{CS} + 0.7 \tag{3}$$

To avoid mistriggering caused by the voltage spike across the shunt resistor at turn-on of the main power switch, a leading edge blanking time, t_{LEB}, is applied to the output of the comparator. In other words, once the gate drive is turned on, the minimum on-time of the gate drive is the leading edge blanking time.

In addition, there is a maximum on-time, t_{OnMax}, limitation implemented in the IC. Once the gate drive has been in the high state for longer than the maximum on-time, it will be turned off to prevent the switching frequency from going too low because of an overly long on-time.

3.8 Current Limitation

Cycle-by-cycle current limitation is realized by the current limit comparator to provide overcurrent detection. The source current of the MOSFET is sensed via a sense resistor Rcs. By means of Rcs the source current is transformed to a sense voltage Vcs, which is fed to the pin CS. If the voltage Vcs exceeds an internal voltage limit, adjusted according to the mains voltage, the comparator immediately turns off the gate drive.

To protect the current limitation process from distortions caused by leading edge spikes, a leading edge blanking time (t_{LEB}) is integrated into the current sensing path.

A further comparator is implemented to detect dangerous current levels (Vcssw) which could occur if one or more transformer windings are shorted or if the secondary diode is shorted. To avoid accidental latch-off, a spike blanking time of tcssw is integrated into the output path of the comparator.

3.9 Foldback Point Correction

When the main bus voltage increases, the switch-on time becomes shorter and therefore the operating frequency is also increased. As a result, for a constant primary current limit, the maximum possible output power is increased, which the converter may not have been designed to support.

To avoid such a situation, the internal foldback point correction circuit varies the Vcs voltage limit according to the bus voltage. This means the Vcs will be decreased when the bus voltage increases. To keep a constant maximum input power of the converter, the required maximum Vcs versus various input bus voltage can be calculated, which is shown in **Figure 6**.

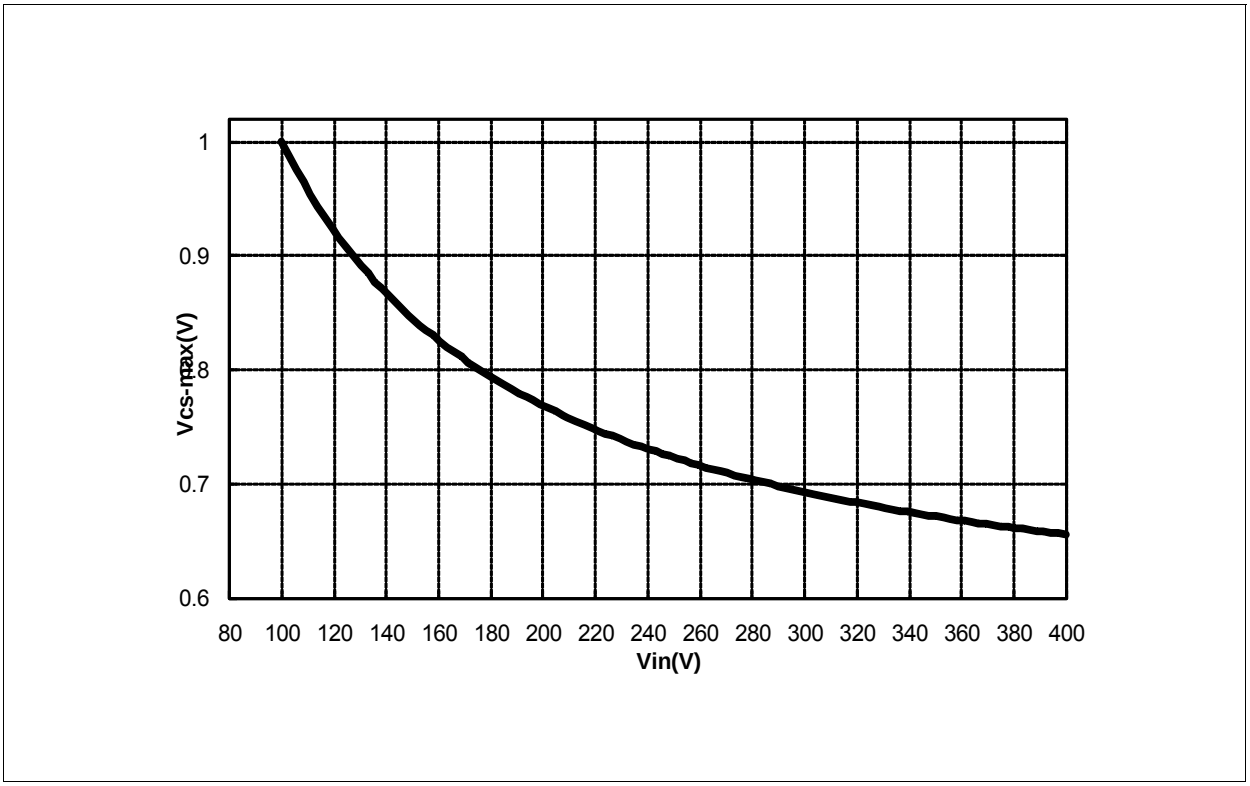


Figure 6) Variation of the VCS limit voltage according to the IZC current

According to the typical application circuit, when the MOSFET is turned on, a negative voltage proportional to the bus voltage will be coupled with the auxiliary winding. Inside the IC, an internal circuit will clamp the voltage at the ZC pin to nearly 0 V. As a result, the current flowing from the ZC pin can be calculated as:

$$I_{ZC} = \frac{V_{BUS} \cdot N_a}{R_{ZC\_1} \cdot N_P} \quad (4)$$

When this current is higher than IZC_1, the amount of current exceeding this threshold is used to generate an offset to decrease the maximum limit on V_{CS}. Since the ideal curve shown in **Figure 6** is nonlinear, a digital block in the IC is implemented to get better control of maximum output power. Another advantage of using digital circuitry is that the production tolerance is lower than that obtained with analog solutions. The typical maximum limit on V_{CS} versus the ZC current is shown in **Figure 7**.

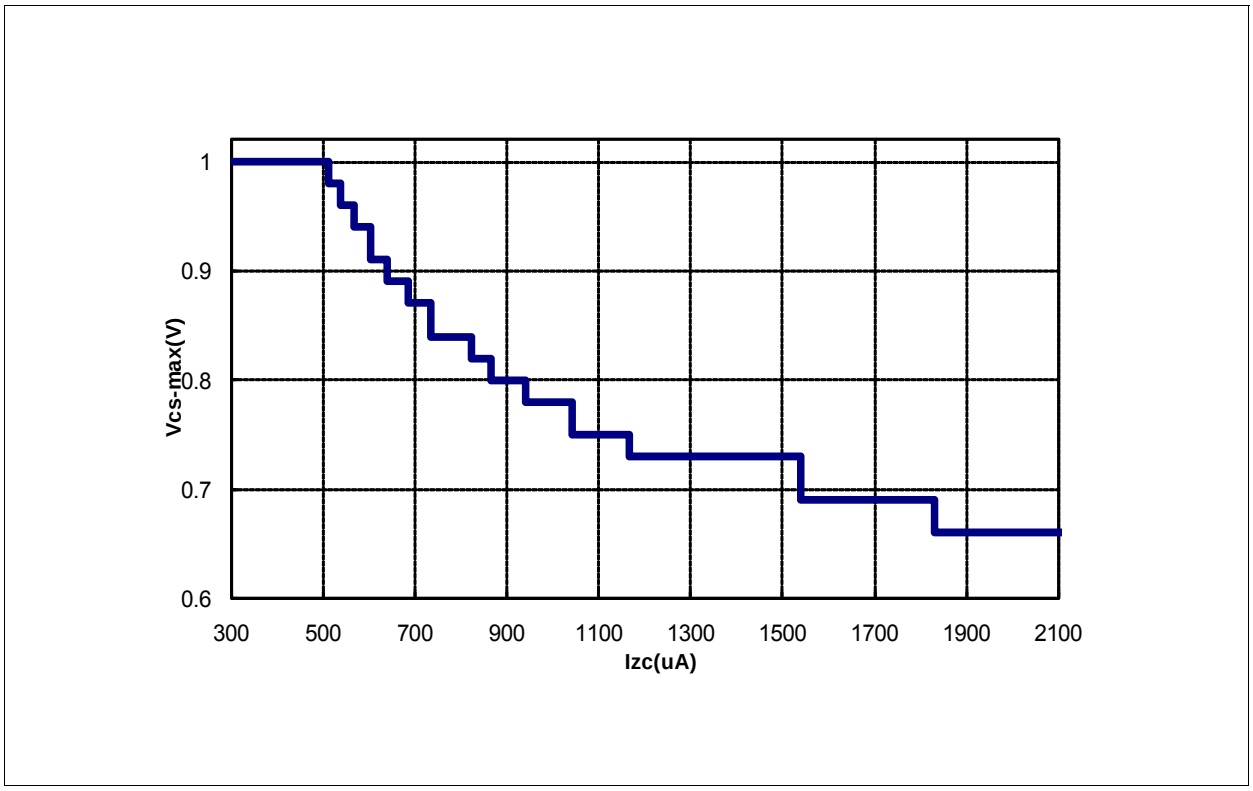


Figure 7) VCS-max versus I_{ZC}

3.10 Protection Functions

The IC provides full protection functions. The following table summarizes these protection functions.

Table 2 Protection features

VCC Overvoltage	Auto Restart Mode
VCC Undervoltage	Auto Restart Mode
Overtemperature	Auto Restart Mode
Output Overvoltage	Latched Off Mode
Short Winding	Latched Off Mode

During operation, the VCC voltage is continuously monitored. In the case of undervoltage or overvoltage, the IC is reset and the main power switch is then kept switched off. Once the VCC voltage falls below the threshold V_{VCCoff}, the startup cell is activated. The VCC capacitor is then charged up. Once the voltage exceeds the threshold V_{VCCon}, the IC begins to operate with a new soft start.

During off-time of the power switch, the voltage at the zero-crossing pin is monitored for output overvoltage detection. If the voltage is higher than the preset threshold V_{ZCOVP}, the IC is latched off after the preset blanking time.

If the junction temperature of IC exceeds 140 °C, the IC enters into the autorestart mode.

If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} during on-time of the power switch, the IC is latched off. This is short-winding protection.

During latch-off protection mode, when the VCC voltage drops to 10.5 V, the startup cell is activated and the VCC voltage is charged to 18 V; then the startup cell is shut down again and repeats the previous procedure.

There is also a maximum on-time limitation applicable to the ICLS8082G. Once the gate voltage is high for longer than t_{OnMAx}, it is turned off immediately.

4 Electrical Characteristics

All voltages are measured with respect to ground (pin 12). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are defined as ratings, which when exceeded may lead to destruction of the integrated circuit. For the same reason make sure that any capacitor to be connected to pin 11 (V_{CC}) is discharged before assembling the application circuit.

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain source voltage	V_{DS}	–	–	800	V	T_j=25°C
VCC supply voltage	V_{VCC}	-0.3	–	27	V	
VR voltage	*VR*	-0.3	–	5.5	V	
ZCV voltage	V_{ZC}	-0.3	–	5.5	V	
CS voltage	V_{CS}	-0.3	–	5.5	V	
Maximum current from ZC pin	I_{ZCMAX}	3	–	–	mA	
Junction temperature	T_J	-40	–	150	°C	Controller and CoolMOS®
Storage temperature	T_S	-55	–	150	°C	
Thermal resistance junction - ambient	R_{thJA}	–	–	85	K/W	With 232 mm², 2-oz. copper area on the drain pin Ta = 25 °C
ESD capability (incl. drain pin)	V_{ESD}	–	–	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kW series resistor).

4.2 Operating Range

Within the operating range the IC operates as described in the functional description.

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC supply voltage	V_{VCC}	V_{VCCoff}	–	V_{VCCovp}	V	
Junction temperature of CoolMOS®	$T_{jCoolMOS}$	-25	–	150	°C	
Junction temperature of controller	T_{jCON}	-25	–	125	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from –25°C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC}=18 V is assumed.

Table 5 Supply Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Startup current	$I_{VCCstart}$	–	300	550	µA	V_{VCC}=V_{VCCon}-0.2V
VCC charge current	$I_{VCCcharge1}$	–	5.0	–	mA	V_{VCC}=0V
	$I_{VCCcharge2}$	0.8		–	mA	V_{VCC}=1V
	$I_{VCCcharge3}$	–	1.0	–	mA	V_{VCC}=V_{VCCon}-0.2V
Maximum input current of startup cell and CoolMOS®	$I_{DrainIn}$	–	–	2	mA	V_{VCC}=V_{VCCon}-0.2V
Leakage current of startup cell	$I_{StartLeak}$	–	0.2	50	µA	V_{Drain}=650V at T_j=100°C
Supply current in normal operation	I_{VCCNM}	–	1.5	2.3	mA	Output low
Supply current in auto restart mode with inactive gate	I_{VCCAR}	–	300	–	µA	I_{FB} =0A
Supply current in latch-off mode	$I_{VCClatch}$	–	300	–	µA	
VCC turn-on threshold	V_{VCCon}	17.0	18.0	19.0	V	
VCC turn-off threshold	V_{VCCoff}	9.8	10.5	11.2	V	
VCC turn-on/off hysteresis	V_{VCChys}	–	7.5	–	V	

4.3.2 Internal Voltage Reference

Table 6 Internal Voltage Reference

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Internal reference voltage	V_{REF}	4.80	5.00	5.20	V	Measured at pin VR I_{VR}=0

4.3.3 PWM Section

Table 7 PWM Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Feedback pull-up resistor	R_{VR}	14	23	33	kΩ	
PWM-OP gain	G_{PWM}	3.25	3.3	3.35	–	
Offset for voltage ramp	V_{PWM}	0.63	0.7	0.77	V	
Maximum on time in normal operation	t_{OnMax}	22	30	41	µs	

4.3.4 Current Sense

Table 8 Current Sense

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CSth}	0.97	1.03	1.09	V	
Leading edge blanking time	t_{LEB}	200	330	460	ns	

4.3.5 Soft Start

Table 9 Soft Start

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Soft start time	t_{SS}	8.5	12	–	ms	
Soft start time step	t_{SS_S} 1)	–	3	–	ms	
Internal regulation voltage at first step	V_{CSth} 1)	–	1.76	–	V	
Internal regulation voltage step at soft start	V_{CSth} 1)	–	0.56	–	V	

1) The parameter is not subjected to production testing - it is verified by design/characterization

4.3.6 Foldback Point Correction

Table 10 Foldback Point Correction

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ZCV current first step threshold	I_{ZC_FS}	0.35	0.5	0.621	mA	
ZCV current last step threshold	I_{ZC_LS}	1.3	1.7	2.2	mA	
CS threshold minimum	V_{CSMF}	–	0.66	–	V	I_{ZC}=2.2mA, V_{VR}=3.8V

4.3.7 Digital Zero Crossing

Table 11 Digital Zero Crossing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Zero crossing threshold voltage	V_{ZCCT}	50	100	170	mV	
Ringing suppression threshold	V_{ZCRS}	–	0.7	–	V	
Minimum ringing suppression time	t_{ZCRS1}	1.62	2.5	4.5	µs	$V_{ZC} > V_{ZCRS}$
Maximum ringing suppression time	t_{ZCRS2}	–	25	–	µs	$V_{ZC} < V_{ZCRS}$
ZCV current for IC switch threshold to high line	I_{ZCSH}	–	1.3	–	mA	
ZCV current for IC switch threshold to low line	I_{ZCSL}	–	0.8	–	mA	
Maximum restart time in normal operation	t_{OffMax}	30	42	57.5	µs	

4.3.8 Protection

Table 12 Protection

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC overvoltage threshold	V_{VCCOVP}	24.0	25.0	26.0	V	
Output overvoltage detection threshold at the ZCV pin	V_{ZCOVP}	3.55	3.7	3.84	V	
Blanking time for output overvoltage protection	t_{ZCOVP}	–	100	–	µs	
Threshold for short-winding protection	V_{CSSW}	1.63	1.68	1.78	V	
Blanking time for short-winding protection	t_{CSSW}	–	190	–	ns	
Overtemperature protection[1)]	T_{jCon}		140		°C	

Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except for V_{VCCOVP}

4.3.9 CoolMOS® Section

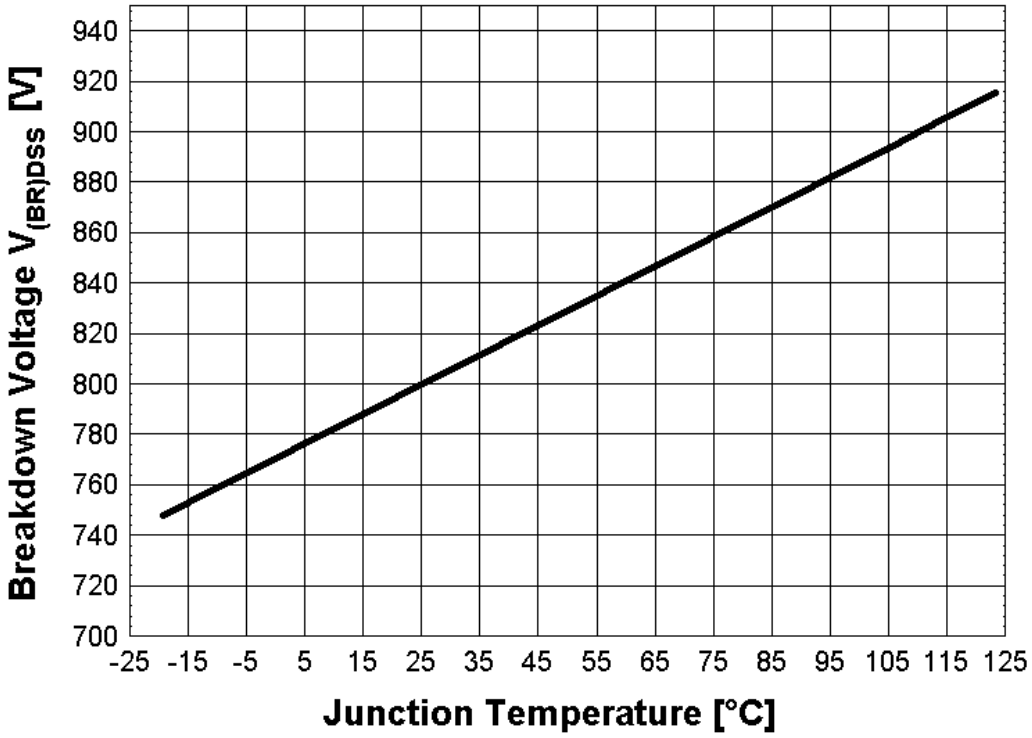
Table 13

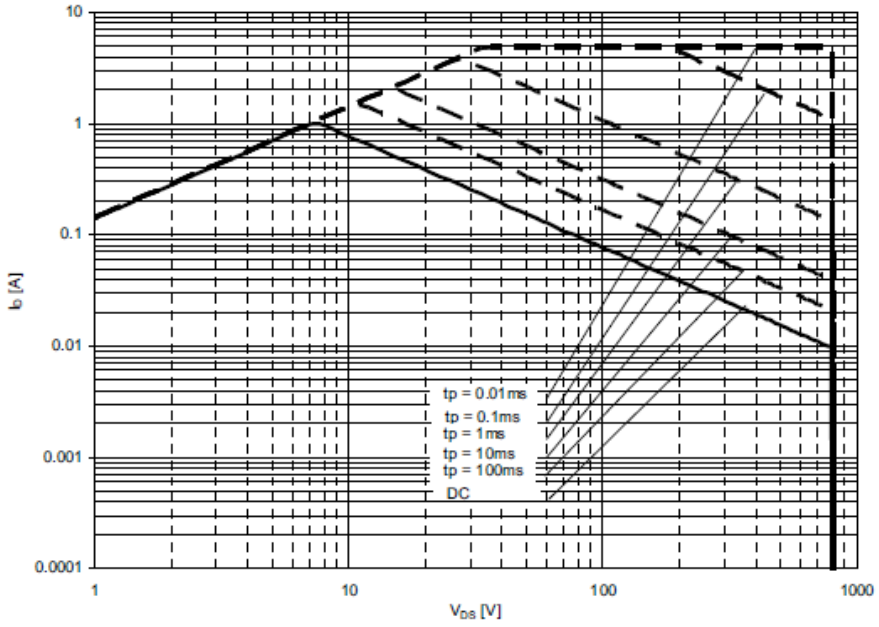
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Effective output capacitance	$C_{o(er)}$	–	16.3[1)]	–	pF	V_{DS}= 0 V to 480 V
Rise time	T_{rise}	–	30[2)]	–	ns	
Fall time	T_{fall}	–	30[2)]	–	ns	
Drain source breakdown voltage	V_{DS}	800 870	–	–	V	T_j = 25 °C T_j = 110 °C
Drain source on-resistance	R_{DSon}	–	2.26 5.02 6.14	2.62 5.81 7.10	V	T_j = 25 °C T_j = 110 °C T_j = 150 °C at I_D = 0.81 A

1) Not subjected to production testing - verified by design/characterization

2) Tested in typical flyback application

5 Typical CoolMOS® Performance Characteristics





Safe Operating Area (SOA) Curve for ICLS8082G

6 Outline Dimension

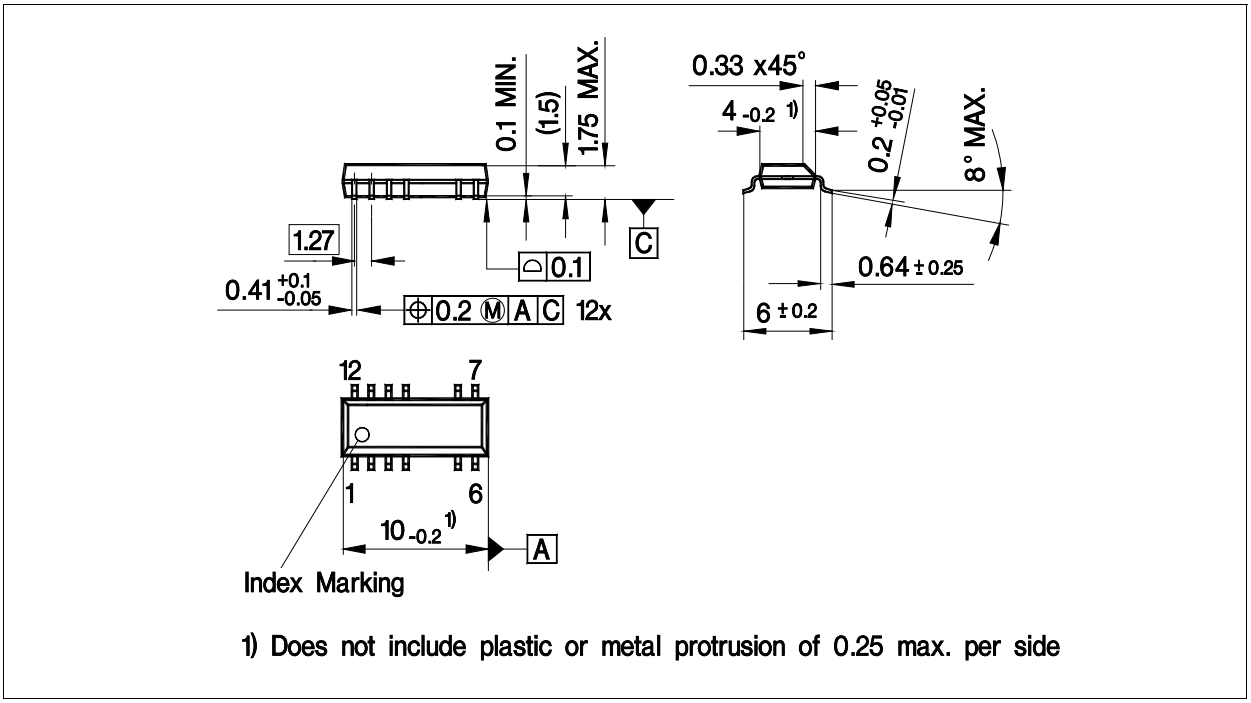


Figure 5 PG-DSO-12 (Pb-free lead plating, Plastic Dual Small Outline)

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