OptiMOS™ P2 Small-Signal-Transistor

Features

- Dual P-channel
- Enhancement mode
- Super Logic Level (2.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant

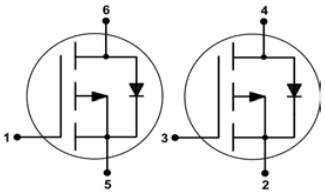
AEC Qualified

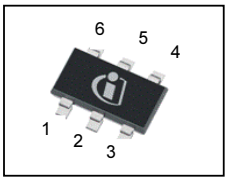
RoHS

Product Summary

V_{DS}		-20	V
$R_{DS(on),max}$	V_{GS}=-4.5 V	150	mΩ
	V_{GS}=-2.5 V	280	
I_D		-1.5	A

PG-TSOP6





Type	Package	Tape and Reel Information	Marking	Lead Free	Packing
BSL215P	PG-TSOP6	L6327: 3000 pcs/ reel	sPG	Yes	Non dry

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter [1]	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_A=25 °C	-1.5	A
		T_A=70 °C	-1.18	
Pulsed drain current	$I_{D,pulse}$	T_A=25 °C	-6	
Avalanche energy, single pulse	E_{AS}	I_D=-1.5 A, R_{GS}=25 Ω	11	mJ
Reverse diode dv/dt	dv/dt	I_D=-1.5 A, V_{DS}=-16V, di/dt=-200A/µs, $T_{j,max}$=150 °C	6	kV/µs
Gate source voltage	V_{GS}		±12	V
Power dissipation	P_{tot}	T_A=25 °C	0.5	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
ESD Class		JESD22-A114 -HBM	0 (<250V)	V
Soldering Temperature			260 °C	°C
IEC climatic category; DIN IEC 68-1			55/150/56	°C

[1] Remark: one of both transistors in operation.

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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint[2)]	-	-	250	K/W
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=-250 µA	-20	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-11 µA	-1.2	-0.9	-0.6	
Drain-source leakage current	I_{DSS}	V_{DS}=-20 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=-20 V, V_{GS}=0 V, T_j=150 °C	-	-	100	
Gate-source leakage current	I_{GSS}	V_{GS}=-12V, V_{DS}=0V	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=-2.5 V, I_D=-1.1 A	-	166	280	mΩ
		V_{GS}=-4.5 V, I_D=-1.5 A	-	105	150	
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-1.18 A	-	4.5	-	S

[2)] Performed on 40mm^2 FR4 PCB. The traces are 1mm wide, 70µm thick and 20mm long; they are present on both sides of the PCB.

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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=-15 V, f=1 MHz	-	260	346	pF
Output capacitance	C_{oss}		-	102	135	
Reverse transfer capacitance	C_{rss}		-	85	128	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-10 V, V_{GS}=-4.5 V, I_D=-1.5 A, R_G=6 Ω	-	6.7	-	ns
Rise time	t_r		-	9.7	-	
Turn-off delay time	$t_{d(off)}$		-	14.5	-	
Fall time	t_f		-	14.0	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=-16 V, I_D=-1.5 A, V_{GS}=0 to -4.5 V	-	-0.49	-	nC
Gate to drain charge	Q_{gd}		-	-1.9	-	
Gate charge total	Q_g		-	-3.55	-	
Gate plateau voltage	$V_{plateau}$		-	-1.9	-	V
Reverse Diode						
Diode continous forward current	I_S	T_A=25 °C	-	-	-0.5	A
Diode pulse current	$I_{S,pulse}$		-	-	-6	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=-1.5 A, T_j=25 °C	-	-0.8	-1.1	V
Reverse recovery time	t_{rr}	V_R=10 V, I_F=-1.5 A, di_F/dt=100 A/µs	-	21.0	-	ns
Reverse recovery charge	Q_{rr}		-	-3.7	-	nC

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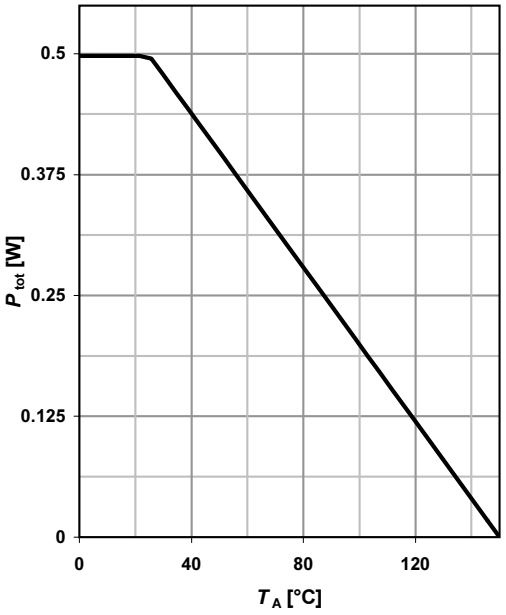
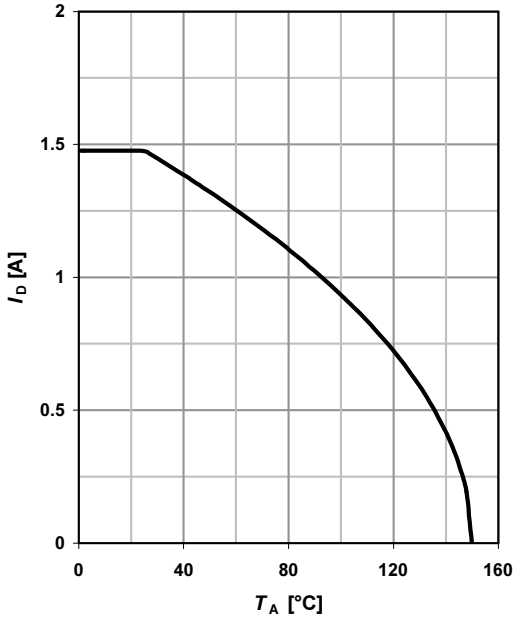
1 Power dissipation

$P_{tot}=f(T_A)$



2 Drain current

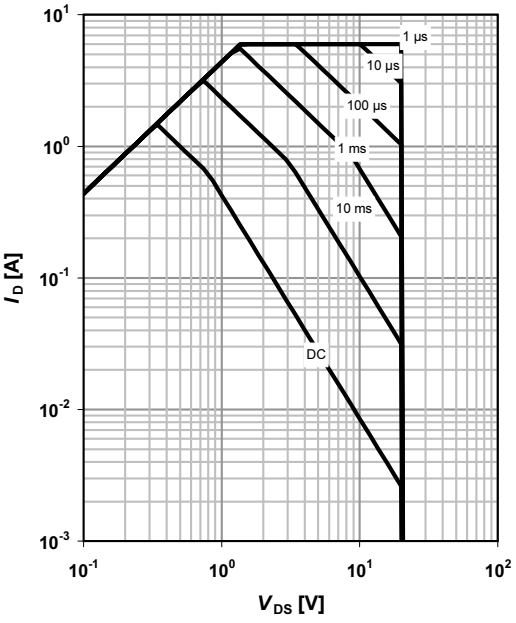
$I_D=f(T_A)$; $V_{GS}\leq$-4.5 V



3 Safe operating area

$I_D=f(V_{DS})$; T_A=25 °C; D=0

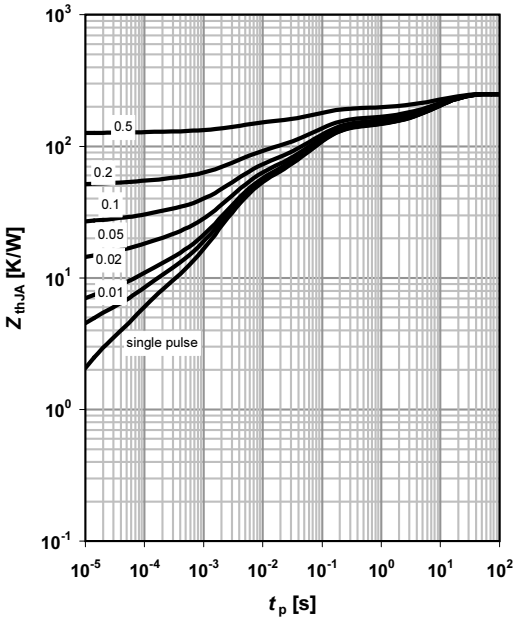
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJA}=f(t_p)$

parameter: $D=t_p/T$



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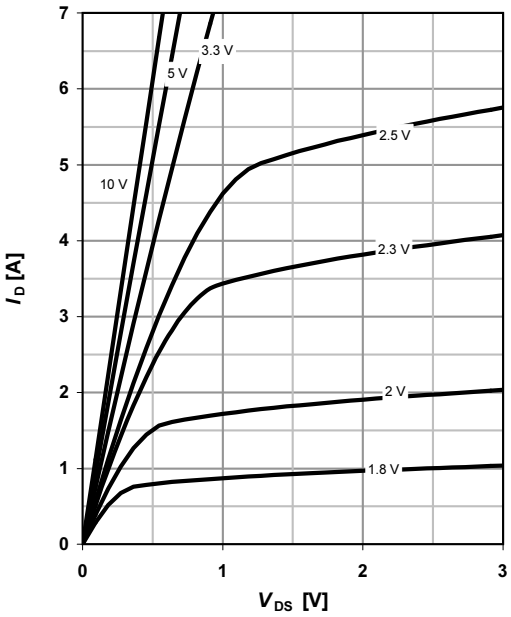
5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

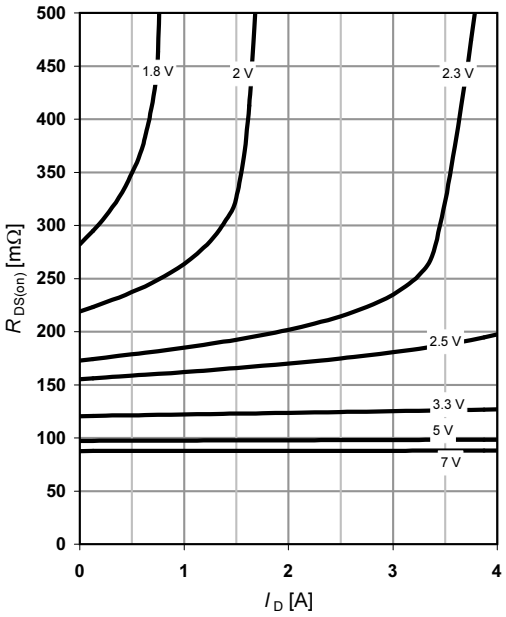
parameter: V_{GS}



6 Typ. drain-source on resistance

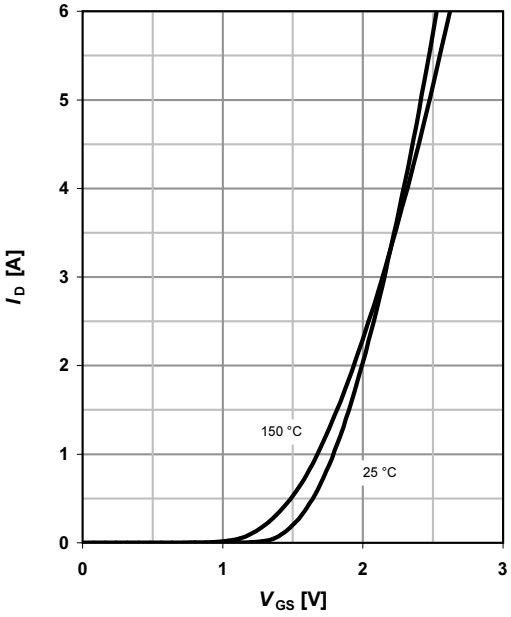
$R_{DS(on)}$=f(I_D); T_j=25 °C

parameter: V_{GS}



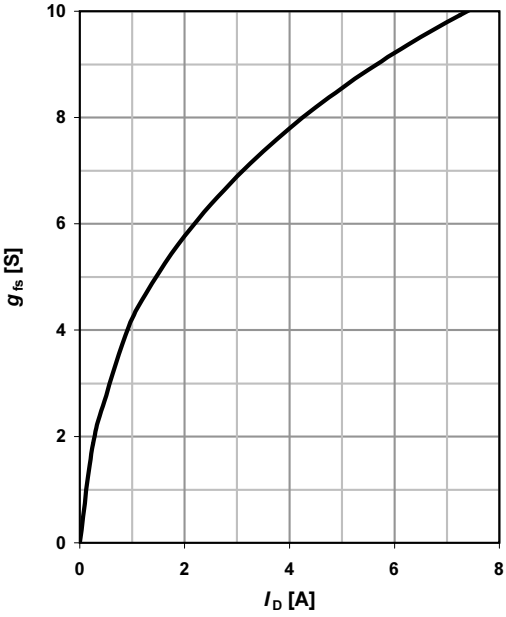
7 Typ. transfer characteristics

I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$



8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



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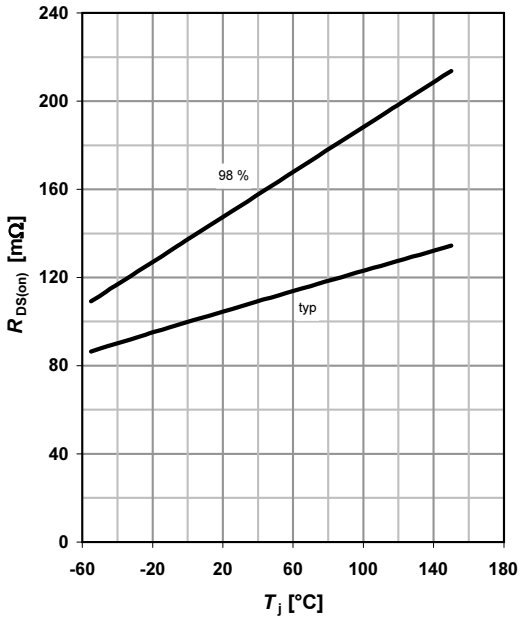
9 Drain-source on-state resistance

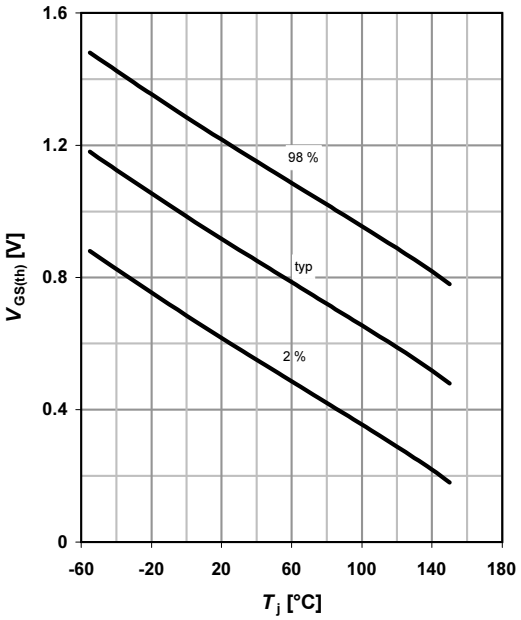
$R_{DS(on)}=f(T_j)$; I_D=-1.5 A; V_{GS}=-4.5 V



10 Typ. gate threshold voltage

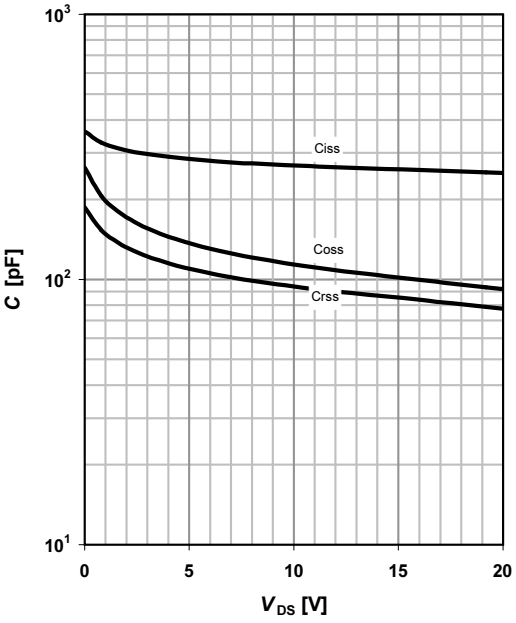
$V_{GS(th)}=f(T_j)$; $V_{DS}=V_{GS}$; I_D=-11 µA

parameter: I_D



11 Typ. capacitances

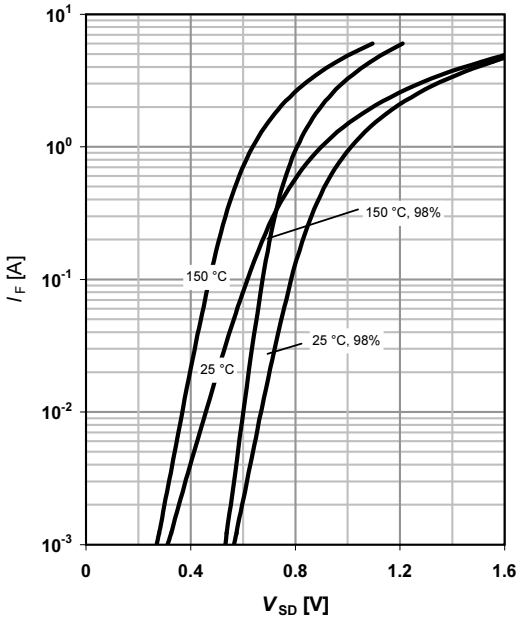
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz; T_j=25°C



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

parameter: T_j



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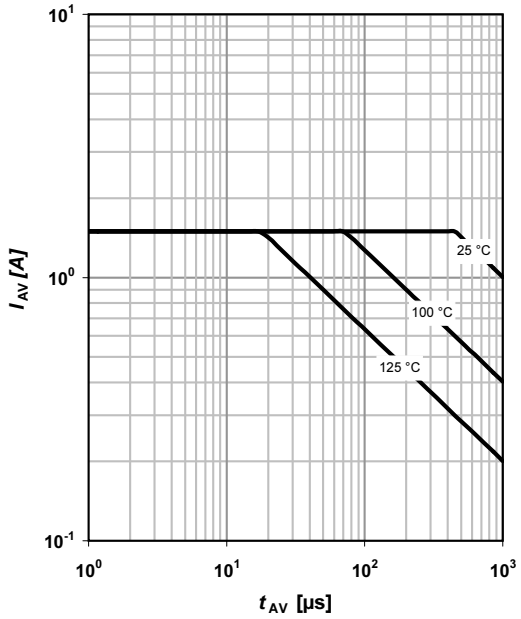
13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25Ω

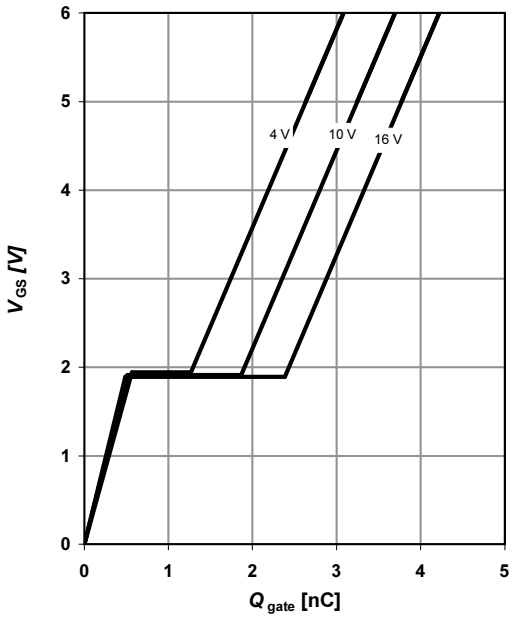
parameter: $T_{j(start)}$



14. Typ. Gate charge

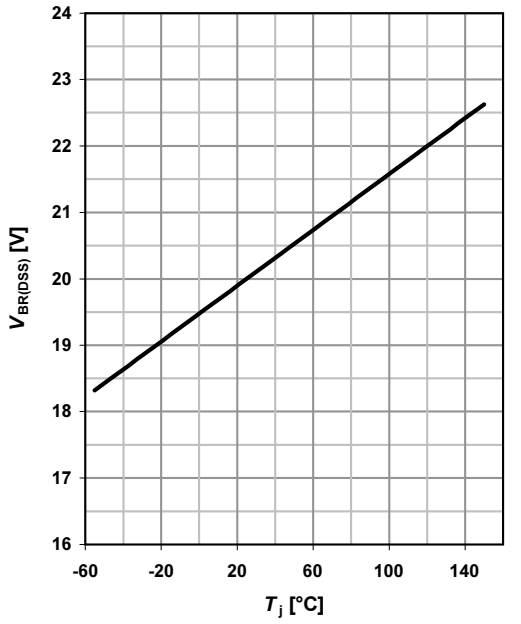
V_{GS}=f(Q_{gate}); ID=-1.5A pulsed

parameter: V_{DD}

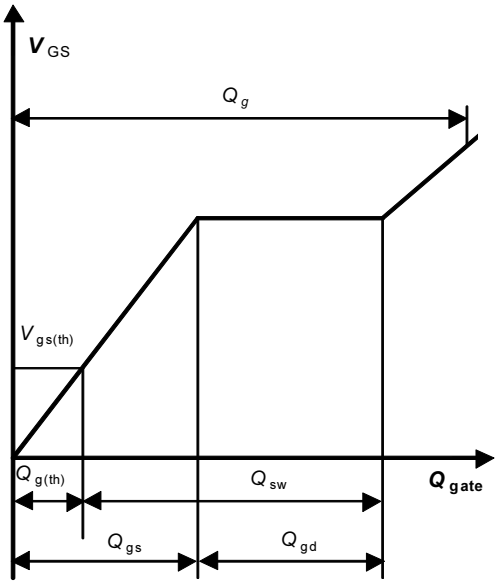


15 Drain-source breackdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=250µA



16 Gate charge waveforms



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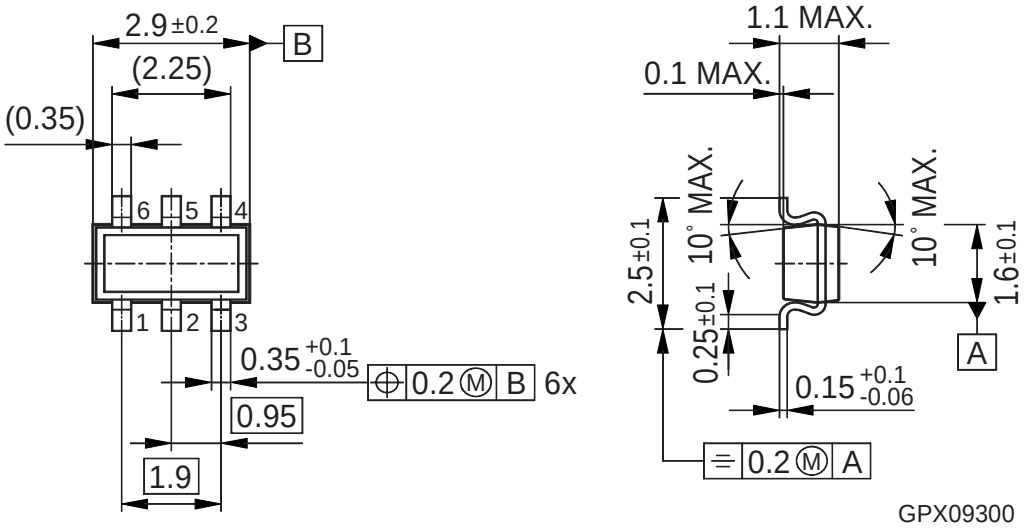
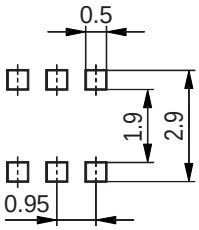
Package Outline:

TSOP6



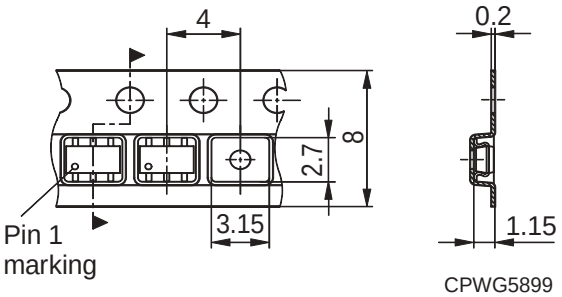
Footprint:



Remark: Wave soldering possible dep. on customers process conditions

HLG09283

Packaging:



Dimensions in mm

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