# SPOC - BTS5461SF

SPI Power Controller
For Advanced Front Light Control

## Data Sheet

Rev. 1.0, 2011-11-17

Automotive Power

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**For Advanced Front Light Control**
**SPI Power Controller**

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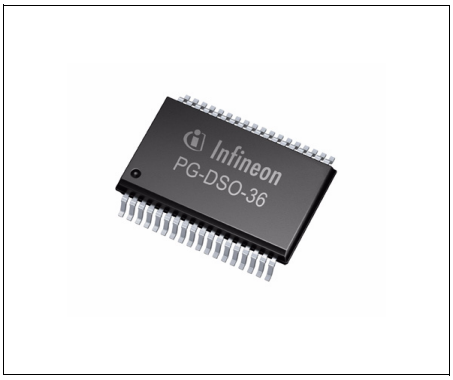
# 1 Overview




PG-DSO-36-43

### Features

- 8 bit serial peripheral interface for control and diagnosis
- 3.3 V and 5 V compatible logic pins
- Very low stand-by current
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LEDs with increased slew rate
- Stable behavior at under voltage
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

### Description

The SPOC - BTS5461SF is a four channel high-side smart power switch in PG-DSO-36-43 package providing embedded protective functions. It is especially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode for channel 2 and channel 3. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is specially designed to drive exterior lamps up to 65W, 27W and 10W and HIDL.

### Product Summary

| | | |
|---|---|---|
| Operating Voltage Power Switch | $V_S$ | 4.5 … 28 V |
| Logic Supply Voltage | $V_{DD}$ | 3.0 … 5.5 V |
| Supply Voltage for Load Dump Protection | $V_{S(LD)}$ | 40 V |
| Maximum Stand-By Current at 25 °C | $I_{S(STB)}$ | 4.5 µA |
| Typical On-State Resistance at $T_j$ = 25 °C<br>channel 0, 1<br>channel 2, 3 | $R_{DS(ON,typ)}$ | <br>3.5 mΩ<br>11 mΩ |
| Maximum On-State Resistance at $T_j$ = 150 °C<br>channel 0, 1<br>channel 2, 3 | $R_{DS(ON,max)}$ | <br>9 mΩ<br>28 mΩ |
| SPI Access Frequency | $f_{SCLK(max)}$ | 5 MHz |

| Type | Package | Marking |
|---|---|---|
| SPOC - BTS5461SF | PG-DSO-36-43 | BTS5461SF |

Configuration and status diagnosis are done via SPI. The SPI is daisy chain capable. The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over load and over temperature flag is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to $V_S$ diagnosis. In OFF state a current source can be switched to the output of one selected channel in order to detect an open load.

The SPOC - BTS5461SF provides a fail-safe feature via limp home input pin.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps.

### Protective Functions

- Reverse battery protection with external components
- Reversave™ - Reverse battery protection by self turn on of all channels
- Short circuit protection
- Over load protection
- Thermal shutdown with latch and dynamic temperature sensor
- Over current tripping
- Over voltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

### Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio ($k_{ILIS}$) configurable for LEDs or bulbs for channel 2 and 3
- Very fast diagnosis in LED mode
- Feedback on over temperature and over load via SPI
- Multiplexed switch bypass monitor provides short circuit to $V_S$ detection
- Integrated, in two steps programmable current source for open load in OFF-state detection

### Application Specific Functions

- Fail-safe activation via LHI pin

### Applications

- High-side power switch for 12 V grounded loads in automotive applications
- Especially designed for standard exterior lighting like high beam, low beam, indicator, parking light and equivalent LEDs
- Load type configuration via SPI (bulbs or LEDs) for optimized load control
- Replaces electromechanical relays, fuses and discrete circuits

# 2 Block Diagram

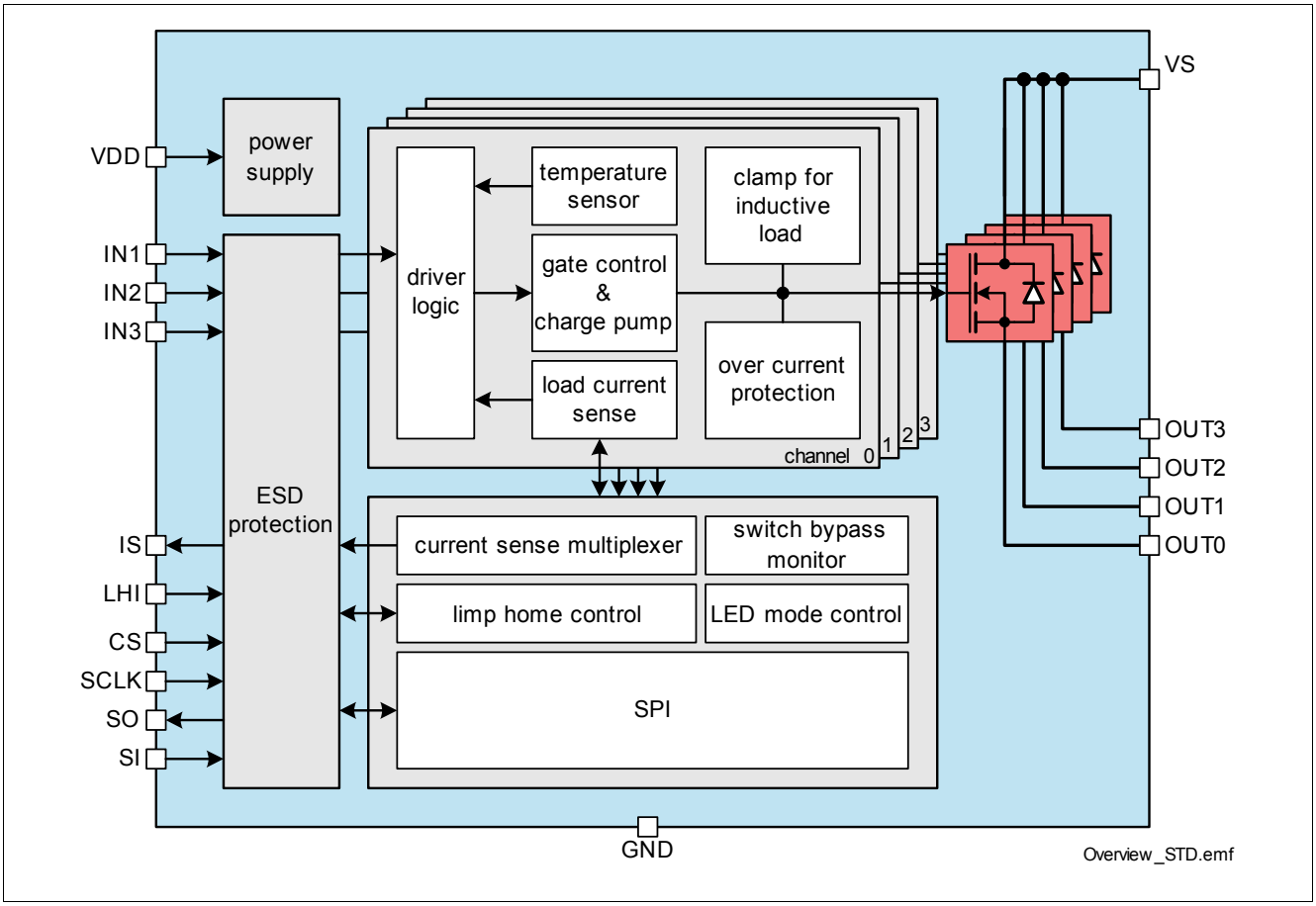



**Figure 1 Block Diagram SPOC - BTS5461SF**

## 2.1 Terms

**Figure 2** shows all terms used in this data sheet.

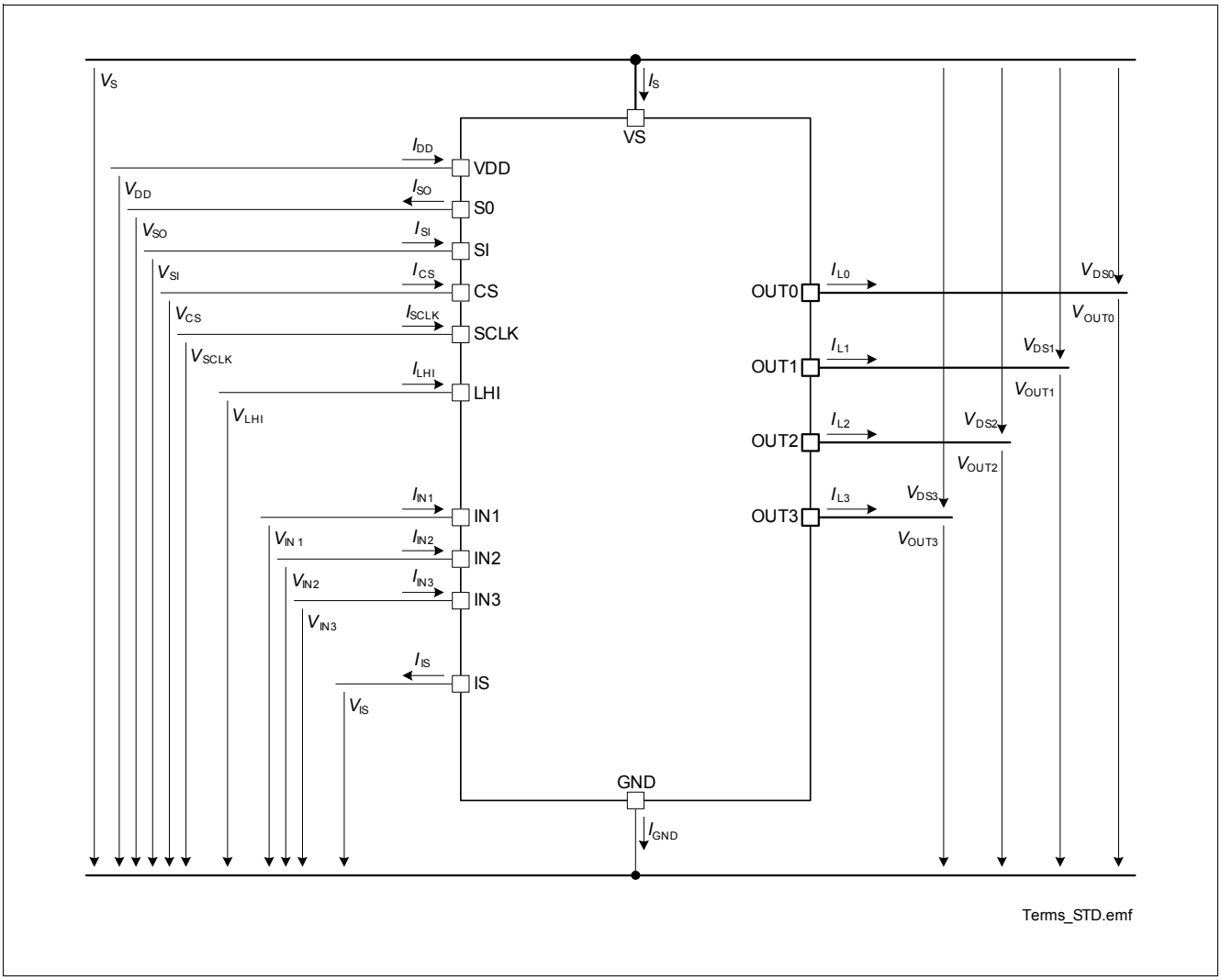



**Figure 2 Terms**

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately (e.g. $V_{DS}$ specification is valid for $V_{DS0}$ ... $V_{DS3}$).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.CL`). In SPI register description, the values in bold letters (e.g. **0**) are default values.

# 3 Pin Configuration

## 3.1 Pin Assignment SPOC - BTS5461SF

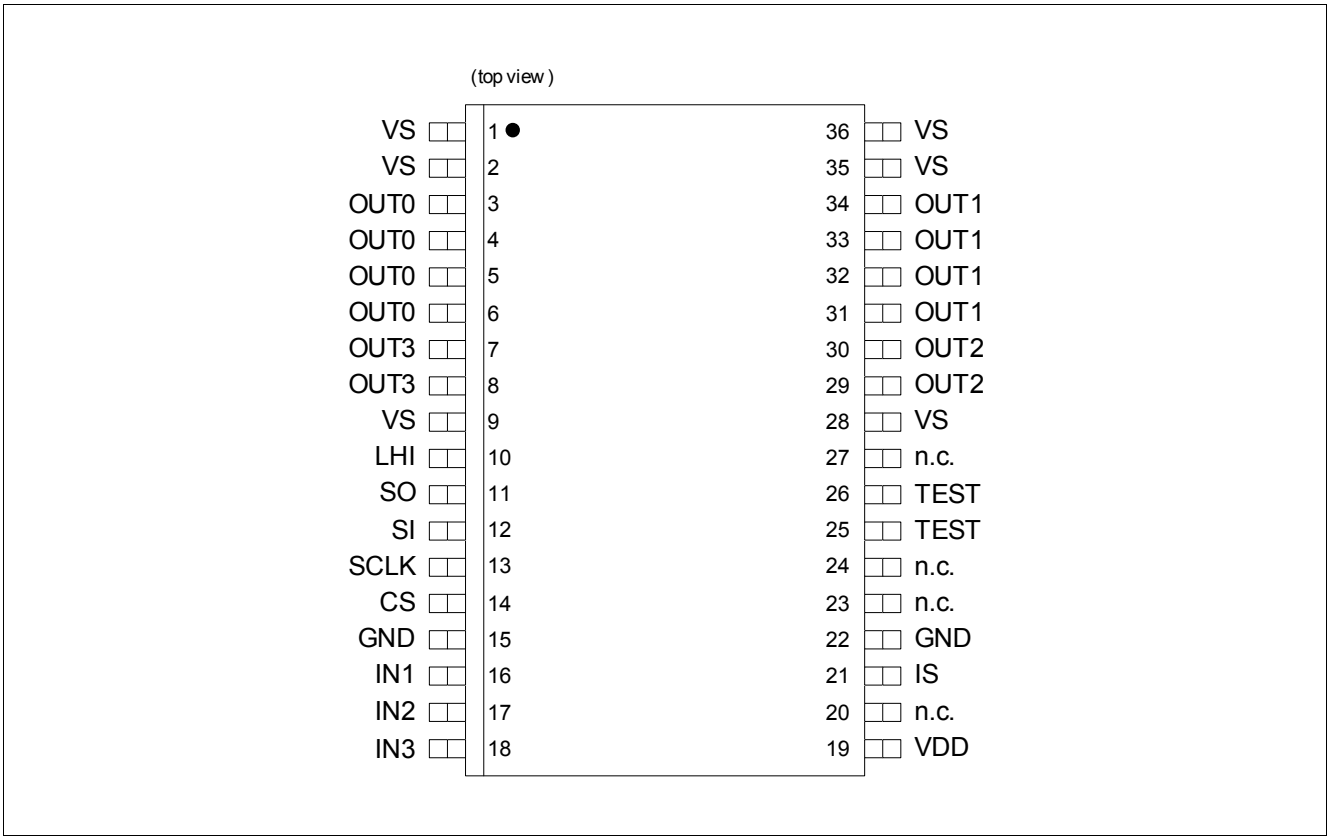



**Figure 3 Pin Configuration PG-DSO-36-43**

## 3.2 Pin Definitions and Functions

| Pin | Symbol | I/O | Function |
|---|---|---|---|
| **Power Supply Pins** | | | |
| 1, 2, 9, 28, 35, 36 [1] | VS | – | Positive power supply for high-side power switch |
| 19 | VDD | – | Logic supply (5 V) |
| 15, 22 | GND | – | Ground connection |
| **Parallel Input Pins (integrated pull-down, leave unused pins unconnected)** | | | |
| 16 | IN1 | I | Input signal of channel 1 (high active) |
| 17 | IN2 | I | Input signal of channel 2 (high active) |
| 18 | IN3 | I | Input signal of channel 3 (high active) |
| **Power Output Pins** | | | |
| 3, 4, 5, 6 [2] | OUT0 | O | Protected high-side power output of channel 0 |
| 31, 32, 33, 34 [2] | OUT1 | O | Protected high-side power output of channel 1 |
| 29, 30 [2] | OUT2 | O | Protected high-side power output of channel 2 |
| 7, 8 [2] | OUT3 | O | Protected high-side power output of channel 3 |
| **SPI & Diagnosis Pins** | | | |
| 14 | CS | I | Chip select of SPI interface (low active); Integrated pull up |
| 13 | SCLK | I | Serial clock of SPI interface |
| 12 | SI | I | Serial input of SPI interface (high active) |
| 11 | SO | O | Serial output of SPI interface |
| 21 | IS | O | Current sense output signal |
| **Limp Home Pin (integrated pull-down, pull-down resistor recommended)** | | | |
| 10 | LHI | I | Limp home activation signal (high active) |
| **Not connected Pins** | | | |
| 20, 23, 24, 27 | n.c. | – | not connected, internally not bonded |
| 25, 26 | TEST | – | Test pins, internally bonded and pulled down, do not connect |

1) All $V_S$ pins have to be connected.

2) All outputs pins of each channel have to be connected.

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Ratings

**Absolute Maximum Ratings [1)]**

$T_j$ = -40 to +150 °C; all voltages with respect to ground (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| **Supply Voltage** | | | | | | |
| 4.1.1 | Power supply voltage | $V_S$ | -0.3 | 28 | V | – |
| 4.1.2 | Logic supply voltage | $V_{DD}$ | -0.3 | 5.5 | V | – |
| 4.1.3 | Reverse polarity voltage according **Figure 26** | $-V_{bat(rev)}$ | – | 16 | V | $T_{jStart}$ = 25 °C<br>$t \leq$ 2 min. [2)] |
| 4.1.4 | Supply voltage for short circuit protection (single pulse) | $V_{S(SC)}$ | | | V | $R_{ECU}$ = 20 mΩ<br>$l$ = 0 or 5 m [3)] |
| | channel 0, 1 | | 0 | 24 | | $R_{Cable}$ = 6 mΩ/m<br>$L_{Cable}$ = 1 µH/m |
| | channel 2, 3 | | 0 | 24 | | $R_{Cable}$ = 16 mΩ/m<br>$L_{Cable}$ = 1 µH/m |
| 4.1.5 | Supply voltage for load dump protection with connected loads | $V_{S(LD)}$ | – | 40 | V | $R_I$ = 2 Ω [4)]<br>$t$ = 400 ms |
| 4.1.6 | Current through ground pin | $I_{GND}$ | – | 25 | mA | $t \leq$ 2 min. |
| 4.1.7 | Current through VDD pin | $I_{DD}$ | -25 | 12 | mA | $t \leq$ 2 min. |
| **Power Stages** | | | | | | |
| 4.1.8 | Load current | $I_L$ | –[5)] | $I_{L(trip)}$ [6)] | A | |
| 4.1.9 | Maximum energy dissipation single pulse | $E_{AS}$ | | | mJ | [7)]<br>$T_{j(0)}$ = 150 °C |
| | channel 0, 1 | | – | 180 | | $I_{L(0)}$ = 5 A |
| | channel 2, 3 | | – | 45 | | $I_{L(0)}$ = 2 A |
| **Diagnosis Pin** | | | | | | |
| 4.1.10 | Current through sense pin IS | $I_{IS}$ | -8 | 8 | mA | $t \leq$ 2 min. |
| **Input Pins** | | | | | | |
| 4.1.11 | Voltage at input pins | $V_{IN}$ | -0.3 | 5.5 | V | – |
| 4.1.12 | Current through input pins | $I_{IN}$ | -0.75<br>-2.0 | 0.75<br>2.0 | mA | –<br>$t \leq$ 2 min. |
| **SPI Pins** | | | | | | |
| 4.1.13 | Voltage at chip select pin | $V_{CS}$ | -0.3 | $V_{DD}$ + 0.3 | V | – |
| 4.1.14 | Current through chip select pin | $I_{CS}$ | -2.0 | 2.0 | mA | $t \leq$ 2 min. |
| 4.1.15 | Voltage at serial input pin | $V_{SI}$ | -0.3 | $V_{DD}$ + 0.3 | V | – |
| 4.1.16 | Current through serial input pin | $I_{SI}$ | -2.0 | 2.0 | mA | $t \leq$ 2 min. |
| 4.1.17 | Voltage at serial clock pin | $V_{SCLK}$ | -0.3 | $V_{DD}$ + 0.3 | V | – |
| 4.1.18 | Current through serial clock pin | $I_{SCLK}$ | -2.0 | 2.0 | mA | $t \leq$ 2 min. |
| 4.1.19 | Voltage at serial output pin | $V_{SO}$ | -0.3 | $V_{DD}$ + 0.3 | V | – |

**Absolute Maximum Ratings** (cont'd)[1)]

$T_j$ = -40 to +150 °C; all voltages with respect to ground

(unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| 4.1.20 | Current through serial output pin | $I_{SO}$ | -2.0 | 2.0 | mA | $t \leq$ 2 min. |
| **Limp Home Pin** | | | | | | |
| 4.1.21 | Voltage at limp home input pin | $V_{LHI}$ | -0.3 | 5.5 | V | – |
| 4.1.22 | Current through limp home input pin | $I_{LHI}$ | -0.75<br>-2.0 | 0.75<br>2.0 | mA | –<br>$t \leq$ 2 min. |
| **Temperatures** | | | | | | |
| 4.1.23 | Junction temperature | $T_j$ | -40 | 150 | °C | – |
| 4.1.24 | Dynamic temperature increase while switching | $\Delta T_j$ | – | 60 | K | – |
| 4.1.25 | Storage temperature | $T_{stg}$ | -55 | 150 | °C | – |
| **ESD Susceptibility** | | | | | | |
| 4.1.26 | ESD susceptibility HBM | $V_{ESD}$ | | | kV | HBM [8)] |
| | OUT pins vs. VS | | -4 | 4 | | – |
| | other pins incl. OUT vs. GND | | -2 | 2 | | – |

1) Not subject to production test, specified by design.

2) Device is mounted on an FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

3) In accordance to AEC Q100-012 and AEC Q101-006.

4) $R_I$ is the internal resistance of the load dump pulse generator.

5) No protection mechanism available. Inverse current needs to be limited by external circuitry to prevent overheating.

6) Over current protection is a protection feature. Operation in over current protection is considered as "outside" normal operating range. Protection features are not designed for continuous repetitive operation.

7) Pulse shape represents inductive switch off: $I_{D(t)} = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$

8) ESD resistivity, HBM according to ANSI/ESDA/JEDEC JS-001-2010

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 4.2.1 | Junction to Soldering Point [1] | $R_{thJSP}$ | – | – | 20 | K/W | measured to pin 1, 2, 9, 28, 35, 36 |
| 4.2.2 | Junction to Ambient [1] | $R_{thJA}$ | – | 35 | – | K/W | [2] |

1) Not subject to production test, specified by design.

2) Specified $R_{thJA}$ values is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

# 5 Power Supply

The SPOC - BTS5461SF is supplied by two supply voltages $V_S$ and $V_{DD}$. The $V_S$ supply line is used by the power switches. The $V_{DD}$ supply line is used by the SPI related circuitry and for driving the SO line. A capacitor between pins VDD and GND is recommended as shown in **Figure 26**.

There is a power-on reset function implemented for the $V_{DD}$ logic power supply. After start-up of the logic power supply, all SPI registers are reset to their default values. The SPI interface including daisy chain function is active as soon as $V_{DD}$ is provided in the specified range independent of $V_S$. First SPI data are the output register values with TER = 1.

Specified parameters are valid for the supply voltage range according $V_{S(nor)}$ or otherwise specified. For the extended supply voltage range according $V_{S(ext)}$ device functionality (switching, diagnosis and protection functions) are still given, parameter deviations are possible.

## 5.1 Power Supply Modes

The following table shows all possible power supply modes for $V_S$, $V_{DD}$ and the pin LHI.

| **Power Supply Modes** | Off | Off | SPI on | Reset | Off | On via INx | Limp Home mode without SPI | Normal operation | Limp Home mode with SPI [1] |
|---|---|---|---|---|---|---|---|---|---|
| $V_S$ | 0 V | 0 V | 0 V | 0 V | 13.5 V | 13.5 V | 13.5 V | 13.5 V | 13.5 V |
| $V_{DD}$ | 0 V | 0 V | 5 V | 5 V | 0 V | 0 V | 0 V | 5 V | 5 V |
| LHI | 0 V | 5 V | 0 V | 5 V | 0 V | 0 V | 5 V | 0 V | 5 V |
| Power stage, protection | – | – | – | – | – | ✓[2] | ✓[2] | ✓ | ✓[2] |
| Limp home | – | – | – | – | – | – | ✓ | – | ✓ |
| SPI (logic) | – | – | ✓ | ✓ | reset | reset | reset | ✓ | reset[3] |
| Stand-by current | – | – | – | – | ✓ | ✓[4] | – | ✓[5] | – |
| Idle current | – | – | – | – | – | – | – | ✓[6] | – |
| Diagnosis | – | – | – | – | – | – | – | ✓ | ✓[7] |

1) SPI read only
2) Channel 1, 2 and/or 3 activated according to the state of INx
3) SPI reset only with applied $V_S$ voltage
4) When INx = low
5) When DCR.MUX = $111_b$ and INx = low
6) When all channels are in OFF-state and DCR.MUX ≠ $111_b$
7) Current sense disabled in limp home mode

### 5.1.1 Stand-by Mode and Device Wake-up Mechanisms

Stand-by mode is entered as soon as the current sense multiplexer (DCR.MUX) is in default (stand-by) position and all input pins are not set. All error latches are cleared automatically in stand-by mode. As soon as stand-by mode is entered, register HWCR.STB is set. To wake-up the device, the current sense multiplexer (DCR.MUX) is programmed different to default (stand-by) position . The power-on wake up time $t_{WU(PO)}$ has to be considered.

Idle mode parameters are valid, when all channels are switched off, but the current sense multiplexer is not in default position, and $V_{DD}$ supply is available.

*Note: A transition from operation to stand-by mode does not reset the SPI registers. So, if $V_{DD}$ is present and SPI is programmed, a changing to MUX = $111_b$ does not reset the SPI registers. An activation of the channels via the input pin INx will wake up the device with the former SPI register settings.*

Activating one of the outputs via the input pins (INx = high) will wake-up the device out of stand-by mode. The power stages are working without VDD supply according to the table above. The output turn-on times will be extended by the stand-by channel wake up time $t_{WU(STCH)}$ as long as no other channel is active. If one channel is active already before channel turn-on times $t_{on}$ (**6.5.12**) can be considered.

*Note: In the operation with $V_{DD}$ = 0 V and INx = high a switching off of all input signals will turn the device in stand-by mode. In stand-by mode the error latches are cleared.*

Limp home (LHI = high) applied for a time longer than $t_{LH(ac)}$ will wake-up the device out of stand-by mode after the power-on wake up time $t_{WU(PO)}$ and it is working without VDD supply. Channels 1, 2 and 3 can be activated via the input pins INx. The error latches can be cleared by a low-high transition at the according input pin.

## 5.2 Reset

There are several reset trigger implemented in the device. They reset the SPI registers including the over temperature latches to their default values. The power stages will switch off, if they are activated via the SPI register `OUTL.n`. If the power stages are activated via the parallel input pins they are not affected by the reset signals. The ERR-flags are cleared by those reset triggers. The over temperature protection and latches are functional after a reset trigger.

*Note: During a reset only the channels 1, 2 and 3 can be activated via the according input pins. The input assigned mode is not available during a reset.*

The first SPI transmission after any kind of reset contains at pin SO the read information from the standard diagnosis, the transmission error bit `TER` is set.

### Power-On Reset

The power-on reset is released, when $V_{DD}$ voltage level is higher than $V_{DD(PO)}$. The SPI interface can be accessed after wake up time $t_{WU(PO)}$.

### Reset Command

There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `HWCR.RST = 1`$_b$, a reset is triggered equivalent to power-on reset. The SPI interface can be accessed after transfer delay time $t_{CS(td)}$.

### Limp Home Mode

The limp home mode will be activated as soon as the pin LHI is set to high for a time longer than $t_{LH(ac)}$. The SPI write-registers are reset with applied $V_S$ voltage. The outputs OUT1 to OUT3 can be activated via the input pins also during activated limp home mode. The error latches can be cleared by a low-high transition at the according input pin. For application example see **Figure 26**. The SPI interface is operating normally, so the limp home register bit LHI as well as the error flags can be read, but any write command will be ignored.

## 5.3 Electrical Characteristics

### Electrical Characteristics Power Supply

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| 5.3.1 | Supply voltage range for normal operation power switch | $V_{S(nor)}$ | 8 | – | 17 | V | – |
| 5.3.2 | Extended supply voltage range for operation power switch | $V_{S(ext)}$ | 4.5 | – | 28[1)] | V | Parameter deviations possible |
| 5.3.3 | Stand-by current for whole device with loads | $I_{S(STB)}$ | <br><br><br>–<br>– | <br><br><br>–<br>– | <br><br><br>4.5<br>28 | µA | $V_{DD}$ = 0 V<br>$V_{LHI}$ = 0 V<br>[1)] $T_j$ = 25 °C<br>[1)] $T_j \leq$ 85 °C |
| 5.3.4 | Idle current for whole device with loads, all channels off | $I_{S(idle)}$ | – | 15 | – | mA | $V_{DD}$ = 5 V<br>DCR.MUX = 110 |
| 5.3.5 | Logic supply voltage | $V_{DD}$ | 3.0 | – | 5.5 | V | – |
| 5.3.6 | Logic supply current | $I_{DD}$ | <br><br><br>–<br>– | <br><br><br>110<br>280 | <br><br><br>–<br>– | µA | $V_{CS}$ = $V_{LHI}$ = 0 V<br>$R_{IS}$ = 2.7 kΩ<br>$V_{IS}$ = 0 V<br>$f_{SCLK}$ = 0 Hz<br>$f_{SCLK}$ = 5 MHz |
| 5.3.7 | Logic stand-by current | $I_{DD(STB)}$ | – | 25 | – | µA | $V_{CS}$ = $V_{DD}$<br>$f_{SCLK}$ = 0 Hz<br>Chip in Stand-by |
| 5.3.8 | Operating current for whole device active | $I_{GND}$ | – | 10 | 25 | mA | $f_{SCLK}$ = 0 Hz |
| **LHI Input Characteristics** | | | | | | | |
| 5.3.9 | L-input level at LHI pin | $V_{LHI(L)}$ | 0 | – | 0.8 | V | – |
| 5.3.10 | H-input level at LHI pin | $V_{LHI(H)}$ | 1.8 | – | 5.5 | V | – |
| 5.3.11 | L-input current through LHI pin | $I_{LHI(L)}$ | 3 | 12 | 80 | µA | [1)] $V_{LHI}$ = 0.6 V |
| 5.3.12 | H-input current through LHI pin | $I_{LHI(H)}$ | 10 | 40 | 80 | µA | $V_{LHI}$ = 5 V |
| **Reset** | | | | | | | |
| 5.3.13 | Power-On reset threshold voltage | $V_{DD(PO)}$ | – | – | 2.4 | V | – |
| 5.3.14 | Power-On wake up time | $t_{WU(PO)}$ | – | – | 200 | µs | [1)] |
| 5.3.15 | Stand-by channel wake up time | $t_{WU(STCH)}$ | – | – | 200 | µs | [1)] |
| 5.3.16 | Limp home acknowledgement time | $t_{LH(ac)}$ | 5 | – | 200 | µs | [1)] |

1) Not subject to production test, specified by design.

*Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature.*

# 6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs (DMOS) with charge pumps. There are four channels implemented in the device. Channels can be switched on via an input pin (please refer to **Section 6.2**) or via SPI register `OUTL`.

## 6.1 Output ON-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage $V_S$ as well as on the junction temperature $T_j$. **Figure 4** shows those dependencies. The behavior in reverse polarity mode is described in **Section 7.5**.

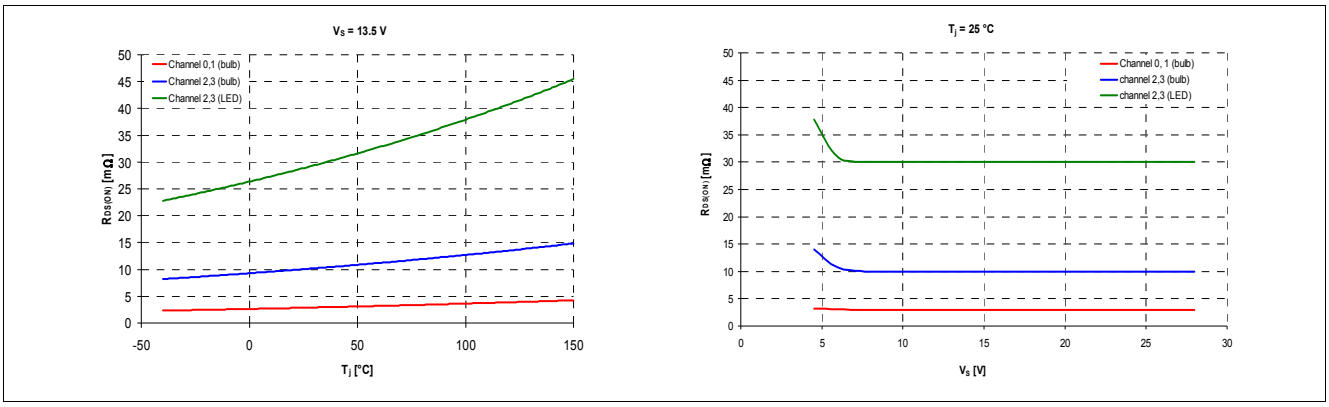



**Figure 4 Typical On-State Resistance**

## 6.2 Input Circuit

The outputs of the SPOC - BTS5461SF can be activated either via the SPI register `OUTL.OUTn` or via the dedicated input pins. There are two different ways to use the input pins, the direct drive mode and the assigned drive mode. The default setting is the direct drive mode. To activate the assigned drive mode the register bit `ICR.INCG` needs to be set.

Additionally, there are two ways of using the input pins in combination with the `OUTL` register by programming the `ICR.COL` parameter.

- `ICR.COL` = $0_b$: A channel is switched on either by the according `OUTL` register bit or the input pin.
- `ICR.COL` = $1_b$: A channel is switched on by the according `OUTL` register bit only, when the input pin is high. In this configuration, a PWM signal can be applied to the input pin and the channel is activated by the SPI register `OUTL`.

**Figure 5** shows the complete input switch matrix.

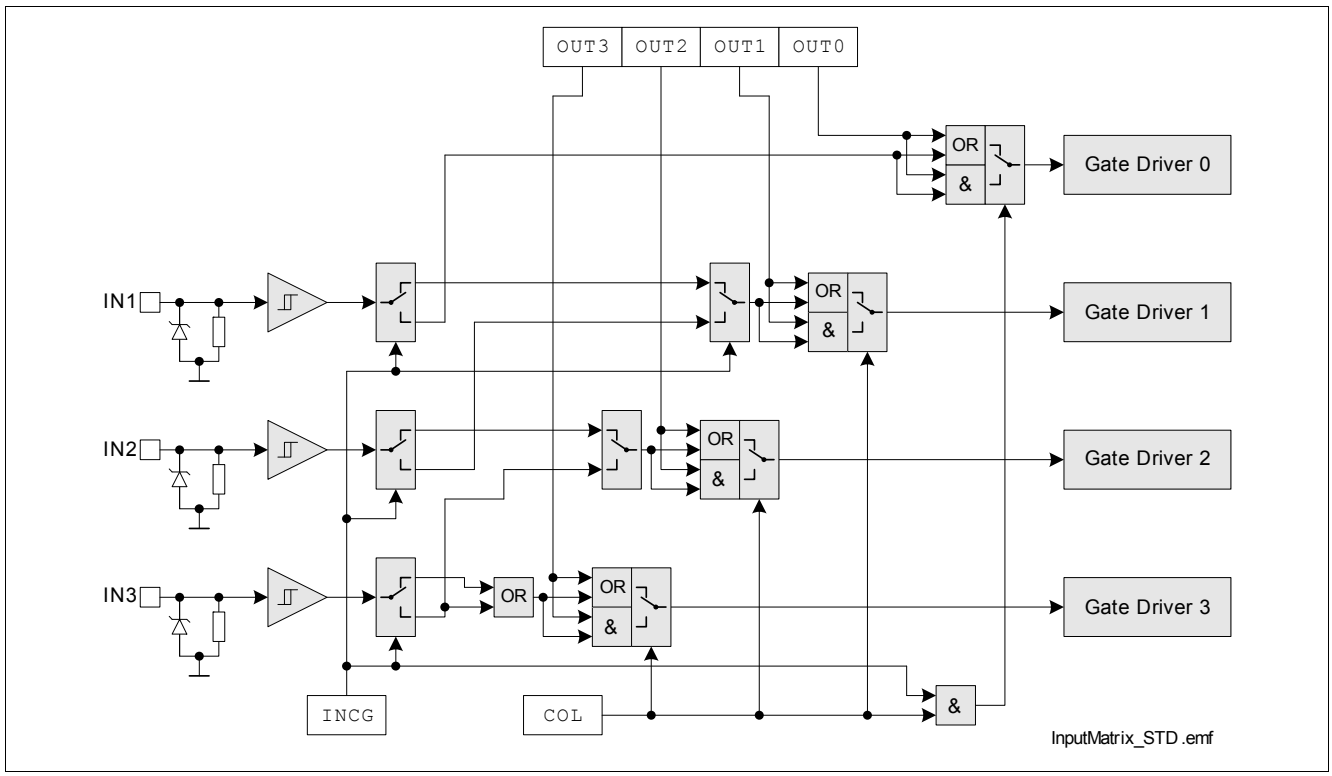



**Figure 5 Input Switch Matrix**

The current sink to ground ensures that the input signal is low in case of an open input pin. The zener diode protects the input circuit against ESD pulses.

### 6.2.1 Input Direct Drive

This mode is the default after the device's wake up and reset. The input pins activate the channels during normal operation (with default setting of bit `ICR.INCG`), stand-by mode and limp home mode. Channel 0 can be activated only via the SPI-bit `OUTL.OUT0` in direct drive mode. The inputs are linked directly to the channels according to:

**Table 1 Direct Drive Mode**

| **Input Pin** | **Assigned channel**, if `ICR.INCG` = $0_b$ |
|---|---|
| IN1 | Channel 1 |
| IN2 | Channel 2 |
| IN3 | Channel 3 |

### 6.2.2 Input Assigned Drive

To activate the assigned drive function the register bit `ICR.INCG` needs to be set. In this mode all output channels can be activated via the input pins. Channel 2 and 3 are assigned to only one input pin. The following mapping is used:

**Table 2 Assigned Drive Mode**

| Input Pin | **Assigned channel**, if `ICR.INCG = 1b` |
|---|---|
| IN1 | Channel 0 |
| IN2 | Channel 1 |
| IN3 | Channel 2, channel 3 |

## 6.3 Power Stage Output

The power stages are built to be used in high side configuration (**Figure 6**).

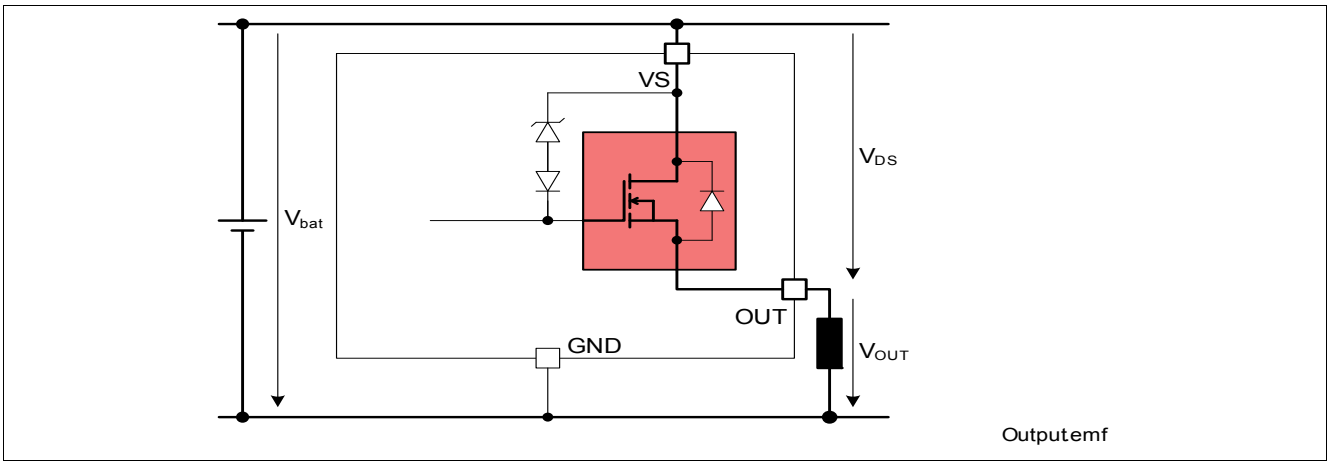



**Figure 6 Power Stage Output**

The power DMOS switches with a dedicated slope, which is optimized in terms of EMC emission. Defined slew rates and edge shaping allow lowest EMC emissions during PWM operation at low switching losses.

### 6.3.1 Bulb and LED mode

Channel 2 and channel 3 can be configured in bulb and LED mode via the SPI registers `HWCR.LEDn`. During LED mode following parameters are changed for an optimized functionality with LED loads: On-state resistance $R_{DS(ON)}$, switching timings ($t_{delay(ON)}$, $t_{delay(OFF)}$, $t_{ON}$, $t_{OFF}$), slew rates $dV/dt_{ON}$ and $dV/dt_{OFF}$, current protections $I_{L(trip)}$ and current sense ratio $k_{ILIS}$.

### 6.3.2 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates can be considered.

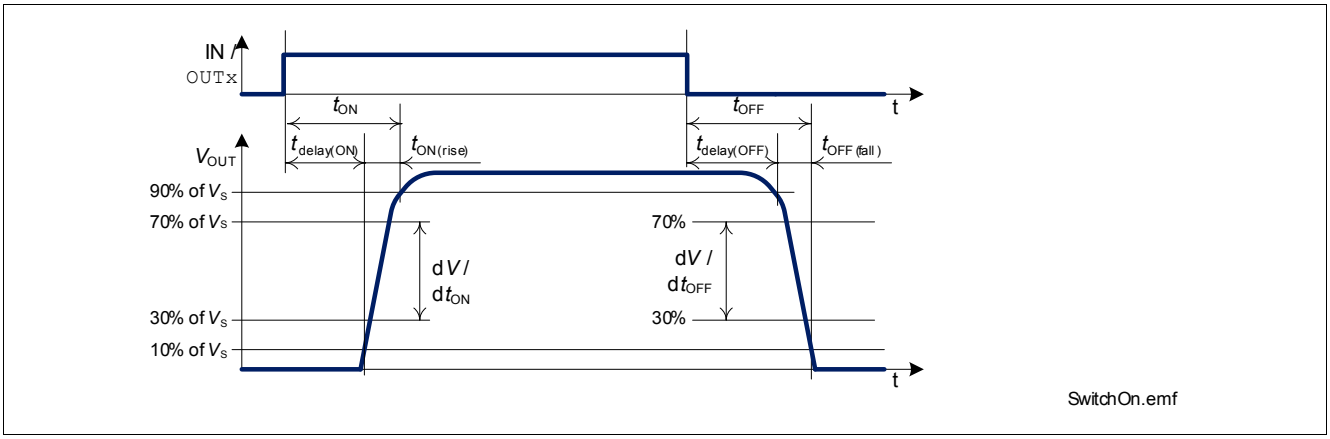



**Figure 7 Switching a Load (resistive)**

### 6.3.3 Switching Inductive Loads

When switching off inductive loads with high-side switches, the voltage $V_{OUT}$ drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a voltage clamp mechanism implemented, which limits that negative output voltage to a certain level ($V_{DS(CL)}$ (**6.5.2**)). See **Figure 6** for details. The device provides SmartClamp functionality. To increase the energy capability, the clamp voltage $V_{DS(CL)}$ increases with the junction temperature $T_j$ and load current $I_L$. Please refer also to **Section 7.6**. The maximum allowed load inductance is limited.

### 6.3.4 Switching high inrush loads

When switching loads with high inrush currents like e.g. high capacitive loads, it has to be ensured that in normal operating range the maximum load current is below the current trip level of the device. If the current trip level is touched, the device would operate under fault conditions that are considered as outside normal operating range. In this case absolute maximum ratings are exceeded ($I_{Ltrip}$ (**4.1.8**)). Please refer to **Section 4** and **Section 7** for further information.

## 6.4 Inverse Current Behavior

During inverse currents ($V_{OUT} > V_S$) the affected channel stays in ON- or in OFF-state. Furthermore, during applied inverse currents no ERR-flag is set.

The functionality of unaffected channels is not influenced by inverse currents applied to other channels (except effects due to junction temperature increase). Influences on the diagnostic function of unaffected channels are possible only for the current sense ratio, please refer to $\Delta k_{ILIS(IC)}$ (**8.5.3**).

*Note: No protection mechanism like temperature protection or current protection is active during applied inverse currents. Inverse currents cause power losses inside the DMOS, which increase the overall device temperature, which could lead to a switch off of the unaffected channels due to over temperature.*

.

## 6.5 Electrical Characteristics

### Electrical Characteristics Power Stages

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Output Characteristics** | | | | | | | |
| 6.5.1 | On-state resistance | $R_{DS(ON)}$ | | | | mΩ | |
| | channel 0, 1 | | | | | | $I_L$ = 7.5 A |
| | | | – | 3.5 | – | | [1] $T_j$ = 25 °C |
| | | | – | 7 | 9 | | $T_j$ = 150 °C |
| | channel 2, 3 | | | | | | `HWCR.LEDn = 0` |
| | | | | | | | $I_L$ = 2.6 A |
| | | | – | 11 | – | | [1] $T_j$ = 25 °C |
| | | | – | 22 | 28 | | $T_j$ = 150 °C |
| | | | | | | | `HWCR.LEDn = 1` |
| | | | | | | | $I_L$ = 0.6 A |
| | | | – | 39 | – | | [1] $T_j$ = 25 °C |
| | | | – | 78 | 100 | | $T_j$ = 150 °C |
| 6.5.2 | Output clamp | $V_{DS(CL)}$ | | | | V | |
| | channel 0, 1 | | 32 | – | 54 | | $T_j$ = 25 °C<br>$I_L$ = 20 mA |
| | | | 40 | – | 55 | | [1] $T_j$ = 150 °C<br>$I_L$ = 6 A |
| | channel 2, 3 | | 32 | – | 54 | | $T_j$ = 25 °C<br>$I_L$ = 20 mA |
| | | | 40 | – | 55 | | [1] $T_j$ = 150 °C<br>$I_L$ = 2 A |
| 6.5.3 | Output leakage current per channel in stand-by | $I_{L(OFFSTB)}$ | | | | µA | `OUTL.OUTn = 0`<br>`DCR.MUX = 111` |
| | channel 0, 1 | | – | – | 2 | | $T_j$ = 25 °C |
| | | | – | – | 10 | | [1] $T_j$ = 85 °C |
| | | | – | – | 50 | | [1] $T_j$ = 105 °C |
| | channel 2, 3 | | – | – | 1 | | $T_j$ = 25 °C |
| | | | – | – | 4 | | [1] $T_j$ = 85 °C |
| | | | – | – | 20 | | [1] $T_j$ = 105 °C |
| 6.5.4 | Output leakage current per channel in idle mode | $I_{L(OFFidle)}$ | | | | µA | `OUTL.OUTn = 0`<br>`DCR.MUX ≠ 111` |
| | channel 0, 1 | | – | – | 60 | | [1] $T_j$ = 85 °C |
| | | | – | – | 80 | | [1] $T_j$ = 105 °C |
| | | | – | – | 530 | | $T_j$ = 150 °C |
| | channel 2, 3 | | – | – | 45 | | [1] $T_j$ = 85 °C |
| | | | – | – | 50 | | [1] $T_j$ = 105 °C |
| | | | – | – | 230 | | $T_j$ = 150 °C |

**Electrical Characteristics Power Stages** (cont'd)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| 6.5.5 | Inverse current capability per channel<br>channel 0, 1<br>channel 2, 3 | $-I_{L(IC)}$ | <br>6<br>2 | <br>–<br>– | <br>–<br>– | A | [1] No influences on switching functionality of unaffected channels, $k_{ILIS}$ influence according $\Delta k_{ILIS(IC)}$ (8.5.3) |
| **Input Characteristics** | | | | | | | |
| 6.5.6 | L-input level | $V_{IN(L)}$ | 0 | – | 0.8 | V | – |
| 6.5.7 | H-input level | $V_{IN(H)}$ | 1.8 | – | 5.5 | V | – |
| 6.5.8 | L-input current | $I_{IN(L)}$ | 3 | 12 | 80 | µA | [1] $V_{IN}$ = 0.6 V |
| 6.5.9 | H-input current | $I_{IN(H)}$ | 10 | 40 | 80 | µA | $V_{IN}$ = 5 V |

**Electrical Characteristics Power Stages** (cont'd)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Timings** | | | | | | | |
| 6.5.10 | Turn-ON delay to 10% $V_S$ | $t_{delay(ON)}$ | | | | µs | [1] $V_S$ = 13.5 V |
| | channel 0, 1 | | – | 35 | – | | – |
| | channel 2, 3 | | – | 25 | – | | HWCR.LEDn = 0 |
| | | | – | 8 | – | | HWCR.LEDn = 1 |
| 6.5.11 | Turn-OFF delay to 90% $V_S$ | $t_{delay(OFF)}$ | | | | µs | [1] $V_S$ = 13.5 V |
| | channel 0, 1 | | – | 55 | – | | – |
| | channel 2, 3 | | – | 30 | – | | HWCR.LEDn = 0 |
| | | | – | 10 | – | | HWCR.LEDn = 1 |
| 6.5.12 | Turn-ON time to 90% $V_S$ including turn-ON delay | $t_{ON}$ | | | | µs | $V_S$ = 13.5 V<br>DCR.MUX ≠ 111 |
| | channel 0, 1 | | – | – | 100 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | – | – | 100 | | HWCR.LEDn = 0<br>$R_L$ = 6.8 Ω |
| | | | – | – | 50 | | HWCR.LEDn = 1<br>$R_L$ = 33 Ω |
| 6.5.13 | Turn-OFF time to 10% $V_S$ including turn-OFF delay | $t_{OFF}$ | | | | µs | $V_S$ = 13.5 V |
| | channel 0, 1 | | – | – | 150 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | – | – | 110 | | HWCR.LEDn = 0<br>$R_L$ = 6.8 Ω |
| | | | – | – | 50 | | HWCR.LEDn = 1<br>$R_L$ = 33 Ω |
| 6.5.14 | Turn-ON rise time from 10% to 90% $V_S$ | $t_{ON(rise)}$ | | | | µs | $V_S$ = 13.5 V<br>DCR.MUX ≠ 111 |
| | channel 0, 1 | | – | – | 55 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | – | – | 55 | | HWCR.LEDn = 0<br>$R_L$ = 6.8 Ω |
| | | | – | – | 11 | | HWCR.LEDn = 1<br>$R_L$ = 33 Ω |
| 6.5.15 | Turn-OFF fall time from 90% to 10% $V_S$ | $t_{OFF(fall)}$ | | | | µs | $V_S$ = 13.5 V |
| | channel 0, 1 | | – | – | 55 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | – | – | 55 | | HWCR.LEDn = 0<br>$R_L$ = 6.8 Ω |
| | | | – | – | 11 | | HWCR.LEDn = 1<br>$R_L$ = 33 Ω |

**Electrical Characteristics Power Stages** (cont'd)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| 6.5.16 | Turn-ON/OFF matching | $\lvert t_{ON} - t_{OFF} \rvert$ | | | | µs | $V_S$ = 13.5 V |
| | channel 0, 1 | | – | – | 90 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | – | – | 70 | | HWCR.LEDn = 0<br>$R_L$ = 6.8 Ω |
| | | | – | – | 50 | | HWCR.LEDn = 1<br>$R_L$ = 33 Ω |
| 6.5.17 | Turn-ON slew rate<br>30% to 70% $V_S$ | $dV/dt_{ON}$ | | | | V/µs | $V_S$ = 13.5 V |
| | channel 0, 1 | | 0.2 | 0.7 | 2.0 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | 0.2 | 0.9 | 2.5 | | HWCR.LEDn = 0<br>$R_L$ = 6.8 Ω |
| | | | 0.6 | 2.5 | 6.0 | | HWCR.LEDn = 1<br>$R_L$ = 33 Ω |
| 6.5.18 | Turn-OFF slew rate<br>70% to 30% $V_S$ | $-dV/dt_{OFF}$ | | | | V/µs | $V_S$ = 13.5 V |
| | channel 0, 1 | | 0.2 | 0.7 | 2.0 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | 0.2 | 0.9 | 2.5 | | HWCR.LEDn = 0<br>$R_L$ = 6.8 Ω |
| | | | 0.6 | 2.5 | 6.0 | | HWCR.LEDn = 1<br>$R_L$ = 33 Ω |

1) Not subject to production test, specified by design.

# 7 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

## 7.1 Over Current Protection

The maximum load current $I_L$ is switched off in case of exceeding the over current trip level $I_{L(trip)}$ by the device itself. Depending on the total short circuit impedance higher current over shoots may occur. A limited auto-restart function is implemented. The number of restarts is dependent of the $V_{DS}$ voltage. Please refer to following figures for details.

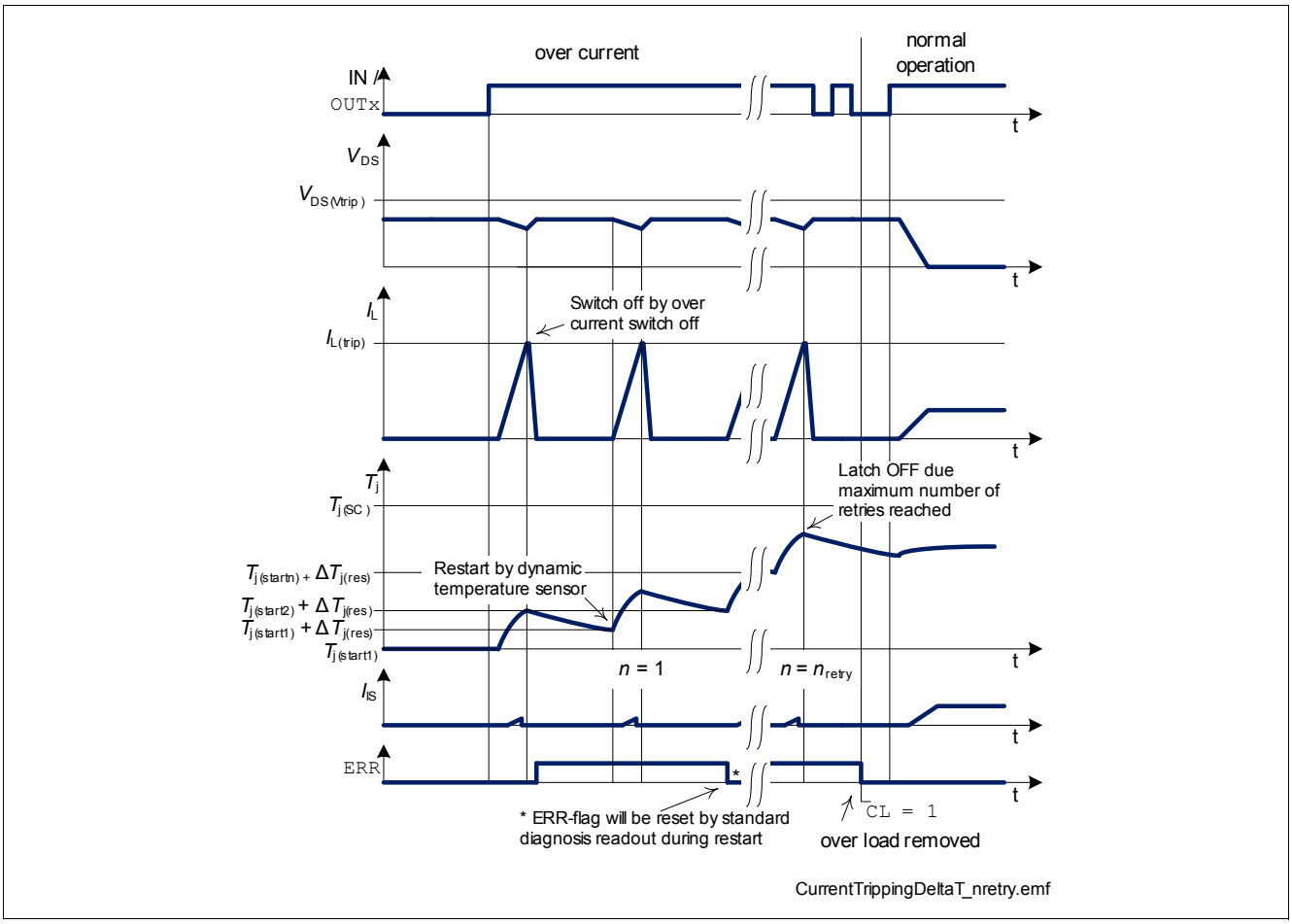



**Figure 8 Over current protection with latch due to reaching maximum number of retries $n_{retry}$**

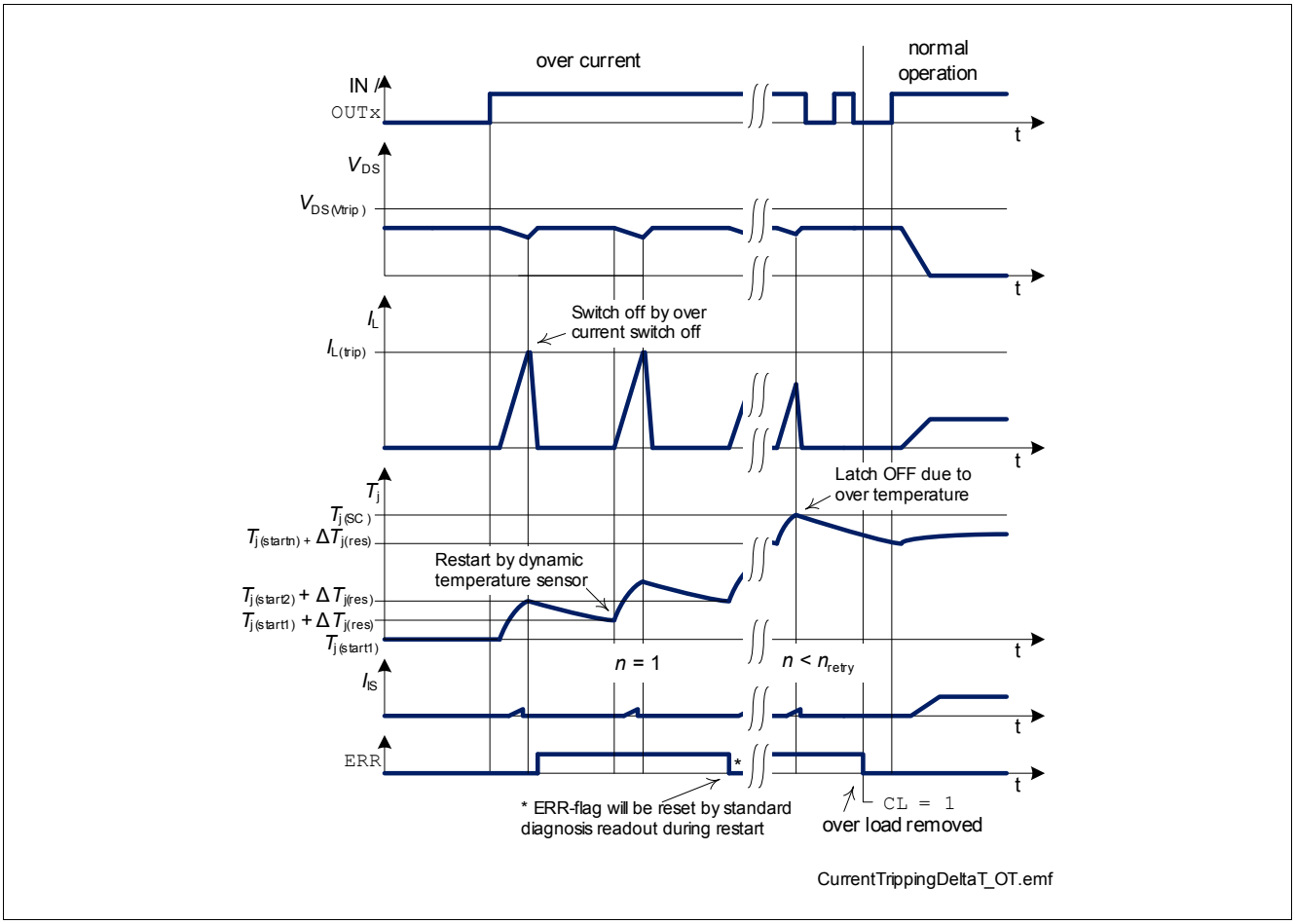



**Figure 9 Over current protection with latch due to reaching over temperature $T_{j(SC)}$**

The ERR-flag will be set during over current shut down. It can be reset by reading the ERR-flag. If the channel is still in over current shut down, the ERR-flag will be set again. During the automatic restart of the channel the ERR-flag can be cleared by reading the ERR-flag. It will be set again as soon as the over current protection is activated again.

The number of restarts $n_{retry}$ is depending on the $V_{DS}$ voltage according to the following figure and **Chapter 7.2**.

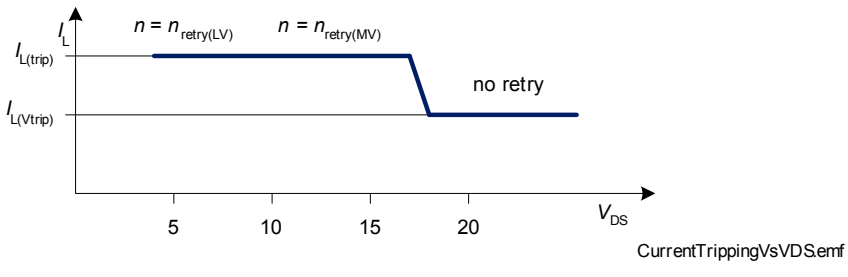



**Figure 10 Number of retries and trip levels dependent of $V_{DS}$**

The retry latch or over temperature latch is cleared by SPI command `HWCR.CL = 1b`. If the input pin or the bit in the SPI register `OUTL` is still set, the channel will be turned on immediately after the command `HWCR.CL = 1b`. To prevent degradation of the device it is recommended to wait $t_{reset(CL)}$ (**7.9.9**) until resetting the latch.

## 7.2 Over Current Protection at high $V_{DS}$

The SPOC - BTS5461SF provides an over current protection for $V_{DS}$ > $V_{DS(Vtrip)}$ (7.9.5). For $V_{DS}$ > $V_{DS(Vtrip)}$ and $I_L$ > $I_{L(Vtrip)}$ during turn on the channel switches off and latches immediately. For details please refer to parameter $I_{L(VTRIP)}$ (7.9.4).

The current trip level $I_{L(Vtrip)}$ is below the current trip level $I_{L(trip)}$ at $V_{DS}$ = 7V. The ratio between $I_{L(trip)}$ and $I_{L(Vtrip)}$ is defined by the parameter $\Delta k_{TR}$ (7.9.6).

The over current latch is cleared by SPI command HWCR.CL = $1_b$. If the input pin or the bit in the SPI register OUTL is still set, the channel will be turned on immediately after the command HWCR.CL = $1_b$. To prevent degradation of the device it is recommended to wait $t_{reset(CL)}$ (7.9.9) until resetting the latch.

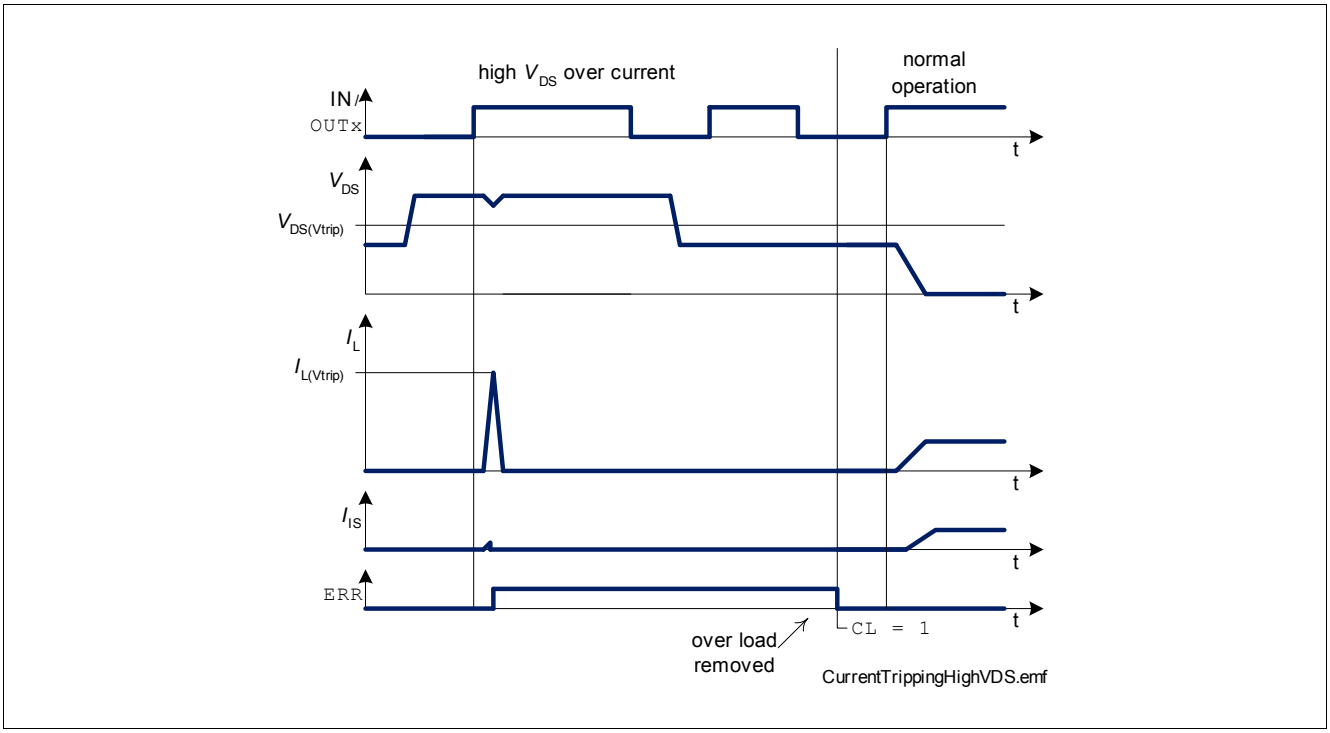



**Figure 11 Over current protection in case of high $V_{DS}$ voltages**

## 7.3 Over Current Protection for Short Circuit Type 2 Protection

After activation of the channels without over temperature shutdown and after the delay time $t_{delay(trip)}$ (7.9.2) the over current protection threshold $I_{L(trip)}$ is reduced to $I_{L(Itrip)}$. The delay time $t_{delay(trip)}$ is reset by an dynamic temperature sensor or over current shutdown and any IN or OUTL. In case of a short circuit to GND event with $I_L$ > $I_{L(Itrip)}$ (7.9.3), which occurs in the on state, the channel is switched off and latched immediately. For more details, please refer to the figure Figure 12.

The current trip level $I_{L(Itrip)}$ is below the current trip level $I_{L(trip)}$ at $V_{DS}$ = 7V. The ratio between $I_{L(trip)}$ and $I_{L(Itrip)}$ is defined by the parameter $\Delta k_{TR}$ (7.9.6).

The over current latch is cleared by SPI command HWCR.CL = $1_b$. If the input pin or the bit in the SPI register OUTL is still set, the channel will be turned on immediately after the command HWCR.CL = $1_b$. To prevent degradation of the device it is recommended to wait $t_{reset(CL)}$ (7.9.9) until resetting the latch.

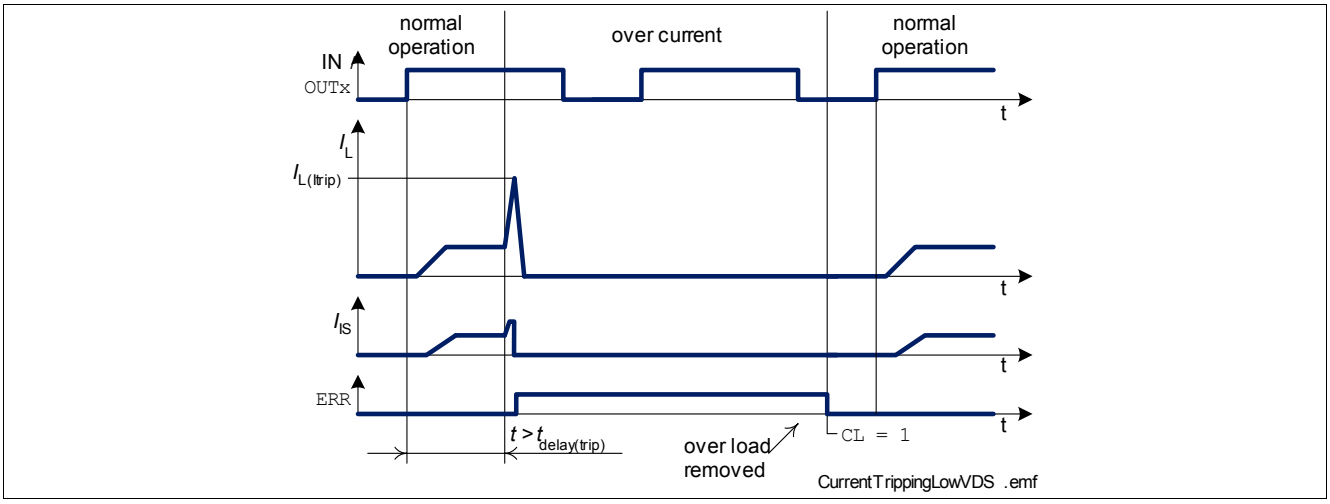



**Figure 12 Shut Down by Over Current due to Short Circuit Type 2**

## 7.4 Over Temperature Protection

Each channel has its own temperature sensor. If the temperature at the channel exceeds the thermal shutdown temperature $T_{j(SC)}$, the channel will switch off and latch to prevent destruction (also in case of $V_{DD}$ = 0V). In order to reactivate the channel, the temperature at the output must drop by at least the thermal hysteresis $\Delta T_j$ and the over temperature latch must be cleared by SPI command `HWCR.CL = 1b`. If the input pin or the bit in the SPI register `OUTL` is still set, the channel will be turned on immediately after the command `HWCR.CL = 1b`.To prevent degradation of the device it is recommended to wait $t_{reset(CL)}$ (7.9.9) until resetting the latch.

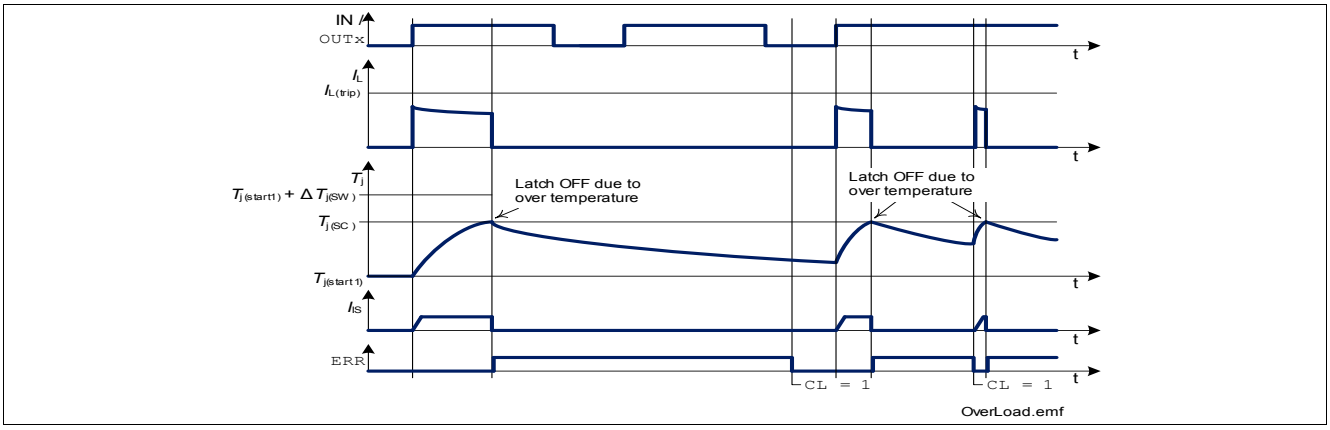



**Figure 13 Shut Down by Over Temperature**

### 7.4.1 Dynamic Temperature Sensor Protection

Additionally, each channel has its own dynamic temperature sensor. The dynamic temperature sensor improves short circuit robustness by limiting sudden increases in the junction temperature. The dynamic temperature sensor turns off the channel if its sudden temperature increase exceeds the dynamic temperature sensor threshold $\Delta T_{j(SW)}$. The number of automatic reactivations is limited by $n_{retry}$ (7.9.7). If this number of retries is exceeded the channel turns off and latches. The retry latch is cleared by SPI command `HWCR.CL = 1b`. If the input pin or the bit in the SPI register `OUTL` is still set, the channel will be turned on immediately after the command `HWCR.CL = 1b`. To prevent degradation of the device it is recommended to wait $t_{reset(CL)}$ (7.9.9) until resetting the latch. For the condition $n < n_{retry}$the counter of automatic reactivations will be reset by every low to high transition on the input pin or the bit in SPI register `OUTL`.

Please refer to **Figure 12** for details.

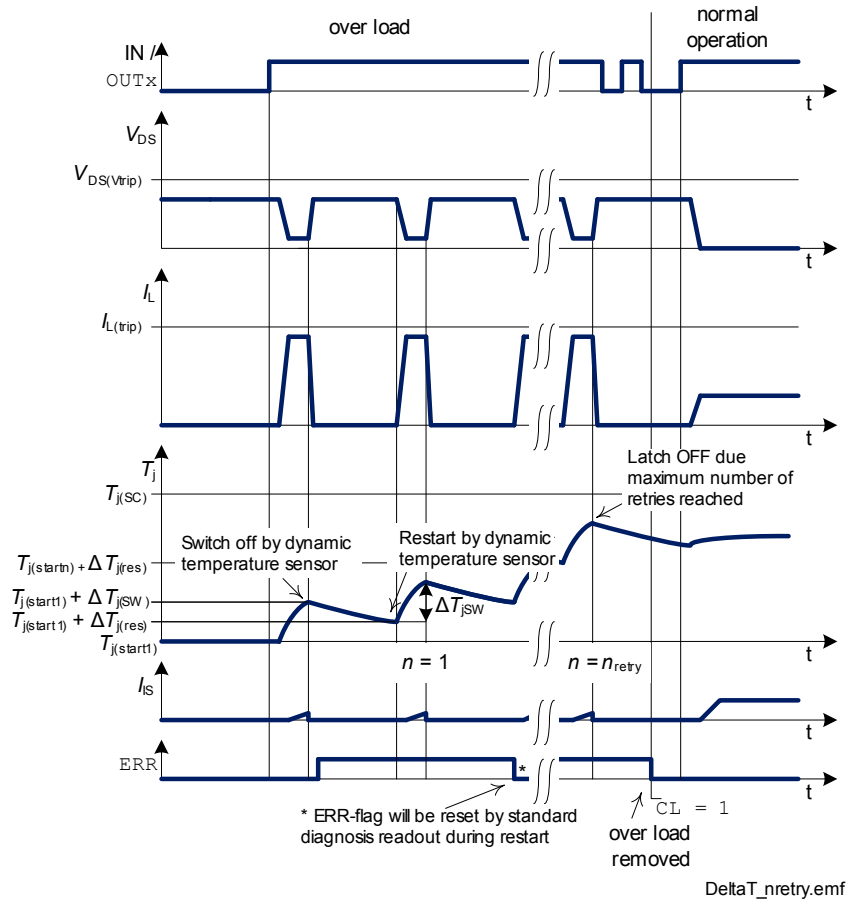



**Figure 14 Dynamic Temperature Sensor Operations with latch due to reaching maximum number of retries $n_{retry}$**

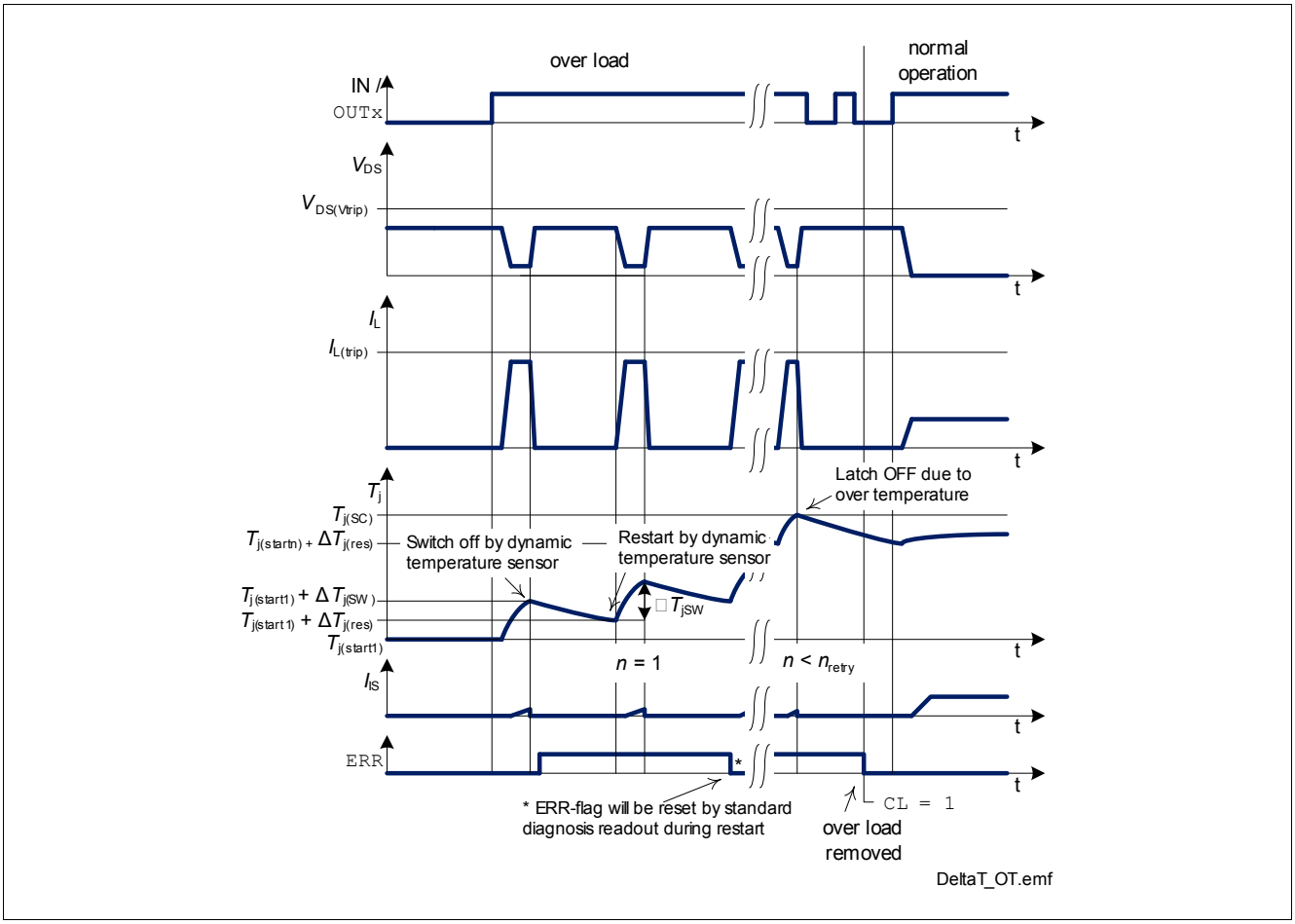



**Figure 15 Dynamic Temperature Sensor Operations with latch due to reaching over temperature $T_{j(SC)}$**

The ERR-flag will be set during dynamic temperature sensor shut down. It can be reset by reading the ERR-flag. If the channel is still in dynamic temperature sensor shut down, the ERR-flag will be set again. During the automatic restart of the channel the ERR-flag can be cleared by reading the ERR-flag. It will be set again as soon as the dynamic temperature sensor is activated again.

## 7.5 Reverse Polarity Protection - Reversave™

In reverse polarity mode, power dissipation is caused by the reverse ON-state resistance $R_{DS(REV)}$ of each channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads. The current through the sense pin IS, the logic power supply pin VDD, the SPI pins, input pins and the limp home input pin has to be limited as well (please refer to the maximum ratings listed on **Page 9**).

For reducing the power loss during reverse polarity Reversave™ functionality is implemented for all channels. They are turned on to almost forward condition in reverse polarity condition, see parameter $R_{DS(REV)}$.

*Note: No protection mechanism like temperature protection or current protection is active during reverse polarity.*

## 7.6 Over Voltage Protection

In the case of supply voltages between $V_{S(SC)\,max}$ and $V_{S(CL)}$ the output transistors are still operational and follow the input or the OUTL register. Parameters are not warranted and lifetime is reduced compared to normal mode.

In addition to the output clamp for inductive loads as described in **Section 6.3**, there is a clamp mechanism available for over voltage protection for the logic and all channels.

## 7.7 Loss of Ground

In case of complete loss of the device ground connections, but connected load ground, the SPOC - BTS5461SF securely changes to or stays in OFF-state.

## 7.8 Loss of $V_S$

In case of loss of $V_S$ connection in on-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from VS to GND. For example, a suppressor diode is recommended between VS and GND.

## 7.9 Electrical Characteristics

### Electrical Characteristics Protection Functions

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Over Load Protection** | | | | | | | |
| 7.9.1 | Load current trip level | $I_{L(trip)}$ | | | | A | $V_{DS}$ < 7 V |
| | channel 0, 1 | | 71 | – | 120 | | $T_j$ = -40 °C |
| | | | – | 90 | – | | 1) $T_j$ = 25 °C |
| | | | 67 | – | 100 | | $T_j$ = 150 °C |
| | channel 2, 3 | | | | | | HWCR.LEDn = 0 |
| | | | 29 | – | 44 | | $T_j$ = -40 °C |
| | | | – | 30 | – | | 1) $T_j$ = 25 °C |
| | | | 23 | – | 39 | | $T_j$ = 150 °C |
| | | | | | | | HWCR.LEDn = 1 |
| | | | 7 | – | 12 | | $T_j$ = -40 °C |
| | | | – | 8.5 | – | | 1) $T_j$ = 25 °C |
| | | | 5.5 | – | 11 | | $T_j$ = 150 °C |
| **Over Current Protection** | | | | | | | |
| 7.9.2 | Over current tripping activation time | $t_{delay(trip)}$ | 7 | – | 14 | ms | 1) |
| 7.9.3 | Load current trip level after $t_{delay(trip)}$ | $I_{L(Itrip)}$ | | | | A | |
| | channel 0, 1 | | 40 | – | 78 | | $T_j$ = -40 °C |
| | | | 35 | – | 70 | | $T_j$ = 150 °C |
| | channel 2, 3 | | | | | | HWCR.LEDn = 0 |
| | | | 17 | – | 35 | | $T_j$ = -40 °C |
| | | | 15.5 | – | 30 | | $T_j$ = 150 °C |
| | | | | | | | HWCR.LEDn = 1 |
| | | | 3.8 | – | 9 | | $T_j$ = -40 °C |
| | | | 3.8 | – | 8 | | $T_j$ = 150 °C |
| 7.9.4 | Load current trip level at high $V_{DS}$ | $I_{L(Vtrip)}$ | | | | A | 1) |
| | channel 0, 1 | | 40 | – | 78 | | $T_j$ = -40 °C |
| | | | 35 | – | 70 | | $T_j$ = 150 °C |
| | channel 2, 3 | | | | | | HWCR.LEDn = 0 |
| | | | 17 | – | 35 | | $T_j$ = -40 °C |
| | | | 15.5 | – | 30 | | $T_j$ = 150 °C |
| | | | | | | | HWCR.LEDn = 1 |
| | | | 3.8 | – | 9 | | $T_j$ = -40 °C |
| | | | 3.8 | – | 8 | | $T_j$ = 150 °C |
| 7.9.5 | Over current tripping at high $V_{DS}$ activation level | $V_{DS(Vtrip)}$ | 15 | – | – | V | 1) |
| 7.9.6 | Current trip at $V_{DS}$ = 7 V to current trip at $V_{DS}$ = 20 V ratio | $\Delta k_{TR}$ | 1.2 | 1.5 | – | | 1) |

**Electrical Characteristics Protection Functions** (cont'd)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Over Temperature Protection** | | | | | | | |
| 7.9.7 | Number of automatic retries at over current or dynamic temperature sensor shut down at low $V_{DS}$ | $n_{retry(LV)}$ | – | 32 | – | | 1) $V_{DS}$ = 9 V |
| 7.9.8 | Number of automatic retries at over current or dynamic temperature sensor shut down at medium $V_{DS}$ | $n_{retry(MV)}$ | – | 8 | – | | 1) $V_{DS}$ = 13 V |
| 7.9.9 | Thermal latch restart time | $t_{reset(CL)}$ | 50 | – | – | ms | 1) |
| 7.9.10 | Thermal shut down temperature | $T_{j(SC)}$ | 150 | 175 | 195 | °C | 1) |
| 7.9.11 | Thermal hysteresis of thermal shutdown | $\Delta T_j$ | – | 10 | – | K | 1) |
| 7.9.12 | Dynamic temperature increase limitation while switching | $\Delta T_{j(SW)}$ | – | 60 | – | K | 1) |
| 7.9.13 | Dynamic temperature sensor restart | $\Delta T_{j(res)}$ | – | 20 | – | K | 1) |
| **Reverse Battery** | | | | | | | |
| 7.9.14 | On-state resistance | $R_{DS(REV)}$ | | | | mΩ | 1) $V_S$ = -13.5 V |
| | channel 0, 1 | | | | | | $I_L$ = -7.5 A |
| | | | – | 4.7 | – | | $T_j$ = 25 °C |
| | | | – | 9.5 | – | | $T_j$ = 150 °C |
| | channel 2, 3 | | | | | | $I_L$ = -2.6 A |
| | | | – | 14.7 | – | | $T_j$ = 25 °C |
| | | | – | 29.5 | – | | $T_j$ = 150 °C |
| **Over Voltage** | | | | | | | |
| 7.9.15 | Over voltage protection | $V_{S(CL)}$ | | | | V | |
| | VS to GND | | 40 | 55 | 71 | | $I_{GND}$ = 5 mA |
| | channel 0, 1 | | 32 | – | 54 | | $T_j$ = 25 °C<br>$I_L$ = 20 mA |
| | | | 40 | – | 55 | | 1) $T_j$ = 150 °C<br>$I_L$ = 6 A |
| | channel 2, 3 | | 32 | – | 54 | | $T_j$ = 25 °C<br>$I_L$ = 20 mA |
| | | | 40 | – | 55 | | 1) $T_j$ = 150 °C<br>$I_L$ = 2 A |

1) Not subject to production test, specified by design.

# 8 Diagnosis

For diagnosis purpose, the SPOC - BTS5461SF provides a current sense signal at pin IS and the diagnosis word via SPI. There is a current sense multiplexer implemented that is controlled via SPI. The sense signal can also be disabled by SPI command. A switch bypass monitor allows to detect a short circuit between the output pin and the battery voltage.

In OFF-state a current source is able to be switched on for a selected channel with the DCR.CSOL bit. This allows open load / short circuit detection to $V_S$ in OFF-state. The current value can be configured to a low or a high value by programming the bit ICR.CSL. Please refer to parameter $I_{L(OL)}$ (8.5.15).

Please refer to Figure 16 for details on diagnosis function:

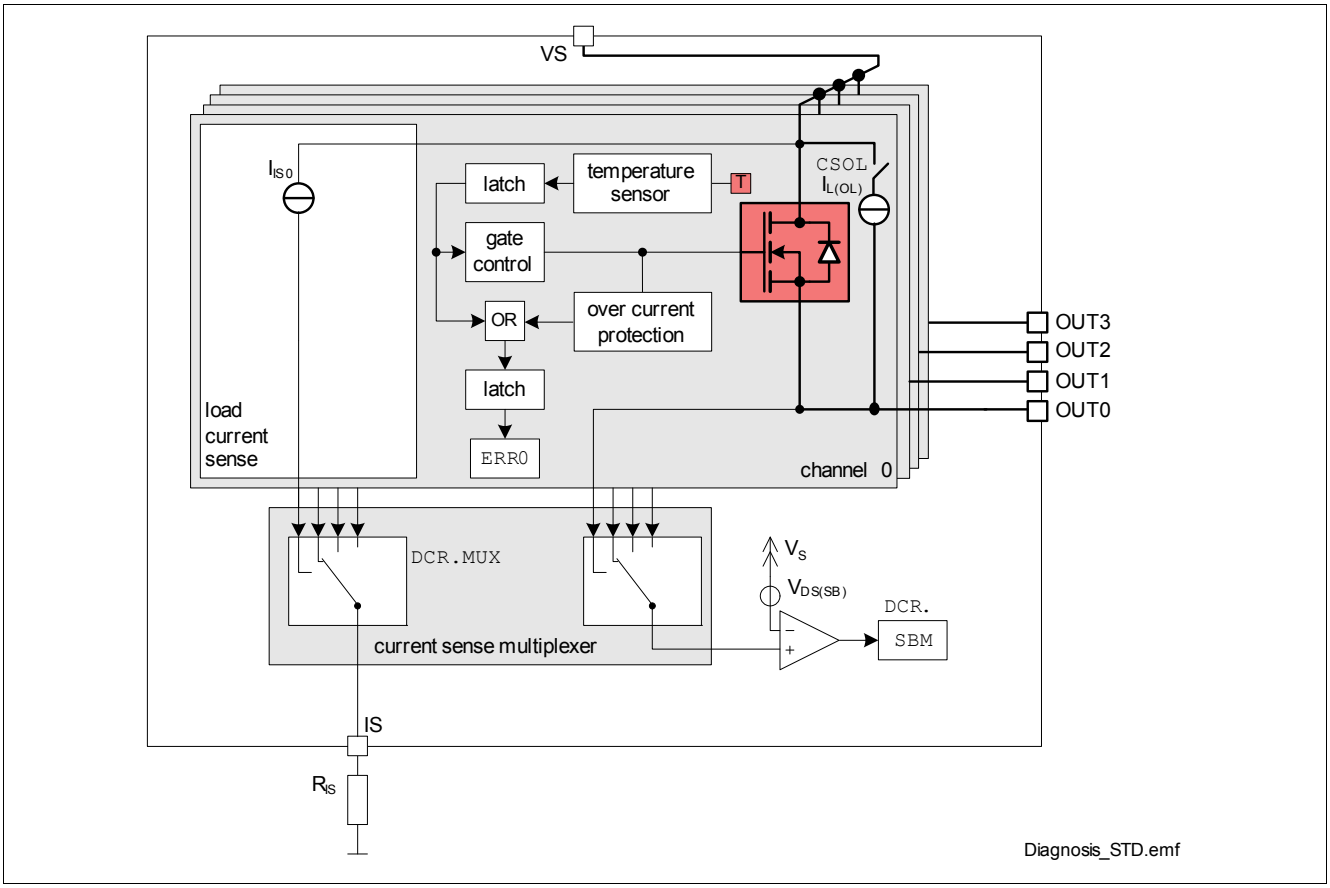



**Figure 16 Block diagram: Diagnosis**

For diagnosis feedback at different operation modes, please see following table.

**Table 3 Operation Modes [1)]**

| Operation Mode | Input Level OUTL.OUTn | Output Level $V_{OUT}$ | Current Sense $I_{IS}$ | Error Flag ERRn[2)] | SBM DCR.SBM |
|---|---|---|---|---|---|
| Normal Operation (OFF) | L / 0 (OFF-state) | GND | Z | 0 | 1 |
| Short Circuit to GND | | GND | Z | 0 | 1 |
| Thermal shut down | | Z | Z | 0 | x |
| Short Circuit to $V_S$ | | $V_S$ | Z | 0 | 0 |
| Open Load | | Z | Z | 0 | 0[3)] |
| Inverse Current | | > $V_S$ | Z | 0 | 0[4)] |
| Normal Operation (ON) | H / 1 (ON-state) | ~ $V_S$ | $I_L$ / $k_{ILIS}$ | 0 | 0 |
| Short Circuit to GND | | ~ GND | Z | 1 | 1 |
| Dynamic Temperature Sensor shut down | | Z | Z | 1 | x |
| Over Current shut down | | Z | Z | 1[5)] | x |
| Thermal shut down | | Z | Z | 1[6)] | x |
| Short Circuit to $V_S$ | | $V_S$ | < $I_L$ / $k_{ILIS}$ | 0 | 0 |
| Open Load | | $V_S$ | Z | 0 | 0 |
| Inverse Current | | > $V_S$ | Z | 0 | 0 |

1) L = low level, H = high level, Z = high impedance, potential depends on leakage currents and external circuit x = undefined
2) The error flags are latched until they are transmitted in the standard diagnosis word via SPI
3) If the current sense multiplexer is set to Channel 0 to 3 and DRC.CSOL bit set
4) If the current sense multiplexer is set to Channel 0 to 3
5) The over current latch off flag is set latched and can be cleared by SPI command HWCR.CL
6) The over temperature flag is set latched and can be cleared by SPI command HWCR.CL

## 8.1 Diagnosis Word at SPI

The standard diagnosis at the SPI interface provides information about each channel. The error flags, an OR combination of the over temperature flags and the over load monitoring signals are provided in the SPI standard diagnosis bits ERRn.

The over load monitoring signals are latched in the error flags and cleared each time the standard diagnosis is transmitted via SPI. In detail, they are cleared between the second and third raising edge of the SCLK signal.

The over temperature flags, which cause an overheated channel to latch off, are latched directly at the gate control block. The over current flags, which cause an channel 0 or 1 driving a too high current to switch off, are latched like the over temperature flags. Those latches are cleared by SPI command HWCR.CL.

Please note: The over temperature and over current information is latched twice. When transmitting a clear latch command (HWCR.CL), the error flag is cleared during command transmission of the next SPI frame and ready for latching after the third raising edge of the SCLK signal. As a result, the first standard diagnosis information after a CL command will indicate a failure mode at the previously affected channels although the thermal latches have been cleared already. In case of continuous over load, the error flags are set again immediately because of the over load monitoring signal.

## 8.2 Load Current Sense Diagnosis

There is a current sense signal available at pin IS which provides a current proportional to the load current of one selected channel. The selection is done by a multiplexer which is configured via SPI.

### Current Sense Signal

The current sense signal (ratio $k_{ILIS} = I_L / I_S$) is provided during on-state as long as no failure mode occurs. The ratio $k_{ILIS}$ can be adjusted to the load type (LED or bulb) via SPI register HWCR for channel 2 and 3. The accuracy of the ratio $k_{ILIS}$ depends on the load current. Usually a resistor $R_{IS}$ is connected to the current sense pin. It is recommended to use resistors 1.5 kΩ < $R_{IS}$ < 5 kΩ. A typical value is 2.7 kΩ.

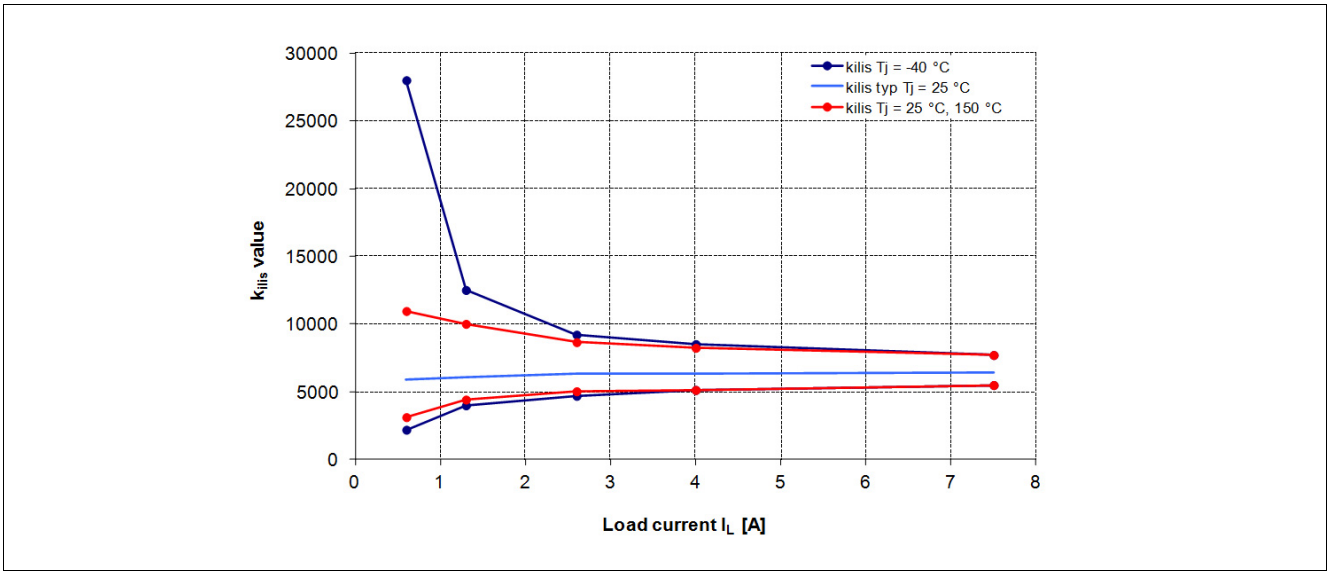



**Figure 17 Current Sense Ratio $k_{ILIS}$ Channel 0, 1** [1)]

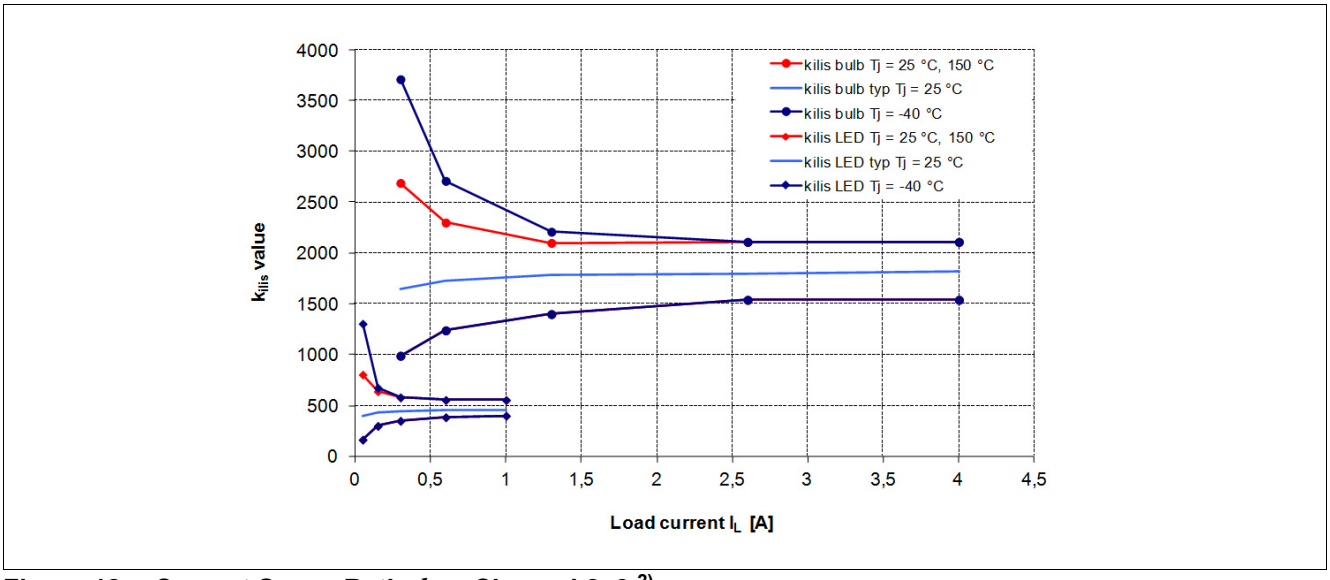



**Figure 18 Current Sense Ratio $k_{ILIS}$ Channel 2, 3** [2)]

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in Section 8.5 (Position 8.5.1).

2) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in Section 8.5 (Position 8.5.1).

In case of off-state, over current, dynamic temperature sensor shut down ($n < n_{retry}$), dynamic temperature sensor latch ($n = n_{retry}$) as well as over temperature, the current sense signal of the affected channel is switched off. To distinguish between over temperature or over current and over load, the SPI diagnosis word can be used. Whereas the over load and dynamic temperature sensor shut down ($n < n_{retry}$) flag is cleared every time the diagnosis is transmitted. The over temperature, dynamic temperature sensor latch ($n = n_{retry}$) and over current flag is cleared by a dedicated SPI command (`HWCR.CL`).

Details about timings between the current sense signal $I_{IS}$ and the output voltage $V_{OUT}$ and the load current $I_L$ can be found in **Figure 19**.

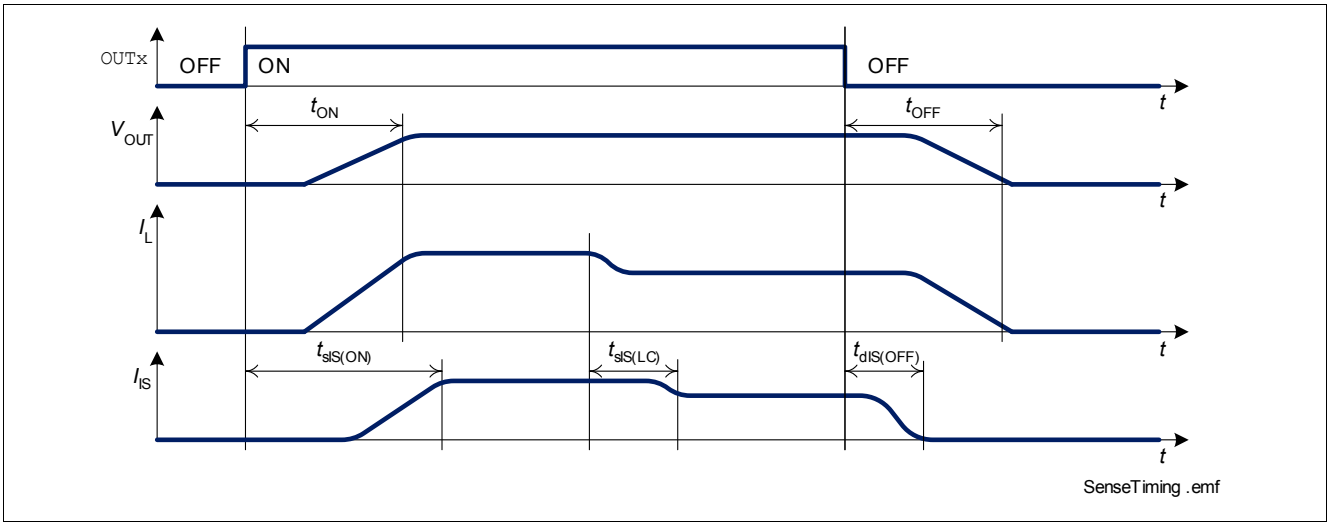



**Figure 19 Timing of Current Sense Signal**

### Current Sense Multiplexer

There is a current sense multiplexer implemented in the SPOC - BTS5461SF that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register `DCR.MUX`. The sense current also can be disabled by SPI register `DCR.MUX`. For details on timing of the current sense multiplexer, please refer to **Figure 20**.

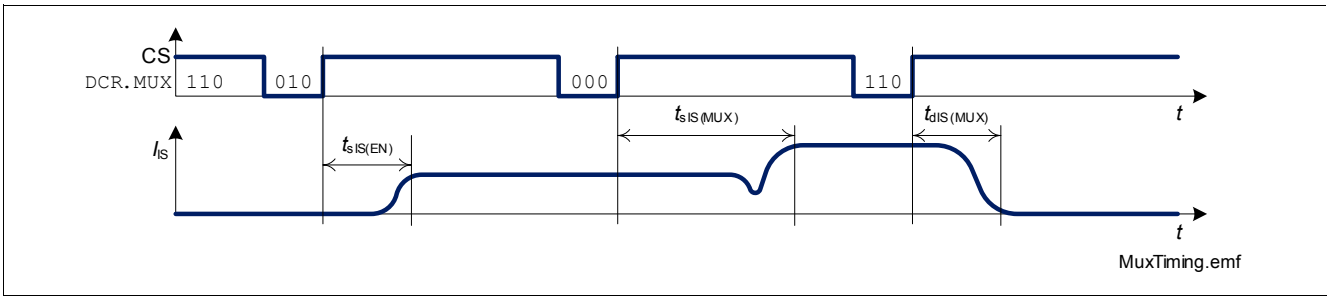



**Figure 20 Timing of Current Sense Multiplexer**

**Current Sense Offset Trimming**

To increase the current sense accuracy of SPOC - BTS5461SF, a circuitry to measure and trim the sense offset current is implemented. This so called calibration mode is activated by the SPI command `ICR.CAL = 1b`. In calibration mode, a current proportional to the positive offset of the operational amplifier is provided on the IS pin. To increase the accuracy of the calibration this current is amplified by a factor of 10 (typical value) when calibration mode is entered. The offset of the operational amplifier can be trimmed by 15 steps which are selected by the bits `KILIS.OSTn`. (see. **Chapter 9.6** for detailed information). To exit the calibration mode `ICR.CAL` is set to `0b`. During calibration the state of the current sense multiplexer should not be changed, otherwise the measured current could be affected. If `DCR.MUX = 111` the device exits calibration mode and stand-by mode is entered. In general the calibration mode does not have any effect on other SPI registers or functions of the device. In case of calibration during operation switching transients on the supply line must be considered.

## 8.3 Switch Bypass Diagnosis

To detect short circuit to $V_S$, there is a switch bypass monitor implemented. In case of short circuit between the output pin OUT and $V_S$ in ON-state, the current will flow through the power transistor as well as through the short circuit (bypass) with undefined ratio. As a result, the current sense signal will show lower values than expected by the load current. In OFF-state, the output voltage will stay close to $V_S$ potential which means a small $V_{DS}$.

The switch bypass monitor compares the voltage $V_{DS}$ across the power transistor of that channel, which is selected by the current sense multiplexer (`DCR.MUX`) with threshold $V_{DS(SB)}$. The result of comparison can be read in SPI register `DCR.SBM` or in the standard diagnosis.

## 8.4 Open Load in OFF-State

For performing a dedicated open load in OFF-state detection a current source can be switched in parallel to the DMOS according to the **Figure 16**. The current source current can be programmed in two steps by the bit `ICR.CSL`.

The following procedure is recommended to use:

- Select the dedicated channel with the multiplexer
- Enable the open load current with the `DCR.CSOL` bit
- Read the `DCR.SBM` or the standard diagnosis
- Disable the open load current with the `DCR.CSOL` bit

## 8.5 Electrical Characteristics

### Electrical Characteristics Diagnosis

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Load Current Sense** | | | | | | | |
| 8.5.1 | Current sense ratio | $k_{ILIS}$ | | | | | $T_j$ = -40 °C |
| | channel 0, 1: | | | | | | |
| | 0.600 A | | 2190 | 5840 | 28000 | | – |
| | 1.3 A | | 3990 | 6140 | 12510 | | – |
| | 2.6 A | | 4690 | 6350 | 9210 | | – |
| | 4.0 A | | 5130 | 6430 | 8510 | | – |
| | 7.5 A | | 5490 | 6480 | 7710 | | – |
| | channel 2, 3 (bulb): | | | | | | HWCR.LEDn = 0 |
| | 0.300 A | | 990 | 1670 | 3710 | | – |
| | 0.600 A | | 1240 | 1750 | 2710 | | – |
| | 1.3 A | | 1400 | 1800 | 2210 | | – |
| | 2.6 A | | 1540 | 1830 | 2110 | | – |
| | 4.0 A | | 1540 | 1840 | 2110 | | – |
| | channel 2, 3 (LED): | | | | | | HWCR.LEDn = 1 |
| | 0.050 A | | 165 | 400 | 1305 | | – |
| | 0.150 A | | 300 | 440 | 675 | | – |
| | 0.300 A | | 350 | 450 | 580 | | – |
| | 0.600 A | | 385 | 460 | 555 | | – |
| | 1.0 A | | 400 | 500 | 555 | | – |
| 8.5.2 | Current sense ratio | $k_{ILIS}$ | | | | | $T_j$ = 25 °C to 150 °C |
| | channel 0, 1: | | | | | | |
| | 0.600 A | | 3120 | 5840 | 10960 | | – |
| | 1.3 A | | 4420 | 6140 | 10010 | | – |
| | 2.6 A | | 5030 | 6350 | 8660 | | – |
| | 4.0 A | | 5130 | 6430 | 8240 | | – |
| | 7.5 A | | 5490 | 6480 | 7710 | | – |
| | channel 2, 3 (bulb): | | | | | | HWCR.LEDn = 0 |
| | 0.300 A | | 990 | 1670 | 2690 | | – |
| | 0.600 A | | 1240 | 1750 | 2300 | | – |
| | 1.3 A | | 1400 | 1800 | 2100 | | – |
| | 2.6 A | | 1540 | 1830 | 2110 | | – |
| | 4.0 A | | 1540 | 1840 | 2110 | | – |
| | channel 2, 3 (LED): | | | | | | HWCR.LEDn = 1 |
| | 0.050 A | | 165 | 400 | 805 | | – |
| | 0.150 A | | 300 | 440 | 640 | | – |
| | 0.300 A | | 350 | 450 | 580 | | – |
| | 0.600 A | | 385 | 460 | 555 | | – |
| | 1.0 A | | 400 | 500 | 555 | | – |

**Electrical Characteristics Diagnosis** (cont'd)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| 8.5.3 | Current sense drift of unaffected channel during inverse current of other channels | $\Delta k_{ILIS(IC)}$ | | | | | 1) |
| | | | | | | | DCR.MUX ≠ 111 |
| | channel 0, 1 | | | | | | $I_{L0,1}$ = 7.5 A |
| | | | -20 % | – | 20 % | | $I_{L1,0\ (IC)}$ = 7.5 A |
| | | | -20 % | – | 20 % | | $I_{L2,3\ (IC)}$ = 2.6 A |
| | channel 2, 3 (bulb) | | | | | | HWCR.LEDn = 0 |
| | | | | | | | $I_{L2,3}$ = 2.6 A |
| | | | -20 % | – | 20 % | | $I_{L0,1\ (IC)}$ = 7.5 A |
| | | | -20 % | – | 20 % | | $I_{L3,2\ (IC)}$ = 2.6 A |
| | channel 2, 3 (LED) | | | | | | HWCR.LEDn = 1 |
| | | | | | | | $I_{L2,3}$ = 0.6 A |
| | | | -20 % | – | 20 % | | $I_{L0,1\ (IC)}$ = 7.5 A |
| | | | -20 % | – | 20 % | | $I_{L3,2\ (IC)}$ = 2.6 A |
| 8.5.4 | Calibration step | $I_{IS(CAL)}$ | | | | µA | 1) $T_j$ = 25 °C |
| | | | – | 7.5 | – | | ICR.CAL = 0 |
| | | | – | 75 | – | | ICR.CAL = 1 |
| 8.5.5 | Maximum steady state current sense output current | $I_{IS(MAX)}$ | 5.5 | – | 20 | mA | 1) $V_{IS}$ = 0 V |
| 8.5.6 | Current sense leakage / offset current | $I_{IS(en)}$ | | | | µA | $I_L$ = 0 A |
| | | | | | | | DCR.MUX ≠ 111 |
| | channel 0, 1 | | – | – | 76 | | |
| | channel 2, 3 | | – | – | 76 | | |
| 8.5.7 | Current sense leakage, while diagnosis disabled | $I_{IS(dis)}$ | – | – | 1 | µA | DCR.MUX = 110 |
| 8.5.8 | Current sense settling time after channel activation | $t_{sIS(ON)}$ | | | | µs | $V_S$ = 13.5 V |
| | | | | | | | $R_{IS}$ = 2.7 kΩ |
| | channel 0, 1 | | – | – | 150 | | $R_L$ = 2.2 Ω |
| | channel 2, 3 | | | | | | HWCR.LEDn = 0 |
| | | | – | – | 150 | | $R_L$ = 6.8 Ω |
| | | | | | | | HWCR.LEDn = 1 |
| | | | – | – | 100 | | $R_L$ = 33 Ω |
| 8.5.9 | Current sense desettling time after channel deactivation | $t_{dIS(OFF)}$ | | | | µs | 1) $V_S$ = 13.5 V |
| | | | | | | | $R_{IS}$ = 2.7 kΩ |
| | | | – | – | 25 | | HWCR.LEDn = 0 |
| | | | – | – | 25 | | HWCR.LEDn = 1 |
| 8.5.10 | Current sense settling time after change of load current | $t_{sIS(LC)}$ | | | | µs | 1) $V_S$ = 13.5 V |
| | | | | | | | $R_{IS}$ = 2.7 kΩ |
| | channel 0, 1 | | – | – | 30 | | $I_L$ = 7.5 A to 4.0 A |
| | channel 2, 3 | | | | | | HWCR.LEDn = 0 |
| | | | – | – | 30 | | $I_L$ = 2.6 A to 1.3 A |
| | | | | | | | HWCR.LEDn = 1 |
| | | | – | – | 30 | | $I_L$ = 0.6 A to 0.3 A |

**Electrical Characteristics Diagnosis** (cont'd)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| 8.5.11 | Current sense settling time after current sense activation | $t_{sIS(EN)}$ | – | – | 25 | µs | $R_{IS}$ = 2.7 kΩ<br>DCR.MUX:<br>110 -> 000 |
| 8.5.12 | Current sense settling time after multiplexer channel change | $t_{sIS(MUX)}$ | – | – | 30 | µs | $R_{IS}$ = 2.7 kΩ<br>$R_{L0}$ = 2.2 Ω<br>$R_{L2}$ = 33 Ω<br>DCR.MUX:<br>010 -> 000 |
| 8.5.13 | Current sense deactivation time | $t_{dIS(MUX)}$ | – | – | 25 | µs | [1] $R_{IS}$ = 2.7 kΩ<br>DCR.MUX:<br>000 -> 110 |
| **Switch Bypass Monitor** | | | | | | | |
| 8.5.14 | Switch bypass monitor threshold | $V_{DS(SB)}$ | 1.5 | – | 4 | V | – |
| **Open load in off current source** | | | | | | | |
| 8.5.15 | Current source in OFF-state | $I_{L(OL)}$ | 100<br>3.0 | –<br>– | 450<br>7.5 | µA<br>mA | ICR.CSL = 0<br>ICR.CSL = 1 |

1) Not subject to production test, specified by design.

# 9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

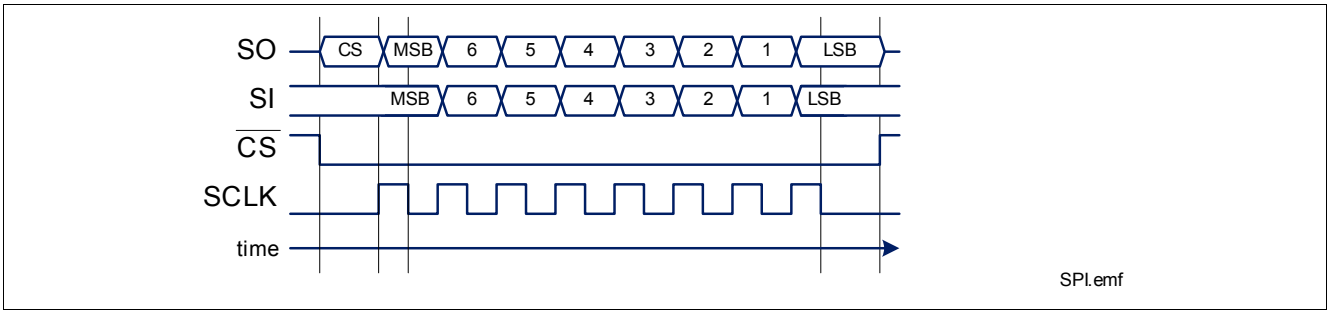



**Figure 21 Serial Peripheral Interface**

## 9.1 SPI Signal Description

**$\overline{CS}$ - Chip Select:**

The system micro controller selects the SPOC - BTS5461SF by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

**$\overline{CS}$ High to Low transition:**

- The requested information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. This information stays available to the first rising edge of SCLK.

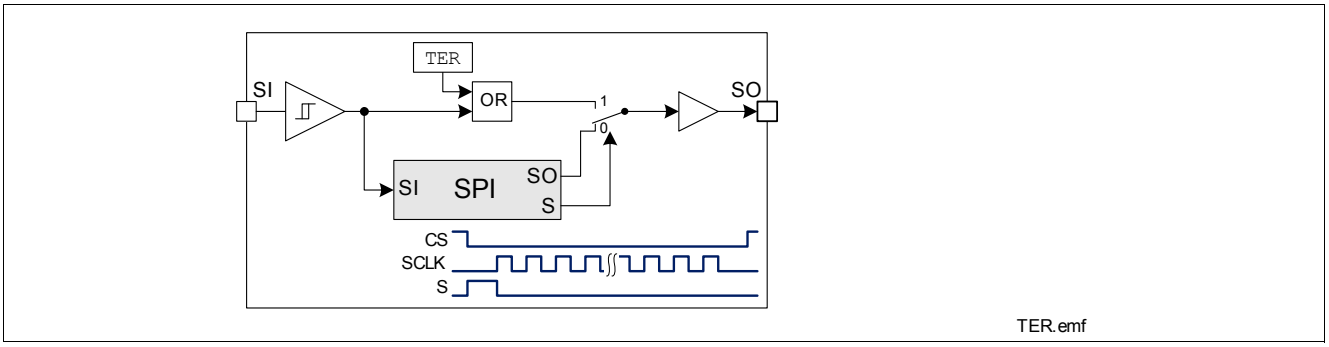



**Figure 22 Combinatorial Logic for TER Flag**

**$\overline{CS}$ Low to High transition:**

- Command decoding is only done, when after the falling edge of $\overline{CS}$ exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

**SCLK - Serial Clock:**

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

**SI - Serial Input:**

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Section 9.5** for further information.

**SO Serial Output:**

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 9.5** for further information.

## 9.2 Daisy Chain Capability

The SPI of SPOC - BTS5461SF provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. The SI line of one device is connected with the SO line of another device (see **Figure 23**), in order to build a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

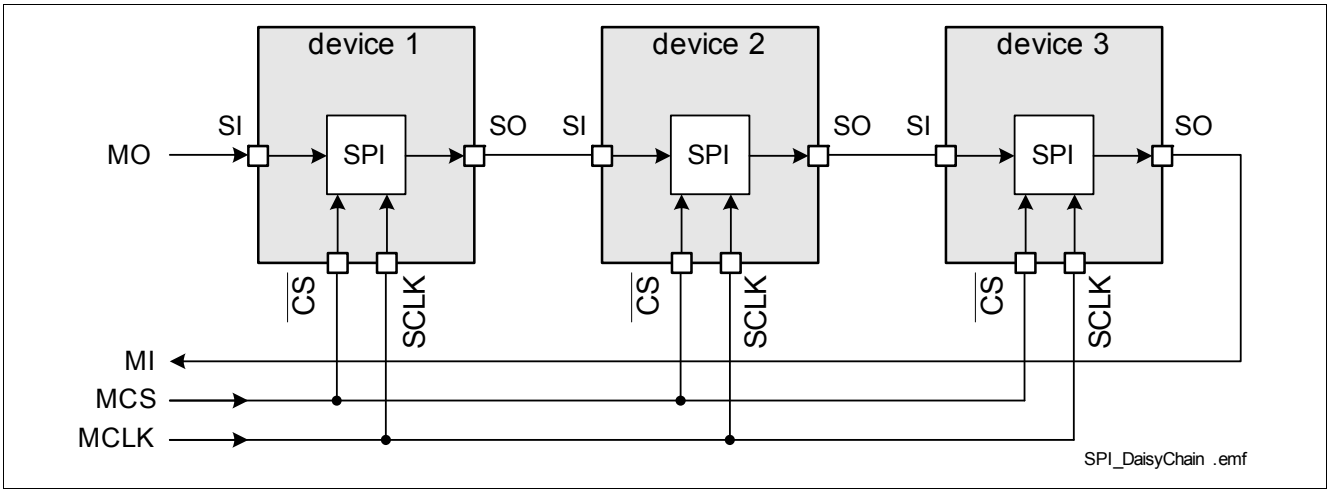



**Figure 23 Daisy Chain Configuration**

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After eight SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must turn high to make the device accept the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, three times eight bits have to be shifted through the devices. After that, the $\overline{MCS}$ line must turn high (see **Figure 24**).

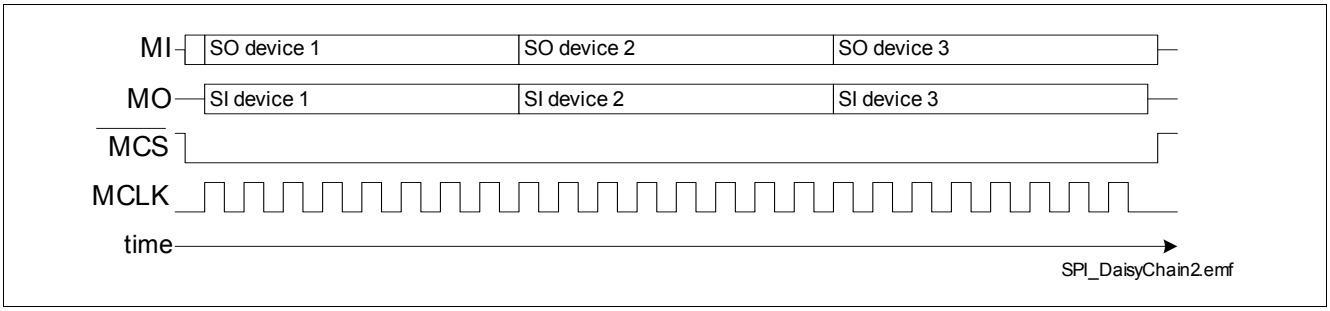



**Figure 24 Data Transfer in Daisy Chain Configuration**

## 9.3 Timing Diagrams

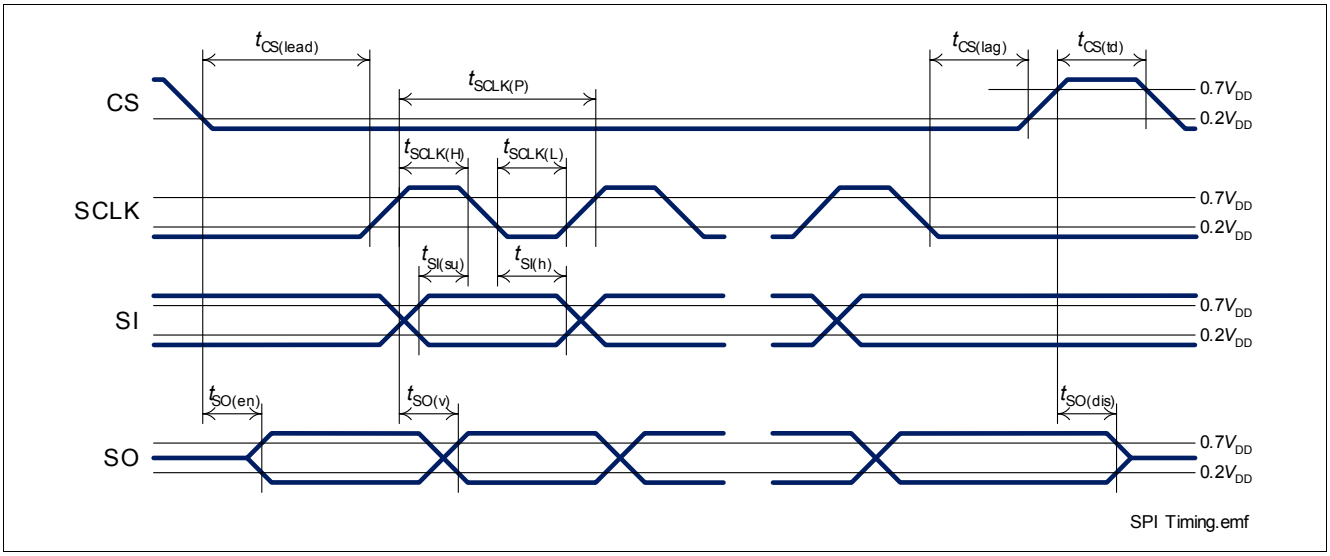



**Figure 25 Timing Diagram SPI Access**

## 9.4 Electrical Characteristics

### Electrical Characteristics Serial Peripheral Interface (SPI)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Input Characteristics ($\overline{CS}$, SCLK, SI)** | | | | | | | |
| 9.4.1 | L level of pin<br>$\overline{CS}$<br>SCLK<br>SI | <br>$V_{CS(L)}$<br>$V_{SCLK(L)}$<br>$V_{SI(L)}$ | 0 | – | 0.2* $V_{DD}$ | V | $V_{DD}$ = 4.3 V |
| 9.4.2 | H level of pin<br>$\overline{CS}$<br>SCLK<br>SI | <br>$V_{CS(H)}$<br>$V_{SCLK(H)}$<br>$V_{SI(H)}$ | 0.4* $V_{DD}$ | – | $V_{DD}$ | V | $V_{DD}$ = 4.3 V |
| 9.4.3 | Pull-up resistor at $\overline{CS}$ pin | $R_{CS}$ | 50 | 120 | 180 | kΩ | $I_{CS}$ = 100 µA |
| 9.4.4 | Pull-down resistor at pin<br>SCLK<br>SI | <br>$R_{SCLK}$<br>$R_{SI}$ | 50 | 120 | 180 | kΩ | –<br>$I_{SCLK}$ = 100 µA<br>$I_{SI}$ = 100 µA |
| **Output Characteristics (SO)** | | | | | | | |
| 9.4.5 | L level output voltage | $V_{SO(L)}$ | 0 | – | 0.4 | V | $I_{SO}$ = -0.5 mA |
| 9.4.6 | H level output voltage | $V_{SO(H)}$ | $V_{DD}$ - 0.4 V | – | $V_{DD}$ | V | $I_{SO}$ = 0.5 mA<br>$V_{DD}$ = 4.3 V |
| 9.4.7 | Output tristate leakage current | $I_{SO(OFF)}$ | -10 | – | 10 | µA | $V_{CS}$ = $V_{DD}$ |
| **Timings** | | | | | | | |
| 9.4.8 | Serial clock frequency | $f_{SCLK}$ | 0<br>0 | –<br>– | 5<br>3 | MHz | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.9 | Serial clock period | $t_{SCLK(P)}$ | 200<br>333 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.10 | Serial clock high time | $t_{SCLK(H)}$ | 100<br>166 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.11 | Serial clock low time | $t_{SCLK(L)}$ | 100<br>166 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.12 | Enable lead time (falling $\overline{CS}$ to rising SCLK) | $t_{CS(lead)}$ | 200<br>333 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.13 | Enable lag time (falling SCLK to rising $\overline{CS}$) | $t_{CS(lag)}$ | 200<br>333 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.14 | Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$) | $t_{CS(td)}$ | 200<br>333 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.15 | Data setup time (required time SI to falling SCLK) | $t_{SI(su)}$ | 20<br>33 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |
| 9.4.16 | Data hold time (falling SCLK to SI) | $t_{SI(h)}$ | 20<br>33 | –<br>– | –<br>– | ns | 1) $V_{DD}$ = 4.3 V<br>2) $V_{DD}$ = 3.0 V |

**Electrical Characteristics Serial Peripheral Interface (SPI)** (cont'd)

Unless otherwise specified: $V_S$ = 8 V to 17 V, $V_{DD}$ = 3.0 V to 5.5 V, $T_j$ = -40 °C to +150 °C
typical values: $V_S$ = 13.5 V, $V_{DD}$ = 4.3 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| 9.4.17 | Output enable time (falling $\overline{CS}$ to SO valid) | $t_{SO(en)}$ | – | – | 200 | ns | [2] $C_L$ = 20 pF, $V_{DD}$ = 4.3 V |
| | | | – | – | 333 | | $V_{DD}$ = 3.0 V |
| 9.4.18 | Output disable time (rising $\overline{CS}$ to SO tri-state) | $t_{SO(dis)}$ | – | – | 200 | ns | [2] $C_L$ = 20 pF, $V_{DD}$ = 4.3 V |
| | | | – | – | 333 | | $V_{DD}$ = 3.0 V |
| 9.4.19 | Output data valid time with capacitive load | $t_{SO(v)}$ | – | – | 100 | ns | [2] $C_L$ = 20 pF, $V_{DD}$ = 4.3 V |
| | | | – | – | 166 | | $V_{DD}$ = 3.0 V |

1) Not subject to production test, specified by design. SPI functional test is performed at $f_{SCLK}$ = 5 MHz.
2) Not subject to production test, specified by design.

## 9.5 SPI Protocol 8 Bit

| | CS[1] | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | Write OUTL and KILIS Register | | | | | | | |
| SI | | 1 | 0 | ADDR | | DATA | | | |
| | | Read OUTL and KILIS Register | | | | | | | |
| SI | | 0 | 0 | ADDR | | x | x | x | 0 |
| | | Write Configuration and Control Registers | | | | | | | |
| SI | | 1 | 1 | ADDR | | DATA | | | |
| | | Read Configuration and Control Registers | | | | | | | |
| SI | | 0 | 1 | ADDR | | x | x | x | 0 |
| | | Read Standard Diagnosis | | | | | | | |
| SI | | 0 | x | x | x | x | x | x | 1 |
| | | Standard Diagnosis | | | | | | | |
| SO | TER | 0 | LHI | SBM | x | ERR3 | ERR2 | ERR1 | ERR0 |
| | | Second Frame of Read Command | | | | | | | |
| SO | TER | 1 | 0 | 0 | 0 | OUT3 | OUT2 | OUT1 | OUT0 |
| SO | TER | 1 | 1 | ADDR | | DATA | | | |

1) The SO pin shows this information between $\overline{CS}$ hi -> lo and first SCLK lo -> hi transition.

*Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame the output at SPI signal SO will contain the requested information. A new command can be executed in the second frame. The standard diagnosis can be accessed either by sending the standard diagnosis read command or it is transmitted after each write command.*

| Field | Bits | Type | Description |
|---|---|---|---|
| W/$\overline{R}$ | 7 | w | 0 Read<br>1 Write |
| RB | 6 | r | **Register Bank**<br>**0** Read / write to OUTL and KILIS register<br>1 Read / write to the other register |
| TER | CS | r | **Transmission Error**<br>**0** Previous transmission was successful (modulo 8 clocks received)<br>1 Previous transmission failed or first transmission after reset |
| ADDR | 6:5 | rw | **Address**<br>Pointer to register for read and write command |
| DATA | 4:0 | rw | **Data**<br>Data written to or read from register selected by address ADDR |
| ERRn<br>n = 3 to 0 | n | r | **Diagnosis of Channel n**<br>**0** No failure<br>1 Over temperature, over current, over load or short circuit for channel 0 to 3 |
| SBM | 5 | r | **Switch Bypass Monitor** [1]<br>0 $V_{DS} < V_{DS(SB)}$<br>1 $V_{DS} > V_{DS(SB)}$ |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUTn<br>n = 3 to 0 | n | r | **Output Status for Channel n**<br>**0** Channel is switched off<br>1 Channel is switched on |
| LHI | 6 | r | **Limp Home Enable** [2]<br>0 H-input signal at LHI pin<br>1 L-input signal at LHI pin |

1) Invalid in stand-by mode

2) Not latching information, read of LHI-status during falling CS

## 9.6 Register Overview

| RB | Address | | Name | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | OUTL | Output Configuration Register Low |
| 0 | 1 | 0 | KILIS | Current Sense Offset Calibration Register |
| 1 | 0 | 1 | ICR | Input and Current Source Configuration Register |
| 1 | 1 | 0 | HWCR | Hardware Configuration Register |
| 1 | 1 | 1 | DCR | Diagnosis Control Register |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | **W/$\overline{R}$** | **RB** | **ADDR** | | **DATA** | | | | **default** [1] |
| OUTL | W/R | 0 | 0 | 0 | OUT3 | OUT2 | OUT1 | OUT0 | $00_H$ |
| KILIS | W/R | 0 | 1 | 0 | OST3 | OST2 | OST1 | OST0 | $28_H$ |
| ICR | W/R | 1 | 0 | 1 | COL | INCG | CSL | CAL | $00_H$ |
| HWCR | R | 1 | 1 | 0 | LED3 | LED2 | STB | CL | $02_H$ |
| | W | 1 | 1 | 0 | LED3 | LED2 | RST | CL | - |
| DCR | R | 1 | 1 | 1 | SBM | MUX | | | $07_H$ |
| | W | 1 | 1 | 1 | CSOL | MUX | | | - |

1) The default values are set after reset.

*Note: A readout of an unused register will return the standard diagnosis.*

| Field | Bits | Type | Description |
|---|---|---|---|
| OUTL<br>n = 3 to 0 | n | rw | **Output Control Register for Channel 0 to 3**<br>**0** OFF<br>1 ON |
| OSTn<br>n = 3 to 0 | n | rw | **IS Offset Trimming**<br>0000 $I_{IS(EN)}$ - 8 x $I_{IS(CAL)}$<br>0001 $I_{IS(EN)}$ - 7 x $I_{IS(CAL)}$<br>0010 $I_{IS(EN)}$ - 6 x $I_{IS(CAL)}$<br>0011 $I_{IS(EN)}$ - 5 x $I_{IS(CAL)}$<br>0100 $I_{IS(EN)}$ - 4 x $I_{IS(CAL)}$<br>0101 $I_{IS(EN)}$ - 3 x $I_{IS(CAL)}$<br>0110 $I_{IS(EN)}$ - 2 x $I_{IS(CAL)}$<br>0111 $I_{IS(EN)}$ - 1 x $I_{IS(CAL)}$<br>**1000** $I_{IS(EN)}$ without Offset calibration<br>1001 $I_{IS(EN)}$ + 1 x $I_{IS(CAL)}$<br>1010 $I_{IS(EN)}$ + 2 x $I_{IS(CAL)}$<br>1011 $I_{IS(EN)}$ + 3 x $I_{IS(CAL)}$<br>1100 $I_{IS(EN)}$ + 4x $I_{IS(CAL)}$<br>1101 $I_{IS(EN)}$ + 5 x $I_{IS(CAL)}$<br>1110 $I_{IS(EN)}$ + 6 x $I_{IS(CAL)}$<br>1111 $I_{IS(EN)}$ + 7 x $I_{IS(CAL))}$ |
| CAL | 0 | rw | **IS Offset Calibration**<br>**0** Calibration mode is deactivated<br>1 Calibration mode is activated |
| CSL | 1 | rw | **Level for Current Source for Open Load Detection**<br>**0** Low level<br>1 High level |
| INCG | 2 | rw | **Input Drive Configuration**<br>**0** Direct drive mode<br>1 Assigned drive mode |
| COL | 3 | rw | **Input Combinatorial Logic Configuration**<br>**0** Input signal OR-combined with according `OUTL` register bit<br>1 Input signal AND-combined with according `OUTL` register bit |
| STB | 1 | r | **Standby Mode**<br>0 Device is awake<br>**1** Device is in Standby mode |
| LEDn<br>n = 3 to 2 | n | rw | **Set LED Mode for Channel n**<br>**0** Channel n is in bulb mode<br>1 Channel n is in LED mode |
| CL | 0 | rw | **Clear Latch**<br>**0** Thermal and over current latches are untouched<br>1 Command: Clear all thermal and over current latches |
| RST | 1 | w | **Reset Command**<br>**0** Normal operation<br>1 Execute reset command |

| Field | Bits | Type | Description |
|---|---|---|---|
| MUX | 2:0 | rw | **Set Current Sense Multiplexer Configuration in OFF-state**<br>000 IS pin is high impedance<br>001 IS pin is high impedance<br>010 IS pin is high impedance<br>011 IS pin is high impedance<br>100 IS pin is high impedance<br>101 IS pin is high impedance<br>110 IS pin is high impedance<br>**111** Stand-by mode (IS pin is high impedance)<br>**Set Multiplexer Configuration in ON-state**<br>000 Current sense of channel 0 is routed to IS pin<br>001 Current sense of channel 1 is routed to IS pin<br>010 Current sense of channel 2 is routed to IS pin<br>011 Current sense of channel 3 is routed to IS pin<br>100 IS pin is high impedance<br>101 IS pin is high impedance<br>110 IS pin is high impedance<br>**111** Stand-by mode (IS pin is high impedance)) |
| SBM | 3 | r | **Switch Bypass Monitor** [1]<br>0 $V_{DS} < V_{DS(SB)}$<br>1 $V_{DS} > V_{DS(SB)}$ |
| CSOL | 3 | w | **Current Source Switch for Open Load Detection**<br>**0** OFF<br>1 ON |

1) Invalid in stand-by mode

# 10 Application Description

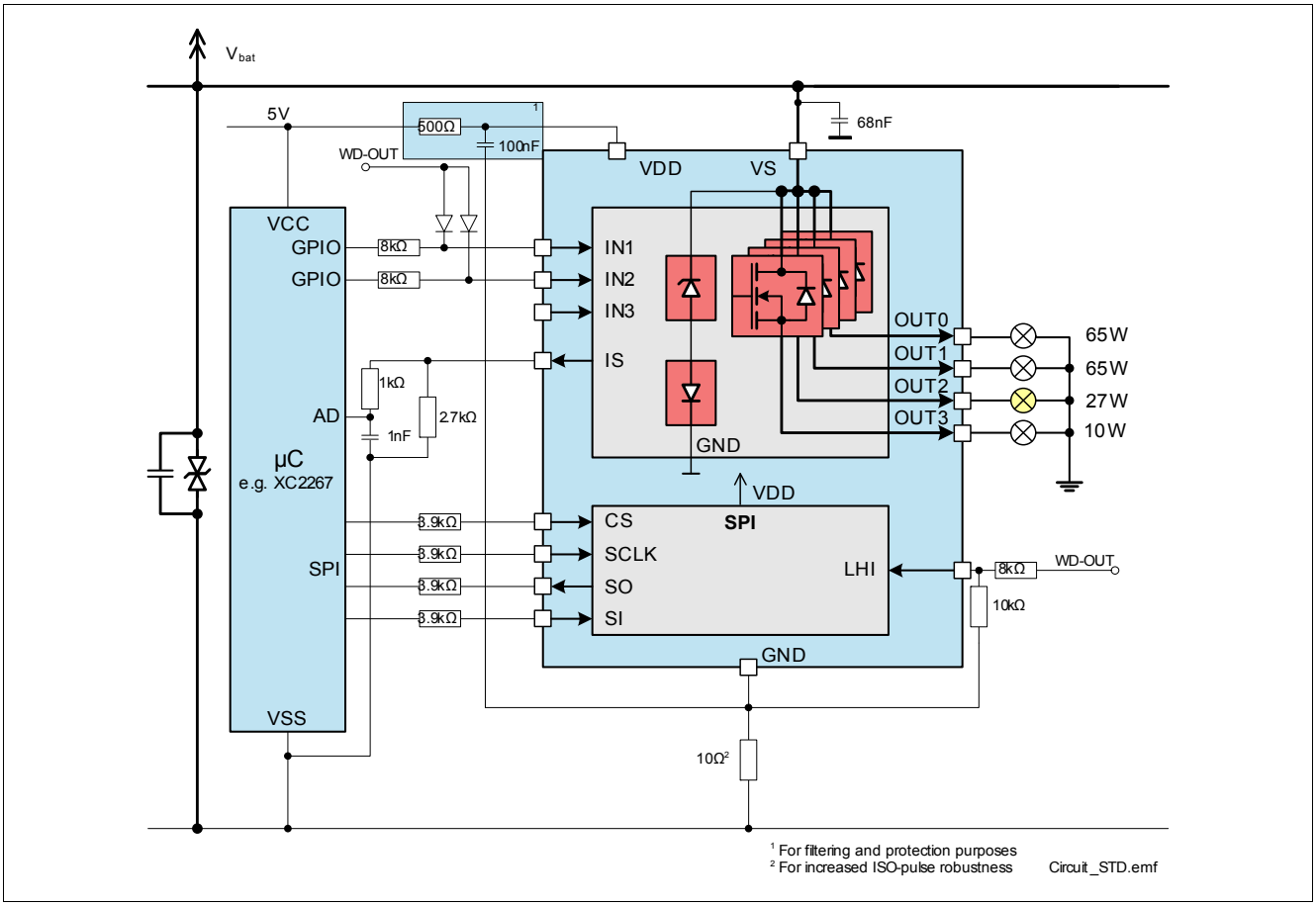



**Figure 26 Application Circuit Example**

# 11 Package Outlines SPOC - BTS5461SF

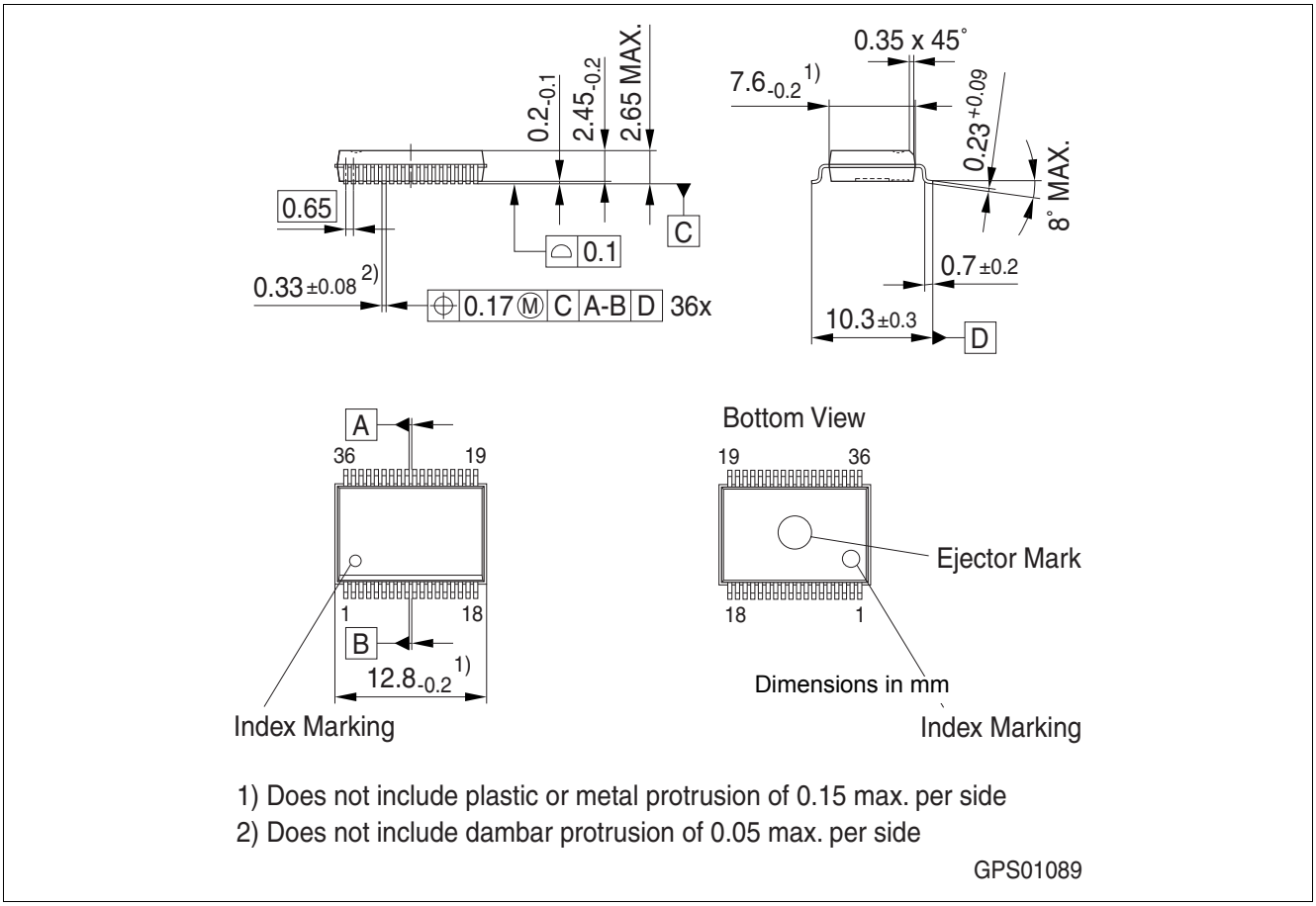



**Figure 27 PG-DSO-36-43** (Plastic Dual Small Outline Package)

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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# 12 Revision History

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 2011-11-17 | Initial revision |

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