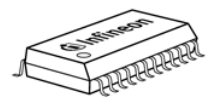
2-Phase Stepper-Motor Driver — TLE 4728 G

Bipolar-IC

Overview



Features

- 2 × 0.7 amp. full bridge outputs
- Integrated driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Max. supply voltage 45 V
- Output stages are free of crossover current
- Offset-phase turn-ON of output stages
- All outputs short-circuit proof
- Error-flag for overload, open load, overtemperature
- SMD package P-DSO-24-3

Type	Ordering Code	Package
TLE 4728 G	Q67006-A9077	P-DSO-24-9

Description

TLE 4728 G is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate by constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 0.7 A per phase at operating voltages up to 16 V.

The direction and value of current are programmable for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in full-bridge configuration include fast integrated free wheeling diodes and are free of crossover current. The device can be driven directly by a microprocessor in several modes by programming phase direction and current control of each bridge independently.

With the two error outputs the TLE 4728 G signals malfunction of the device. Setting the control inputs high resets the error flag and by reactivating the bridges one by one the location of the error can be found.

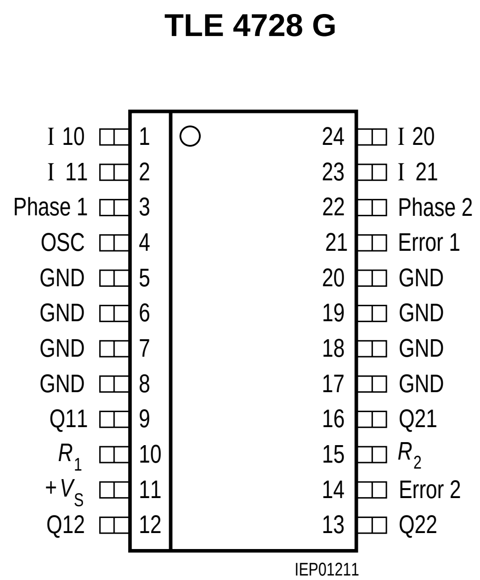


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

<table>
<tr><th>Pin No.</th><th>Function</th></tr>
<tr><td>1, 2, 23, 24</td><td>Digital control inputs IX0, IX1 for the magnitude of the current of the particular phase.

I_{set} = 450 mA with R_{sense} = 1 Ω
<table>
<tr><th>IX1 IX0</th><th>Phase Current</th><th>Example of Motor Status</th></tr>
<tr><td>H H</td><td>0</td><td>No current[1)]</td></tr>
<tr><td>H L</td><td>$0.155 \times I_{set}$</td><td>Hold</td></tr>
<tr><td>L H</td><td>I_{set}</td><td>Normal mode</td></tr>
<tr><td>L L</td><td>$1.55 \times I_{set}$</td><td>Accelerate</td></tr>
</table>
1) “No current” in both bridges inhibits the circuit and current consumption will sink below 3 mA</td></tr>
<tr><td>3</td><td>Input phase 1; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.</td></tr>
<tr><td>5 ... 8, 17 ... 20</td><td>Ground; all pins are connected at leadframe internally.</td></tr>
<tr><td>4</td><td>Oscillator; works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.</td></tr>
<tr><td>10</td><td>Resistor R_1 for sensing the current in phase 1.</td></tr>
<tr><td>9, 12</td><td>Push-pull outputs Q11, Q12 for phase 1 with integrated free-wheeling diodes.</td></tr>
<tr><td>11</td><td>Supply voltage; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 47 μF in parallel with a ceramic capacitor of 100 nF.</td></tr>
<tr><td>14</td><td>Error 2 output; signals with “low” the errors: short circuit to ground of one or more outputs or overtemperature.</td></tr>
<tr><td>13, 16</td><td>Push-pull outputs Q22, Q21 for phase 2 with integrated free-wheeling diodes.</td></tr>
<tr><td>15</td><td>Resistor R_2 for sensing the current in phase 2.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

Pin No.	Function
21	**Error 1 output;** signals with "low" the errors: open load or short circuit to + V_S of one or more outputs or short circuit of the load or overtemperature.
22	**Input phase 2;** controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L-potential in the reverse direction.

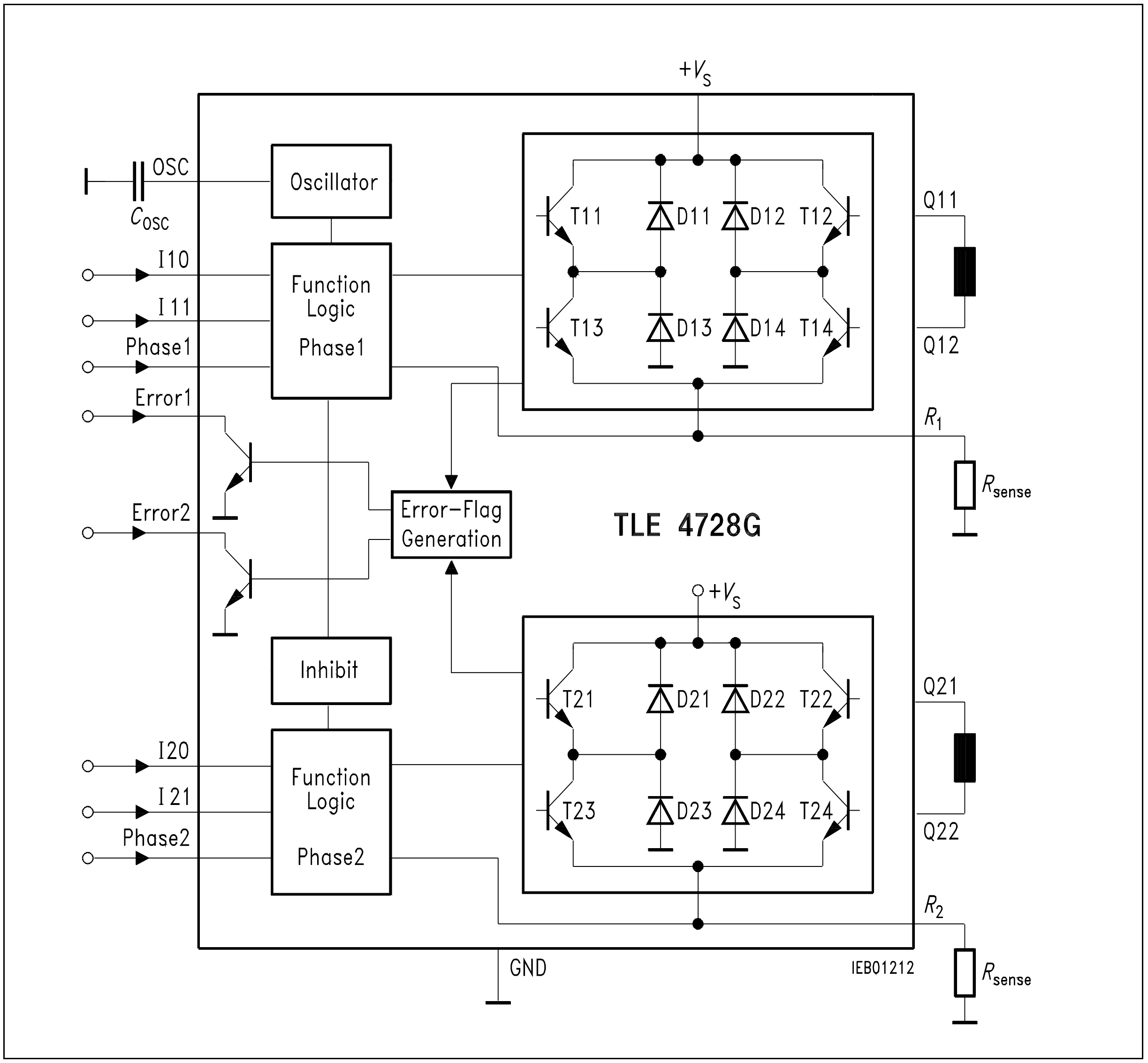


Figure 2 Block Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	45	V	–
Error outputs	V_{Err} I_{Err}	– 0.3 –	45 3	V mA	– –
Output current	I_Q	– 1	1	A	–
Ground current	I_{GND}	– 2	–	A	–
Logic inputs	V_{IXX}	– 15	15	V	IXX; Phase 1, 2
Oscillator voltage	V_{OSC}	– 0.3	6	V	–
R_1, R_2 input voltage	V_{RX}	– 0.3	5	V	–
Junction temperature	T_j T_j	– –	125 150	°C °C	– Max. 10,000 h
Storage temperature	T_{stg}	– 50	125	°C	–
Thermal resistances Junction-ambient Junction-ambient (soldered on a 35 µm thick 20 cm^2 PC board copper area) Junction-case	 $R_{th\ ja}$ $R_{th\ ja}$ $R_{th\ jc}$	 – – –	 75 50 15	 K/W K/W K/W	 – – Measured on pin 5

***Note:** Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	5	16	V	–
Case temperature	T_C	– 40	110	°C	Measured on pin 5 P_{diss} = 2 W
Output current	I_Q	– 800	800	mA	–
Logic inputs	V_{IXX}	– 5	6	V	IXX; Phase 1, 2
Error outputs	V_{Err} I_{Err}	– 0	25 1	V mA	– –

Note: In the operating range, the functions given in the circuit description are fulfilled.

For details see next four pages.
These parameters are not 100% tested in production, but guaranteed by design.

Characteristics

V_S = 6 to 16 V; T_j = – 40 to 130 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
From + V_S	I_S	0.8	1.7	2.7	mA	IXX = H
From + V_S	I_S	20	30	50	mA	IXX = L; $I_{Q1,2}$ = 0 A
Oscillator						
Output charging current	I_{OSC}	90	120	135	µA	–
Charging threshold	V_{OSCL}	0.8	1.3	1.9	V	–
Discharging threshold	V_{OSCH}	1.7	2.3	2.9	V	–
Frequency	f_{OSC}	18	24	30	kHz	C_{OSC} = 2.2 nF

Characteristics (cont'd)

V_S = 6 to 16 V; T_j = – 40 to 130 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Phase Current (V_S = 9 … 16 V)						
Mode "no current"	I_Q	– 2	0	2	mA	IX0 = H; IX1 = H
Voltage threshold of current Comparator at R_{sense} in mode:						
Hold	V_{ch}	40	70	100	mV	IX0 = L; IX1 = H
Setpoint	V_{cs}	410	450	510	mV	IX0 = H; IX1 = L
Accelerate	V_{ca}	630	700	800	mV	IX0 = L; IX1 = L
Logic Inputs (IX1; IX0; Phase X)						
Threshold	V_I	1.2	1.7	2.2	V	–
Hysteresis	V_{IHy}	–	50	–	mV	–
L-input current	I_{IL}	– 10	– 1	1	µA	V_I = 1.2 V
L-input current	I_{IL}	– 100	– 20	– 5	µA	V_I = 0 V
H-input current	I_{IH}	– 1	0	10	µA	V_I = 5 V
Error Outputs						
Saturation voltage	V_{ErrSat}	50	200	500	mV	I_{Err} = 1 mA
Leakage current	I_{ErrL}	–	–	10	µA	V_{Err} = 25 V
Thermal Protection						
Shutdown	T_{jsd}	140	150	160	°C	$I_{Q1,2}$ = 0 A
Prealarm	T_{jpa}	120	130	140	°C	V_{Err} = L
Delta	ΔT_j	10	20	30	K	$\Delta T_j = T_{jsd} - T_{jpa}$

Characteristics (cont'd)

V_S = 6 to 16 V; T_j = – 40 to 130 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Outputs						
Diode Transistor Sink Pair (D13, T13; D14, T14; D23, T23; D24, T24)						
Saturation voltage	V_{satI}	0.1	0.3	0.5	V	I_Q = – 0.45 A
Saturation voltage	V_{satI}	0.2	0.5	0.8	V	I_Q = – 0.7 A
Reverse current	I_{RI}	500	1000	1500	µA	V_S = V_Q = 40 V
Forward voltage	V_{FI}	0.6	0.9	1.2	V	I_Q = 0.45 A
Forward voltage	V_{FI}	0.7	1	1.3	V	I_Q = 0.7 A
Diode Transistor Source Pair (T11, D11; T12, D12; T21, D21; T22, D22)						
Saturation voltage	V_{satuC}	0.6	1	1.2	V	I_Q = 0.45 A; charge
Saturation voltage	V_{satuD}	0.1	0.3	0.6	V	I_Q = 0.45 A; discharge
Saturation voltage	V_{satuC}	0.7	1.2	1.5	V	I_Q = 0.7 A; charge
Saturation voltage	V_{satuD}	0.2	0.5	0.8	V	I_Q = 0.7 A; discharge
Reverse current	I_{Ru}	400	800	1200	µA	V_S = 40 V, V_Q = 0 V
Forward voltage	V_{Fu}	0.7	1	1.3	V	I_Q = – 0.45 A
Forward voltage	V_{Fu}	0.8	1.1	1.4	V	I_Q = – 0.7 A
Diode leakage current	I_{SL}	0	3	10	mA	I_F = – 0.7 A
Error Output Timing						
Time Phase X to IXX	t_{PI}	–	5	15	µs	–
Time IXX to Phase X	t_{IP}	–	12	–	µs	–
Delay Phase X to Error 2	t_{PEsc}	–	45	80	µs	–
Delay Phase X to Error 1	t_{PEoI}	–	15	30	µs	–
Delay IXX to Error 2	t_{IEsc}	–	30	60	µs	–
Reset delay after Phase X	t_{RP}	–	3	10	µs	–
Reset delay after IXX	t_{RI}	–	1	5	µs	–

Diagrams

Timing between IXX and Phase X to prevent setting the error flag

Operating conditions:
+ V_S = 14 V, T_j = 25 °C, I_{err} = 1 mA, load = 3.3 mH, 1 Ω

a) If t_{PI} < typ. 5 µs, an error “open load” will be set.

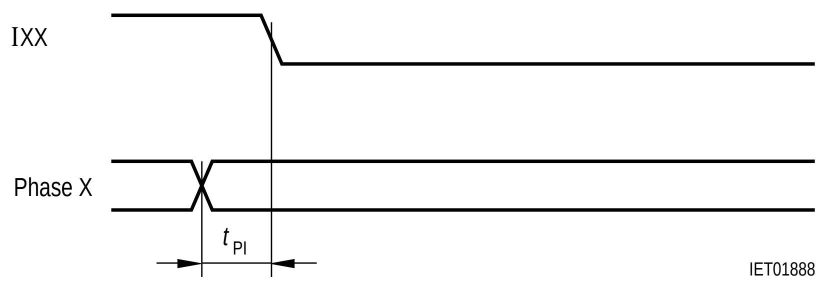


Figure 3

b) If t_{IP} < typ. 12 µs, an error “open load” will be set.

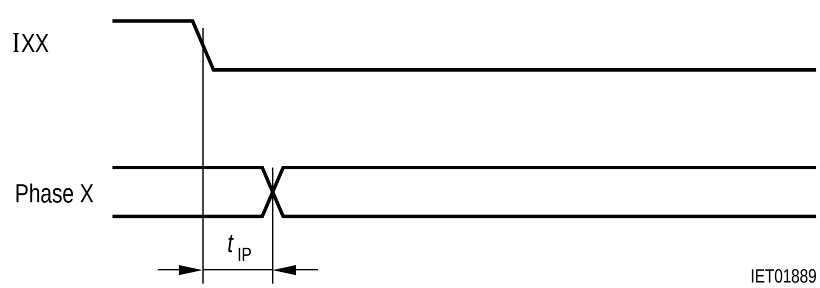
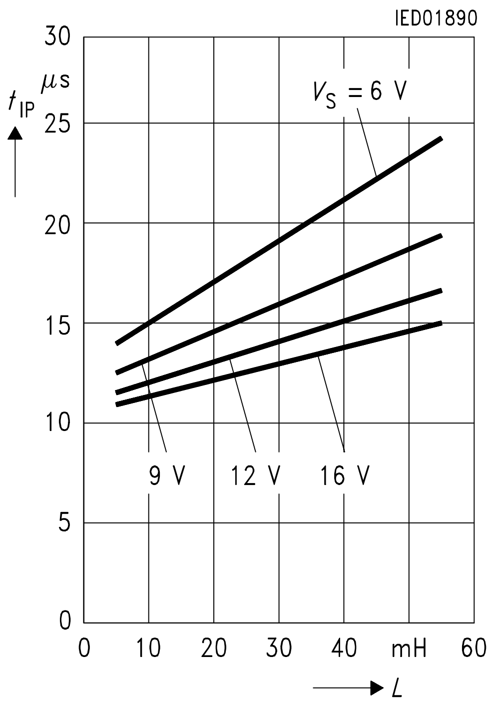


Figure 4

This time strongly depends on + V_S and inductivity of the load, see diagram below.

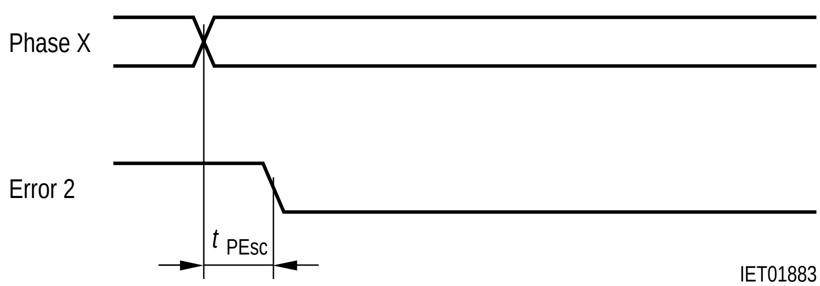
Time t_{IP} versus Load Inductivity



Propagation Delay of the Error Flag

Operating conditions:
+ V_S = 14 V, T_j = 25 °C, I_{err} = 1 mA, load = 3.3 mH, 1 Ω

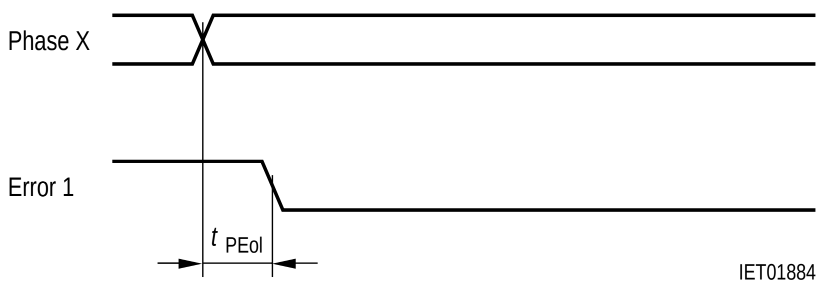
a) IXX = L, error condition: short circuit to GND.



typ. t_{PEsc}: 45 µs

Figure 5

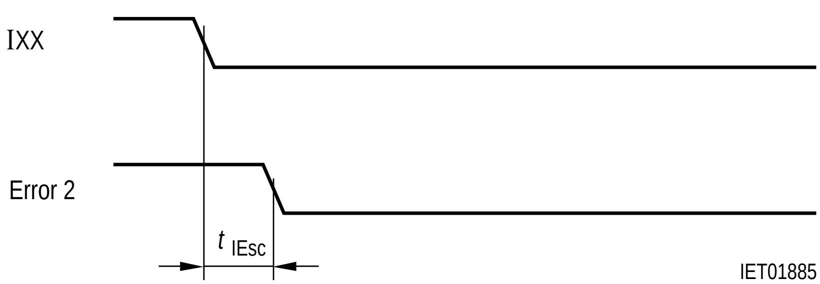
b) IXX = L, error condition: open load (equivalent: short circuit to + V_S).



typ. t_{PEol}: 15 µs

Figure 6

c) Phase X = H or L, const.; error condition: short circuit to GND.

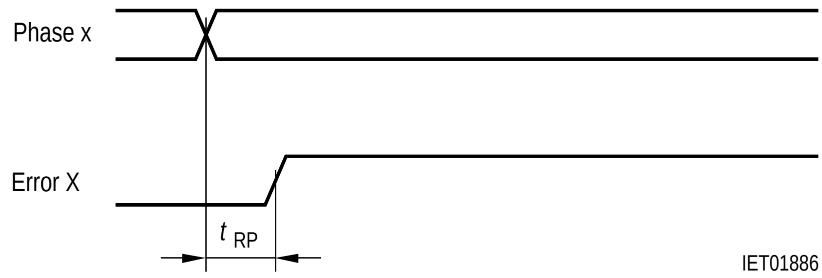


typ. t_{IEsc}: 30 µs

t_{IEsc} is also measured under the condition: begin of short circuit to GND till error flag set.

Figure 7

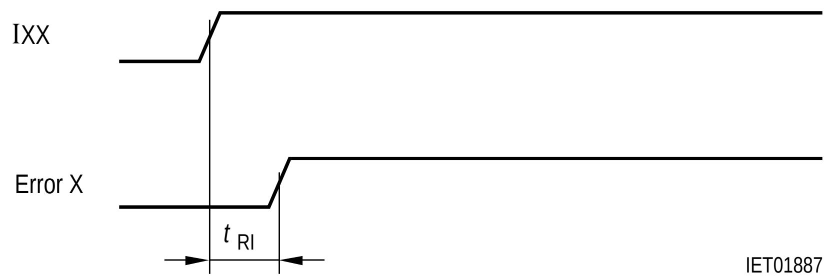
d) IXX = L, reset of error flag when error condition is not true.



typ. t_{RP}: 3 µs

Figure 8

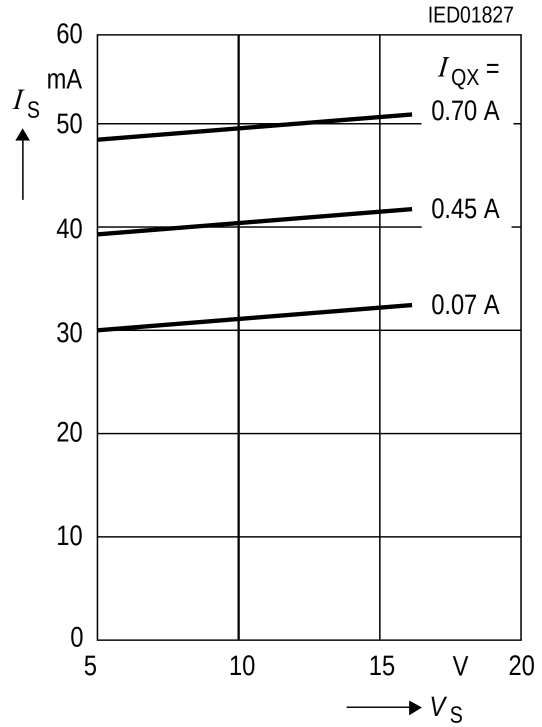
e) Phase X = H or L, const.; reset of error flag when error condition is not true.



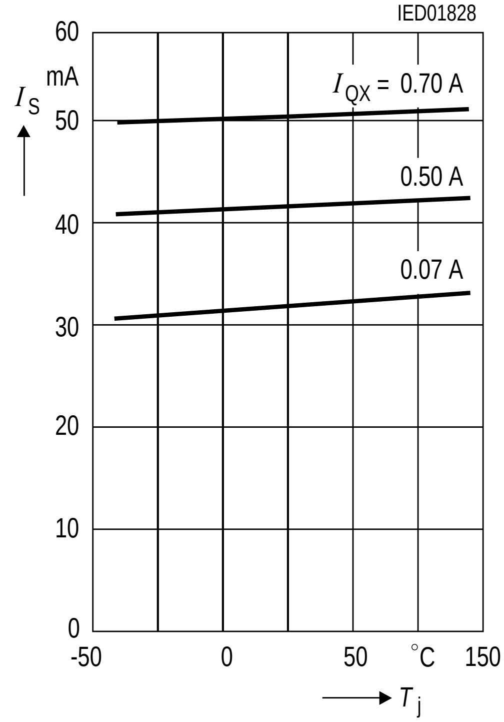
typ. t_{RI}: 1 µs

Figure 9

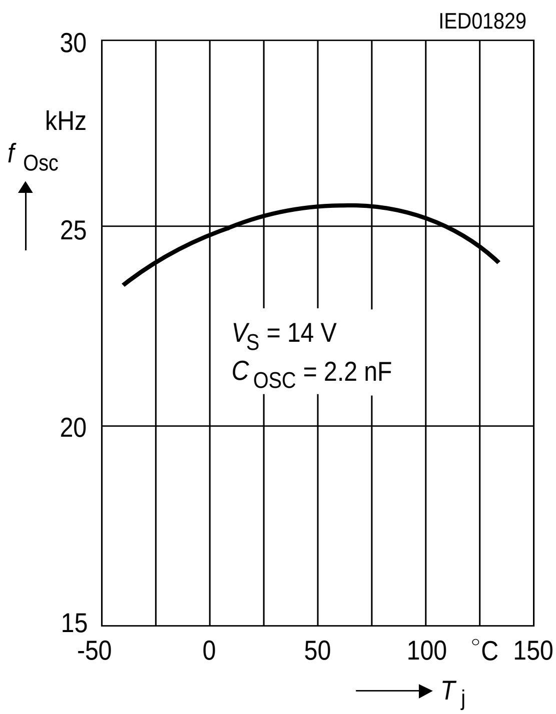
Quiescent Current I_S versus Supply Voltage V_S; bridges not chopping; T_j = 25 °C



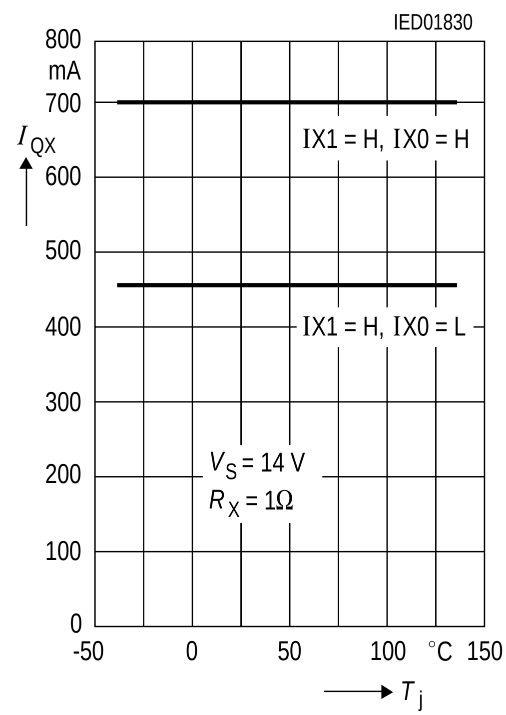
Quiesc. Current I_S versus Junct. Temp. T_j; bridges not chopping, V_S = 14 V



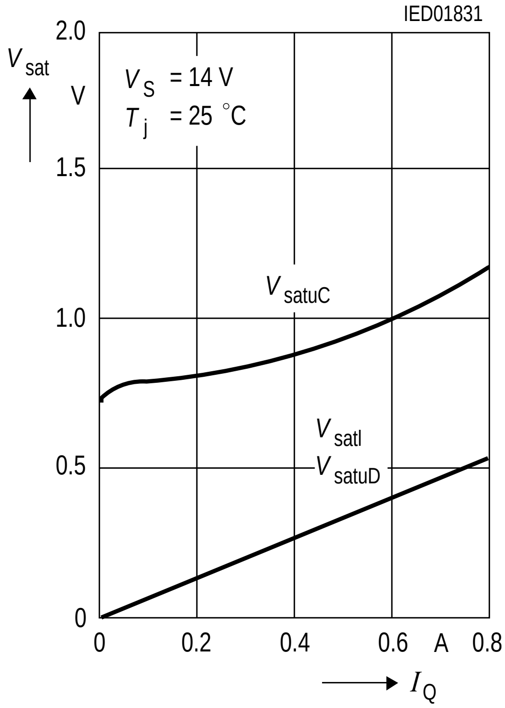
Oscillator Frequency f_{Osc} versus Junction Temperature T_j



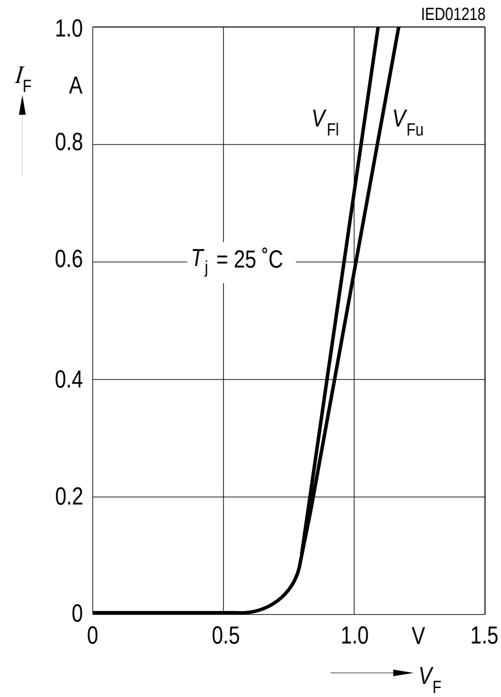
Output Current I_{QX} versus Junction Temperature T_j



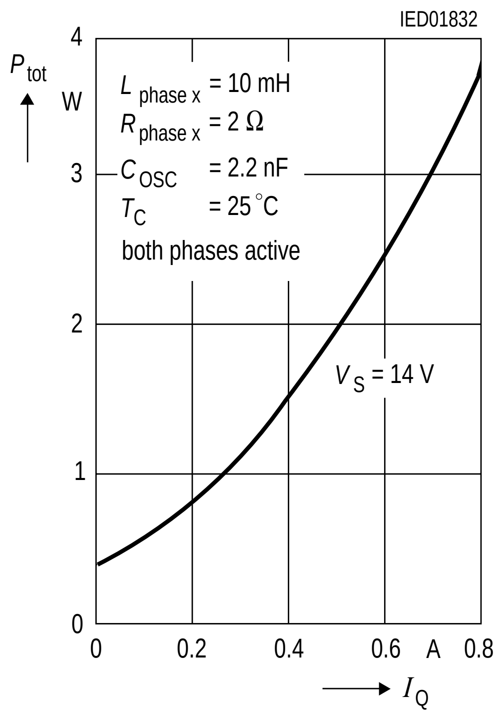
Output Saturation Voltages V_{sat} versus Output Current I_Q



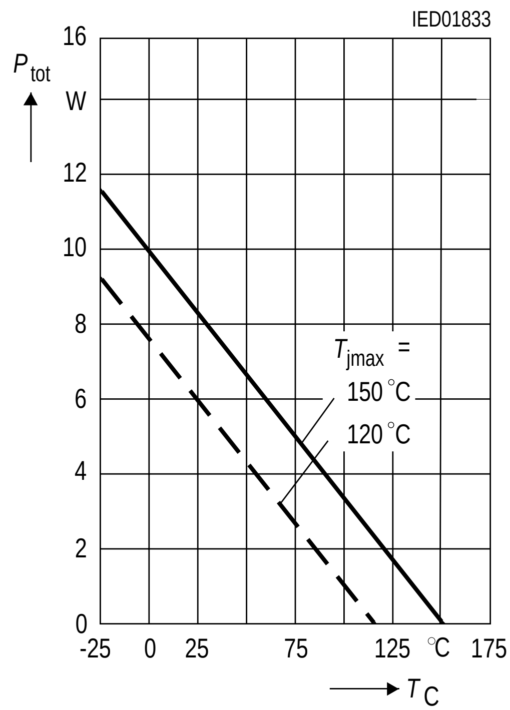
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



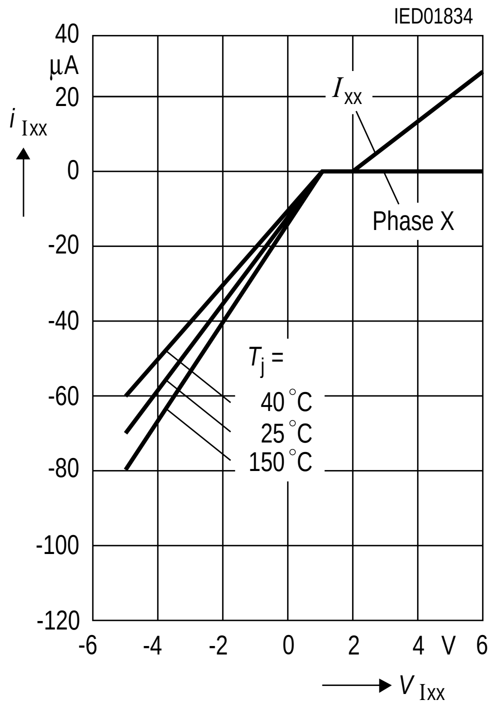
Typical Power Dissipation P_{tot} versus Output Current I_Q (non stepping)



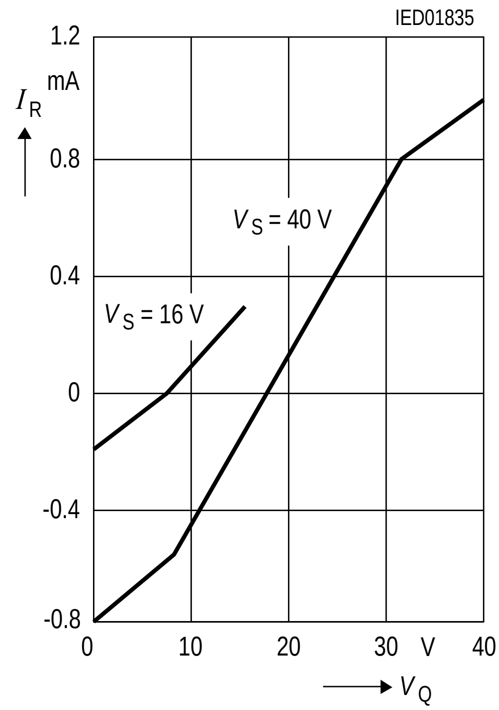
Permissible Power Dissipation P_{tot} versus Case Temp. T_C (measured at pin 5)



Input Characteristics of I_{XX}, Phase X



Output Leakage Current



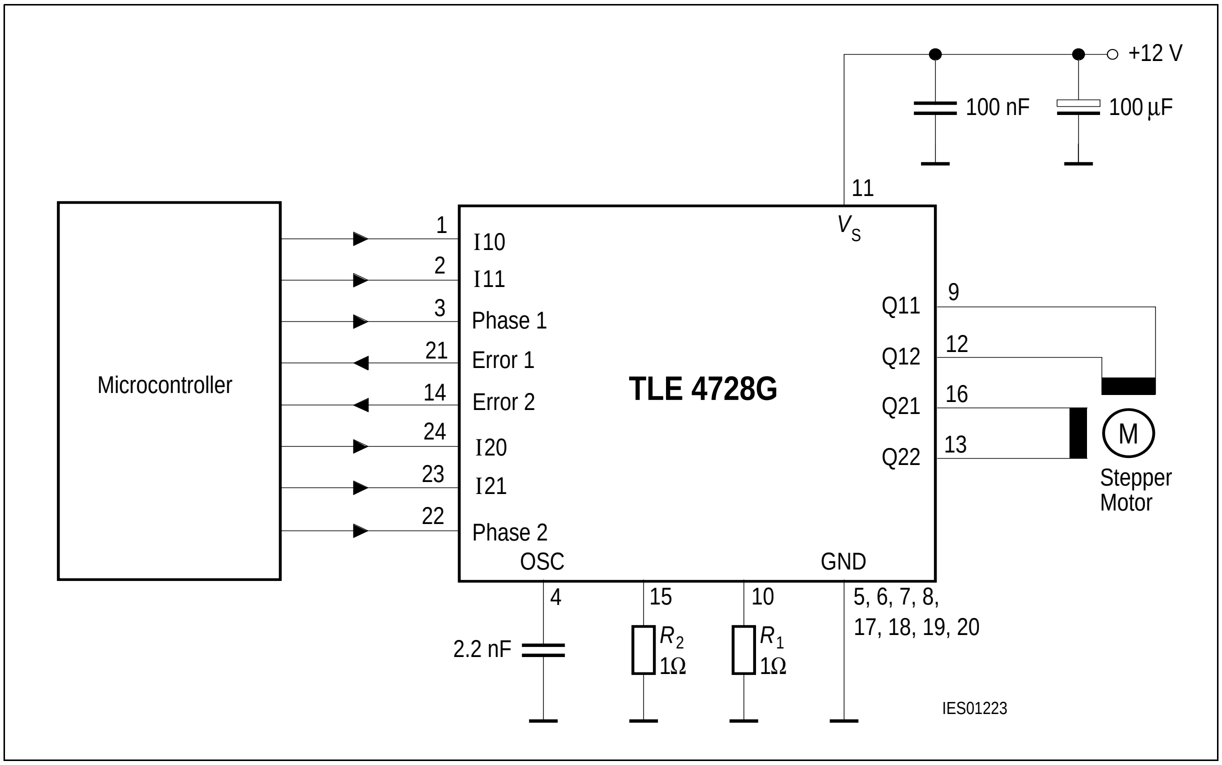


Figure 10 Application Circuit

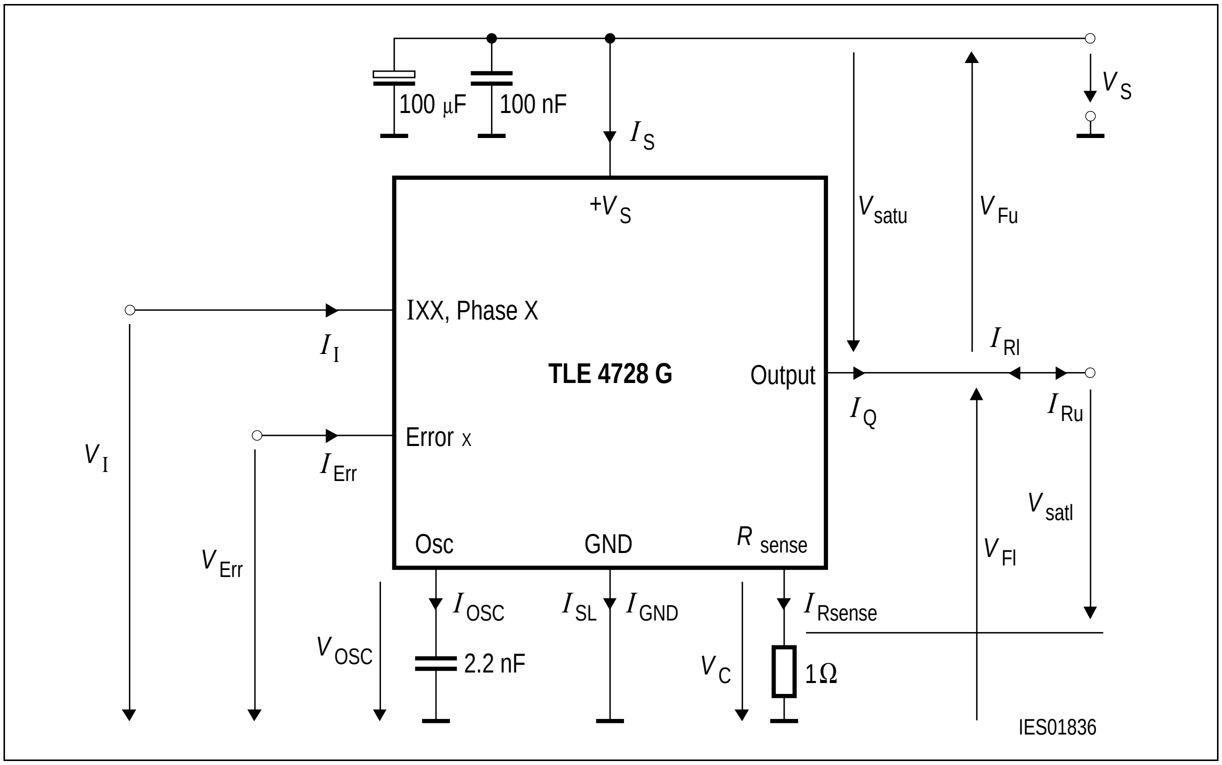


Figure 11 Test Circuit

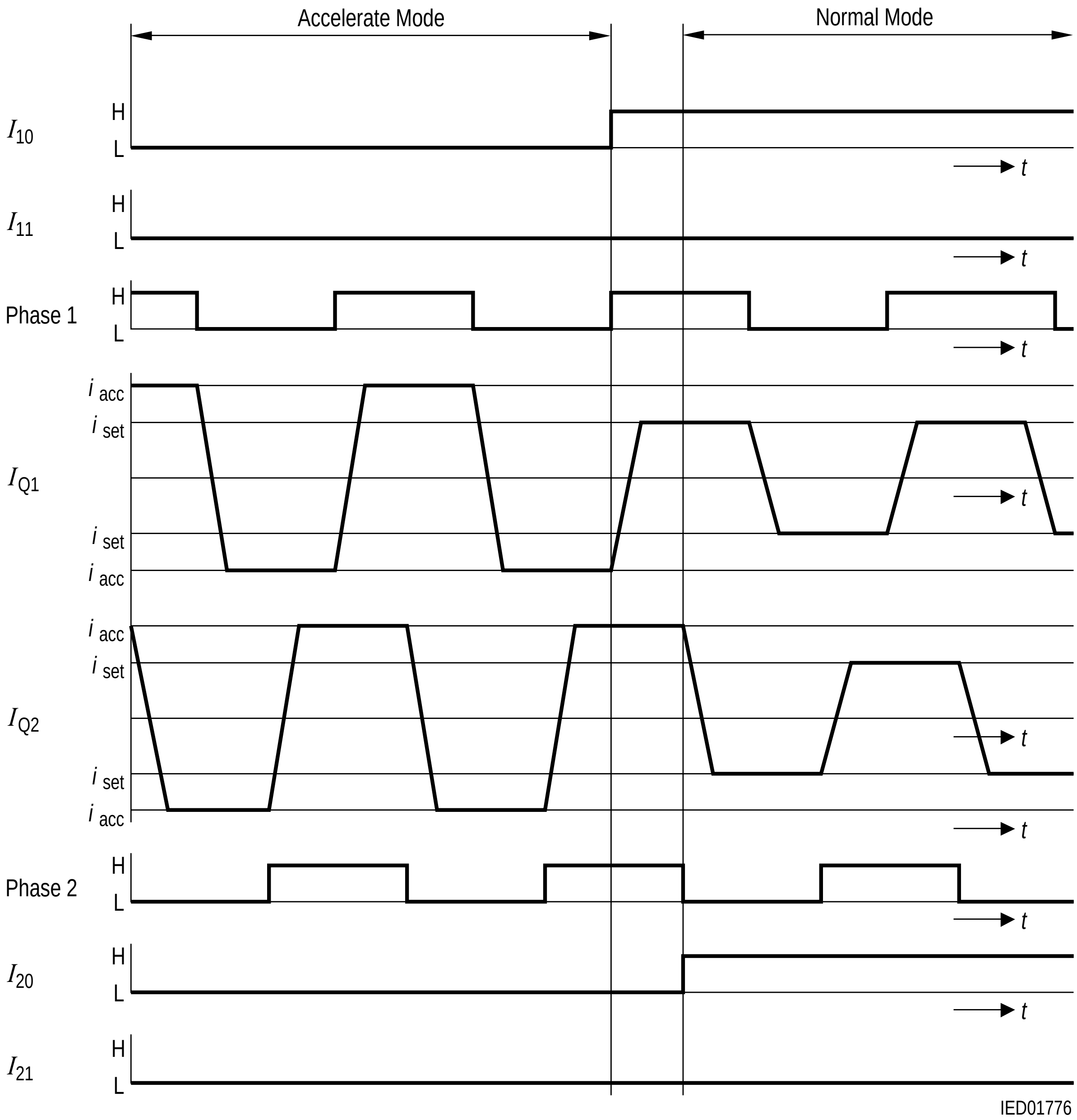


Figure 12 Full Step Operation

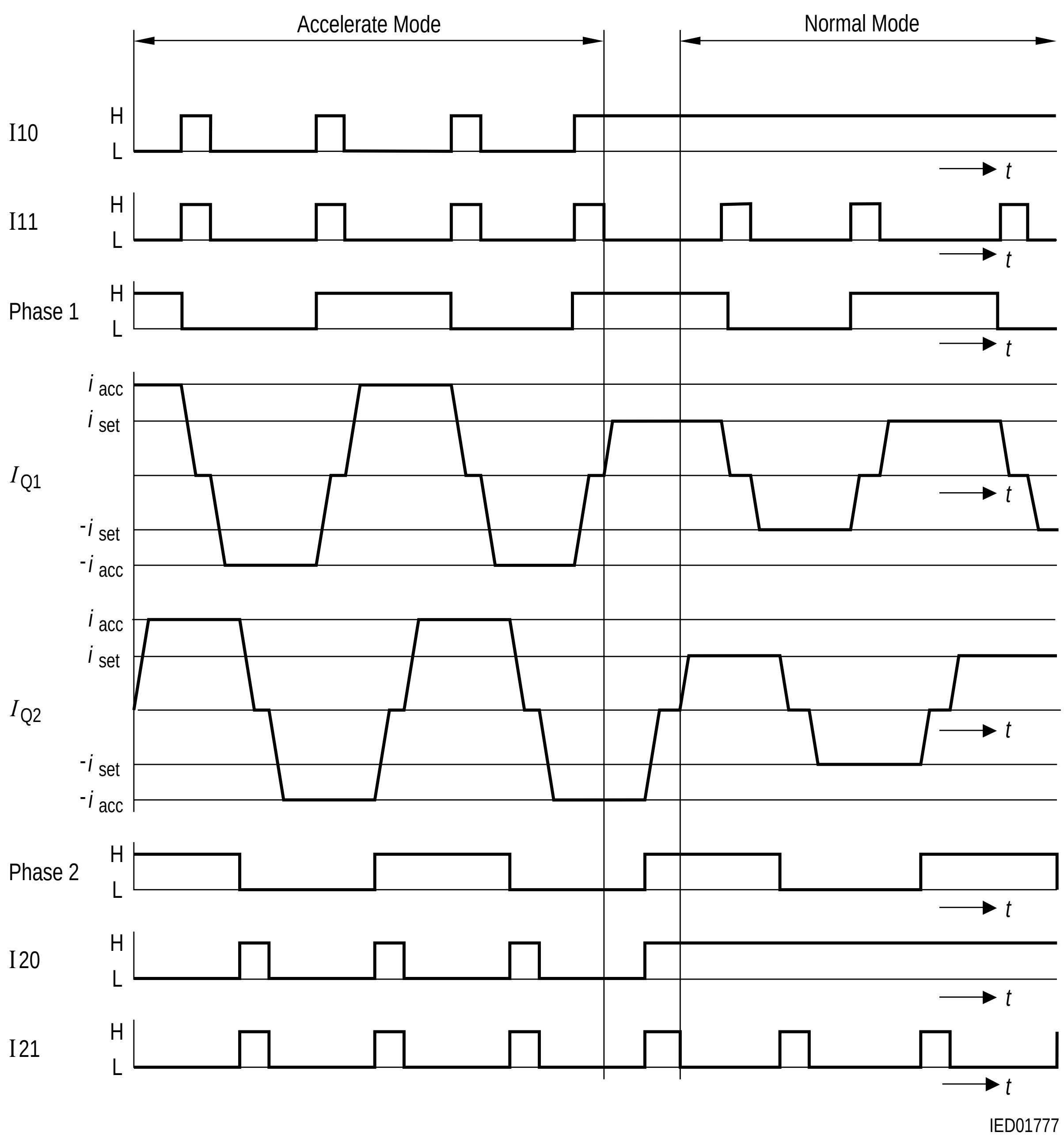
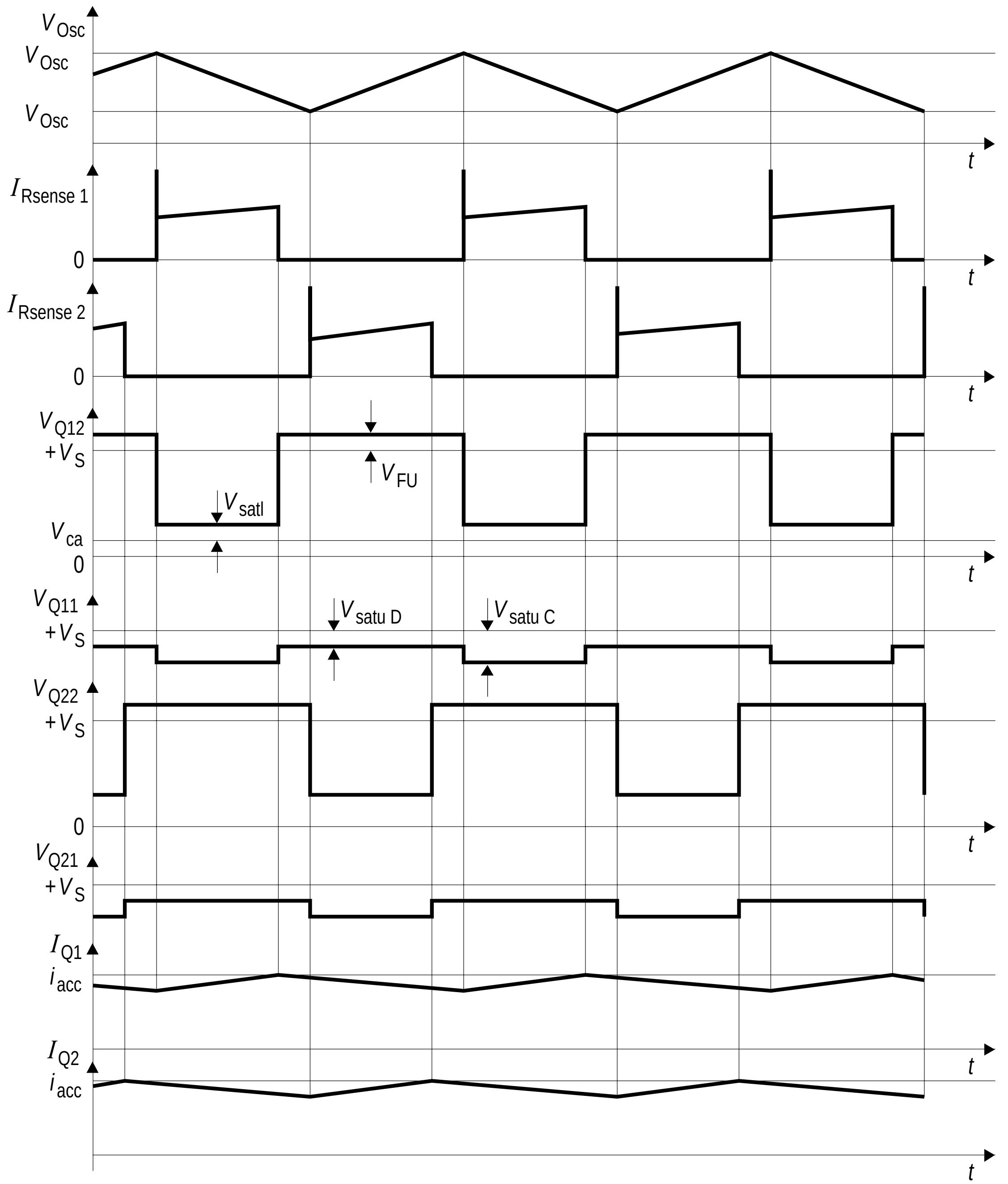


Figure 13 Half Step Operation



Operating conditions:

V_S	= 14 V	Phase = H
$L_{\text{phase x}}$	= 10 mH	IXX = L
$R_{\text{phase x}}$	= 4 Ω	

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Figure 14 Current Control in Chop-Mode

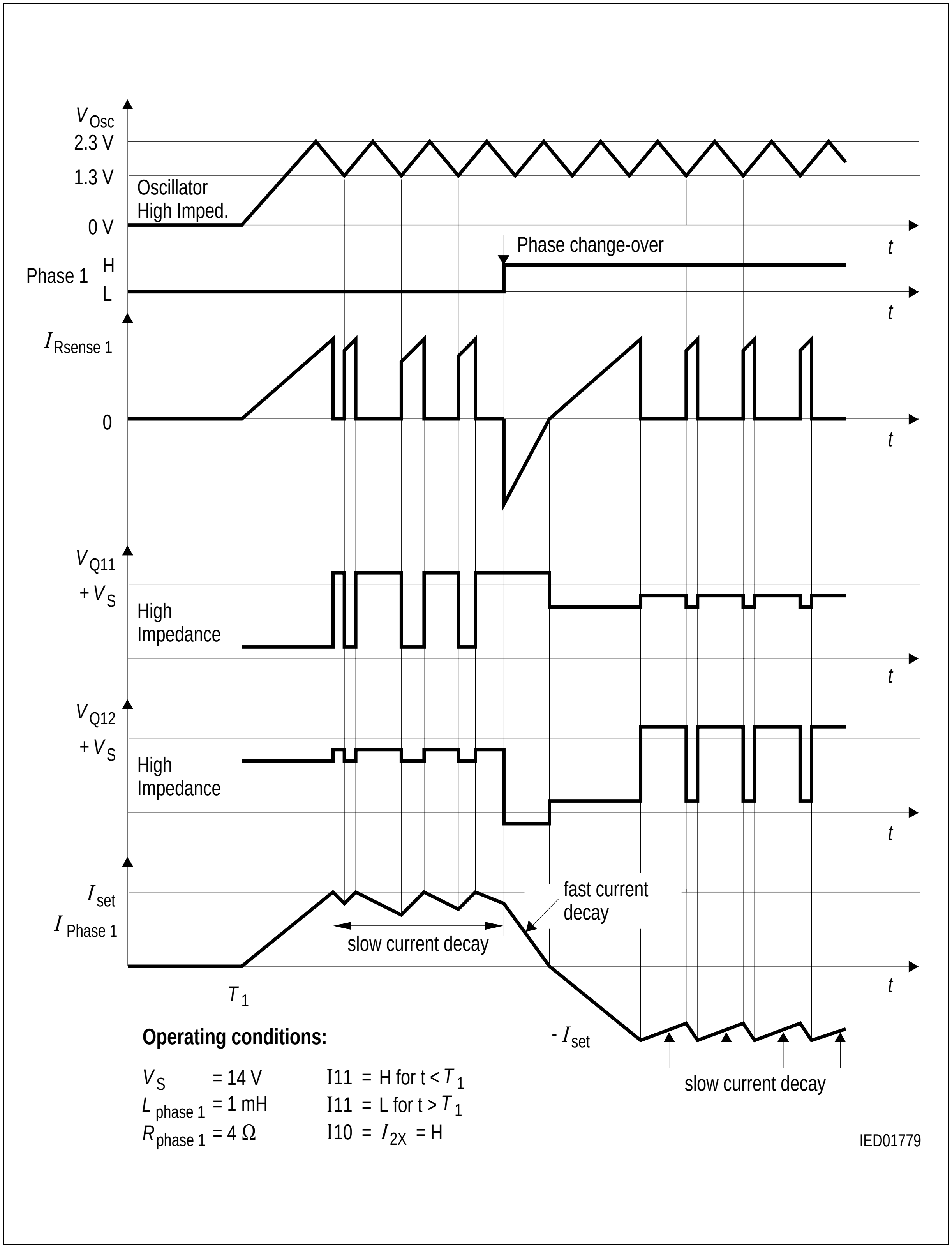


Figure 15 Phase Reversal and Inhibit

Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat}	(transistor saturation voltage and diode forward voltages),
quiescent losses P_q	(quiescent current times supply voltage) and
switching losses P_s	(turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

$$P_{tot} = 2 \times P_{sat} + P_q + 2 \times P_s$$

where

$$P_{sat} \cong I_N \{ V_{satl} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d) \}$$

$$P_q = I_q \times V_S$$

$$P_q \cong \frac{V_S}{T} \left\{ \frac{i_D \times t_{DON}}{2} + \frac{(i_D + i_R) \times t_{ON}}{4} + \frac{I_N}{2}(t_{DOFF} + t_{OFF}) \right\}$$

I_N	= nominal current (mean value)
I_q	= quiescent current
i_D	= reverse current during turn-on delay
i_R	= peak reverse current
t_p	= conducting time of chopper transistor
t_{ON}	= turn-ON time
t_{OFF}	= turn-OFF time
t_{DON}	= turn-ON delay
t_{DOFF}	= turn-OFF delay
T	= cycle duration
d	= duty cycle t_p / T
V_{satl}	= saturation voltage of sink transistor (TX3, TX4)
V_{satuC}	= saturation voltage of source transistor (TX1, TX2) during charge cycle
V_{satuD}	= saturation voltage of source transistor (TX1, TX2) during discharge cycle
V_{Fu}	= forward voltage of free-wheeling diode (DX1, DX2)
V_S	= supply voltage

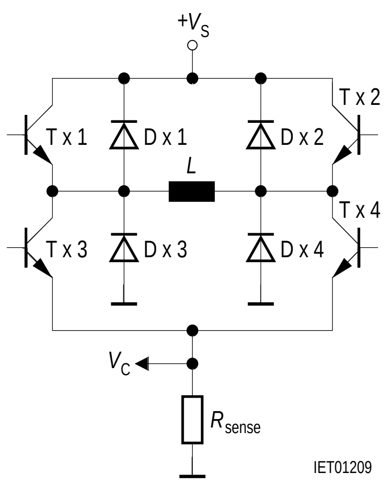


Figure 16

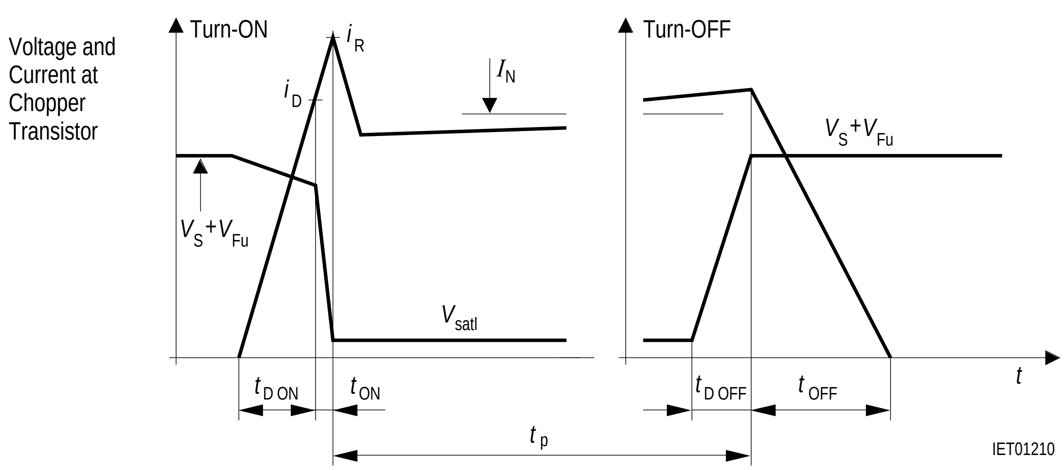


Figure 17 Voltage and Current on Chopper Transistor

Application Hints

The TLE 4728 G is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TLE 4728 G will work with supply voltages ranging from 5 V to 16 V at pin V_S. Surges exceeding 16 V at V_S wont harm the circuit up to 45 V, but whole function is not guaranteed. As soon as the voltage drops below approximately 16 V the TLE 4728 G works promptly again.

As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.1 µF ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_{sense}. Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.07 V, 0.45 V and 0.7 V). These thresholds are not affected by variations of V_S. Consequently unstabilized supplies will not affect the performance of the regulation. For precise current level it must be considered, that internal bounding wire (typ. 60 mΩ) is a part of R_{sense}.

Due to chopper control fast current rises (up to 10 A/µs) will occur at the sensing resistors. To prevent malfunction of the current sensing mechanism R_{sense} should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchrone chopping of several stepper motor drivers may be desirable to reduce acoustic interference. This can be done by forcing the oscillator of the TLE 4728 G by a pulse generator overdriving the oscillator loading currents (approximately ± 120 µA). In these applications low level should be between 0 V and 0.8 V while high level should between 3 V and 5 V.

Optimizing Noise Immunity

Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TLE 4728 G uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the phase inputs should be avoided by proper control signals.

To lower EMI a ceramic capacitor of max. 3 nF is advisable from each output to GND.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented.

Error Monitoring

The error outputs signal corresponding to the logic table the errors described below.

Logic Table

Kind of Error		Error Output	
		Error 1	**Error 2**
a)	No error	H	H
b)	Short circuit to GND	H	L
c)	Open load [1)]	L	H
d)	b) and c) simultaneously	H	L
e)	Temperature pre-alarm	L	L

1) Also possible: short circuit to + V_S or short circuit of the load.

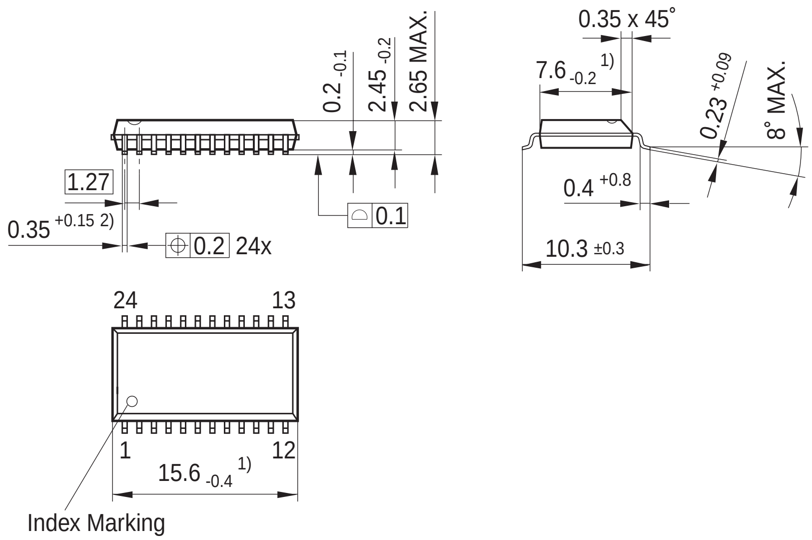
Overtemperature is implemented as pre-alarm; it appears approximately 20 K before thermal shut down. To detect an **open load**, the recirculation of the inductive load is watched. If there is no recirculation after a phase change-over, an internal error flipflop is set. Because in most kinds of **short circuits** there won't flow any current through the motor, there will be no recirculation after a phase change-over, and the error flipflop for open load will be set, too. Additionally an **open load error** is signaled after a phase change-over during hold mode.

Only in the case of a **short circuit to GND**, the most probably kind of a short circuit in automotive applications, the malfunction is signaled dominant (see d) in logic table) by a separate error flag. Simultaneously the output current is disabled after 30 µs to prevent disturbances.

A phase change-over or putting both current control inputs of the affected bridge on high potential resets the error flipflop. Being a separate flipflop for every bridge, the error can be located in easy way.

Package Outlines

P-DSO-24-9
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm