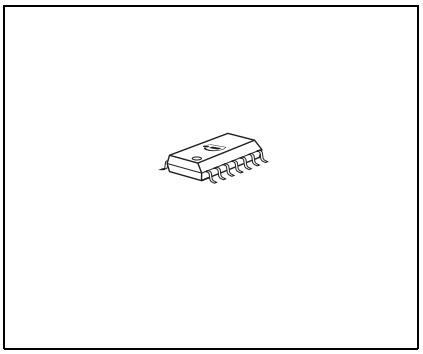
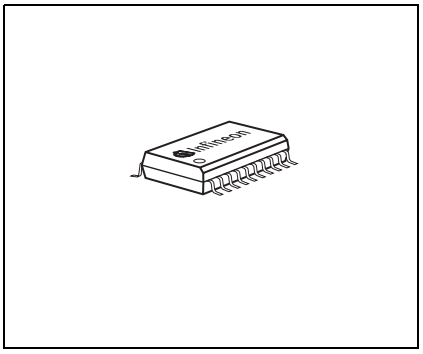
# 5-V Low Drop Voltage Regulator

# TLE 4262

## Features

- Output voltage tolerance ≤ ±2%
- 200 mA output capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Wide temperature range
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)
- AEC Qualified





## Functional Description

TLE 4262 GM is a 5-V low-drop voltage regulator in a PG-DSO-14 or PG-DSO-20 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and includes a temperature protection which turns off the IC at overtemperature.

The IC regulates an input voltage $V_I$ in the range of 6 V < $V_I$ < 45 V to $V_{Q,nom}$ = 5.0 V. A reset signal is generated for an output voltage of $V_{Q,rt}$ < 4.5 V. This voltage threshold can be decreased to 3.5 V by external connection of a voltage divider. The reset delay can be set externally with a capacitor. The IC can be switched off via the inhibit input, which reduces the current consumption from 900 µA to typical 0 µA.

| Type | Package |
|---|---|
| TLE 4262 GM | PG-DSO-14-30 |
| TLE 4262 G | PG-DSO-20-35 |

## Dimensioning Information on External Components

The input capacitor $C_I$ is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with $C_I$, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay, the spread of the capacitance of the dalay capacitor and its temperature coefficient should be noted.

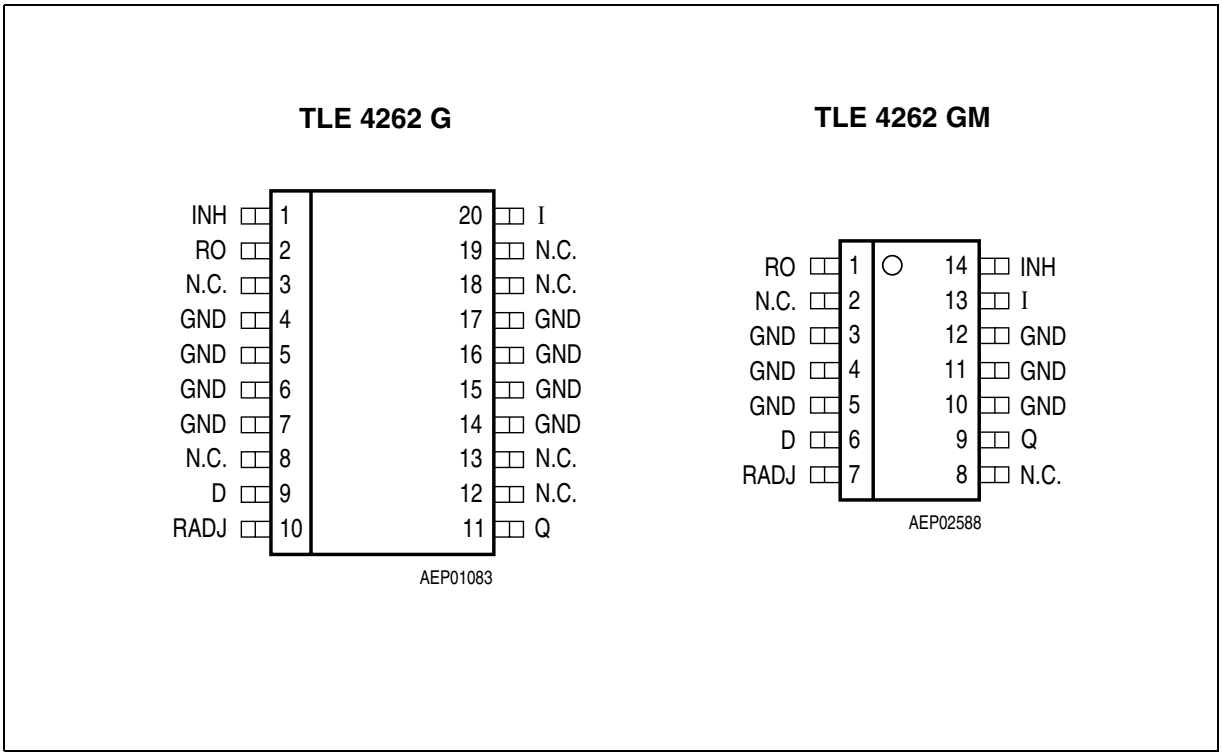



**Figure 1 Pin Configuration** (top view)

**Table 1 Pin Definitions and Functions**

| Pin PG-DSO-14-30 | Pin PG-DSO-20-35 | Symbol | Function |
|---|---|---|---|
| 1 | 2 | RO | **Reset output;** open-collector output internally connected to the output via a resistor of 30 kΩ. |
| 2, 8 | 3, 8, 12, 13, 18, 19 | N.C. | Not connected |
| 3 - 5, 10 - 12 | 4 - 7, 14 - 17 | GND | **Ground** |
| 6 | 9 | D | **Reset delay;** connect capacitor to GND for setting delay time |
| 7 | 10 | RADJ | **Reset threshold;** for setting the switching threshold connect by a voltage divider from output to ground. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V. |
| 9 | 11 | Q | **5-V output voltage;** block to ground by capacitor with $C \geq 22$ µF, ESR ≤ 3 Ω at 10 kHz. |
| 13 | 20 | I | **Input voltage;** block to ground directly at the IC by a ceramic capacitor. |
| 14 | 1 | INH | **Inhibit;** TTL-compatible, low-active input |

## Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold $V_{DRL}$, a reset signal is issued on the reset output and not cancelled again until the upper threshold $V_{DU}$ is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. The IC can be switched at the TTL-compatible, low-active inhibit input. It also includes a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

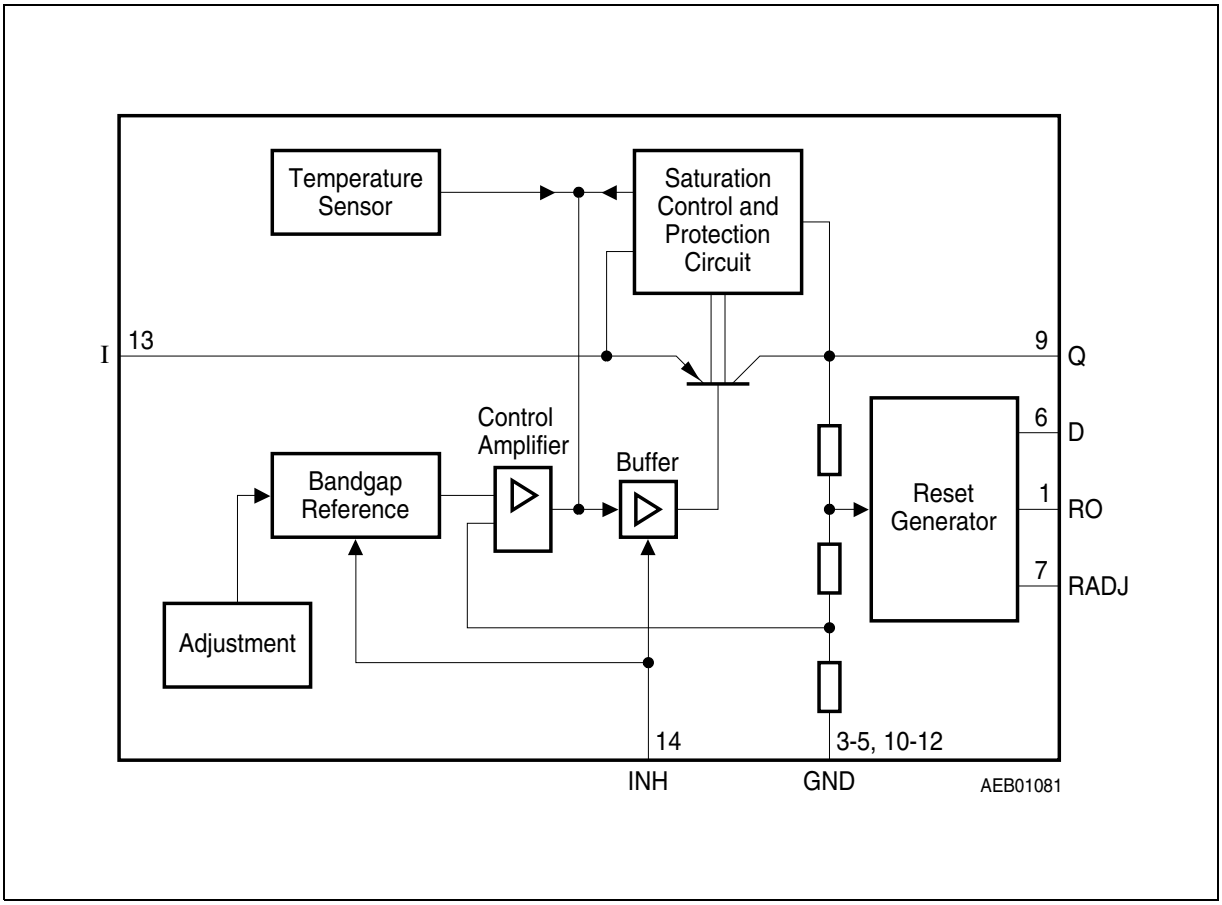



**Figure 2 Block Diagram**

**Table 2 Absolute Maximum Ratings**

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| **Input I** | | | | | |
| Input voltage | $V_I$ | -42 | 45 | V | – |
| Input current | $I_I$ | – | – | – | internally limited |
| **Reset Output RO** | | | | | |
| Voltage | $V_{RO}$ | -0.3 | 42 | V | – |
| Current | $I_{RO}$ | – | – | – | internally limited |
| **Reset Input RADJ** | | | | | |
| Voltage | $V_{RADJ}$ | -0.3 | 6 | V | – |
| **Reset Delay D** | | | | | |
| Voltage | $V_D$ | -0.3 | 42 | V | – |
| Current | $I_D$ | – | – | – | internally limited |
| **Output Q** | | | | | |
| Voltage | $V_Q$ | -5.25 | $V_I$ | V | – |
| Current | $I_Q$ | – | – | – | internally limited |
| **Inhibit INH** | | | | | |
| Voltage | $V_{INH}$ | -42 | 45 | V | – |
| **Ground GND** | | | | | |
| Current | $I_{GND}$ | -0.5 | – | A | – |
| **Temperature** | | | | | |
| Junction temperature | $T_j$ | – | 150 | °C | – |
| Storage temperature | $T_{stg}$ | -50 | 150 | °C | – |
| **Operating Range** | | | | | |
| Input voltage | $V_I$ | 5.2 | 45 | V | 1) |
| Junction temperature | $T_j$ | -40 | 150 | °C | – |
| Thermal resistance | | | | | |
| junction-ambient | $R_{thj\text{-}a}$ | – | 112 | K/W | 2) |
| junction-case | $R_{thj\text{-}p}$ | – | 32 | K/W | 3) |

1) Corresponds with characteristics of drop voltage, output current and power description (**see diagrams**).

2) Package mounted on PCB 80 × 80 × 1.5 mm$^3$; 35µ Cu; 5µ Sn; Footprint only; zero airflow.

3) Measured to pin 4.

**Table 3 Characteristics**

$V_I$ = 13.5 V; $T_j$ = 25 °C; $V_{INH}$ > 3.5 V; (unless specified otherwise)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Normal Operation** | | | | | | |
| Output voltage | $V_Q$ | 4.90 | 5.00 | 5.10 | V | 5 mA ≤ $I_Q$ ≤ 150 mA;<br>6 V ≤ $V_I$ ≤ 28 V;<br>-40 °C ≤ $T_j$ ≤ 125 °C |
| Output voltage | $V_Q$ | 4.90 | 5.00 | 5.10 | V | 6 V ≤ $V_I$ ≤ 32 V;<br>$I_Q$ = 100 mA<br>$T_j$ = 100 °C |
| Output current limiting | $I_Q$ | 200 | 250 | – | mA | – |
| Current consumption;<br>$I_q = I_i - I_Q$ | $I_q$<br>$I_q$<br>$I_q$<br>$I_q$ | –<br>–<br>–<br>– | 0<br>0.9<br>10<br>15 | 50<br>1.3<br>18<br>23 | µA<br>mA<br>mA<br>mA | $V_{INH}$ = 0 V<br>$I_Q$ = 0 mA<br>$I_Q$ = 150 mA<br>$I_Q$ = 150 mA; $V_i$ = 4.5 V |
| Drop voltage | $V_{DR}$ | – | 0.35 | 0.50 | V | $I_Q$ = 150 mA[1)] |
| Load regulation | $\Delta V_{Q,lo}$ | – | – | 25 | mV | $I_Q$ = 5 mA to 150 mA |
| Line regulation | $\Delta V_{Q,li}$ | – | 3 | 25 | mV | $V_I$ = 6 V to 28 V;<br>$I_Q$ = 150 mA |
| Power Supply Ripple Rejection | $PSRR$ | – | 54 | – | dB | $f_r$ = 100 Hz;<br>$V_r$ = 0.5 Vpp |
| **Reset Generator** | | | | | | |
| Switching threshold | $V_{Q,rt}$ | 4.5 | 4.65 | 4.8 | V | $V_{RADJ}$ = 0 V |
| Reset adjust threshold | $V_{RADJ}$ | 1.26 | 1.35 | 1.44 | V | $V_Q$ > 3.5 V |
| Saturation voltage | $V_{RO}$ | – | 0.10 | 0.40 | V | $I_{RO}$ = 1 mA |
| Saturation voltage | $V_{D,sat}$ | – | 50 | 100 | mV | $V_Q$ < $V_{RT}$ |
| Charge current | $I_{D,c}$ | 6 | 10 | 15 | µA | – |
| Upper timing threshold | $V_{DU}$ | 1.4 | 1.8 | 2.2 | V | – |
| Lower timing threshold | $V_{DRL}$ | 0.20 | 0.35 | 0.55 | V | – |
| Reset delay time | $t_{rd}$ | – | 17 | – | ms | $C_D$ = 100 nF |
| Reset reaction time | $t_{rr}$ | – | 1.2 | – | µs | $C_D$ = 100 nF |

**Table 3 Characteristics** (cont'd)

$V_I$ = 13.5 V; $T_j$ = 25 °C; $V_{INH}$ > 3.5 V; (unless specified otherwise)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Inhibit** | | | | | | |
| Switch-ON voltage | $V_{INH,ON}$ | 3.6 | – | – | V | IC turned on |
| Switch-OFF voltage | $V_{INH,OFF}$ | – | – | 0.8 | V | IC turned off |
| Input current | $I_{INH}$ | 5 | 10 | 25 | µA | $V_{INH}$ = 5 V |

1) Drop voltage $V_I \geq 4.5$ V; drop voltage = $V_I$ - $V_Q$ (below regulating range)

*Note: The reset output is low within the range 1 V* $\leq V_Q \leq V_{Q,rt}$.

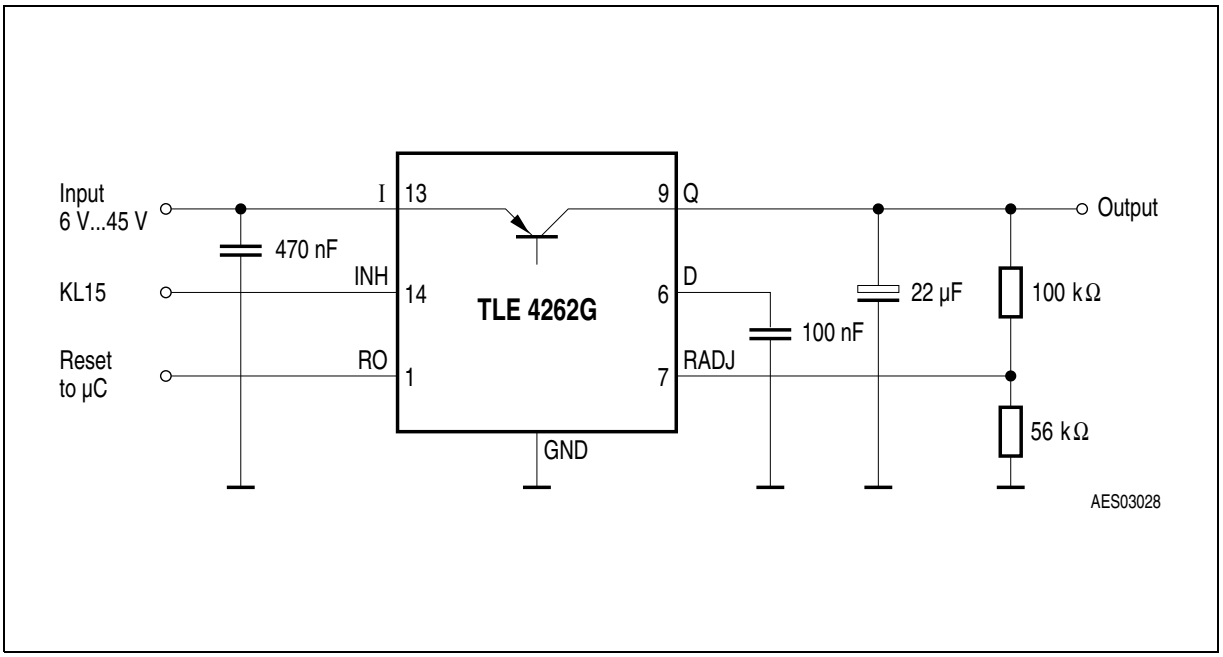



**Figure 3 Application Circuit**

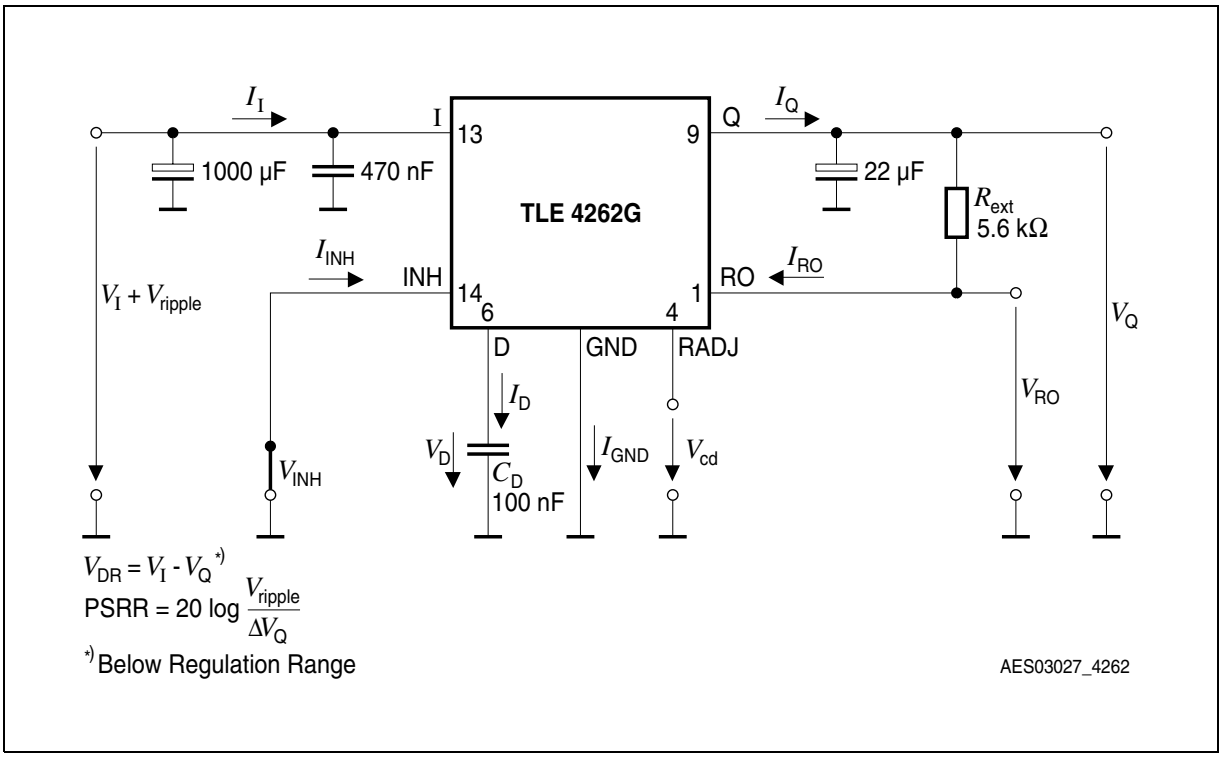



**Figure 4 Test Circuit**

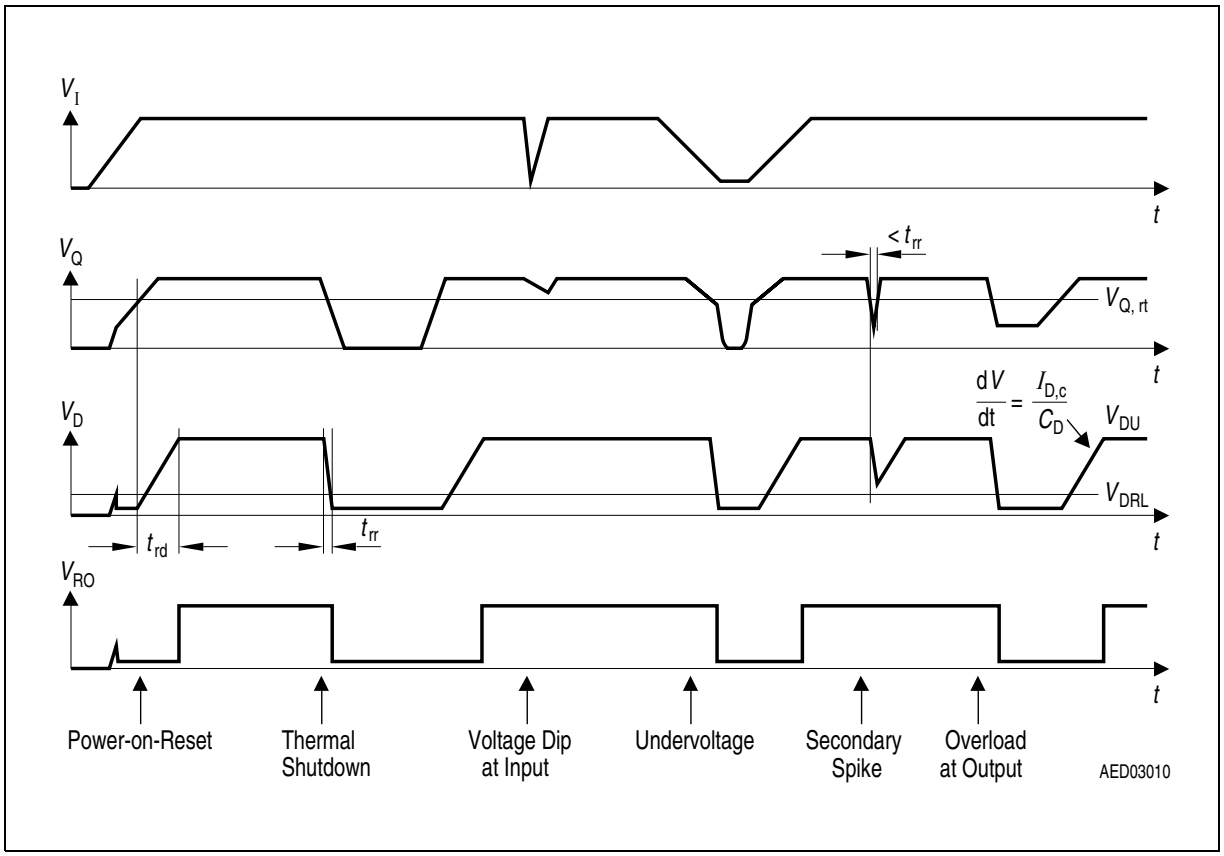



**Figure 5 Time Response**

### Reset Timing

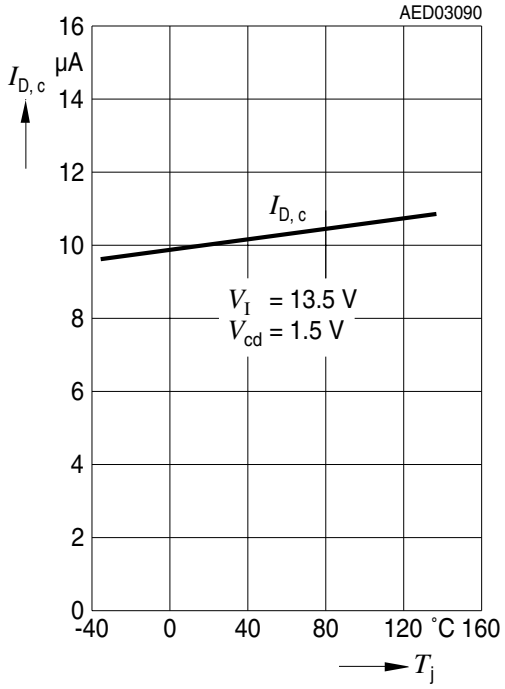
The power-on reset delay time is defined by the charging time of an external capacitor $C_D$ which can be calculated as follows:

$$C_D = (\Delta t_{rd} \times I_{D,c})/\Delta V \quad (1)$$

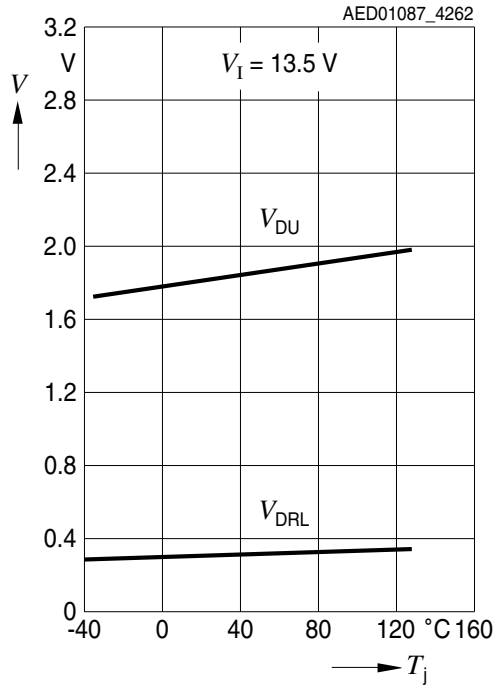
Definitions:

- $C_D$ = delay capacitor
- $\Delta t_{rd}$ = delay time
- $I_{D,c}$ = charge current, typical 10 µA
- $\Delta V = V_{DU}$, typical 1.8 V
- $V_{DU}$ = upper delay switching threshold at $C_D$ for reset delay time

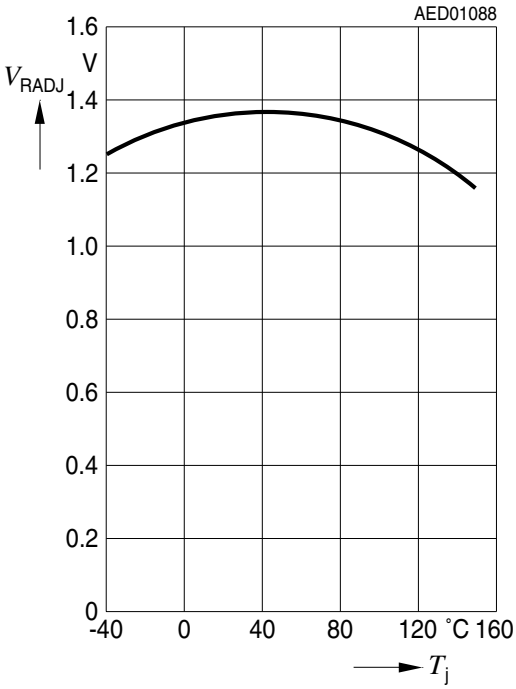
### Charge Current versus Temperature



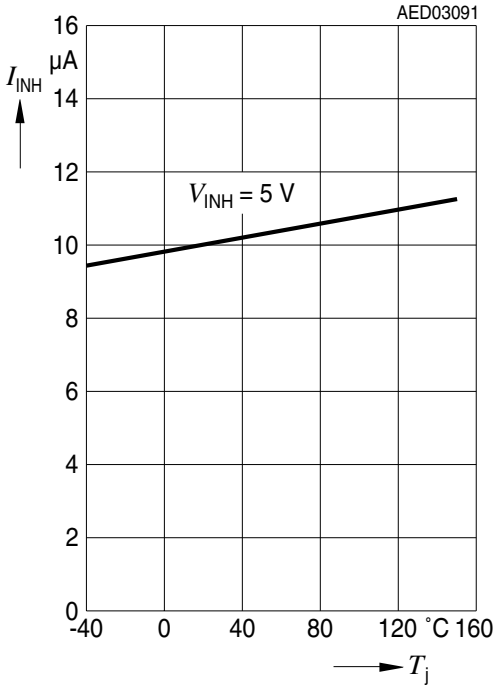

### Upper and Lower Timing Threshold $V_{DU}$ and $V_{DRL}$ versus Temperature



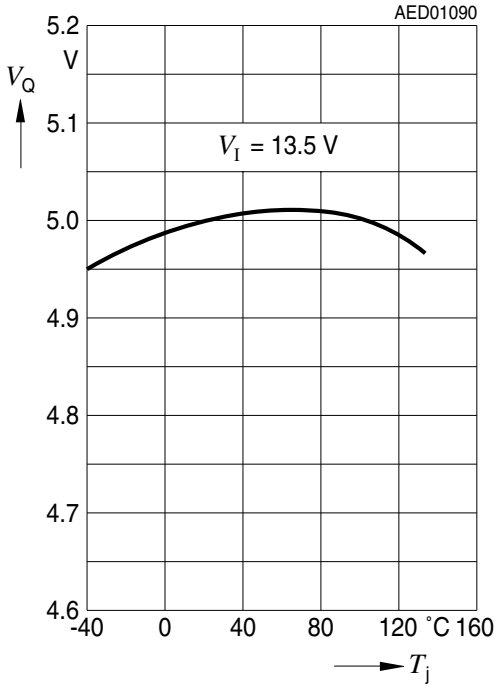

### Reset Switching Threshold versus Temperature



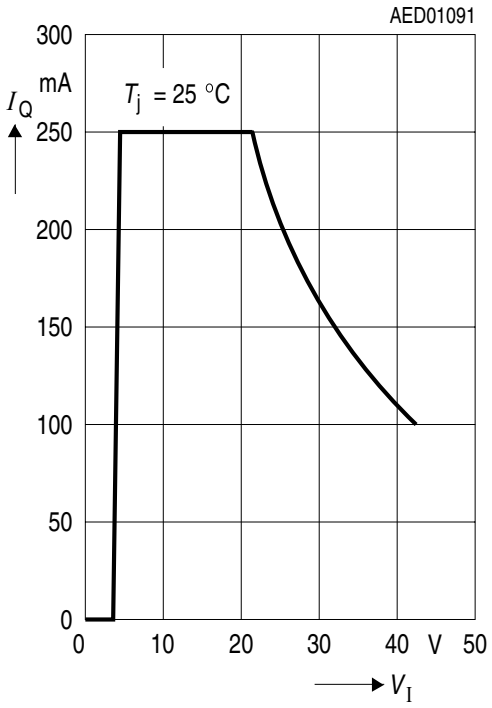

### Current Consumption of Inhibit versus Temperature Output Current



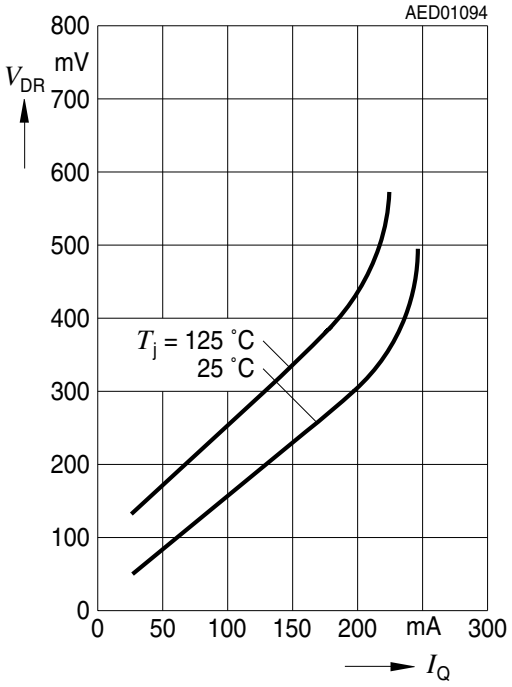
### Output Voltage versus Temperature



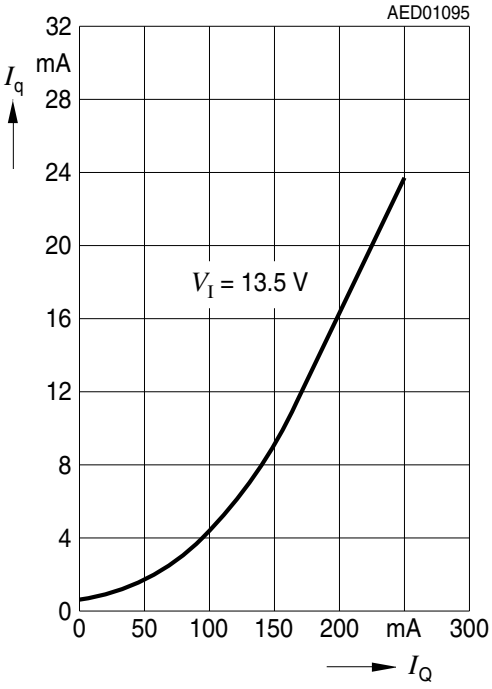

### Output Current versus Input Voltage



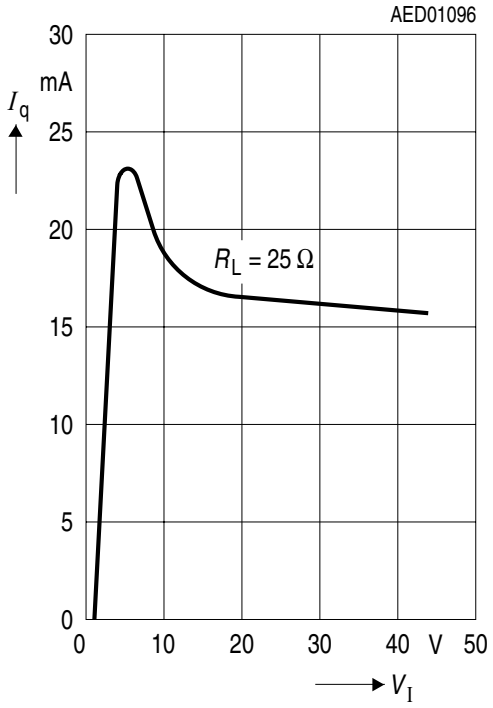

### Drop Voltage versus Output Current



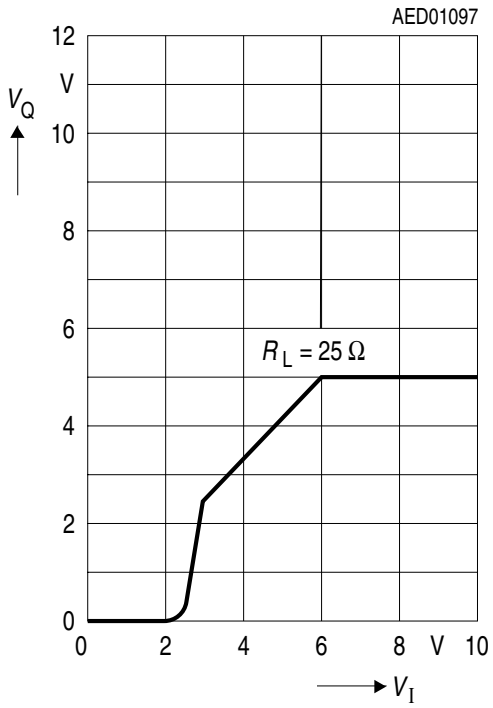

### Current Consumption versus Output Current



## Current Consumption versus Input Voltage




## Output Voltage versus Input Voltage



## Package Outlines

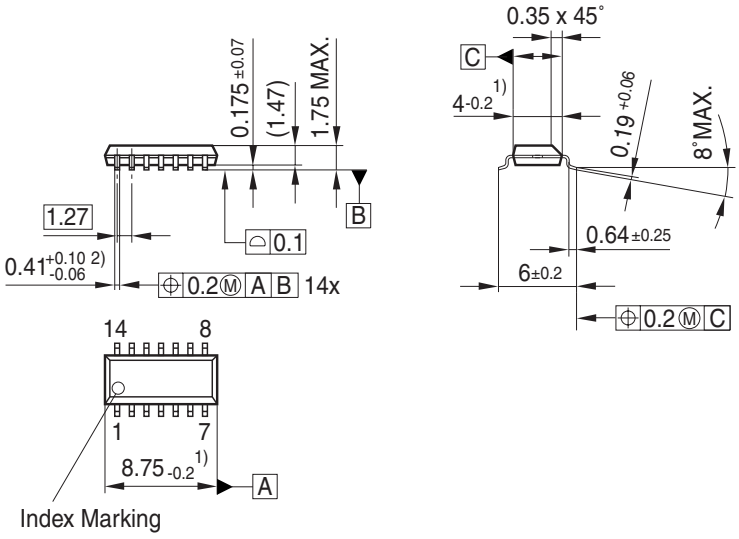



**Figure 6** **PG-DSO-14-30** (Plastic Dual Small Outline)

**Green Product** (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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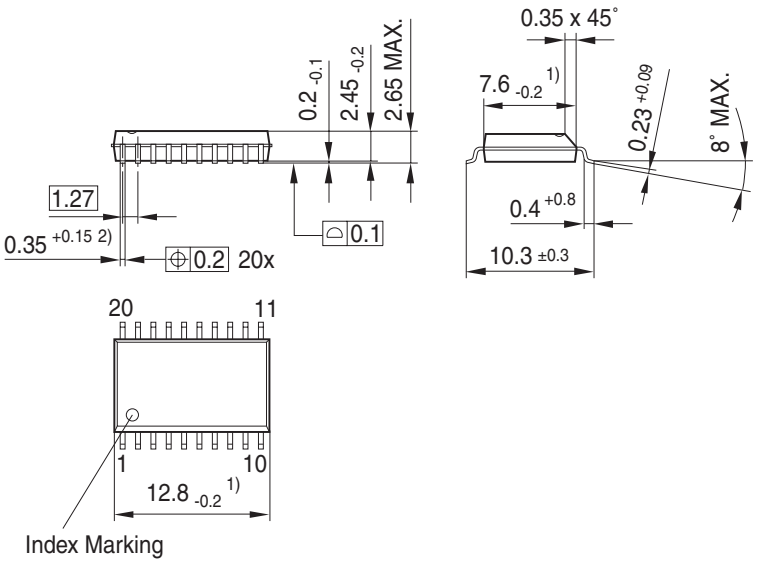
SMD = Surface Mounted Device

Dimensions in mm




1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05094

**Figure 7** **PG-DSO-20-35** (Plastic Dual Small Outline)

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SMD = Surface Mounted Device

Dimensions in mm

## Revision History

| Version | Date | Changes |
|---|---|---|
| Rev. 2.8 | 2008-05-19 | Modification according to PCN No. 2008-096:<br>Typo corrected: Current consumption $I_q$ specification @ $I_Q$ = 150mA on page 6. |
| Rev. 2.7 | 2007-03-20 | Initial version of RoHS-compliant derivate of TLE 4262<br>**Page 1**: AEC certified statement added<br>**Page 1** and **Page 13** ff: RoHS compliance statement and Green product feature added<br>**Page 1** and **Page 13** ff: Package changed to RoHS compliant version<br>Legal Disclaimer updated |

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