TLE8263-2E

Universal System Basis Chip
HERMES
Rev. 1.0

Automotive Power

Never stop thinking

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HERMES
Rev. 1.0

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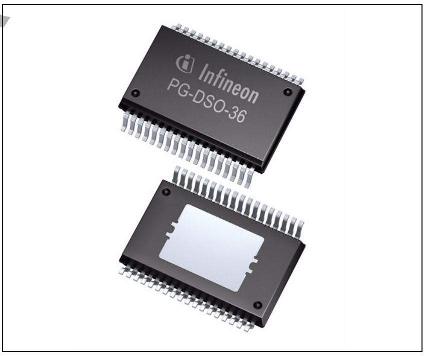
1 HERMES Overview



PG-DSO-36-38

Scalable System Basis Chip Family

- Six products for complete scalable application coverage
- Complete compatibility (hardware and software) across the family
- TLE8264-2E (3LIN), TLE8263-2E (2LIN) - 3 Limp Home outputs
- TLE8264E (3LIN), TLE8263E (2LIN) - 1 Limp Home output
- TLE8262E (1LIN), TLE8261E (no LIN) - 1 Limp Home output

Basic Features

- Very low quiescent current in Stop and Sleep Modes
- Reset input, output
- Power on and scalable undervoltage reset generator
- Standard 16-bit SPI interface
- Overtemperature and short circuit protection
- Short circuit proof to GND and battery
- One universal wake-up input
- Wide input voltage and temperature range
- Cyclic wake in Stop Mode
- Green Product (RoHS compliant)
- AEC Qualified

Description

The devices of the SBC family are monolithic integrated circuits in an enhanced power package with identical software functionality and hardware features except for the number of LIN cells. The devices are designed for CAN-LIN automotive applications e.g. body controller, gateway applications.

To support these applications, the System Basis Chip (SBC) provides the main functions, such as HS-CAN transceiver and LIN transceivers for data transmission, low dropout voltage regulators (LDO) for an external 5 V supply, and a 16-bit Serial Peripheral Interface (SPI) to control and monitor the device. Also implemented are a Time-out or a Window Watchdog circuit with a reset feature, Limp Home circuitry output, and an undervoltage reset feature.

The devices offer low power modes in order to support application that are connected permanent to the battery. A wake-up from the low power mode is possible via a message on the buses or via the bi-level sensitive monitoring/wake-up input as well as from the SPI command. Each wake-up source can be inhibited.

The device is designed to withstand the severe conditions of automotive applications.

Type	Package	Marking
TLE8263-2E	PG-DSO-36-38	TLE8263-2E

HS CAN Transceiver

- Compliant to ISO 11898-2 and 11898-5 as well as SAE J2284
- CAN data transmission rate up to 1 MBaud
- Supplied by dedicated input V_{ccHSCAN}
- Low power mode management
- Bus wake-up capability via CAN message
- Excellent EMC performance (very high immunity and very low emission)
- Bus pins are short circuit proof to ground and battery voltage
- 8 kV ESD gun test on CANH / CANL / SPLIT
- Bus failure detection

LIN Transceiver

- LIN2.1 conformance, LIN2.1 is back compatible to LIN1.3 and LIN2.0
- SAE J2602-2 conformance
- Compatible to ISO 9141 (K-L-Line)
- Transmission rate up to 20 kBaud, LIN Flash Mode 115kBaud
- 8 kV ESD gun test on Bus pins

Voltage Regulators

- Low-dropout voltage regulator
- $V_{\text{cc1µC}}$, 200 mA, 5 V ±2% for external devices, such as microcontroller and RF receiver
- V_{cc2}, 200 mA, 5 V ±2% for external devices or the internal HS CAN cell
- V_{cc3}, current limitation by shunt resistor (up to 400 mA with 220 mΩ shunt resistor), 5 V ±4% with external PNP transistor; for example: to supply additional external CAN transceivers
- $V_{\text{cc1µC}}$, undervoltage Time-out

Supervision

- Reset output with integrated pull-up resistor
- Time-out or Window Watchdog, SPI configured
- Watchdog Timer from 16 ms to 1024 ms
- Check sum bit for Watchdog configuration
- Reset due to Watchdog failure can be inhibited with Test pin (SBC SW Development Mode)

Interrupt Management

- Complete enabling / disabling of interrupt sources
- Timing filter mechanism to avoid multiple / infinite Interrupt signals

Limp Home

- Open drain Limp Home outputs
- Dedicated internal logic supply
- Maximum safety architecture for Safety Operation Mode
- Configurable Fail-Safe behavior
- Dedicated side indicators signal 1.25Hz 50% duty cycle
- Dedicated PWM signal 100Hz 20% duty cycle

2 Block Diagram

The simplified block diagram illustrates only the basic elements of the SBC devices. Please refer to the information for each device in the product family for more specific hardware configurations.

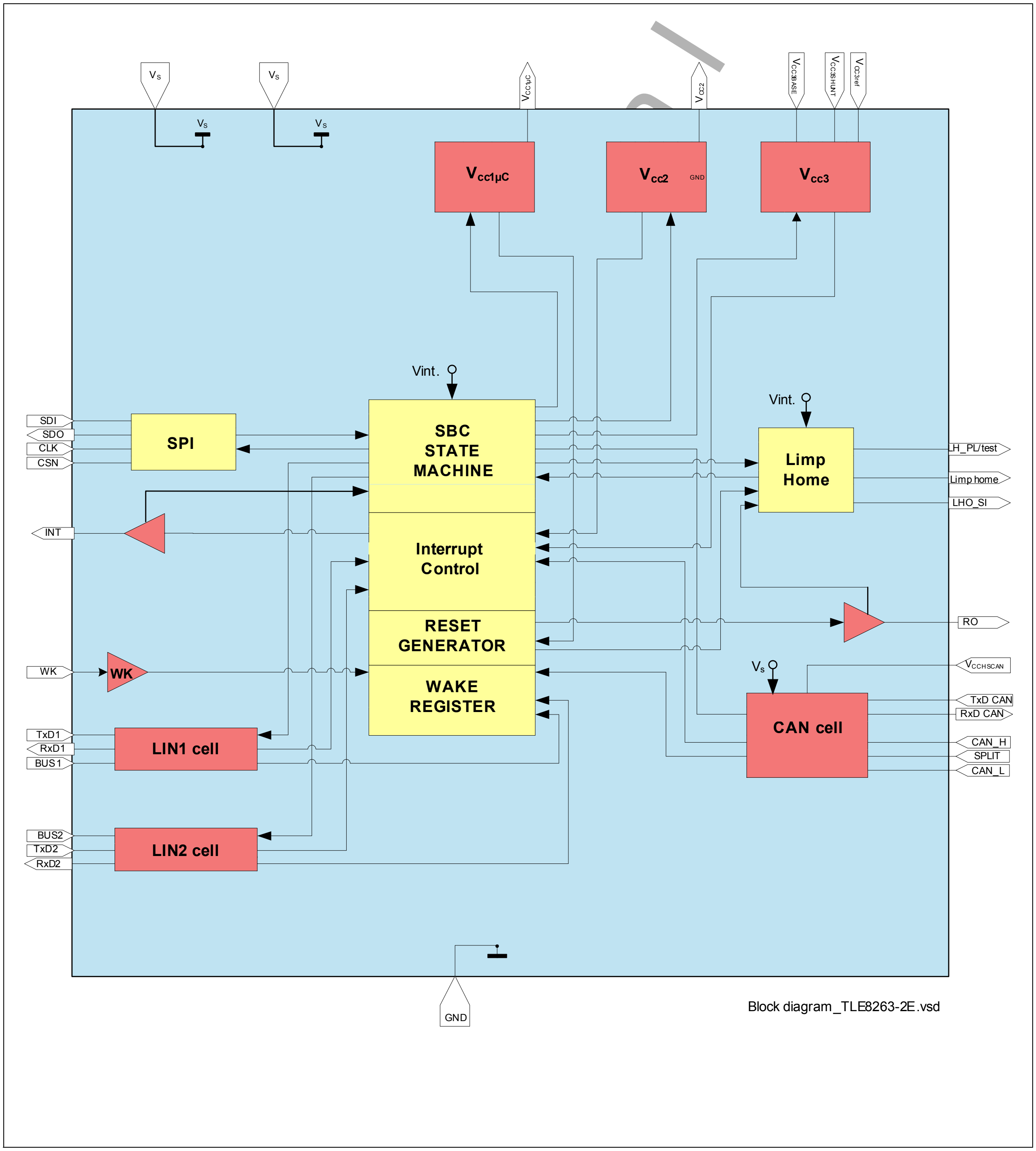


Figure 1 Simplified Block Diagram

3 Pin Configuration

3.1 Pin Assignments

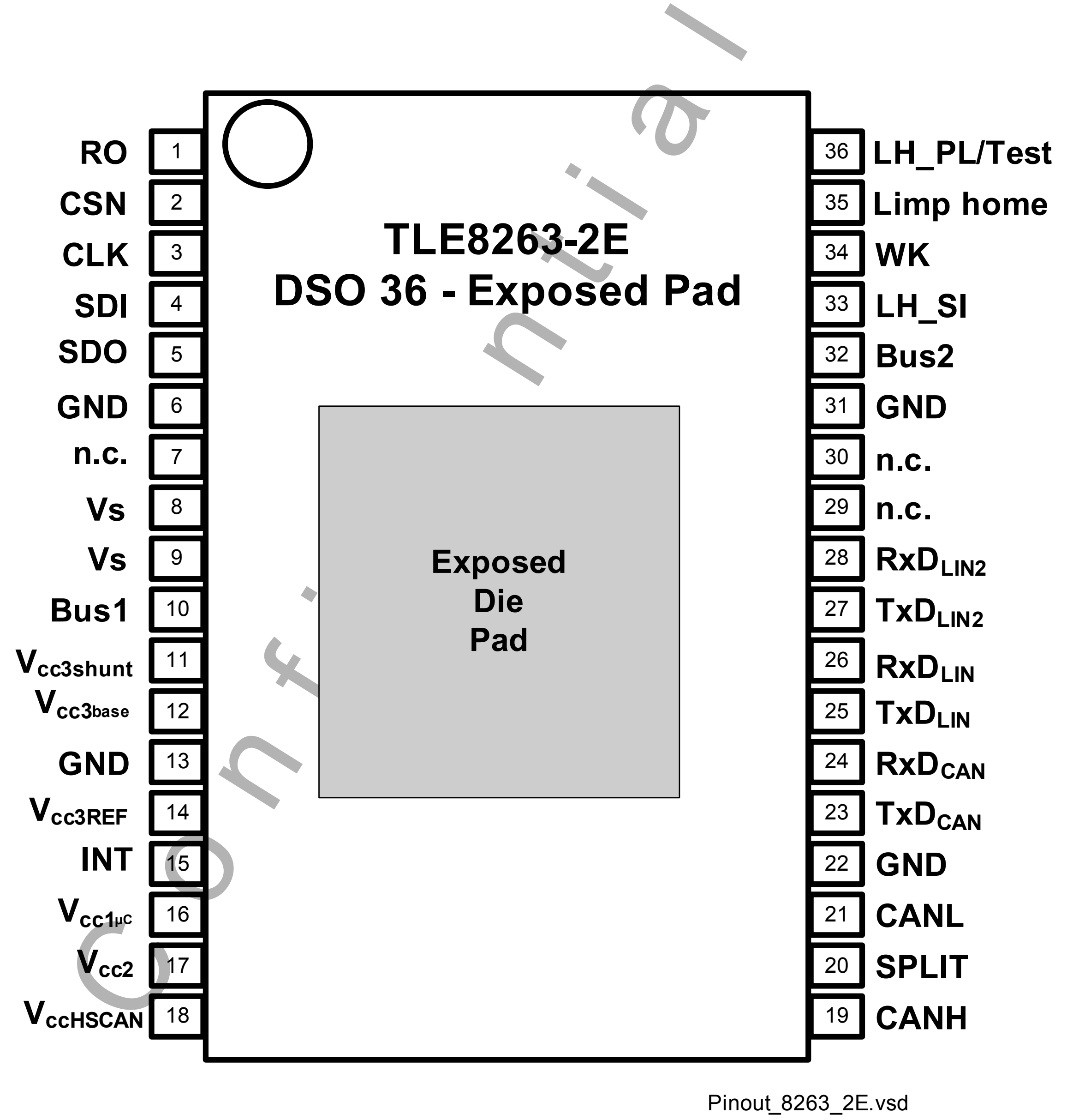


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	RO	**Reset Input/Output;** open drain output, integrated pull-up resistor; active low.
2	CSN	**SPI Chip Select Not Input;** CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should be set to low only when CLK is low; CSN has an internal pull-up resistor and requires CMOS logic level inputs.
3	CLK	**SPI Clock Input;** clock input for shift register; CLK has an internal pull-down resistor and requires CMOS logic level inputs.
4	SDI	**SPI Data Input;** receives serial data from the control device; serial data transmitted to SDI is a 16-bit control word with the Least Significant Bit (LSB) transferred first: the input has a pull-down resistor and requires CMOS logic level inputs; SDI will accept data on the falling edge of the CLK signal.
5	SDO	**SPI Data Output;** this tri-state output transfers diagnostic data to the control device; the output will remain tri-stated unless the device is selected by a low on Chip Select Not (CSN).
6	GND	**Ground**
7	n.c.	**Not connected**
8	V_s	**Power Supply Input;** block to GND directly at the IC with ceramic capacitor. Ensure to have no current flow from PIN8 to PIN9. PIN8 and PIN9 can be directly connected.
9	V_s	**Power Supply Input;** block to GND directly at the IC with ceramic capacitor. Ensure to have no current flow from PIN8 to PIN9. PIN8 and PIN9 can be directly connected.
10	Bus1	**LIN Bus 1;** Bus line for the LIN interface, according to ISO. 9141 and LIN specification 2.1 as well as SAE J2602-2.
11	$V_{\mathrm{cc3\ shunt}}$	**PNP Shunt;** External PNP emitter voltage.
12	$V_{\mathrm{cc3\ base}}$	**PNP Base;** External PNP base voltage.
13	GND	**Ground**
14	V_{cc3REF}	External PNP Output Voltage
15	INT	**Interrupt Output, configuration Input;** used as wake-up flag from SBC Stop Mode and indicating failures. Active low. Integrated pull up. During start-up used to set the SBC configuration. External Pull-up sets config 1/3, no external Pull-up sets config 2/4.
16	$V_{\mathrm{cc1\ \mu c}}$	**Voltage Regulator Output;** 5 V supply; to stabilize block to GND with an external capacitor.
17	V_{cc2}	**Voltage Regulator Output;** 5 V supply; to stabilize block to GND with an external capacitor.
18	V_{ccHSCAN}	**Supply Input;** for the internal HS CAN cell.
19	CANH	**CAN High Line;** High in dominant state.
20	SPLIT	**Termination Output;** to support recessive voltage level of the bus lines.
21	CANL	**CAN Low Line;** Low in dominant state.
22	GND	**Ground**
23	$\mathrm{TxD_{CAN}}$	**CAN Transmit Data Input;** integrated pull-up resistor.
24	$\mathrm{RxD_{CAN}}$	**CAN Receive Data Output**
25	$\mathrm{TxD_{LIN}}$	**LIN Transceiver Data input;** according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2. integrated pull-up resistor.

Pin	Symbol	Function
26	RxD_{LIN}	**LIN Transceiver Data Output;** according to the ISO 9141 and LIN specification 2.1 as well as SAE J2602-2; push-pull output; LOW in dominant state.
27	TxD_{LIN2}	**LIN Transceiver Data Input;** according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2. integrated pull-up resistor.
28	RxD_{LIN2}	**LIN Transceiver Data Output;** according to the ISO 9141 and LIN specification 2.1 as well as SAE J2602-2; push-pull output; LOW in dominant state.
29	n.c.	**Not connected**
30	n.c.	**Not connected**
31	GND	**Ground**
32	Bus2	**LIN Bus 2;** Bus line for the LIN interface, according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2.
33	LH_SI	**Limp Home side indicator;** Side indicators 1.25Hz 50% duty cycle output; Open drain. Active LOW.
34	WK	**Monitoring / Wake-Up Input;** bi-level sensitive input used to monitor signals coming from, for example, an external switch panel; also used as wake-up input;
35	Limp Home	**Fail-Safe Function Output**; Open drain. Active LOW.
36	LH_PL/Test	**SBC SW Development Mode entry;** Connect to GND for activation; Integrated pull-up resistor. Connect to V_S or leave open for normal operation. **Limp Home Pulsed Light output**: Brake/rear light 100Hz 20% duty cycle output; Open drain. Active LOW.
EDP	-	**Exposed Die Pad;** For cooling purposes only, do not use it as an electrical ground.1)

1) The exposed die pad at the bottom of the package allows better dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC and can be left floating or it can be connected to GND for the best EMC performance.

4 State Machine

4.1 Block Description

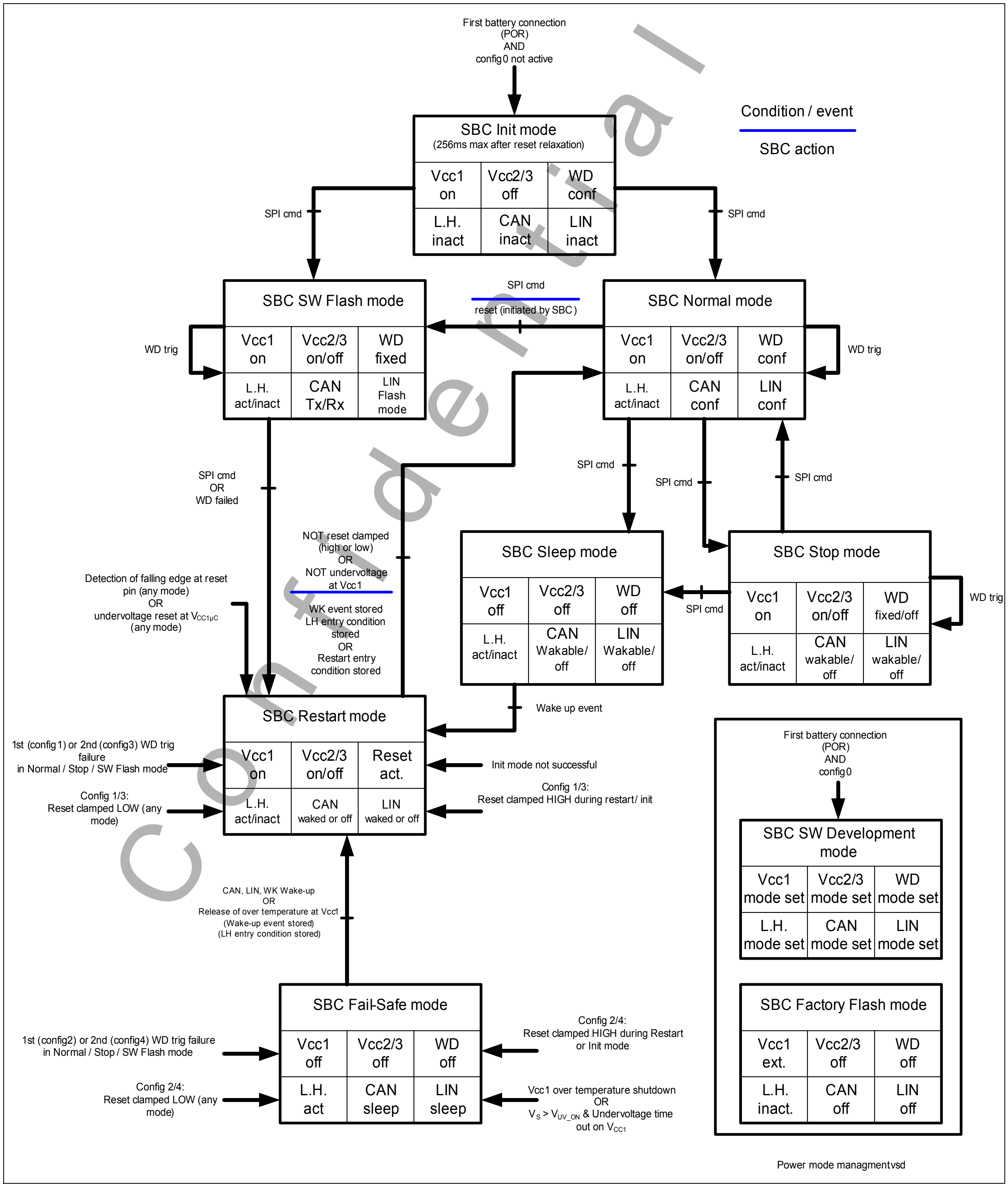


Figure 3 Power Mode Management

4.2 State Machine Description

The System Basis Chip (SBC) offers ten operating modes: Power On Reset, Init, Normal, Restart, Software Flash, Sleep, Stop, Fail-Safe, Software Development, and Factory Flash Mode. The modes are controlled with one test pin and via three mode select bits MS2..0, within the SPI. Additionally, the SBC allows five configurations, accessed via two external pins and one SPI bit.

4.2.1 Configuration Description

Table 1 provides descriptions and conditions for entry to the different configurations of the SBC.

Table 1 SBC Configuration

Configuration	Description	Test pin	INT Pin	WD to LH bit
config 0	Software Development Mode	0V	n.a	n.a
config 1	After missing the WD trigger for the first time, the state of $V_{cc1\mu C}$ remain unchanged, LH pin is active, SBC in Restart Mode	Open / V_S	External pull-up	0
config 2	After missing the WD trigger for the first time, $V_{cc1\mu C}$ turns OFF, LH pin is active, SBC in Fail-Safe Mode		No ext. pull-up	0
config 3	After missing the WD trigger for the second time, the state of $V_{cc1\mu C}$ remain unchanged, LH pin is active, SBC in Restart Mode		External pull-up	1
config 4	After missing the WD trigger for the second time, $V_{cc1\mu C}$ turns OFF, LH pin is active, SBC in Fail-Safe Mode		No ext. pull-up	1

In SBC SW Development Mode, Config 1 to 4 are accessible.

4.2.2 SBC Power ON Reset (POR)

At $V_S > V_{UVON}$, the SBC starts to operate, by reading the test pin and then by turning ON $V_{cc1\mu C}$. When $V_{cc1\mu C}$ reaches the reset threshold V_{RT1}, the reset output remains activated for t_{RD1} and the SBC enters then the Init Mode.

In the event that V_s decreases below V_{UVOFF}, the device is completely disabled. For more details on the disable behavior of the SBC blocks, please refer to the chapter specific to each block.

4.2.3 SBC Init Mode

At entering the SBC Init Mode, the SBC starts to read the Test pin. The SBC starts-up in SBC Init Mode, and, after powering-up, waits for the microcontroller to finish its startup and initialization sequences. $V_{cc2/3}$ are OFF and the Watchdog is configurable but not active. CAN and LIN modules are inactive and Limp Home output is inactive. From this transition mode, the SBC can be switched via SPI command to the desired operating mode, SBC Normal or Software Flash Mode. If the SBC does not receive any SPI command, or receive wrong SPI command (i.e. not send the device to SBC Normal or SBC SW Flash Mode) within a 256 ms time frame after the reset relaxation, it will enter into SBC Restart Mode and activate the Limp Home output.

Note: In Init Mode it is recommended to send one SPI command that sets the device to Normal Mode, triggers the watchdog the first time and sets the required watchdog settings.

4.2.4 SBC Normal Mode

SBC Normal Mode is used to transmit and receive CAN and LIN messages. In this mode, $V_{cc1\mu C}$ is always "ON" V_{cc2} and V_{cc3} can be turned-on or off by SPI command. In Normal Mode the watchdog needs to be triggered. It can be configured via SPI, window watchdog and time-out watchdog is possible (default value is time-out 256 ms). All the wake-up sources can be inhibited in this mode. The Limp Home output can be enabled or disabled via SPI command. Via SPI command, the SBC can enter Sleep, Stop or Software Flash Mode. A reset is triggered by the SBC when entering the Software Flash Mode. It is recommended to send at first SPI command the watchdog setting. Please refer to **Chapter 13.4**.

4.2.5 SBC Sleep Mode

During SBC Sleep Mode, the lowest power consumption is achieved by having the main and external voltage regulators switched-off. As the microcontroller is not supplied, the integrated Watchdog is disabled in Sleep Mode. The last Watchdog configuration is not stored. The CAN and LIN modules are in their respective Wake-capable or OFF modes and the Limp Home output is unchanged, as before entering the Sleep Mode. If a wake-up appears in this mode, the SBC goes into Restart Mode automatically. In Sleep Mode, not all wake-up sources should be inhibited, this is required to not program the device in a mode where it can not wake up. If all wake sources are inhibited when sending the SBC to Sleep Mode, the SBC does not go to Sleep Mode, the microcontroller is informed via the INT output, and the SPI bit "Fail SPI" is set. The first SPI output data when going to SBC Normal Mode will always indicate the wake up source, as well as the SBC Sleep Mode to indicate where the device comes from and why it left the state.

Note: Do not change the transceiver settings in the same SPI command that sends the SBC to Sleep Mode.

4.2.6 SBC Stop Mode

The Stop Mode is used as low power mode where the µC is supplied. In this mode the voltage regulator $V_{cc1\mu C}$ remains active. The other voltage regulator ($V_{cc2/3}$) can be switched on or off.

The watchdog can be used or switched off. If the watchdog is used the settings made in Normal Mode are also valid in Stop Mode and can not be changed.

The CAN and LIN modules are not active. They can be selected to be off or used as wake-up source. If all wake up sources are disabled, (CAN, LIN, WK, cyclic wake) the watchdog can not be disabled, the SBC stays in Normal Mode and the watchdog continues with the old settings.

If a wake-up event occurs the INT pin is set to low. The µC can react on the interrupt and set the device into Normal Mode via SPI. There is no automatic transition to SBC Normal Mode.

There are 4 Options for SBC Stop Mode

- WD on (the watchdog needs to be served as in Normal Mode
- WD off (special sequence required see **Chapter 11.2.4**)
- Cyclic Wake up with acknowledge (interrupt is sent after set time and needs to be acknowledged by SPI read)
- Cyclic Wake-up, Watchdog off (interrupt is sent after set time)

Cyclic Wake-Up Feature

SBC Stop Mode supports the cyclic wake-up feature. By default, the function is OFF. It is possible to activate the cyclic wake-up via "Cyclic WK on/off" SPI bit. This feature is useful to monitor battery voltage, for example, during parking of the vehicle or for tracking RF data coming via the RF receiver. The Cyclic Wake-up feature sends an interrupt via the pin INT to the µC after the set time. The cyclic wake-up feature shares the same clock as the Watchdog. The time base set in the SPI for the Watchdog will be used for the cyclic wake-up. The timer has to be set before activating the function. With the cyclic wake-up feature the watchdog is not working as known from the other modes. In the case that both functions (Watchdog and cyclic wake-up) are selected, the cyclic wake-up is activated and each interrupt has to be acknowledged by reading the SPI Wake register before the next Cyclic Wake-Up comes. Otherwise, the SBC goes to SBC Restart Mode.

4.2.7 SBC Software Flash Mode

SBC Software Flash Mode is similar to SBC Normal Mode regarding voltage regulators. In this mode, the Limp Home output can be set to active LOW via SPI and the communication on CAN and LIN modules is activated to receive flash data. In the LIN module the slope control mechanism is switched off. The Watchdog configuration is fixed to the settings used before entering the SBC SW Flash Mode. When the device comes from SBC Normal Mode, a reset is generated at the transition.

From the SBC Software Flash Mode, the SBC goes into SBC Restart Mode, the config setting has no influence on the behavior. A mode change to SBC Restart Mode can be caused by a SPI command, a time-out or Window Watchdog failure or an undervoltage reset. When leaving the SBC Software Flash Mode a reset is generated.

4.2.8 SBC Restart Mode

They are multiple reasons to enter the SBC Restart Mode and multiple SBC behaviors described in **Table 2**.

In any case, the purpose of the SBC Restart Mode is to reset the microcontroller.

- From SBC SW Flash Mode, it is used to start the new downloaded code.
- From SBC Normal, SBC Stop Mode and SBC SW Flash Mode it is reached in case of undervoltage on $V_{\text{cc1µC}}$, or due to incorrect Watchdog triggering.
- From SBC Sleep Mode it is used to ramp up $V_{\text{cc1µC}}$ after wake
- From SBC Init Mode, it is used to avoid the system to remain undefined.
- From SBC Fail-safe Mode it is used to ramp up $V_{\text{cc1µC}}$ after wake or cool down of Vcc1µC.

From SBC Restart Mode, the SBC goes automatically to SBC Normal Mode. The delay time t_{RDx} is programmable by the “Reset delay” SPI bit. The Reset output (RO) is released at the transition. SBC Restart Mode is left automatically by the SBC without any microcontroller influence. The first SPI output data will provide information about the reason for entering Restart Mode. The reason for entering Restart Mode is stored and kept until the microcontroller reads the corresponding “LH0..2” or “RM0..1” SPI bits. In case of a wake up from Sleep Mode the wake source is seen at the interrupt bits (Configuration select 000), an interrupt is not generated.

Entering or leaving the SBC Restart Mode will not result in deactivation of the Limp Home output (if activated).

The first SPI output data when going to SBC Normal Mode will always indicate the reason for the SBC Restart event.

Table 2 SBC Restart Mode Entry Reasons and Actions

SBC Mode and Configuration		Entering reason	Actions			
Mode	**Config**		**LH output**	$V_{\mathrm{cc1\mu C}}$	**RO**	**SPI Out Bits**
Init Mode	n.a	Init Mode time-out	ON	remains ON	LOW	LH 0..2
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Normal[1]	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	config 1	WD trigger failure	ON	remains ON	LOW	LH 0..2
	config 3		OFF after 1st ON after 2nd			RM 0..1 after 1st LH 0..2 after 2nd
	config 4		OFF after 1st			RM 0..1 after 1st[2]
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Software Flash	n.a	undervoltage reset	unchanged	remains ON	LOW	RM 0..1
	n.a	SPI cmd	unchanged	remains ON	LOW	RM 0..1
	n.a	WD trigger failure	unchanged	remains ON	LOW	RM 0..1
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Sleep	n.a	Wake-up event	unchanged	ramping up	LOW	WK bits register
Stop[1]	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	config 1	WD trigger failure	ON	remains ON	LOW	LH 0..2
	config 3		OFF after 1st ON after 2nd			RM 0..1 after 1st LH 0..2 after 2nd
	config 4		OFF after 1st			RM 0..1 after 1st[2]
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Fail-Safe	n.a.	Wake-up event	ON	ramping up	LOW	LH 0..2
Software Development Mode	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2

[1] Config 2 will never enter Restart Mode in case of WD failure but directly Fail-Safe Mode

[2] Goes to Fail-Safe Mode after the second consecutive failure

4.2.9 SBC Fail-Safe Mode

In SBC Fail-Safe Mode, all voltage regulators are OFF and the transceivers are in Wake-Capable Mode. The Limp Home output is active.

Conditions to enter the SBC Fail-Safe Mode are:

- Watchdog trigger failure in configuration 2 or 4
- $V_{\mathrm{cc1\mu C}}$ undervoltage time-out in any configuration if V_{S} is above V_{LHUV} range.
- Temperature shutdown of $V_{\mathrm{cc1\mu C}}$ in any configuration.
- Reset clamped in Config. 2/4

In case of $V_{\mathrm{cc1\mu C}}$ overtemperature shutdown, the SBC will latch and wait to cool down below the thermal hysteresis, and will go back to SBC Restart Mode.

In case of a wake-up event, the SBC will go to SBC Restart Mode (not in case of $V_{\mathrm{cc1\mu C}}$ overtemperature shutdown), storing the wake-up event and resetting the Watchdog trigger failure counter. The first SPI output data when going to SBC Normal Mode will always indicate the reason for the SBC Fail-Safe Mode.

4.2.10 SBC Software Development Mode

If the Test pin is connected to GND (Config 0 active) during powering-up, the SBC enters SBC Software Development Mode. SBC Software Development Mode is a super set of the other modes so it is possible to use all the modes of the SBC with the following difference. In SBC Software Development Mode, no reset is generated and $V_{\mathrm{CC1\mu C}}$ is not switched off due to Watchdog trigger failure. If a Watchdog trigger failure occurs, it will be indicated by the INT output (reset bit). The SBC Fail-Safe Mode or SBC Restart Mode are not reached in case of wrong Watchdog trigger but the other reasons to enter these modes are still valid.

4.2.11 SBC Factory Flash Mode

In this mode, the SBC is completely powered OFF and the microcontroller is supplied externally. The mode is detected when $V_{\mathrm{CC1\mu C}}$ is powered from external and the voltage on V_{s} is not powered from external. The current flow out of V_{s} must be limited to the maximum rating. The external supply voltage should be below the absolute maximum rating stated in **Chapter 5.1**. The reset can be driven by an external circuit, or pulled high with a pull-up resistor.

Note: Please respect the absolute maximum ratings when the device is in SBC Factory Flash Mode.

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Absolute Maximum Ratings 1)

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			Min.	Max.		
Voltages						
5.1.1	Supply Voltage	V_S	-0.3	40	V	–
5.1.2	Supply Voltage Slew Rate	$dV_{S/dt}$	-0.5	5	V/µs	–
5.1.3	Regulator Output Voltage	$V_{cc1\mu C/2/3}$	-0.3	5.5	V	–
5.1.4	CAN Bus Voltage (CANH, CANL)	$V_{CANH/L}$	-27	40	V	–
5.1.5	Differential Voltage CANH, CANL, SPLIT	$V_{diffESD}$	-40	40	V	CANH-CANL<|40 V|; CANH-SPLIT<|40 V| CANL-SPLIT<|40 V|;
5.1.6	Input Voltage at $V_{CCHSCAN}$	$V_{CCHSCAN}$	-0.3	5.5	V	–
5.1.7	Voltage at SPLIT, WK	V_{SPLIT}	-27	40	V	–
5.1.8	Voltage at LH_PL/Test	$V_{Test,max}$	-0.3	40	V	–
5.1.9	Voltage at $V_{cc3base}$, $V_{cc3shunt}$, V_{cc3REF}	$V_{cc3base}$	-0.3	40	V	–
5.1.10	Voltage at Limp Home (LH, LH_SI pin)	V_{LH}	-0.3	40	V	–
5.1.11	Logic Voltages Input Pin (SDI, CLK, CSN, TxDLINx, TxDCAN)	V_I	-0.3	$V_{CC1\mu C}$ + 0.3V	V	0 V < V_S < 28 V 0 V < $V_{CC1\mu C}$ < 5.5 V
5.1.12	Logic Voltage Output PIN (SDO, RO, INT, RxDLINx, RxDCAN)	$V_{DRI,RD}$	-0.3	$V_{CC1\mu C}$ + 0.3V	V	0 V < V_S < 28 V 0 V < $V_{CC1\mu C}$ < 5.5 V
5.1.13	LIN Line Bus Input Voltages	V_{bus}	-27	40	V	–
Currents						
5.1.14	Reverse current on pin Vs	I_{VS}	-500	–	mA	V_S < V_{CC}
Temperatures						
5.1.15	Junction Temperature	T_j	-40	150	°C	–
5.1.16	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
5.1.17	Electrostatic Discharge Voltage at BusX, CANH, CANL, SPLIT versus GND	V_{ESD}	-6	6	kV	2) HBM (100 pF via 1.5 kΩ)
5.1.18	Electrostatic Discharge Voltage	V_{ESD}	-2	2	kV	2) HBM (100 pF via 1.5 kΩ)
5.1.19	Electrostatic Discharge CDM Corner Pins (Pin 1, 18, 19, 36)	$V_{ESD\_CDM\_C}$	-750	750	V	3)
	Electrostatic Discharge CDM	V_{ESD_CDM}	-500	500	V	3)

1) Not subject to production test; specified by design

2) ESD susceptibility Human Body Model “HBM” according to JESD22-A114

3) ESD susceptibility Charged Device Model “CDM” according to ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

5.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			Min.	**Max.**		
5.2.1	Supply Voltage	V_S	$V_{UV\ OFF}$	28	V	After V_S rising above $V_{UV\ ON}$;[1]
5.2.2	Supply Voltage	V_S	$V_{UV\ OFF}$	40	V	[2]t_{pulse} = 400 ms 40 V load dump; Ri = 2Ω
5.2.3	SPI Clock Frequency	f_{clkSPI}	–	4	MHz	[3]$V_S > 5.5$ V
5.2.4	SPI Clock Frequency	f_{clkSPI}	–	1	MHz	If $V_{UV\ ON} > V_S > V_{UV\ OFF}$;
5.2.5	Junction Temperature	T_j	-40	150	°C	–
5.2.6	Undervoltage "OFF"	$V_{UV\ OFF}$	3	4	V	-[1]
5.2.7	Undervoltage "ON	$V_{UV\ ON}$	4.5	5.5	V	-[1]
5.2.8	Supply Voltage for Limp Home Output Active	V_{S_LH}	5.5	40	V	Pull up to V_S R_{LHO} = 40kΩ

1) In the case $V_s < V_{UVOFF}$, the SBC is switched OFF and will restart in INIT Mode at next V_s rising.

2) During load dump, the others pins remains in their absolute maximum ratings

3) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.3 Thermal Characteristics

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
5.3.1	Junction Ambient	R_{thJA_1L}	–	40		K/W	[1] [3] 300 mm^2 cooling area
	Junction Ambient	R_{thJA_4L}	–	25		K/W	[2] [3]2s2p + 600 mm^2 cooling area
5.3.2	Junction to Soldering Point	R_{thJSP}	–	5	–	K/W	[3]
Thermal Prewarning and Shutdown Junction Temperatures;							
5.3.3	$V_{CC1\mu C}$, Thermal Pre-warning ON Temperature	T_{jPW}	120	145	170	°C	-[3]
5.3.4	$V_{CC1\mu C}$, Thermal Prewarning Hysteresis	ΔT_{PW}	–	25	–	K	[3]
5.3.5	$V_{CC1\mu C}$, V_{CC2} Thermal Shutdown Temperature	T_{jSDVcc}	150	185	200	°C	[3]
5.3.6	$V_{CC1\mu C}$, V_{CC2} Thermal Shutdown Hysteresis	ΔT_{SDVcc}	–	35	–	K	[3]
5.3.7	$V_{CC1\mu C}$, Ratio of SD to PW Temperature	$T_{jSDVcc/}$ T_{jPW}	–	1.20	–	–	[3]
5.3.8	CAN Transmitter Thermal Shutdown Temperature	T_{jSDCAN}	150	–	200	°C	[3]
5.3.9	CAN Transmitter Thermal Shutdown Hysteresis	ΔT_{CAN}	–	10	–	K	[3]
5.3.10	LIN Transmitter Thermal Shutdown Temperature	T_{jSDLIN}	150	–	200	°C	[3]
5.3.11	LIN Transmitter Thermal Shutdown Hysteresis	ΔT_{LIN}	–	10	–	K	[3]

1) Specified Rthja value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 single layer. The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board.

2) According to Jedec JESD51-2,-5,-7 at natural convection on 2s2p board for 2W. Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (35µm thick)., with thermal via array under the exposed pad contacted the first inner copper layer and 600mm2 cooling are on the top layer (70µm)

3) Not subject to production test; specified by design;

5.4 Current Consumption

V_S = 5.5 V to 28 V; all outputs open; Without V_{CC3}; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
Normal Mode;							
5.4.1	Current Consumption for Internal Logic	I_{VS_logic}	–	–	2	mA	SBC Normal Mode $I_{CC1\mu C} = I_{CC2}$ = 0mA; CAN OFF mode; LIN OFF mode
5.4.2	Additional current Consumption for CAN Cell	I_{VS_CAN}	–	–	10	mA	CAN Normal Mode; Recessive state; V_{CC2} connected to $V_{CCHSCAN}$ $V_{TxD} = V_{cc1\mu C}$; without R_L
			–	–	12	mA	CAN Normal Mode; dominant state; V_{CC2} connected to $V_{CCHSCAN}$ V_{TxD} = low; without R_L;
5.4.3	Additional Current Consumption per LIN Cell	I_{VS_LIN}	–	–	3.0	mA	LIN Normal Mode; recessive state; without R_L; $V_{TxD} = V_{cc1\mu C}$
			–	–	5.0	mA	LIN Normal Mode; dominant state; without R_L; V_{TxD} = low
Stop Mode							
5.4.4	Current Consumption	I_{VS}	–	58	75	µA	SBC Stop Mode; V_s = 13.5 V; $V_{CC1\mu C}$"ON"; $V_{CC2/3}$"OFF" CAN/LIN wake capable; T_j = 25°C
				65	85		T_j = 85°C[1]
			–	70	90	µA	SBC Stop Mode; V_s = 13.5 V; $V_{CC1\mu C/2}$"ON"; V_{CC3}"OFF" CAN/LIN wake capable; T_j = 25°C
			–	78	100		T_j = 85°C[1]

5.4 Current Consumption (cont'd)

V_S = 5.5 V to 28 V; all outputs open; Without V_{CC3}; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
Sleep Mode							
5.4.5	Current consumption, all Wake Up Sources available.	$I_{VS\_sleep\_SBC}$	–	28	40	µA	SBC Sleep Mode; T_j = 25°C V_s = 13.5 V; $V_{CC1µC/2/3}$"OFF" CAN/LIN wake capable;
				32	50		T_j = 85°C[1]
5.4.6	Quiescent Current Reduction when one Wake Capable LIN Cell Disabled	$I_{VS\_sleep\_LIN}$	0.5	1	–	µA	[1]SBC Sleep Mode; T_j = 25°C; V_S = 13.5 V; $V_{CC1µC/2/3}$"OFF" CAN/LIN 1_2 wake capable; LIN3 OFF
5.4.7	Quiescent Current Reduction when Wake Capable CAN Cell Disabled	$I_{VS\_sleep\_CAN}$	5	12	–	µA	[1]SBC Sleep Mode; T_j = 25°C; V_S = 13.,5 V; $V_{CC1µC/2/3}$"OFF" LIN 1..3 wake capable; CAN OFF

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1) Not subject to production test; specified by design

6 Internal Voltage Regulator

6.1 Block Description

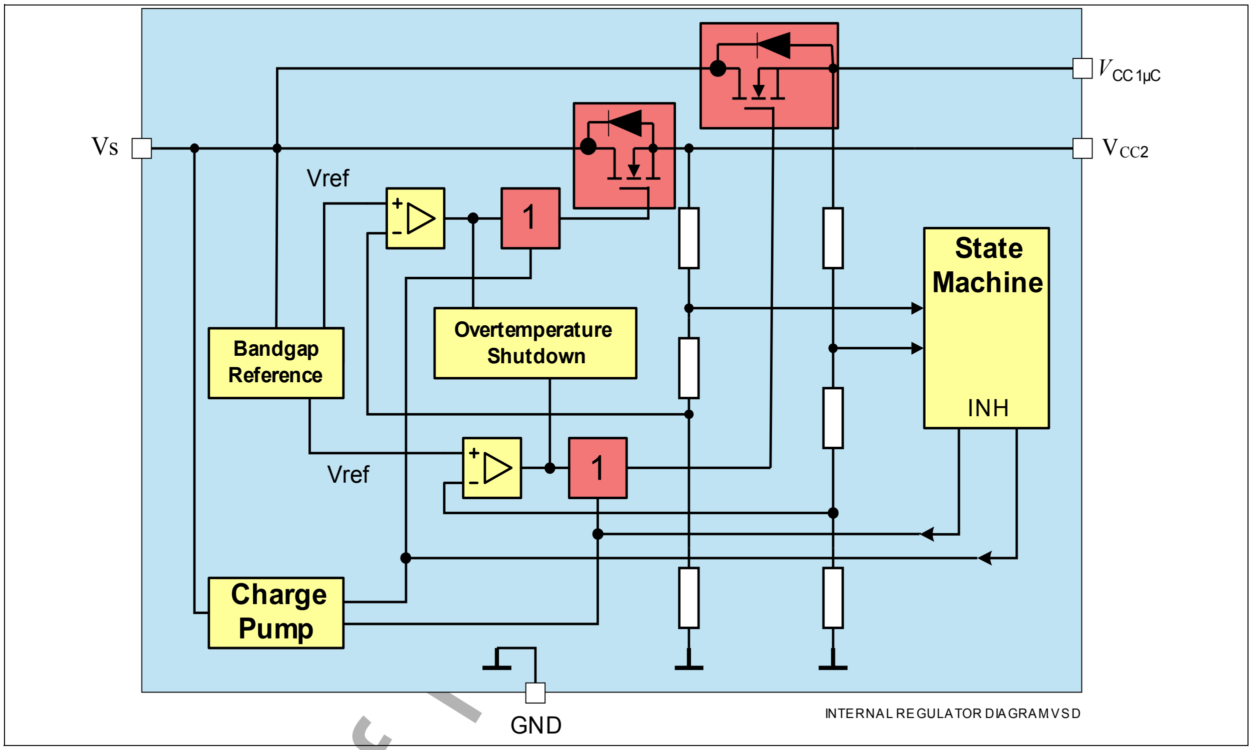

Figure 4 Functional Block Diagram

The internal voltage regulators are dual low-drop voltage regulators that can supply loads up to $I_{CC1µC/2\_max}$. An input voltage up to V_{SMAX} is regulated to $V_{cc1µC/2\_nom}$ = 5.0 V with a precision of ±2%. Due to its integrated reset circuitry, featuring two SPI configurable power-on timing (t_{RDx}) and three SPI configurable output voltages (V_{RTx}) monitoring, the device is well suited for microcontroller supply. The design enables stable operation even with ceramic output capacitors down to 470nF, with ESR < 1 Ω @ f = 10 kHz. The device is designed for automotive applications, therefore it is protected against overload, short circuit, and overtemperature conditions. **Figure 4** shows the functional block diagram. If the V_S voltage is lower than V_{UV_OFF}, the DMOS of the voltage regulator is switched to high impedance. The body diodes of the DMOS might go into conduction when $V_{CC1µC}$ or $V_{CC2} > V_S$ (no reverse protection).

6.2 Internal Voltage Regulator Modes

It is possible to turn $V_{cc1µC}$ via SBC Modes and V_{cc2} activity ON or OFF via SPI command or by entering SBC modes. The limiting current for the both regulators is $I_{CC1µC\_max}/I_{CC2}$.

6.3 Internal Voltage Regulator Modes with SBC Mode

Depending on the SBC Mode in use, $V_{cc1µC}$ and V_{cc2} can be either ON or OFF by definition, V_{cc2} can be also turned ON or OFF, via SPI. **Table 3** identifies the possible states of the voltage regulators, based on the various SBC modes.

Table 3 Internal Voltage Regulators States

SBC Mode	Vcc1µC	Vcc2	
INIT Mode	ON	OFF	
Normal Mode	ON	ON	OFF
Sleep Mode	OFF	OFF	
Restart Mode	ON	unchanged	
Software Flash Mode	ON	ON	OFF
Stop Mode	ON	ON	OFF
Fail-Safe Mode	OFF	OFF	

6.4 Application information

6.4.1 Timing Diagram

Figure 5 shows the ramp up and down of the V_S, and the dependency of $V_{cc1\mu C}$. At the first ramp up from SBC Init Mode, the reset threshold V_{RT} and time t_{RO} are set to the default value. See **Chapter 11.1**

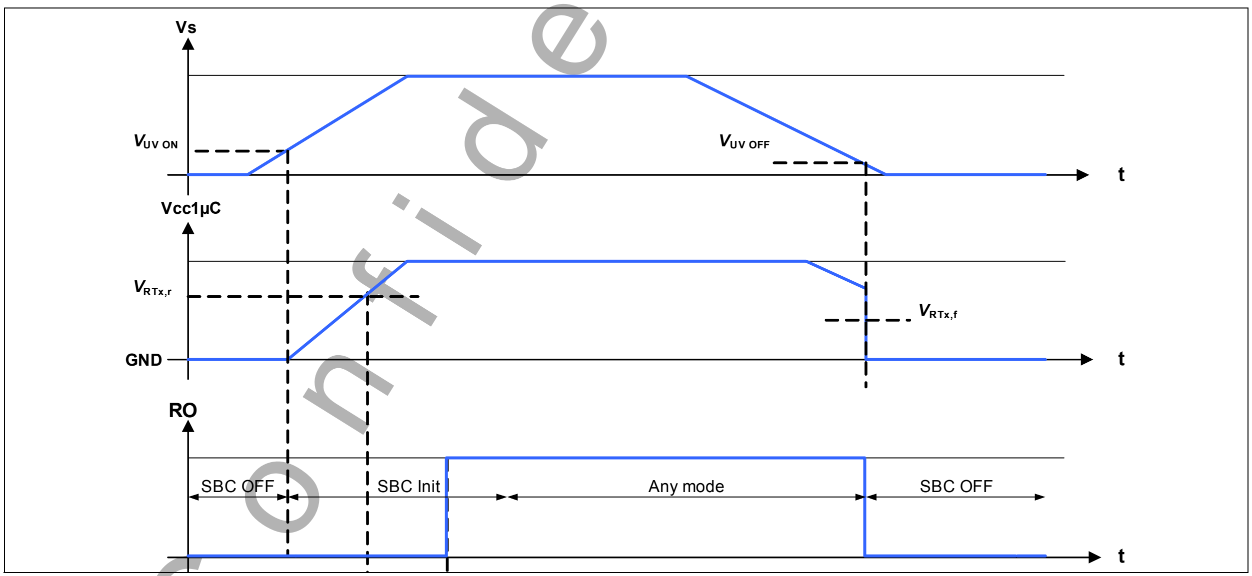

Figure 5 Ramp up / Down of Main Voltage Regulator

An undervoltage time-out on $V_{cc1\mu C}$ is implemented. Refer to **Chapter 13** for more information on this function.

6.4.2 Under voltage detection at V_{cc2}

The V_{cc2} voltage regulator integrates an under voltage detection. When V_{cc2} voltage goes below V_{UV_VCC2}, the failure is indicated by an interrupt and the failure is reported into the diagnosis frame of the SPI.

6.5 Electrical Characteristics

V_S = 5.5 V to 28 V; $C_{CC1\mu C}$ = C_{CC2} = 470 nF; all outputs open; SBC Normal Mode;
T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
Voltage Regulator; Pin $V_{cc1\ \mu C}$							
6.5.1	Output Voltage	$V_{CC1\mu C}$	4.9	5.0	5.1	V	0 mA $<I_{CC1\mu C}<$200 mA; 5.5 V < V_S < 28 V;
6.5.2	Line Regulation	$\Delta V_{CC1\mu C,Li}$	–	–	20	mV	6 V < V_S < 16 V; $I_{CC1\mu C}$ = 0 A
6.5.3	Load Regulation	$\Delta V_{CC1\mu C,Lo}$	–	–	50	mV	5 mA $<I_{CC1\mu C}<$200 mA; V_S = 6 V
6.5.4	Power Supply Ripple Rejection	PSRR	–	40	–	dB	V_r = 1 Vpp; f_r = 100 Hz;[1]
6.5.5	Output Current Limit	$I_{cc1\mu C\ max}$	200	–	500	mA	$V_{cc1\mu C}$ = 4.5 V; power transistor thermally monitored;
6.5.6	Drop Voltage	$V_{DR\ Vcc1\mu C}$	–	–	0.5	V	$I_{CC1\mu C}$ = 150 mA; [2]
Voltage Regulator; Pin V_{cc2}							
6.5.7	Output Voltage	V_{CC2}	4.9	5.0	5.1	V	0 $<I_{CC2}<$200 mA; 5.5 V < V_S < 28 V;
6.5.8	Line Regulation	$\Delta V_{CC2,Li}$	–	–	20	mV	6 V < V_S < 16 V; I_{CC2} = 0 A;
6.5.9	Load Regulation	$\Delta V_{CC2,Lo}$	–	–	50	mV	5 mA $<I_{CC2}<$200 mA; V_S = 6 V
6.5.10	Power Supply Ripple Rejection	PSRR	–	40	–	dB	V_r = 1 Vpp; f_r = 100 Hz;[1]
6.5.11	Output Current Limit	I_{cc2}	200	–	500	mA	V_{cc2} = 4.5 V; power transistor thermally monitored;
6.5.12	Drop Voltage	V_{DR_Vcc2}	–	–	0.5	V	I_{CC2} = 150 mA;[2]
6.5.13	Under voltage detection on V_{cc2}	V_{UV_VCC2}	4.5	4.65	4.8	V	V_{CC2} falls until INT = LOW

1) specified by design; not subject to production test.

2) Measured when the output voltage has dropped 100 mV from the nominal Value obtained at V_s = 13.5 V. Specified drop voltage for Vs > 4 V.

7 External Voltage Regulator

7.1 Block Description

V_{cc3} is activated via SPI. The external voltage regulator circuitry is designed to drive an external PNP transistor to increase output current flexibility. Four pins are used: V_S, $V_{cc3base}$, $V_{cc3shunt}$ and V_{cc3ref}. One transistor is tested during production. An input voltage up to V_{SMAX} is regulated to $V_{Q,nom}$ = 5.0 V with a precision of ±4%. The output current of the transistor is monitored via an external shunt resistor. The state of V_{cc3} is reported in the diagnostic SPI register. When battery voltage is below the minimum operating battery voltage $V_s < V_{VextUV}$, the external voltage regulator switches off. **Figure 7** shows the behavior during this phase. The shunt is used for overcurrent limitation. If this feature is not needed, connect pins $V_{cc3shunt}$ and V_s together.

Since the junction temperature of the external PNP transistor cannot be read, it cannot be protected against over temperature by the SBC, and so the thermal behavior has to be checked by the application.

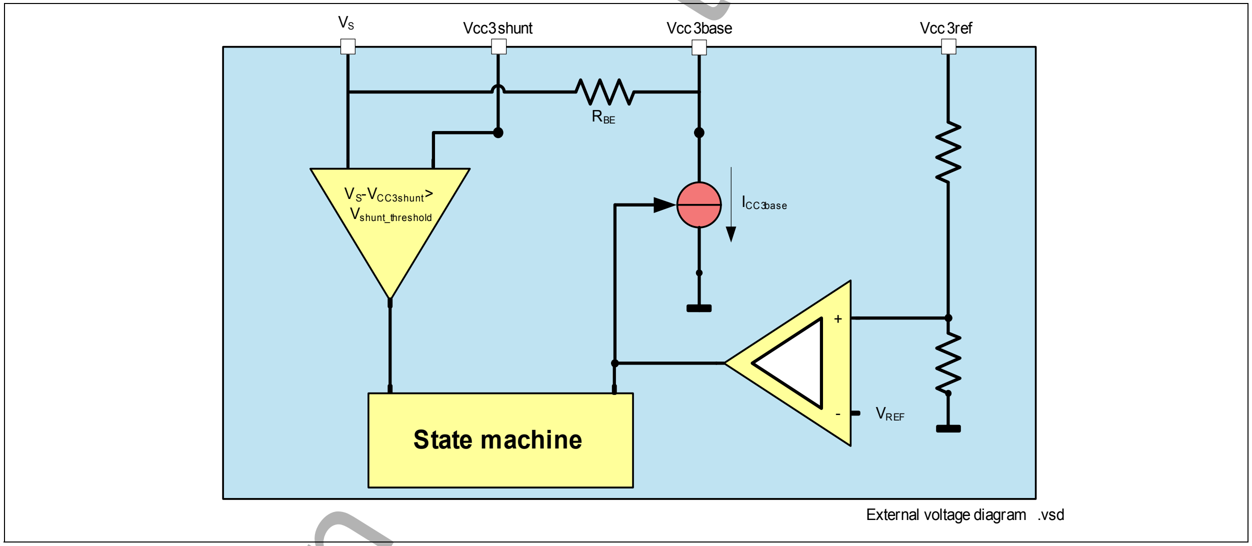

Figure 6 Functional Block Diagram

7.2 External Voltage Regulator Mode

It is possible to turn the V_{cc3} ON or OFF via SPI command, depending on the SBC modes. **Table 4** identifies the possible states, based on the different SBC modes.

7.3 External Voltage Regulator State by SBC Mode

Table 4 shows the possible states of the V_{cc3} external voltage regulator as a function of the SBC mode.

Table 4 External Voltage Regulator State by SBC Mode

SBC Mode	V_{cc3}	
INIT Mode	OFF	
Normal Mode	ON	OFF
Sleep Mode	OFF	
Restart Mode	Unchanged	
SW Flash Mode	ON	OFF
Stop Mode	ON	OFF
Fail-Safe Mode	OFF	

7.4 Application Information

7.4.1 Timing information

Figure 7 shows the typical timing, ramp up and ramp down of the External Voltage Regulator, in regards to the V_S pin.

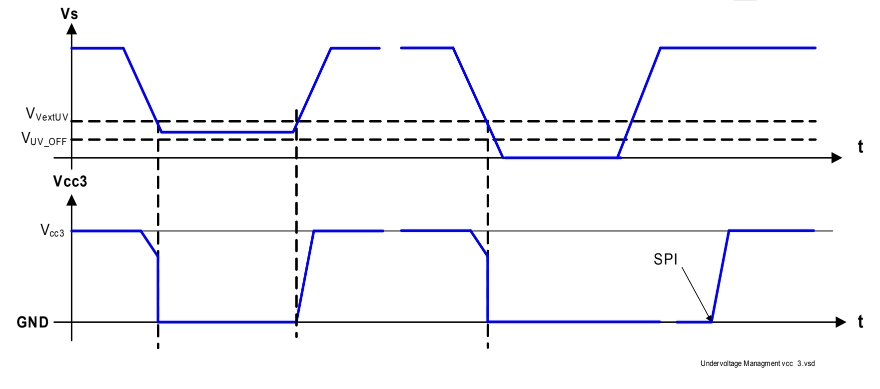

Figure 7 Supply Voltage Management

7.4.2 External Components

During production test, the listed parameter are tested with the PNP transistor MJD253 from ON semi. Characterization is done with the BCP52-16 from Infineon (I_{CC3}<200 mA). Other PNP transistors can be used. Function must be checked in the application.

Figure 8 shows the hardware set up used.

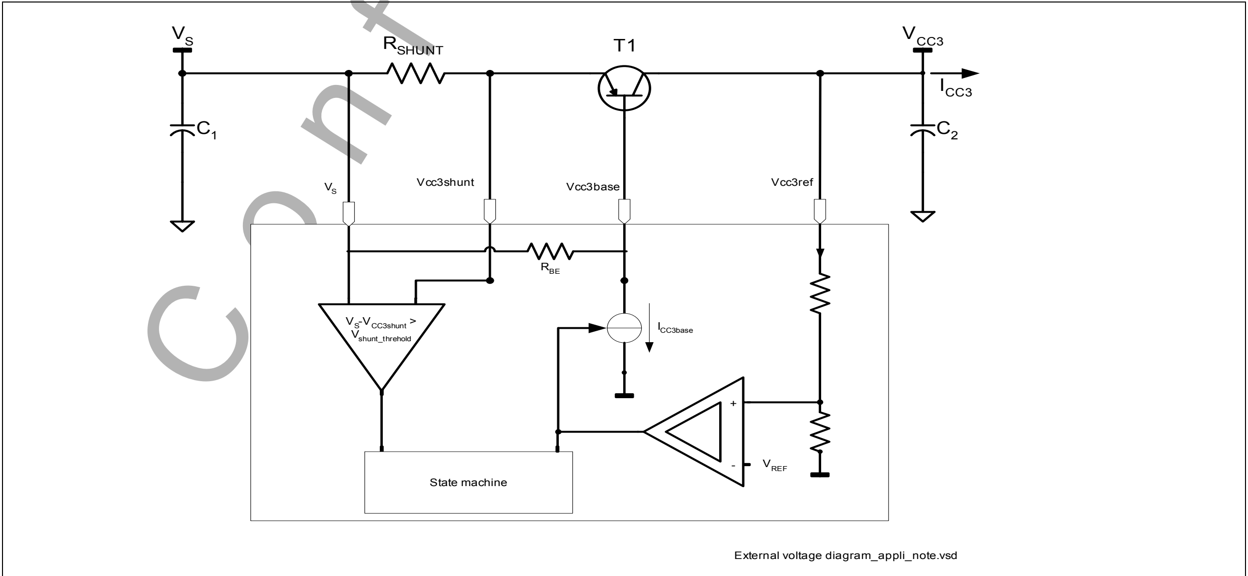

Figure 8 Hardware Set Up

Table 5 Bills of material for the V_{CC3} function

Device	Vendor	Reference / Value
C_2	Murata	10µF/10V GCM31CR71AA106K
R_{SHUNT}	-	220mΩ
T_1	ON semi	MJD253

7.4.3 Calculation of R_{SHUNT}

The maximum current I_{CC3max} where the limit starts and the bit I_{CC3}>I_{CC3max} is set is determined by the shunt resistor R_{Shunt} and the Output Current Shunt Voltage Threshold $V_{shunt\_threshold}$.

The resistor can be calculated as following

$$R_{SHUNT} = \frac{U_{shunt\_threshold}}{I_{CC3max}}$$

7.4.4 Unused Pins

In case the Vcc3 is not used in the application, it is recommended to connect the unused pins of Vcc3 as followed.

Connect Vcc1shunt to Vs. (It is also possible to leave the pin open)

Leave Vcc3base open

Leave Vcc3ref open

Do not enable the Vcc3 via SPI as this leads to increased current consumption.

7.5 Electrical Characteristics

V_S = 5.5 V to 28 V; SBC Normal Mode; all outputs open;
T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
Parameters independent from test set-up							
7.5.1	External Regulator Control Drive Current Capability	$I_{cc3base}$	20		70	mA	$V_{CC3base}$ = 28V
7.5.2	Input Current V_{cc3ref}	I_{cc3ref}	10	25	50	µA	V_{cc3ref} = 5 V
7.5.3	Input Current V_{cc3} Shunt Pin	$I_{cc3shunt}$	10	25	50	µA	$V_{cc3shunt}$ = V_S
7.5.4	V_{CC3} Undervoltage Detection	$V_{CC3,UV}$	4.0	4.25	4.5	V	–
7.5.5	V_{CC3} Undervoltage detection hysteresis	$V_{CC3,UV,hys}$	20	100	250	mV	
7.5.6	Output Current Shunt Voltage Threshold	$V_{shunt\_threshold}$	88	110	130	mV	[1]
7.5.7	Current increase regulation reaction time	t_{rlinc}	-	-	5	µs	V_{cc3} = 6V to 0V; $I_{CC3base,50\%}$ = 20mA **Figure 9**
7.5.8	Current decrease regulation reaction time	t_{rldec}	-	-	5	µs	V_{cc3} = 0V to 6V; $I_{CC3base,50\%}$ = 20mA **Figure 9**
7.5.9	Leakage current of $V_{cc3base}$ when Vcc3 disabled	$I_{cc3base\_lk}$	-	-	5	µA	$V_{CC3base}$ = V_S T_j = 25°C
7.5.10	Leakage current of V_{cc3ref} when Vcc3 disabled	I_{cc3ref_lk}	-2	0	2	µA	V_{CC3ref} = 5V T_j = 25°C
7.5.11	Leakage current of $V_{cc3shunt}$ when Vcc3 disabled	$I_{cc3shunt\_lk}$	-	-	5	µA	$V_{CC3shunt}$ = V_S T_j = 25°C
7.5.12	Base to emitter resistor	R_{BE}	50	100	200	kΩ	$V_{CC3base}$ = V_S - 0.3V V_{CC3} OFF
7.5.13	External regulator minimum Vs voltage	V_{VextUV}	4.5	-	5.5	V	
7.5.14	External regulator minimum Vs voltage hysteresis	$V_{VextUVhys}$	-	0.2	-	V	
Parameters dependent on the test set-up, according to the Figure 8							
7.5.15	External Regulator Output Voltage	V_{cc3}	4.8	5	5.2	V	0 mA <I_{CC3}<400 mA; 5.5 V < V_S < 28 V;[2]
7.5.16	Load Regulation	$\Delta V_{CC3,Lo}$	-	-	50	mV	2 mA <I_{CC3}<200 mA;
7.5.17	Line Regulation	$\Delta V_{CC3,Li}$	-	-	50	mV	6 V < V_S <16 V;

1) Threshold at which the current limitation starts to operate.

2) Tolerance includes load regulation and line regulation.

Timing diagram for regulator reaction time “current increase regulation reaction time” and “current decrease regulation reaction time”

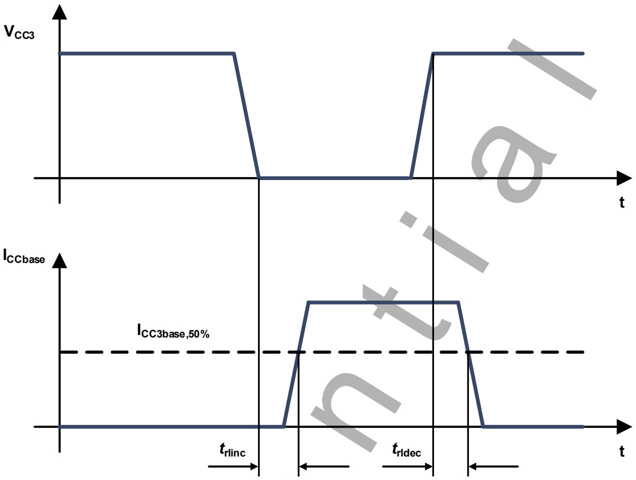

Figure 9 Regulator Reaction Time

8 High Speed CAN Transceiver

8.1 Block Description

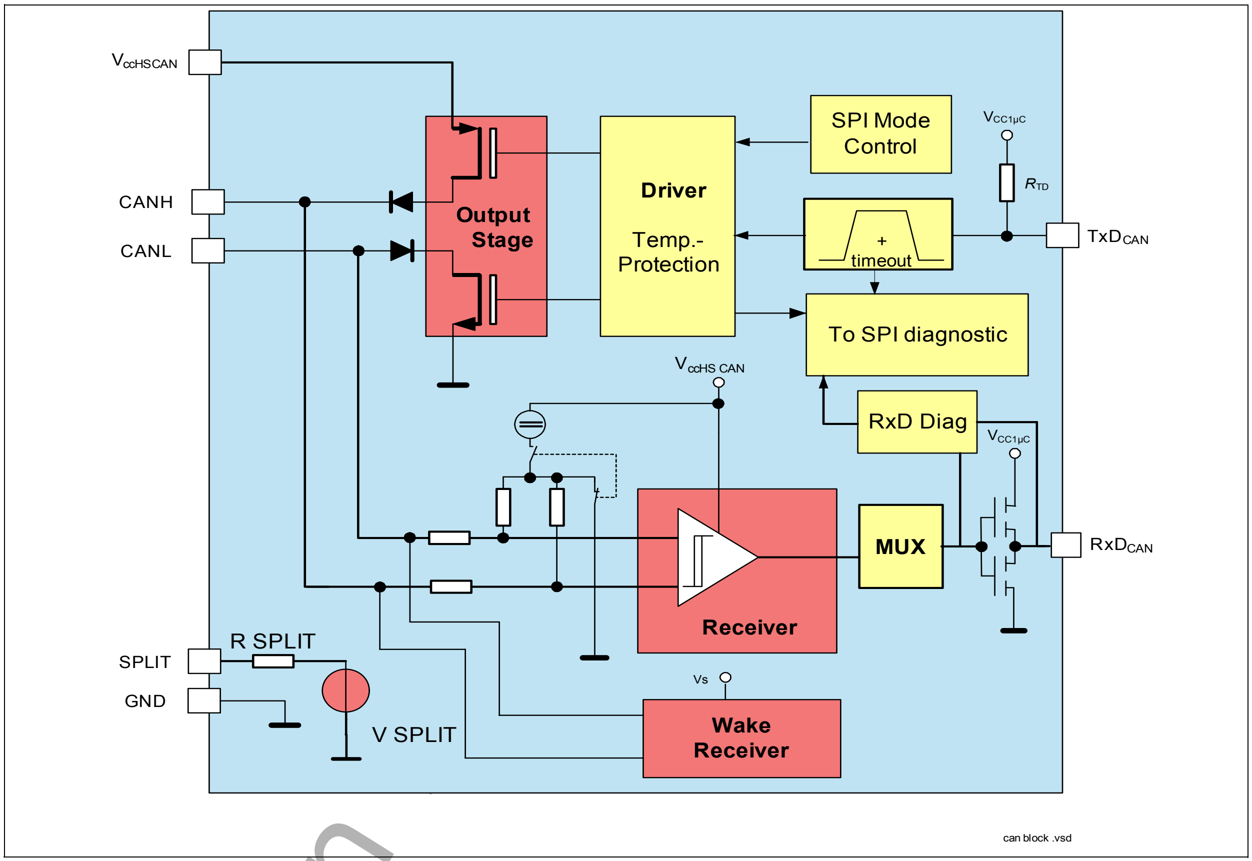

Figure 10 **Functional Block Diagram**

8.2 High-speed CAN Description

The Controller Area Network (CAN) transceiver part of the SBC provides high-speed (HS) differential mode data transmission (up to 1 Mbaud) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible to ISO/DIS 11898-2 and 11898-5 as well as SAE J2284.

The CAN transceiver offers low power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive-only Mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp15/30 applications).

A wake-up from the CAN Wake capable Mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and will be woken up by the CAN bus activities.

Refer to **Figure 11** for a description of the matching of the transceiver modes with the SBC mode.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

8.2.1 CAN Normal Mode

To transfer the CAN transceiver into the CAN Normal Mode, an SPI word must be sent. This mode is designed for normal data transmission/reception within the HS CAN network. It can be accessed in Normal Mode of the SBC, as well as in SBC Software Flash Mode, and SBC Software Development Mode.

Transmission

The signal from the microcontroller is applied to the TxDCAN input of the SBC. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

Reception

Analog CAN bus signals are converted into digital signals at RxD via the differential input receiver. In CAN Normal and CAN Receive Only Mode, the split pin is used to stabilize the Recessive Common Mode signal. The RxD pin is diagnosed and the detected failure is reported to the SPI diagnostic register.

8.2.2 CAN Wake Capable Mode

This mode, which can be used in SBC Stop, Sleep, Restart and Normal Modes by programming via SPI and is automatically accessed in SBC Fail-Safe Mode, is used to monitor bus activities. A wake up signal on the bus results in different behavior of the SBC, as described in **Table 6**. After wake-up the transceiver can be switched to CAN Normal Mode for communication. To enable the CAN wakeable mode after a wake via CAN, the CAN transceiver must be switched to CAN Normal Mode, CAN Receive Only Mode or CAN Off, before switching to CAN Wakeable Mode again.

Table 6 Action Due to a CAN Wake Up

SBC Mode	SBC Mode after wake	Vcc1µC	INT	RxD	Int. Bit WK CAN
Sleep Mode	Restart Mode	Ramping up	HIGH	LOW	1
Stop Mode	Stop Mode	ON	LOW[1]	LOW	1
Restart Mode	Restart Mode	Ramping up / ON	HIGH	LOW	1
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW	1
Normal Mode	Normal Mode	ON	LOW[1]	LOW	1

1) When not masked via SPI

Wake-Up in SBC Sleep Mode

Wake-up is possible via a CAN message (filtering time t > t_{WU}), it automatically transfers the SBC into the SBC Restart Mode and from there to Normal Mode the RxD pins in set to LOW, see **Figure 11**. The microcontroller is able to detect the low signal on RxD and to read the wake source out of the “Wake Register Interrupt” register (000) via SPI. No Interrupt is generated when coming out of Sleep Mode.

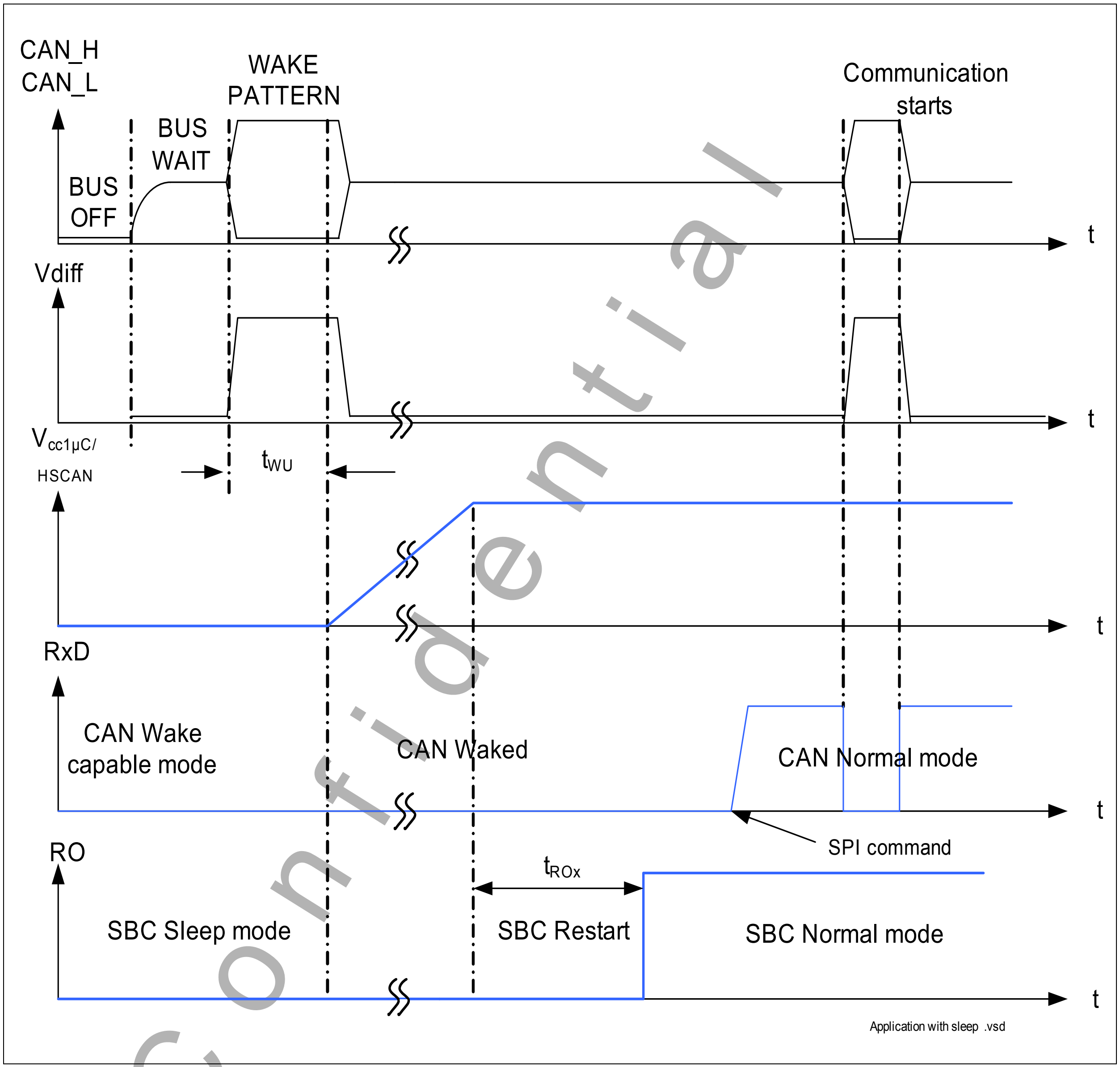

Figure 11 Timing during Transition from Sleep to Normal Mode

Wake-Up in SBC Stop Mode

In SBC Stop Mode, if a wake-up is detected, it is signaled by the INT output and by the “WK CAN” SPI bit. It is also signaled by RxDCAN put to low. The microcontroller should set the device to SBC Normal Mode, there is no automatic transition to Normal Mode. In Normal Mode the transceiver can be enabled via SPI.

Wake-Up in SBC Restart or SBC Fail-Safe Mode

In SBC Restart or SBC Fail-Safe Mode, if a wake-up is detected, it is signaled by the “WK CAN” SPI bit.

Wake-Up in SBC Normal Mode

In SBC Normal Mode, if a wake-up is detected, it is signaled by the “WK CAN” SPI bit and INT output, and RxD remains LOW.

8.2.3 CAN OFF Mode

CAN OFF Mode, which can be accessed in the SBC Stop, Sleep, Restart and Normal modes, and automatically accessed in SBC Init and Factory Flash modes, is used to completely stop CAN activities. In CAN OFF Mode, a wake up event on the bus will be ignored.

8.2.4 CAN Receive Only Mode

In CAN Receive Only Mode (RxD only), the driver stage is de-activated but reception is still operational. This mode is accessible by an SPI command.

8.2.5 CAN Cell in Disabled State

During disable state, when $V_s < V_{UV\_OFF}$, the CAN cell does not have enough supply voltage. In this state, the CANH and CANL pins are set to high impedance, to guarantee passive behavior. The maximum current that can flow in the CANH and CANL pins in this mode are specified by $I_{CANH,lk}$ and $I_{CANL,lk}$.

8.3 CAN Cell Mode with SBC Mode

Table 7 shows all the CAN modes accessible to the current SBC Mode. Automatic transition from one CAN mode to an other is only allowed in the same column.

Table 7 HS CAN States, Based on SBC modes

SBC Mode	CAN Mode			
INIT Mode	OFF			
Normal Mode	OFF	Wake capable	Normal	Receive only
Stop Mode	OFF	Wake capable		
Sleep Mode	OFF	Wake capable		
Restart Mode	OFF	Wake capable		
Fail-Safe Mode	Wake capable			
SW Flash Mode	Normal			

8.3.1 SBC Normal Transition to Sleep or Stop Mode

During the transition from SBC Normal to Sleep or Stop Modes, the receiver module is deactivated and replaced by the low power mode receiver for wake-up capability. The next message can be only a wake-up call. It is possible to set the SBC directly from SBC Normal Mode (with CAN Normal Mode) to SBC Sleep or Stop Mode, but this is not recommended, because a wake pattern on the CAN network that could occurs during SPI communication could get lost. It is preferable, in SBC Normal Mode to first send the CAN transceiver into CAN Wake Capable Mode, and then set the entire device to SBC Sleep or Stop Mode. In the unlikely case that the device would see a wake up call during the transmission order “SBC go to sleep”, the device will store this event and bypass the “SBC go to sleep” command to go back into SBC Restart Mode.

Do not change the Transciever setting with the same SPI command that is used to sent the device to Sleep Mode.

8.3.2 Transition from SBC Sleep to other Modes

In SBC Sleep Mode, a wake-up on the CAN cell will set the SBC to Restart Mode automatically if the CAN Wake Capable Mode of the SBC is selected via SPI. **Figure 11** shows the typical timing.

8.4 Failure Detection

All failures are reported in the SPI diagnostic encoder, the TxD time-out is reported as TxD shorted to GND. In case of local failure and Bus Dominat Clamped failure, the transceiver is automatically switched to the CAN Receive only Mode.

8.4.1 TxD Time-out Feature

If the TxD signal is dominant for a time t > t_{TxD}, the TxD time-out function deactivates the transmission of the signal at the bus. This is implemented to prevent the bus from being blocked permanently due to an error. The transmission is released after switching the CAN to Active Mode via SPI. Refer to **Figure 12**.

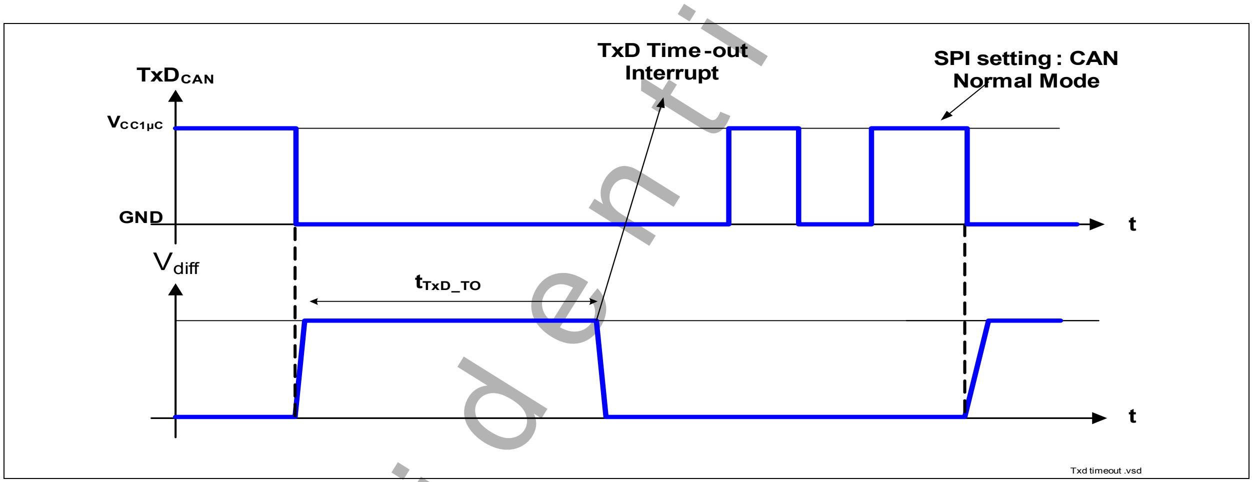

Figure 12 **TxD Time-out diagram**

8.4.2 Bus Dominant Clamping

If the HS CAN bus signal in dominant for a time $t > t_{BUS\_TO}$, a bus dominant clamping is detected. The CAN transceiver is switched to Receive Only Mode. The failure is signaled via SPI. If the bits are not masked the INT pin is set to low. For operation the transceiver needs to be switched back to Normal Mode via SPI.

8.4.3 TxD to RxD Short Circuit Feature

Similar to the TxD time-out, a TxD to RxD short circuit would also block the bus communication. To avoid this, the CAN transceiver provides TxD to RxD short circuit detection. In this case, it is recommended to switch OFF the SBC HS CAN supply (e.g. V_{cc2}) via SPI command to prevent disturbances on the CAN bus. This failure is reported into the diagnostic frame of the SPI. The INT pin is set LOW if not disabled via SPI. The transmitter is automatically inhibited and goes back to normal operation after a SPI command.

8.4.4 Overtemperature

The driver stages are protected against overtemperature. Exceeding the shutdown temperature results in deactivation of the CAN transceiver. The CAN transceiver is activated gain after cooling down, the device stays in CAN Active Mode. To avoid a bit failure after cooling down, the signals can be transmitted again only after a dominant to recessive edge at TxD.

Figure 13 shows how the transmission stage is deactivated and activated again. First, an overtemperature condition causes the CAN transceiver to be deactivated. After the overtemperature condition is no longer present, the transmission is released automatically after the TxD bus signal has changed to recessive level.

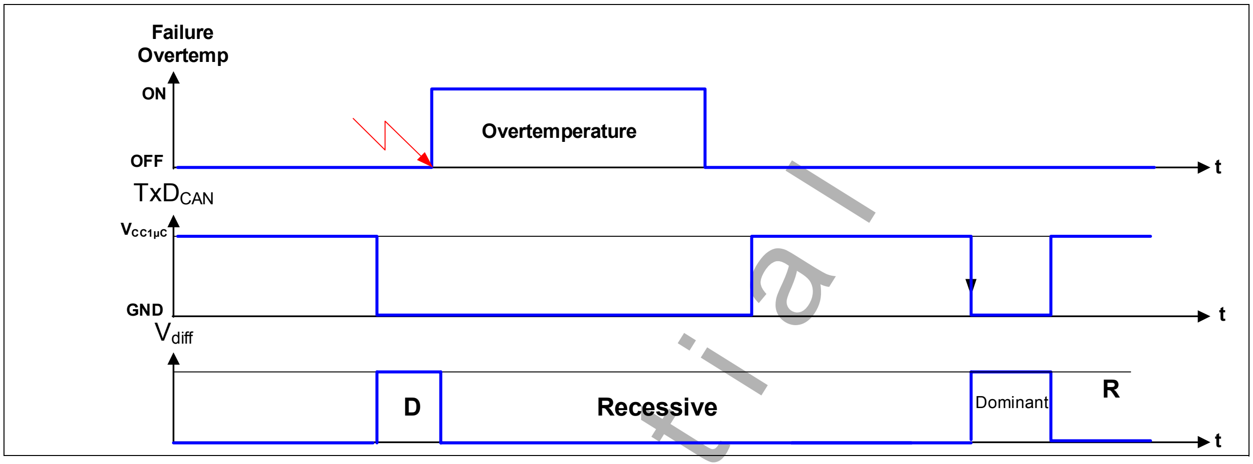

Figure 13 Release of the Transmission after Overtemperature

8.4.5 Permanent RxD Recessive Clamping

If the RxD signal is permanently recessive (such as shorted to $V_{cc1µC}$), although there is a message sent on the bus, the host microcontroller of this transceiver could start a message at any time because the bus appears to be idle. To prevent this node from disturbing communication on the bus, the SBC offers permanent RxD recessive clamping. If the RxD signal is permanently recessive, the failure is diagnosed and the transmitter is deactivated as long as the error occurs. The transmitter is reactivated after an SPI command.

8.4.6 $V_{ccHSCAN}$ Undervoltage

The CAN transceiver cell has no dedicated under voltage detection and use the V_{CC2} or V_{CC3} under voltage circuitry. The µC can switch of the CAN in case of undervoltage.

8.4.7 Bus failures

In case one of the following bus failures is detected by the SBC the interrupt bit CAN BUS is set to “1” and an interrupt is generated, if not masked. The CAN transceiver does not change the mode due to a detected bus failure.

Bus Failures

- CANH short to GND
- CANH short to Vs
- CANH short to Vcc
- CANL short to GND
- CANL short to Vs
- CANL short to Vcc

A short of CANH to CANL is detected by the microcontroller as the signal sent on TxD is not received on RxD.

8.5 SPLIT Circuit

SPLIT circuitry is activated during CAN Normal and Receive Only Mode and de-activated (SPLIT pin high ohmic) during CAN Wake Capable and OFF Modes. The SPLIT pin is used to stabilize the recessive common mode signal in Normal Mode and RxD Only Mode. This is achieved with a stabilized voltage of 0.5 x $V_{ccHSCAN}$ typical at SPLIT.

A correct application of the SPLIT pin is shown in **Figure 14**. The SPLIT termination for the left and right nodes is implemented with two 60 Ω resistors and one 10 nF capacitor. The center node in this example is a stub node and the recommended value for the split resistances is 1.5 kΩ.

In the case the application doesn't request the SPLIT pin feature, the pin has to be left open.

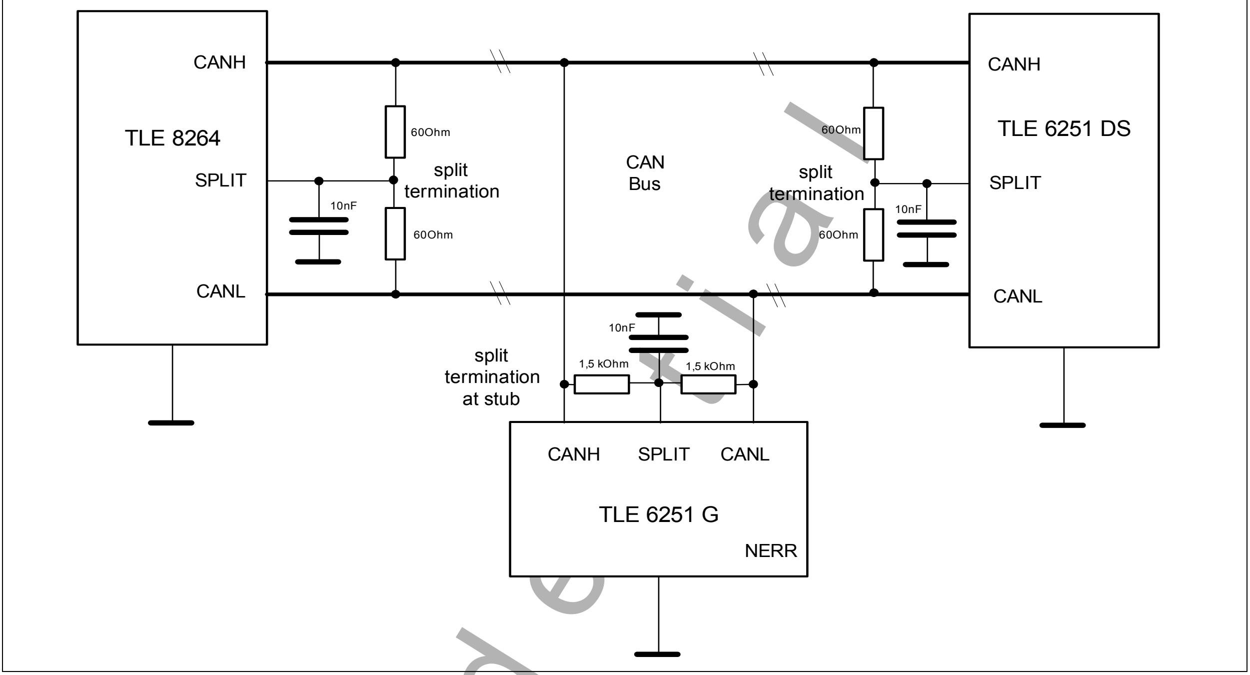

Figure 14 Application example for the SPLIT Pin

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8.6 Electrical Characteristics

4.75 V < V_{ccHSCAN} < 5.25 V; V_S = 5.5 V to 28 V; R_L = 60 Ω; CAN Normal Mode; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
CAN Bus Receiver							
8.6.1	Differential Receiver Threshold Voltage, recessive to dominant edge	$V_{\mathrm{diff,rd\_N}}$	–	0.80	0.90	V	$V_{\mathrm{diff}} = V_{\mathrm{CANH}} - V_{\mathrm{CANL}}$ CAN Normal Mode
8.6.2	Differential Receiver Threshold Voltage, dominant to recessive edge	$V_{\mathrm{diff,dr\_N}}$	0.50	0.60	–	V	$V_{\mathrm{diff}} = V_{\mathrm{CANH}} - V_{\mathrm{CANL}}$ CAN Normal Mode
8.6.3	Common Mode Range	CMR	-12	–	12	V	–
8.6.4	Differential Receiver Hysteresis	$V_{\mathrm{diff,hys\_N}}$	–	110	–	mV	CAN Normal Mode
8.6.5	CANH, CANL Input Resistance	R_i	10	20	30	kΩ	Recessive state
8.6.6	Differential Input Resistance	R_{diff}	20	40	60	kΩ	Recessive state
8.6.7	Wake-up Receiver Threshold Voltage, recessive to dominant edge	$V_{\mathrm{diff,\ rd\_W}}$	–	0.8	1.15	V	CAN Wake Capable Mode
8.6.8	Wake-up Receiver Threshold Voltage, dominant to recessive edge	$V_{\mathrm{diff,\ dr\_W}}$	0.4	0.7	–	V	CAN Wake Capable Mode
8.6.9	Wake-up Receiver Differential Receiver Hysteresis	$V_{\mathrm{diff,\ hys\_W}}$	–	120	–	mV	CAN Wake Capable Mode

8.6 Electrical Characteristics (cont'd)

4.75 V < $V_{ccHSCAN}$ < 5.25 V; V_S = 5.5 V to 28 V; R_L = 60 Ω; CAN Normal Mode; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
CAN Bus Transmitter							
8.6.10	CANH/CANL Recessive Output Voltage	$V_{CANL/H}$	2.0	–	3.0	V	CAN Normal Mode no load
8.6.11	CANH, CANL Recessive Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_r\_N}$	-500	–	50	mV	CAN Normal Mode $V_{TxD} = V_{cc1\mu C}$; no load
8.6.12	CANL Dominant Output Voltage	V_{CANL}	0.5	–	2.25	V	CAN Normal Mode V_{TxD} = 0 V; $V_{ccHSCAN}$ = 5 V
8.6.13	CANH Dominant Output Voltage	V_{CANH}	2.75	–	4.5	V	CAN Normal Mode V_{TxD} = 0 V; $V_{ccHSCAN}$ = 5 V
8.6.14	CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_d\_N}$	1.5	–	3.0	V	CAN Normal Mode V_{TxD} = 0 V; $V_{ccHSCAN}$ = 5 V
8.6.15	CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_d\_N}$	1.5	–	3.0	V	CAN Normal Mode V_{TxD} = 0 V; $V_{ccHSCAN}$ = 5 V R_L = 50Ω
8.6.16	CANH Short Circuit Current	I_{CANHsc}	-200	-80	-50	mA	CAN Normal Mode $V_{CANHshort}$ = 0 V
8.6.17	CANL Short Circuit Current	I_{CANLsc}	50	80	200	mA	CAN Normal Mode $V_{CANLshort}$ = 18 V
8.6.18	Leakage Current	$I_{CANH,lk}$ $I_{CANL,lk}$	–	2	–	μA	$V_S = V_{ccHSCAN}$ = 0 V; 0 V < $V_{CANH,L}$< 5 V
SPLIT Termination Output; Pin SPLIT							
8.6.20	SPLIT Output Voltage	V_{SPLIT}	0.3 × $V_{ccHSCAN}$	0.5 × $V_{ccHSCAN}$	0.7 × $V_{ccHSCAN}$	V	CAN Normal Mode -500 μA < I_{SPLIT} < 500 μA
8.6.21	Leakage Current	I_{SPLIT}	-5	0	5	μA	CAN Wake capable Mode; -27 V < V_{SPLIT} < 40 V
8.6.22	SPLIT Output Resistance	R_{SPLIT}	–	600	–	Ω	–1)
Receiver Output RxD							
8.6.23	HIGH level Output Voltage	$V_{RxD,H}$	0.8 × $V_{CC1\mu C}$	–	–	V	CAN Normal Mode $I_{RxD(CAN)}$ = -2 mA;
8.6.24	LOW Level Output Voltage	$V_{RxD,L}$	–	–	0.2 × $V_{cc1\mu C}$	V	CAN Normal Mode $I_{RxD(CAN)}$ = 2 mA;
Transmission Input TxD							
8.6.26	HIGH Level Input Voltage Threshold	$V_{TD,H}$	–	–	0.7 × $V_{cc1\mu C}$	V	CAN Normal Mode recessive state
8.6.27	LOW Level Input Voltage Threshold	$V_{TD,L}$	0.3 × $V_{cc1\mu C}$	–	–	V	CAN Normal Mode dominant state

8.6 Electrical Characteristics (cont'd)

4.75 V < $V_{ccHSCAN}$ < 5.25 V; V_S = 5.5 V to 28 V; R_L = 60 Ω; CAN Normal Mode; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	**Typ.**	**Max.**		
8.6.28	TxD Input Hysteresis	$V_{TD,hys}$	–	$0.12 \times V_{cc1\mu C}$	–	mV	[1]
8.6.29	TxD Pull-up Resistance	R_{TD}	20	40	80	kΩ	–
Dynamic CAN-Transceiver Characteristics							
8.6.30	Min. Dominant Time for Bus Wake-up	t_{WU}	0.75	3	5	µs	CAN Wake capable Mode
8.6.31	Propagation Delay TxD-to-RxD LOW (recessive to dominant)	$t_{d(L),TR}$	–	150	255	ns	CAN Normal Mode C_L = 47 pF; R_L = 60 Ω; $V_{ccHSCAN}$ = 5 V; C_{RxD} = 15 pF
8.6.32	Propagation Delay TxD-to-RxD HIGH (dominant to recessive)	$t_{d(H),TR}$	–	150	255	ns	CAN Normal Mode C_L = 47 pF; R_L = 60 Ω; $V_{ccHSCAN}$ = 5 V; C_{RxD} = 15 pF
8.6.33	Propagation Delay TxD LOW to bus dominant	$t_{d(L),T}$	–	50	120	ns	CAN Normal Mode C_L = 47 pF; R_L = 60 Ω; $V_{ccHSCAN}$ = 5 V
8.6.34	Propagation Delay TxD HIGH to bus recessive	$t_{d(H),T}$	–	50	120	ns	CAN Normal Mode C_L = 47 pF; R_L = 60 Ω; $V_{ccHSCAN}$ = 5 V
8.6.35	Propagation Delay bus dominant to RxD LOW	$t_{d(L),R}$	–	100	135	ns	CAN Normal Mode C_L = 47 pF; R_L = 60 Ω; $V_{ccHSCAN}$ = 5 V; C_{RxD} = 15 pF
8.6.36	Propagation Delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	100	135	ns	CAN Normal Mode C_L = 47 pF; R_L = 60 Ω; $V_{ccHSCAN}$ = 5 V; C_{RxD} = 15 pF
8.6.37	TxD Permanent Dominant Time-out	t_{TxD_TO}	0.3	0.6	1.0	ms	CAN Normal Mode
8.6.38	Bus Dominant Time-out	t_{BUS_TO}	0.3	0.6	1.0	ms	CAN Normal Mode[1]

1) Not subject to production test; specified by design.

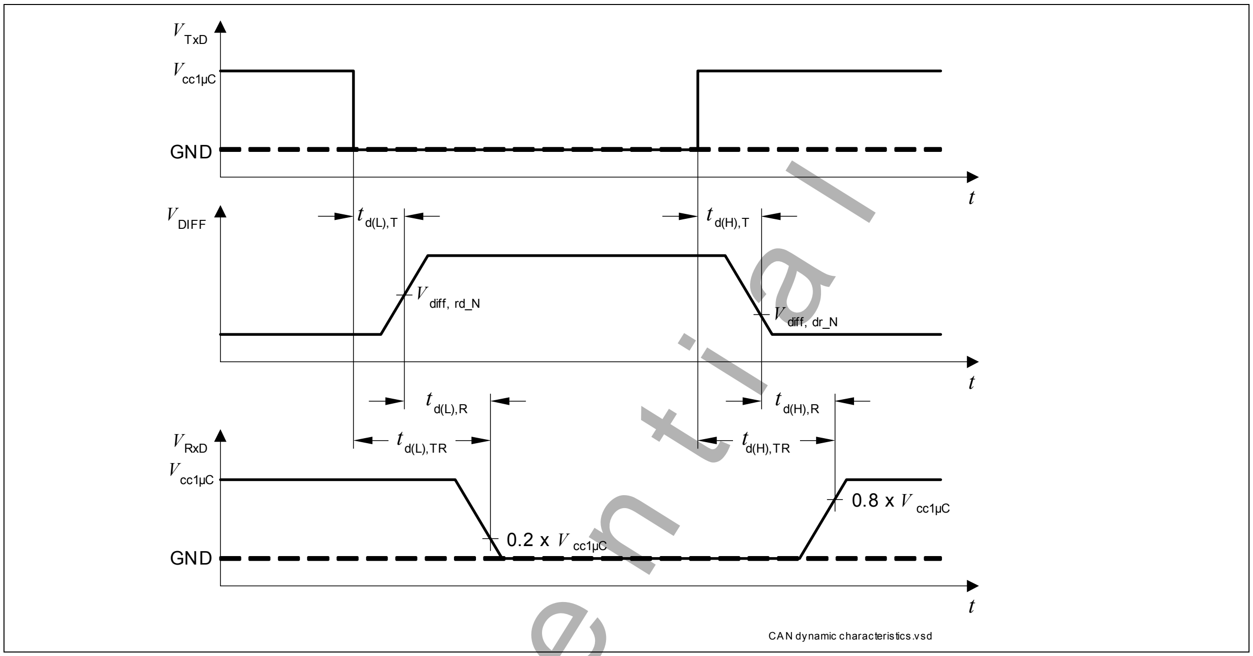


Figure 15 Timing Diagrams for Dynamic Characteristics

9 WK Pin

9.1 Block Description

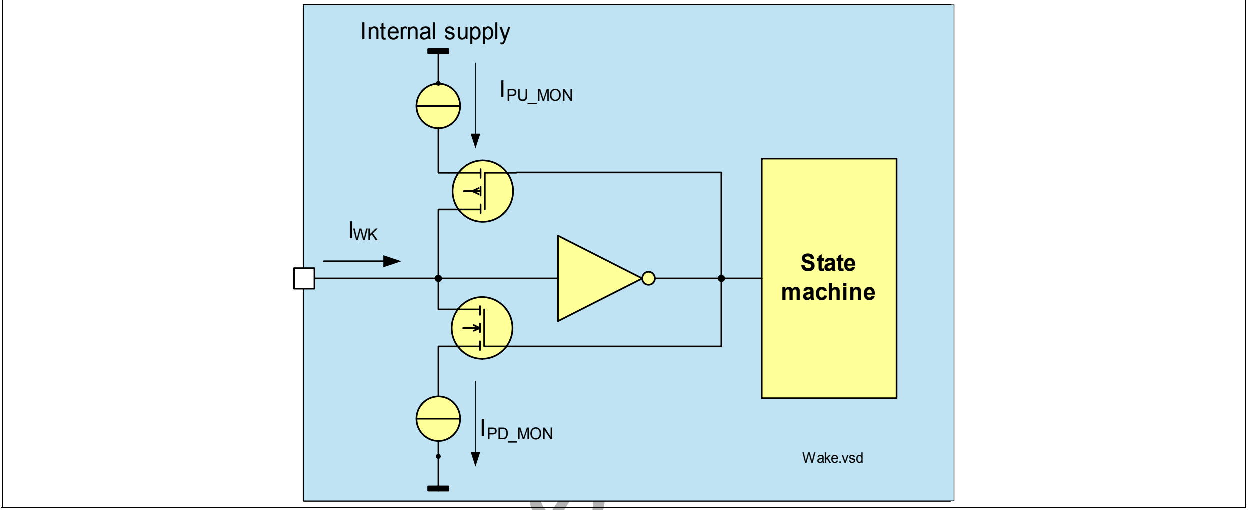


Figure 16 Functional Block Diagram

The internal voltage regulator ($V_{cc1\mu C}$) and the entire SBC can wake up by changing the wake input voltage. The WK input pin is a bi-level sensitive input. This means that both transitions, HIGH to LOW and LOW to HIGH, result in a wake-up. The filtering time is $t_{WK,\,f.}$The wake-up capability can be enabled or disabled via SPI command. In case of reverse polarity, no special protection must be set if the absolute maximum rating is respected. When the SBC is below the minimum V_{UVOFF}, (SBC OFF Mode) the pin WK is at high impedance; a wake event will be ignored.

The state of the WK pin (low or high) can always be read in Normal Mode, Stop Mode and SW Flash Mode at the bit WK State. When setting the bit "WK PIN on/off" to 1, the device wakes up from Sleep Mode with a high to low or low to high transition. From Fail-Safe Mode the device will always go to Restart Mode with a high to low or low to high transition. If the bit "WK PIN on/off" is set to 1 in Normal, Stop or SBC SW Flash Mode the interrupt bits "WK 0 WK pin" and/or "WK 1 WK pin" are set in case of a change on the WK pin and an interrupt is generated if not masked. With the bits "WK 0 WK pin" and "WK 1 WK pin" the interrupt for low to high transition and high to low transition can be masked separately.

9.2 Wake-Up Timing

Figure 17 shows typical wake-up timing and parasitic filtering. The filtering time is $t_{WK,\,f.}$. This is used to avoid a parasitic wake-up due to EMC disturbances. Specifically, the voltage transition on pin WK must be higher than the $V_{WK,TH}$ and longer than $t_{WK,f}$ to be understood as a wake-up signal.

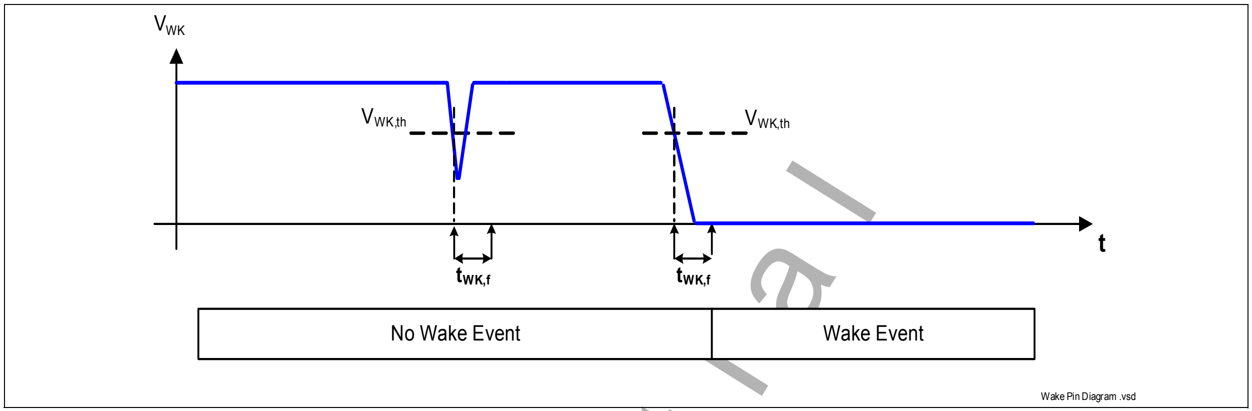


Figure 17 Wake-up Timing

9.2.1 Transition from Normal to Sleep Mode.

The SBC can not be sent from Normal Mode to Sleep Mode with uncleared interrupt in the WK interrupt bits “WK 0 WK pin” and “WK 1 WK pin”. This is implemented to avoid that a wake information from the WK pin gets lost during the transition from Normal to Sleep Mode. If a wake up appears during the µC sets the SBC to Sleep Mode, the SBC will wake up directly after going to Sleep Mode. There is no difference if the bits “WK 0 WK pin” or “WK 1 WK pin” bit were set during the transition or were just not cleared before sending the SPI command for Sleep Mode, the SBC will wake-up after entering the Sleep Mode. Therefore it always needs to be ensured that the bits are cleared before sending the SBC to Sleep Mode.

9.3 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
9.3.1	WK Input Threshold Voltage	$V_{WK,th}$	2	3	4	V	–
9.3.2	Input Hysteresis	$V_{I, hys.}$	0.1	–	0.7	V	
9.3.3	WK Filter Time	$t_{WK, f}$	10	–	25	µs	–
9.3.4	Input Current	I_{WK}	-2	–	2	µA	V_{WK} = 0 V; V_{WK} > 5V
9.3.5	WK pin pull up current	I_{PU_MON}	-30	–	-3	µA	V_{WK} = 3.8 V
9.3.6	WK pin pull down current	I_{PD_MON}	3	–	30	µA	V_{WK} = 2 V

10 LIN Transceiver

The SBC includes up to three LIN blocks, but this chapter describes only one because all three LIN block are completely identical.

10.1 Block Description

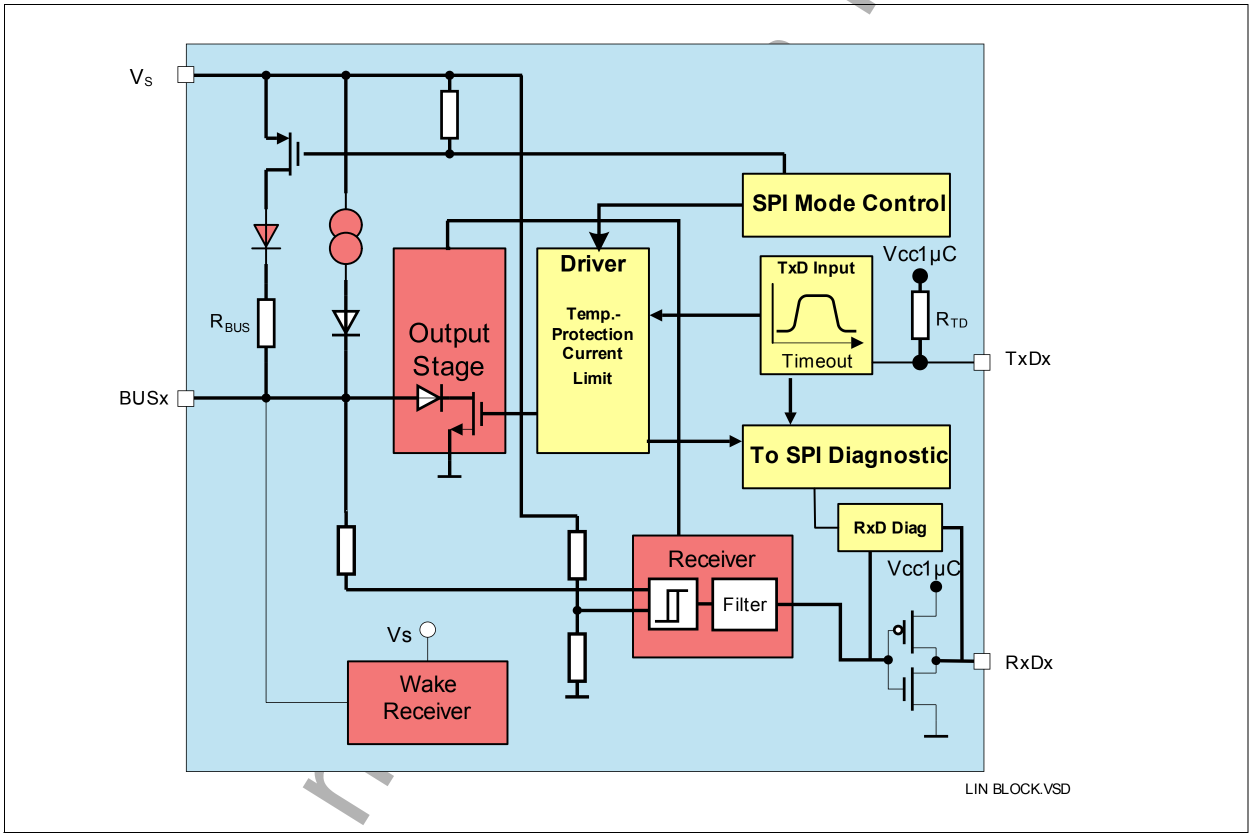


Figure 18 Functional Block Diagram

10.2 LIN Description

The LIN transceiver cells of the SBC is an interface between the protocol controller and the physical bus. It is especially suitable for driving the bus line in LIN systems in automotive and industrial applications. It is compatible to LIN 2.1 as well as SAE J2602-2.

To reduce current consumption, the LIN transceiver offers a LIN Wake Capable Mode and a LIN OFF Mode. The LIN transceiver has a bus short to GND feature implemented to avoid a battery discharge. The transceiver offers very good EMC performance within a broad frequency range independent of battery voltage. This is achieved by implementing a slope control mechanism based on a constant slew rate. In case the $V_s < V_{UVOFF}$, the LIN bus pin has high impedance and the maximum current which can flow in is set to I_{BUSlk}

10.2.1 LIN Normal Mode

In this mode, it is possible to transmit and receive messages on each BusX. The LIN transceiver enters the LIN Normal Mode after the microcontroller sends an SPI word (see **Chapter 15**) and also by entering SBC Software Flash Mode.

10.2.2 Slope Selection

The LIN transceiver offers a LIN Low Slope Mode for 10.4 kBaud communication and a LIN Normal Slope Mode for 20 kBaud communication. The only difference is the behavior of the transmitter. In LIN Low Slope Mode, the transmitter uses a lower slew rate to further reduce the EME compared to Normal Mode. This complies with SAE J2602 requirements.

The selection is done for all transceivers at the same time so that the chip is working in either LIN Low slope Mode or in LIN Normal Slope Mode. By default, the device works in LIN Low Slope Mode. The selection of LIN Normal Slope Mode is done by an SPI word. The selection is accessible in SBC Normal Mode only.

10.2.3 LIN OFF Mode

In this mode, the LIN transceiver is completely disabled. Only an SPI command can reactivate the LIN cell. This mode is accessible in SBC Normal, Stop, and Sleep Modes and is the default behavior in SBC Init Mode.

10.2.4 LIN Wake Capable Mode

This mode, which can be used in SBC Stop, Sleep, Restart and Normal Modes by programming via SPI and is automatically accessed in SBC Fail-Safe Mode, is used to monitor bus activities. A wake up signal on the bus results in different behavior of the SBC, as described in **Table 8**. After wake-up the transceiver can be switched to LIN Normal Mode for communication. To enable the LIN Wakeable Mode after a wake via this LIN tranceiver, the deticated LIN transceiver must be switched to LIN Normal Mode, LIN Receive Only Mode or LIN Off, before switching to LIN Wakeable Mode again.

Table 8 Action Due to a CAN Wake Up

SBC Mode	SBC Mode after wake	Vcc1µC	INT	RxD	Int. Bit WK CAN
Sleep Mode	Restart Mode	Ramping up	HIGH	LOW	1
Stop Mode	Stop Mode	ON	LOW(1)	LOW	1
Restart Mode	Restart Mode	Ramping up / ON	HIGH	LOW	1
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW	1
Normal Mode	Normal Mode	ON	LOW(1)	LOW	1

1) When not masked via SPI

Wake-Up in SBC Sleep Mode

Wake-up is possible via a LIN message (filtering time t > $t_{\mathrm{WK,bus}}$), it automatically transfers the SBC into the SBC Restart Mode and from there to Normal Mode the corresponding RxD pins in set to LOW, see **Figure 19**. The microcontroller is able to detect the low signal on RxD and to read the wake source out of the “Wake Register Interrupt” register (000) via SPI. No Interrupt is generated when coming out of Sleep Mode. The µC can now switch the CAN transceiver into LIN Normal Mode via SPI to start communication.

Wake-Up in SBC Stop Mode

In SBC Stop Mode, if a wake-up is detected, it is signaled by the INT output and by the “WK LINx” SPI bit. It is also signaled by RxDLINx put to low.The microcontroller should set the device to SBC Normal Mode, there is no automatic transition to Normal Mode. In Normal Mode the transceiver can be enabled via SPI.

10.2.5 LIN Receive Only Mode

In LIN Receive Only Mode (RxD only), the driver stage is de-activated but reception is still possible. This mode is accessible by an SPI command.

10.2.6 LIN Flash Mode

In LIN Flash Mode, the slope control mechanism is de-activated. This mode is accessible only in the SBC SW Flash mode. A communication up to 100kbaud is possible.

10.3 LIN Cell Mode with SBC Mode

Table 9 shows the LIN modes accessible in the different SBC modes. Automatic transition from one LIN mode to an other is only allowed in the same column.

Table 9 LIN States Based on SBC Modes

SBC Mode	LIN Mode			
INIT Mode	OFF			
Normal Mode	OFF	Wake capable	Normal / Low slope	Receive Only
Sleep Mode	OFF	Wake capable		
Restart Mode	OFF	Wake capable		
Stop Mode	OFF	Wake capable		
Fail-Safe Mode	Wake capable			
SW flash Mode	Flash			

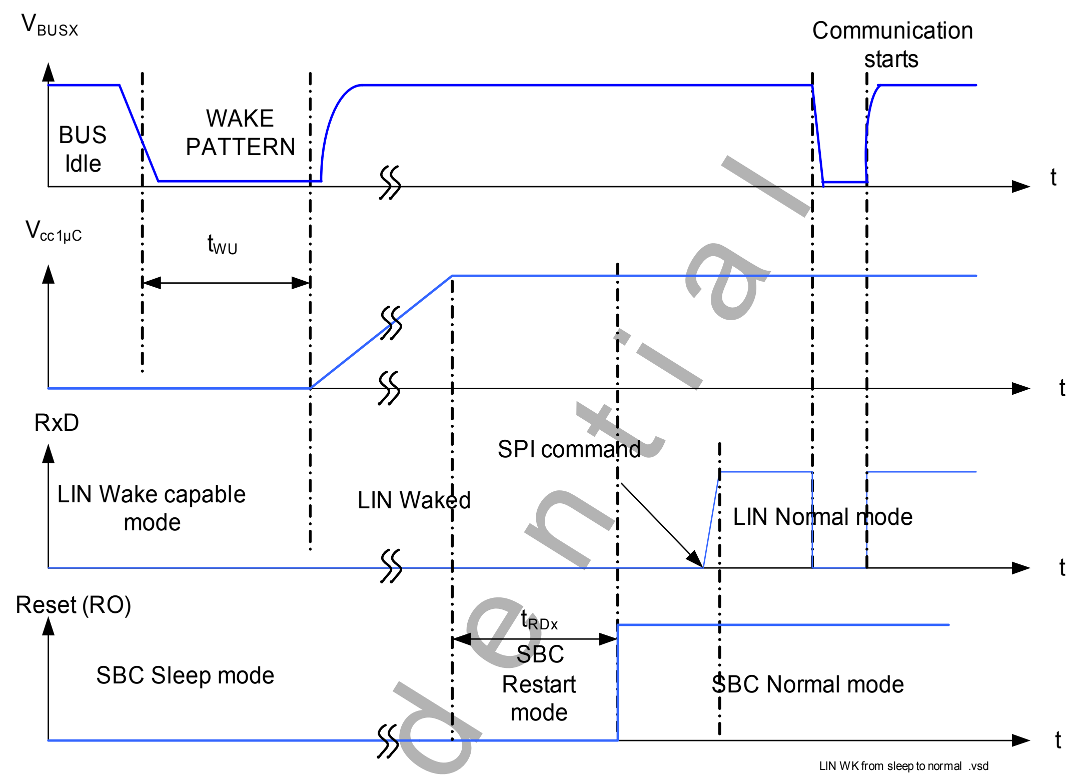


Figure 19 Timing during Transition from SBC Sleep to SBC Normal Mode

10.3.1 Transition from SBC Normal to Sleep / Stop Mode

It is recommended to first set the LIN Wake Capable Mode before setting the SBC Sleep or Stop Mode to avoid missing a wake up event. The reason is identical to the CAN behavior. For additional information, see **Chapter 8.3.1**.

Do not change the Transciever setting with the same SPI command that is used to sent the device to Sleep Mode.

10.4 Application Information

10.4.1 Bus Short to GND Feature

The LIN transceiver has a feature implemented to protect the battery from running out of charge in case of a bus short to GND. When the LIN transceiver is switched to Wake capable or Off, the internal pull-up resistor is switched off to prevent a large current from flowing to GND. In addition, the transceiver only wakes up on a dominant-to-recessive edge on the LIN bus, so with the bus shorted to GND the transceiver does not wake up.

10.4.2 Oscillator Tolerance

As required by LIN 2.1, an oscillator clock tolerance < 2% for the protocol handler is possible with LIN transceiver.

10.4.3 LIN Specification

The device fulfills the Physical Layer Specification of LIN 2.1.

The device fulfills the Physical Layer Specification SAE J2602-2.

10.5 Failure Detection

All failures are reported in the SPI Diagnostic Encoder except the TxD time-out feature, reported as TxD shorted to GND and over temperature, which is not reported. In case of failure, the transceiver is automatically switched to the LIN Receive only mode. The reactivation of the transmitter appears only after the microcontroller has requested it via SPI, except the over temperature. In this particular case, the transmitter is reactivated after a transition from dominant to recessive.

10.5.1 TxD Time-out Feature

If the TxD signal is dominant for a time t > t_{TxD_TO}, the TxD time-out function deactivates the transmission of the signal at the bus. This is done to prevent the bus from being permanently blocked due to an error. The transmission is released by sending the SPI command for LIN Normal Mode. Refer to **Figure 20**.

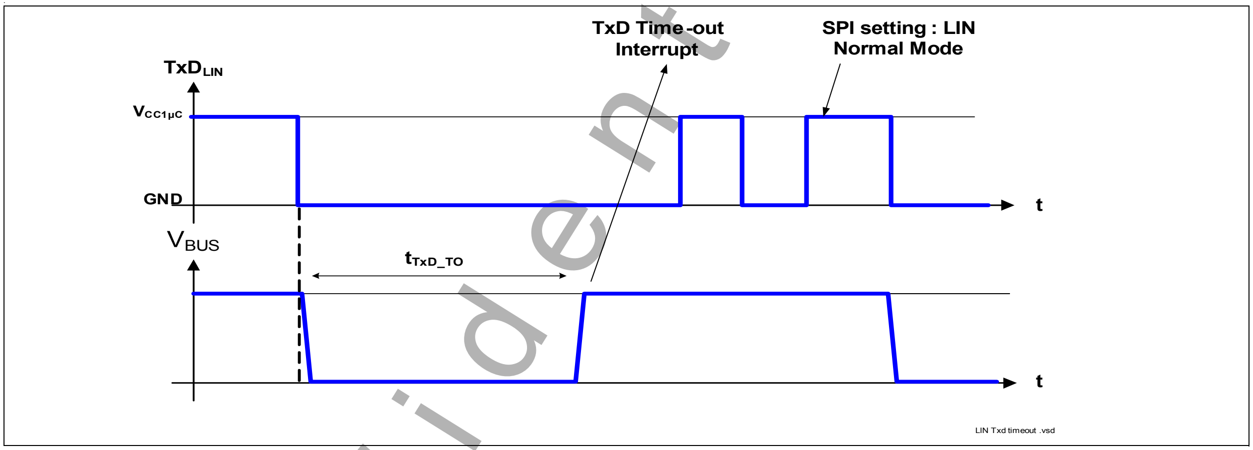


Figure 20 TxD Time-out Diagram

10.5.2 Bus Dominant Clamping

If the LIN bus signal in dominant for a time $t > t_{LIN\_TO}$, a bus dominant clamping is detected. The LIN transceiver is switched to Receive Only Mode. The failure is signaled via SPI. If the bits are not masked, the INT pin is set to low. For operation the transceiver needs to be switched back to Normal Mode via SPI.

10.5.3 TxD to RxD Short Circuit Feature

Similar to the TxD Time-out, a TxD to RxD short circuit would also block the bus communication. To avoid this, the LIN transceiver has TxD to RxD short circuit detection. This failure is reported to the diagnostic frame of the SPI. The transmitter is automatically inhibited and is reactivated after an SPI command.

10.5.4 Overtemperature

Figure 21 shows how the transmission stage is deactivated and activated again. The driver stages are protected against overtemperature. Exceeding the shutdown temperature results in deactivation of the driving stages. Nevertheless, the SBC can still receive messages via the RxD output, by setting automatically the LIN into LIN Receive Only Mode. To avoid a bit failure after cooling down, the signals can be transmitted again only after a dominant to recessive edge at TxD.

An overtemperature condition causes the transmission stage to deactivate. After the overtemperature condition is no longer present, transmission is reactivated after the TxD bus signal has changed to recessive level. The failure is not indicated in the SPI and doesn't generate any interrupt.

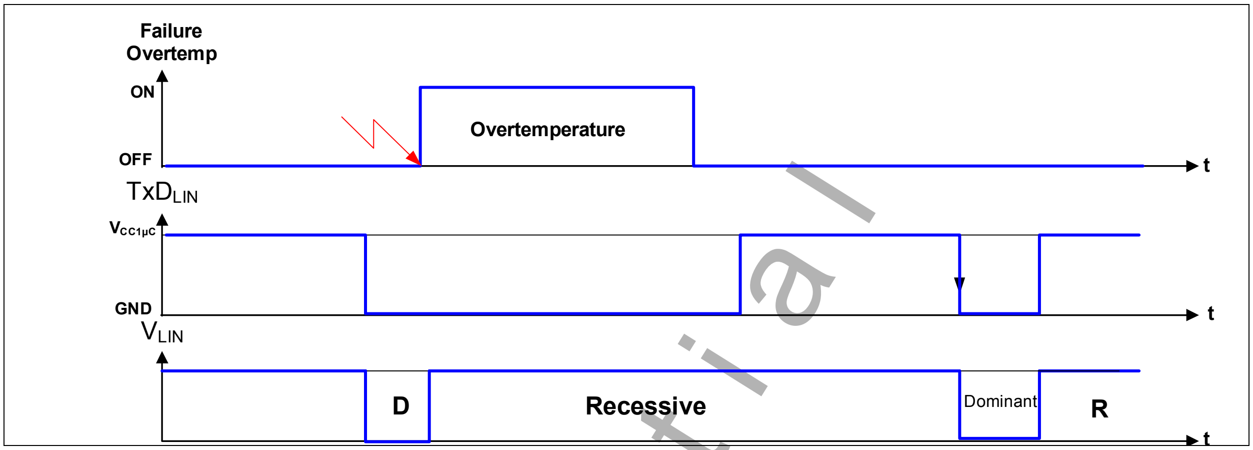


Figure 21 Release of the Transmission after Overtemperature

10.5.5 Permanent RxD Recessive Clamping

If the RxD signal is permanently recessive (for example, shorted to $V_{\mathrm{cc1\mu C}}$), although there is a message sent on the bus, the host microcontroller of this transceiver could start a message at any time, because the bus appears to be idle. To prevent this node from disturbing communication on the bus, the SBC offers permanent RxD recessive clamping. If the RxD signal is permanently recessive, the failure is diagnosed and the transmitter is deactivated as long as the error occurs. The transmitter is reactivated only after a SPI command.

10.6 Electrical Characteristics

V_S = 6 to 18 V[1); R_L = 500 Ω; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test condition
			Min.	Typ.	Max.		
Receiver Output RxDX Push Pull							
10.6.1	HIGH level Output Voltage	$V_{RxD,H}$	0.8 × $V_{CC1µC}$	–	–	V	LIN Normal Mode $I_{RxD(LIN)}$ = -1.6 mA; V_{bus} = V_S
10.6.2	LOW Level Output Voltage	$V_{RxD,L}$	–	–	0.2 × $V_{cc1µC}$	V	LIN Normal Mode $I_{RxD(LIN)}$ = 1.6 mA; V_{bus} = 0 V
Transmission Input TxDX							
10.6.3	HIGH Level Input Voltage Threshold	$V_{TxD,H}$	–	–	0.7 × $V_{cc1µC}$	V	LIN Normal Mode recessive state
10.6.4	Input Hysteresis	$V_{TxD,hys}$	–	0.12 × $V_{cc1µC}$	–	V	[3)
10.6.5	LOW Level Input Voltage Threshold	$V_{TxD,L}$	0.3 × $V_{cc1µC}$	–	–	V	LIN Normal Mode dominant state
10.6.6	Pull-up Resistance	R_{TD}	20	40	80	kΩ	V_{TxD} = 0 V

10.6 Electrical Characteristics (cont'd)

V_S = 6 to 18 V[1]; R_L = 500 Ω; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test condition
			Min.	Typ.	Max.		
Bus Receiver BusX							
10.6.7	Receiver Threshold Voltage, recessive to dominant edge	$V_{Bus,rd}$	$0.42 \times V_S$	$0.45 \times V_S$	–	V	LIN Normal Mode
10.6.8	Receiver Dominant State	$V_{Bus,dom}$	–	–	$0.42 \times V_S$	V	LIN Normal Mode (LIN 2.1 Param. 17)
10.6.9	Receiver Threshold Voltage, dominant to recessive edge	$V_{Bus,dr}$	–	$0.55 \times V_S$	$0.58 \times V_S$	V	LIN Normal Mode
10.6.10	Receiver Recessive State	$V_{Bus,rec}$	$0.58 \times V_S$	–	–	V	LIN Normal Mode (LIN 2.1 Param. 18)
10.6.11	Receiver Center Voltage	$V_{Bus,c}$	$0.475 \times V_S$	$0.5 \times V_S$	$0.525 \times V_S$	V	LIN Normal Mode (LIN2.1 Param. 19)
10.6.12	Receiver Hysteresis	$V_{Bus,hys}$	$0.07 \times V_S$	$0.1 \times V_S$	$0.175 \times V_S$	V	LIN Normal Mode $V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$ (LIN2.1 Param. 20)
10.6.13	Wake-up Threshold Voltage	$V_{Bus,wk}$	$0.40 \times V_S$	$0.5 \times V_S$	$0.6 \times V_S$	V	LIN Wake Capable Mode
10.6.14	Dominant Time for Bus Wake-up	$t_{WK,Bus}$	30	–	150	μs	LIN Wake Capable Mode

10.6 Electrical Characteristics (cont'd)

V_S = 6 to 18 V$^{1)}$; R_L = 500 Ω; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test condition
			Min.	Typ.	Max.		
Bus Transmitter BusX							
10.6.15	Bus Serial Diode Voltage Drop	$V_{serdiode}$	0.4	0.7	1.0	V	LIN Normal Mode $V_{TxD} = V_{CC1µC}$
10.6.16	Bus Recessive Output Voltage	$V_{Bus,ro}$	$0.8 \times V_S$	–	V_S	V	LIN Normal Mode $V_{TxD} = V_{CC1µC}$
10.6.17	Bus Dominant Output Voltage	$V_{Bus,do}$	–	–	1.2	V	LIN Normal Mode V_{TxD} = 0 V; V_S = 7V; R_L = 500 Ω;
			–	–	2.0	V	LIN Normal Mode V_S = 18 V; R_L = 500 Ω;
10.6.18	Bus Dominant Output Voltage	$V_{Bus,do}$	0.6	–	–	V	LIN Normal Mode V_{TxD} = 0 V; V_S = 7V; R_L = 1kΩ;
			0.8	–	–	V	LIN Normal Mode V_S = 18 V; R_L = 1 kΩ;
10.6.19	Bus Short Circuit Current	$I_{Bus,sc}$	40	100	150	mA	LIN Normal Mode V_{BUS} = 13.5 V; (LIN2.1 Param. 12)
10.6.20	Leakage Current	$I_{Bus,lk}$	-1000	-450	–	µA	V_S = 0 V; V_{BUS} = -12 V; (LIN2.1 Param. 15)
			–	–	5	µA	V_S = 0 V; V_{BUS} = 18 V; (LIN2.1 Param. 16)
			-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; (LIN2.1 Param. 13)
			–	–	5	µA	V_S = 8 V; V_{BUS} = 18 V; (LIN2.1 Param. 14)
10.6.21	Bus Pull-up Resistance	R_{Bus}	20	30	47	kΩ	LIN Normal Mode (LIN2.1 Param. 26)
10.6.22	LIN Output Current	I_{Bus}	-60	-30	-5	µA	LIN Wake Capable / OFF Mode; V_S = 18 V; V_{BUS} = 0V

10.6 Electrical Characteristics (cont'd)

V_S = 6 to 18 V[1]; R_L = 500 Ω; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test condition
			Min.	Typ.	Max.		
Dynamic Transceiver Characteristics BusX							
10.6.30	Propagation Delay, bus dominant to RxD LOW	$t_{d(L),R}$	–	1	6	µs	$V_{cc1\mu C}$ = 5 V; C_{RxD} = 20 pF; (LIN2.1 Param. 31)
10.6.31	Propagation Delay, bus recessive to RxD HIGH	$t_{d(H),R}$	–	1	6	µs	$V_{cc1\mu C}$ = 5 V; C_{RxD} = 20 pF; (LIN2.1 Param. 31)
10.6.32	Receiver Delay Symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; (LIN2.1 Param. 32)
10.6.34	TxD Dominant Time-out	t_{TxD_TO}	6	12	20	ms	V_{TxD} = 0 V
10.6.35	BUS Dominant Time-out	t_{LIN_TO}	6	12	20	ms	[3]
10.6.36	TxD Dominant Time-out Recovery Time	t_{torec}	–	10	–	µs	[3]
10.6.37	Duty Cycle D1 (for worst case at 20 kBit/s)	tduty1	0.396	–	–		LIN Normal slope Mode; duty cycle 1[2] $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; V_S = 7.0 … 18 V; t_{bit} = 50µs; $D1 = t_{bus\_rec(min)}/2\ t_{bit}$; (LIN2.1 Param. 27)
10.6.38	Duty Cycle D2 (for worst case at 20 kBit/s)	tduty2	–	–	0.581		LIN Normal slope Mode; duty cycle 2[2] $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$ V_S = 7.6 … 18 V; t_{bit} = 50µs; $D2 = t_{bus\_rec(max)}/2\ t_{bit}$; (LIN2.1 Param. 28)

10.6 Electrical Characteristics (cont'd)

V_S = 6 to 18 V[1]; R_L = 500 Ω; T_j = -40 °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test condition
			Min.	Typ.	Max.		
10.6.39	Duty Cycle D3 (for worst case at 10.4 kBit/s) Low Slope Mode	t_{duty3}	0.417	–	–		LIN Low slope Mode; duty cycle 3[2] TH_{Rec}(max) = 0.778 × V_{S}; TH_{Dom}(max) =0.616 × V_S; V_S = 7.0 … 18 V; t_{bit} = 96µs; D3 = $t_{bus\_rec(min)}$/2 t_{bit}; (LIN2.1 Param. 29)
10.6.40	Duty Cycle D4 (for worst case at 10.4 kBit/s) Low Slope Mode	t_{duty4}	–	–	0.590		LIN Low slope Mode; duty cycle 4[2] TH_{Rec}(min)= 0.389 × V_S; TH_{Dom}(min)= 0.251 × V_S V_S = 7.6 … 18 V; t_{bit} = 96µs; D4 = $t_{bus\_rec(max)}$/2 t_{bit}; (LIN2.1 Param. 30)
10.6.41	LIN Input Capacitance			15		pF	[3]

1) LIN specification is defined between 6 V and 18 V only.
2) Bus load conditions concerning LIN spec 2.0 C_{bus}, R_{bus} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω / 10 nF, 500 Ω
3) Not subject to production test, specified by design

11 Supervision Functions

11.1 Reset Function

11.1.1 Description

The reset output pin RO provides information to the microcontroller, for example, in the event that the output voltage has fallen below the undervoltage threshold $V_{RT1/2/3}$. When connecting the SBC to battery voltage, the reset signal remains LOW initially. When the output voltage $V_{cc1\mu C}$ has reached the reset threshold $V_{RT1,r}$, the reset output RO remains LOW for the reset delay time t_{rd1}. After that the RO is released to HIGH. A reset can also occur due to faulty Watchdog refresh.See **Chapter 11.2**. The reset threshold as well as the reset delay time can be adjusted via SPI. The RO pin has an integrated pull-up resistor.

11.1.2 Reset diagnosis

The RO pin is diagnosed for both short circuit to V_{ccx} and GND. Depending on the configuration, in case of RO failure, the SBC goes to SBC Fail-Safe or Restart Mode and activate the Limp Home output.

In case of short circuit to GND, it is detected in any SBC mode except SBC Restart Mode. At the falling edge of the RO, when supposed to be HIGH, the SBC enters automatically the SBC Restart Mode. If after the t_{rd} and RO relaxation, the RO pin is still LOW, then the SBC detects the clamping to LOW failure. The microcontroller is in permanent reset.

In case of short circuit to V_{ccx}, the SBC cannot detect the short circuit before a reset should occur. So reset clamped is detected when the SBC goes to SBC Restart Mode or during Init Mode.

11.1.3 Reset Timing

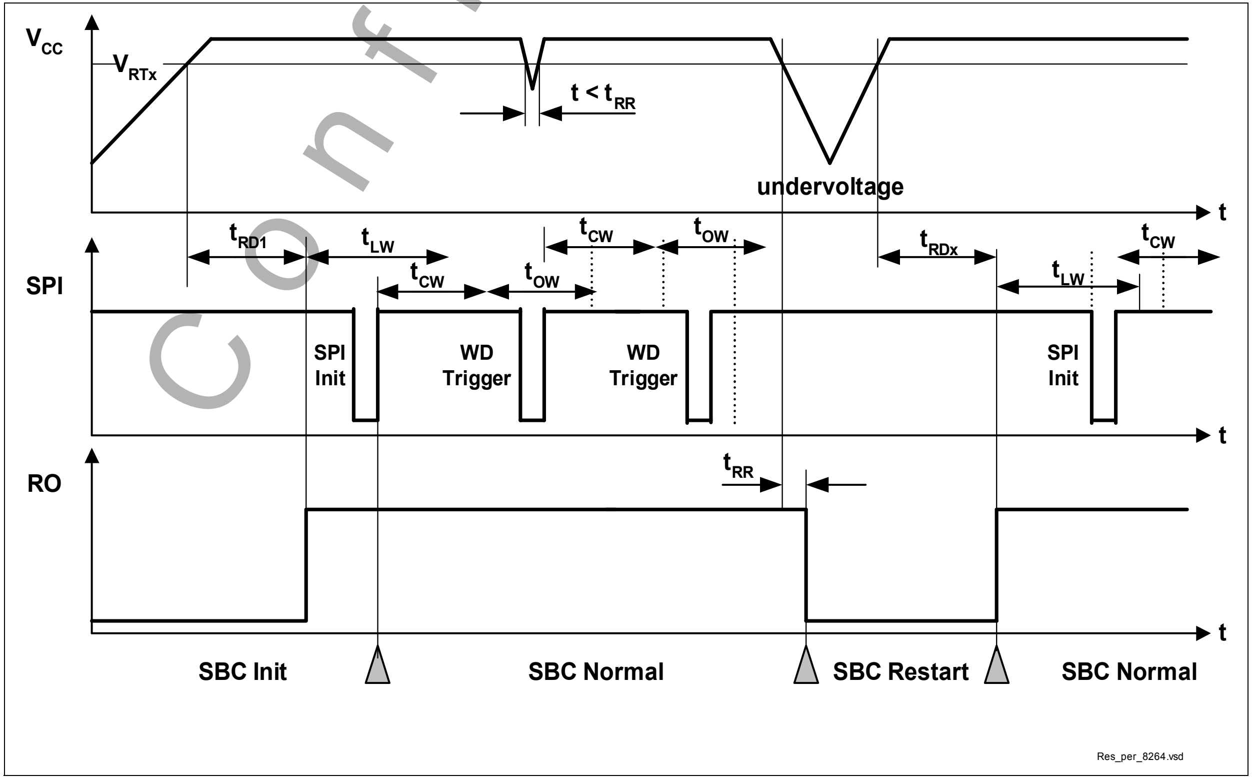


Figure 22 Reset Timing Diagram

11.1.4 Reset from Outside

If the reset pin RO is pulled to low from outside while no reset low is issued by the SBC, the device goes to Restart Mode. In Restart Mode an reset is issued by the SBC, the RO pin is set to low for the time t_{RD1} or t_{RD2}. If the RO pin is pulled to low for longer time Reset clamped is detected.

11.2 Watchdog

Two different Watchdogs are possible in the SBC. It can be either a Window Watchdog or a Time-out Watchdog. The Watchdog can also be inhibited in SBC Stop Mode and SBC SW Flash Mode via SPI. The Watchdog timing is programmed via SPI command. As soon as the Watchdog is activated, the timer starts running and the Watchdog must be served. Please refer to **Table 10** to match the SBC Modes with the Watchdog Modes.

The default setting for the Watchdog is Time-out Watchdog with a 256 ms timer. The long open window allows the microcontroller to run its initialization sequences and then to trigger the Watchdog via the SPI.

The Watchdog is served by a SPI bit and should toggle with the correct frequency. The default value is a 0, so the first trigger bit must be a 1.

In case of a Watchdog reset, the Watchdog immediately starts with a long open window when entering SBC Normal Mode. With the reset the watchdog bit is set to 0, so the first watchdog trigger after reset is a change to 1.

In SBC Software Development Mode, no reset is generated due to watchdog failure, if a watchdog failure occurs it is indicated by the SPI Reset bit and via INT pin. All watchdog modes are accessible in regards to the normal operation modes.

Table 10 Watchdog Functionality by SBC Modes

SBC Mode	Watchdog Mode	Remarks
INIT Mode	Watchdog Programmable; Watchdog is not active.	INIT Mode should be left in less than 256 ms (see **Chapter 13**)
Normal Mode	WD Programmable; Time-out or Window Watchdog	–
Software Flash Mode	Mode is fixed	SBC retains the set-up as in the mode before entering the Software Flash Mode
Stop Mode	Mode is fixed	SBC retains the set up as in the mode before entering the Stop Mode
Sleep Mode	OFF	SBC does not retain the set-up.
Fail-Safe Mode	OFF	SBC does not retain the set-up
Restart Mode	OFF	SBC will start default Watchdog setting (256ms Time-out Watchdog) when entering Normal Mode.

11.2.1 Time-out Watchdog

The Time-out Watchdog is an easier and less secure type of watchdog. Compared to the Window Watchdog there is no closed window existing. The watchdog trigger can be done any time within the watchdog time.

A watchdog trigger is detected as a write access to the “WD Refresh” within the SPI control word. The bit needs to be toggle (transition HIGH to LOW or LOW to HIGH) within the watchdog window. The trigger is accepted when the CSN input becomes HIGH.

A correct watchdog trigger starts a new window. The period is selected via the Window Watchdog timing bit field in the range of 16 ms to 1024 ms. For the safe trigger area the tolerance of the oscillator has to be taken into consideration, so the safe trigger time is below 90% of the programmed Watchdog time. It is possible to refresh the Watchdog with any SPI programming with the mode selection Normal, Stop, SW Flash or Read Only.

Should the trigger signal not meet the window, depending on the configuration, the SBC will go to SBC Restart Mode or to Fail-Safe Mode. A watchdog reset is created by setting the reset output RO low. In config 1 and config 3 the watchdog starts again in Normal Mode with the default watchdog setting (256ms Time-out Watchdog). The watchdog failure can be read at the bits RM0, RM1, LH0, LH1, LH2 via SPI.

11.2.2 Window Watchdog

A Watchdog trigger is detected as a write access to the “WD Refresh” within the SPI control word. The bit needs to be toggle (transition HIGH to LOW or LOW to HIGH) in the open window. The trigger is accepted when the CSN input becomes HIGH.

A correct Watchdog trigger results in starting the Window Watchdog by a closed window with a width of typically 50% of the selected Window Watchdog reset period. This period, selected via the Window Watchdog timing bit field, is in the range of 16 ms to 1024 ms. This closed window is followed by an open window, with a width of typical 50% of the selected period. From now on, the microcontroller must serve the Watchdog by periodically toggling the Watchdog bit. This bit toggling access must meet the open window. The tolerance of the oscillator has to be taken into consideration, so the safe window to trigger the Watchdog is from 55% to 90% of the programmed Window Watchdog time. It is possible to refresh the Watchdog with any SPI programming with the mode selection Normal, Stop, SW Flash or Read Only. A correct Watchdog service immediately results in starting the next closed window (see **Figure 23**, safe trigger area).

Should the trigger signal not meet the open window, depending on the configuration the SBC will go to SBC Restart Mode or to Fail-Safe Mode. A watchdog reset is created by setting the reset output RO low (see **Figure 24**). In config 1 and config 3 the watchdog starts again in Normal Mode with the default watchdog setting (256ms Time-out Watchdog). The watchdog failure can be read at the bits RM0, RM1, LH0, LH1, LH2 via SPI.

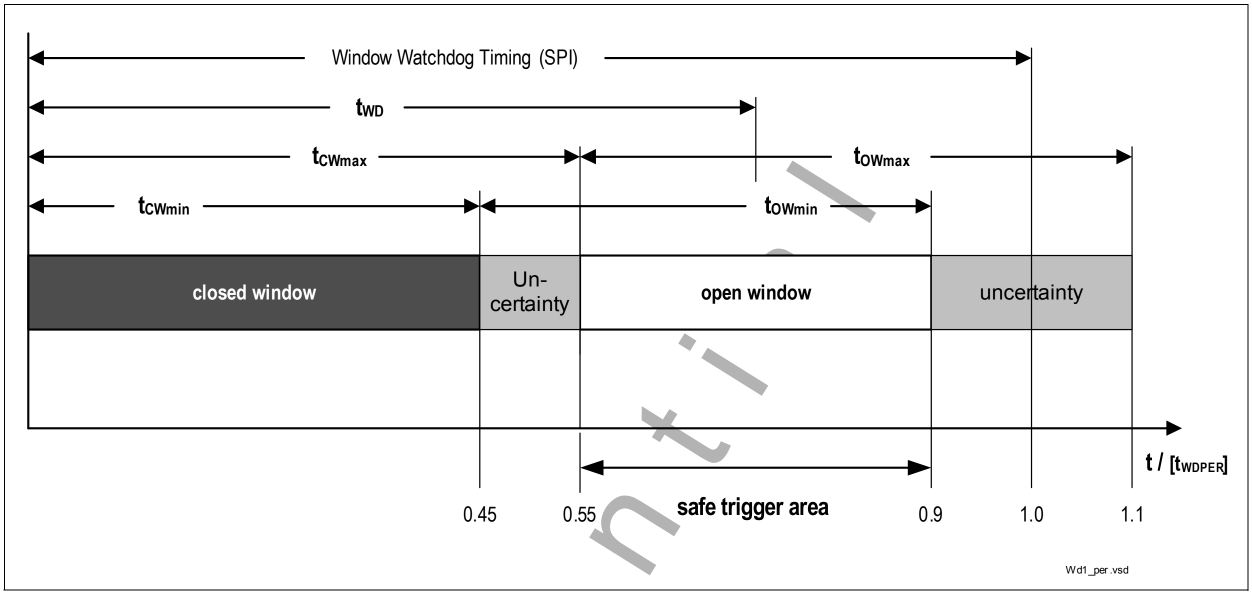


Figure 23 Window Watchdog Definitions

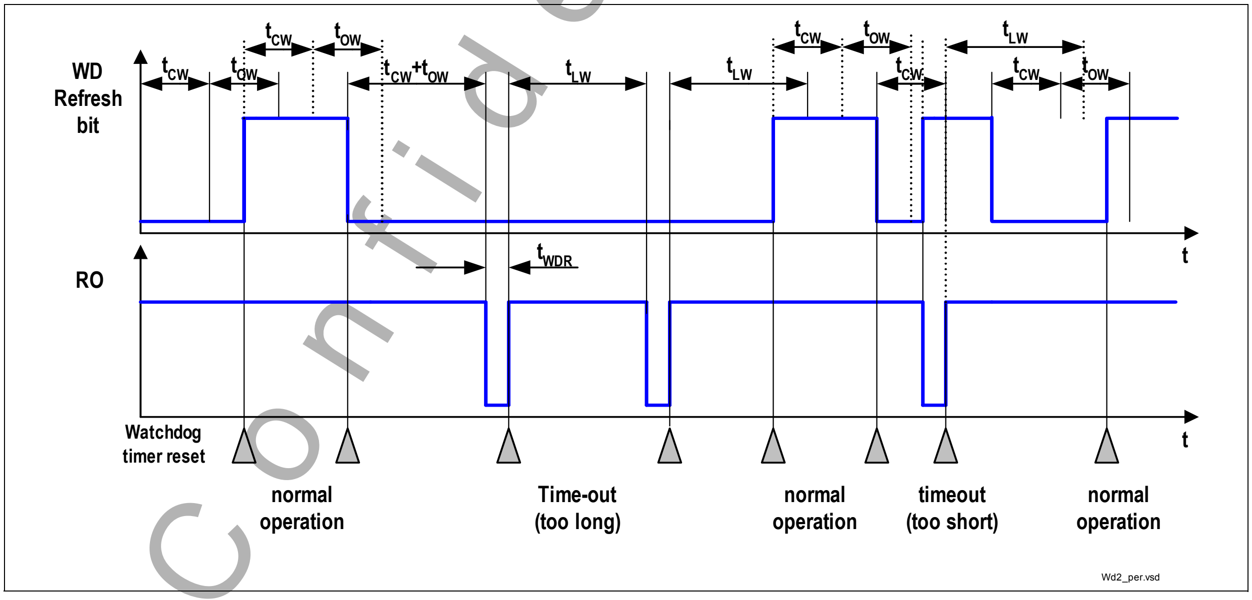


Figure 24 Window Watchdog Timing Diagram for config 1 and config 3

11.2.3 Changing the Watchdog Settings

The settings of the watchdog can be changed during the operation of the watchdog. The change is done with a SPI programming into the Watchdog Configuration Register. The new setting is programmed together with a valid watchdog trigger according to the old settings. The timer with the new settings starts with this SPI command. The toggling of the “WD Refresh” bit needs to be continued (transition HIGH to LOW or LOW to HIGH) with the new settings.

If the new settings were not valid, the watchdog will continue with the old settings and generate a “Wrong WD Set” interrupt.

11.2.4 Inhibition of the watchdog

During SBC Stop Mode and SBC SW Flash Mode, it is possible to deactivate the watchdog. To avoid unwished deactivation of the watchdog, a special protocol has to be followed, prior deactivating the watchdog. Please refer to **Figure 25**. In the case the exact process below is not respected, the SBC remains in the previous state, and an interrupt is generated (if not inhibited), and the *Wrong WD set* bit in the SPI is set.

When the microcontroller requests the SBC to go back to SBC Normal Mode, the Watchdog is reactivated. The watchdog settings that were valid before entering Stop Mode with watchdog off are valid. The watchdog timer starts with entering Normal Mode. In case window watchdog was selected the watchdog starts with a closed window. When setting the WD Refresh bit to 0 for the command that sends the device to Normal Mode the first watchdog trigger is a change to 1. As in Stop Mode the watchdog settings can not be changed, it is also not possible to change the watchdog settings with the command that sets the SBC from Stop Mode into Normal Mode.

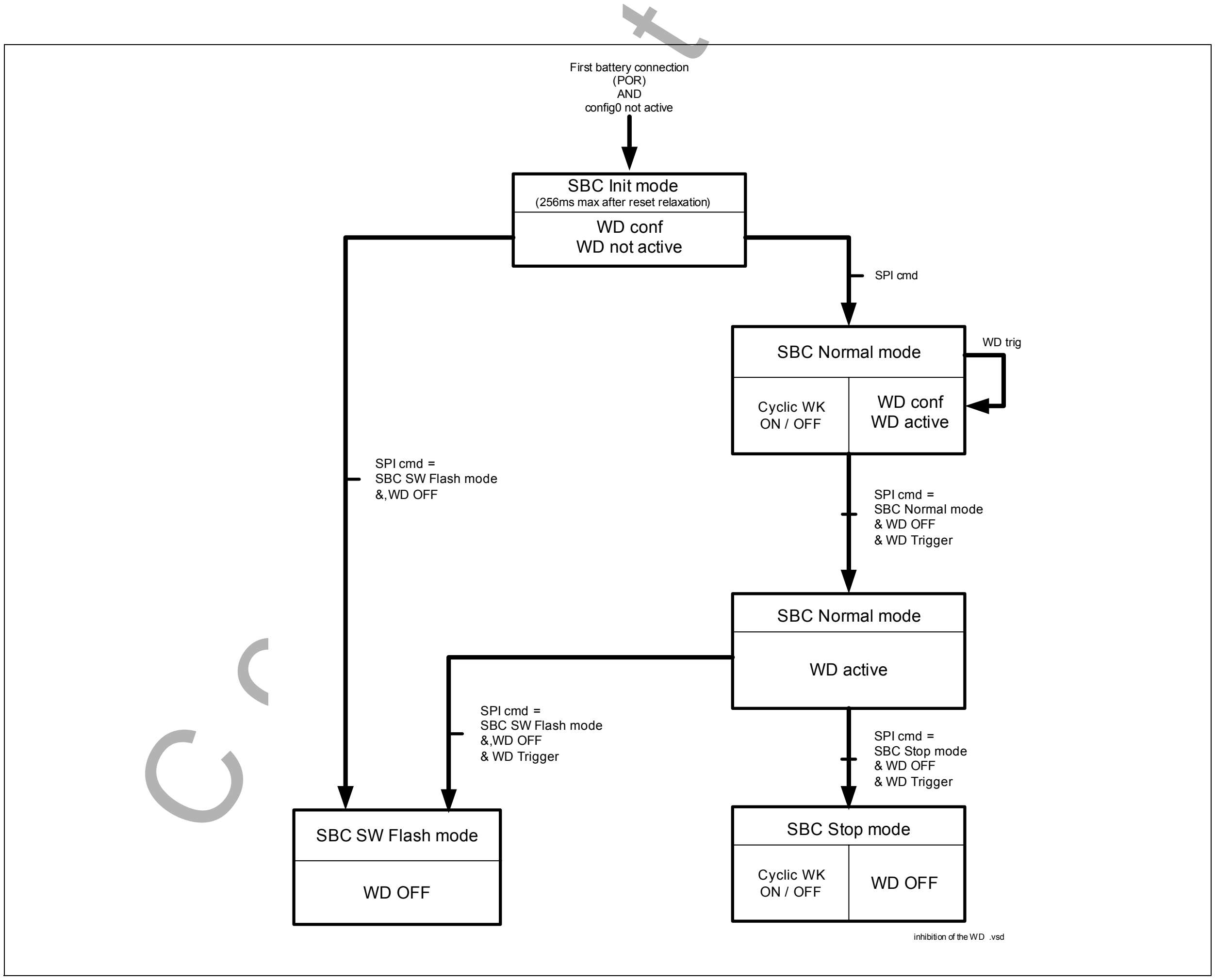


Figure 25 Inhibition of the watchdog

During SBC Stop Mode, when the cyclic wake feature is used and the watchdog is not disabled, it is necessary that the microcontroller acknowledges the interrupt by reading the SPI Wake register before the next Cyclic Wake occures. Otherwise, a reset is performed by setting the SBC to SBC Restart Mode.

11.3 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
Reset Generator; Pin RO							
11.3.1	Reset Threshold Voltage,	$V_{RT1,f}$	4.5	4.65	4.75	V	default setting, Vcc falling
		$V_{RT1,r}$	4.6	4.75	4.85	V	default setting, Vcc rising
		$V_{RT2,f}$	3.5	3.65	3,75	V	SPI option;Vcc falling
		$V_{RT2,r}$	3.6	3.75	3,85	V	SPI option; Vcc rising
		$V_{RT3,f}$	3.2	3.35	3.45	V	SPI option; $V_S \geq 4$ V; Vcc falling
		$V_{RT3,r}$	3.3	3.45	3.55	V	SPI option; $V_S \geq 4$ V, Vcc rising
	Reset Threshold Voltage Headroom	V_{RT1_HR}	250	–	–	mV	default setting[1]
		V_{RT2_HR}	1.25	–	–	V	SPI option;[1]
		V_{RT3_HR}	1.55	–	–	V	SPI option; $V_S \geq 4$ V [1]
11.3.2	Reset Threshold Hysteresis	$V_{RT,hys}$	20	100	200	mV	-
11.3.3	Reset Low Output Voltage	V_{RO}	–	0.2	0.4	V	I_{RO} = 1 mA for $V_{CC1\mu C} = V_{RT1/2/3}$; I_{RO} = 200 µA for $V_{RT1/2/3} > V_{CC1\mu C} \geq 1$ V
11.3.4	Reset High Output Voltage	V_{RO}	0.7 x $V_{CC1\mu C}$	–	$V_{CC1\mu C}$ + 0.3 V	V	I_{RO} = -20µA
11.3.5	Reset Pull-up Resistor	R_{RO}	10	20	40	kΩ	V_{RO} = 0 V
11.3.6	Reset Reaction Time	t_{RR}	4	10	26	µs	$V_{CC1\mu C} < V_{RT1/2}$ to RO = L
11.3.7	Reset Delay Time	t_{RD1}	4.5	5.0	5.5	ms	default SPI setting; after Power-On-Reset
		t_{RD2}	450	500	550	µs	SPI setting option
Watchdog Generator							
11.3.8	Long Open Window	t_{LW}	–	256	–	ms	[2]default setting
Internal Oscillator							
11.3.9	Internal Oscillator tolerance	f_{CLKSBC}	-10	0	10	%	–

1) Headroom between actual output voltage on $V_{CC1\mu C}$ and Reset Threshold Voltage for falling Vcc.

2) Specified by design; not subject to production test. Tolerance defined by internal oscillator tolerance f_{CLKSBC}.

12 Interrupt Function

12.1 Interrupt Description

The interrupt pin has a general purpose function to point out to the microcontroller either a wake up, a failure condition or the switch on of a voltage regulator. **Table 11** shows the possible interrupt sources in the device, and **Figure 26** gives the hardware set-up. The interrupt function is designed to inform the microcontroller of any wake-up event, overtemperature or overtemperature pre-warning as well as other failures. These events turn the INT pin to active LOW. All interrupt sources can be masked via a SPI bit, then no interrupt is generated for this event. For failures on under-voltage the interrupt is dual-sensitive. This means that an interrupt is generated when the failure appears, as well as when the failure disappears. For failures on over-temperature, communication failures and voltage regulator over current and undervoltage, the dedicated SPI interrupt bit indicated first the interrupt source and then the state of the device. So, the bit is set to failure I at the event, and remains latched at least until the microcontroller reads the bit. For the SBC failure (Wrong WD Setting, Reset, Fail SPI) and wake events, the INT indicates only an event and the bit is cleared with a dedicated SPI read.
The INT pin is released when an SPI read is done to Interrupt Register 000 with a "Read Only" command, or after interrupt time out t_{INTTO}. If the interrupt cause was a wake event, the interrupt bit can be read in Interrupt Register 000 and the bit is cleared. If it was an other interrupt source the bit INT is set, and interrupt register 001 and 010 need to be read. With a "Read Only"command the event triggered interrupt bits are cleared. The INT bit will be set to "0" when all bits in interrupt register 001 and 010 are set to "0". If an interrupt is masked (bit set to "0") only the interrupt does not occur, the interrupt bit in the SPI is shown.

Figure 26 shows a simplified diagram of the INT output. In Init Mode before RO goes high the INT pin is used to set the configuration of the device to config 1/3 or config 2/4, see **Chapter 14**.

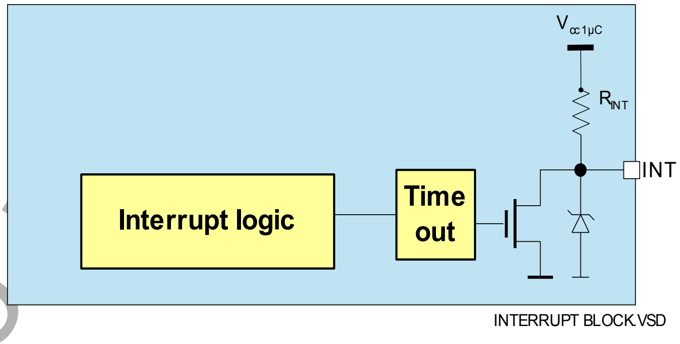


Figure 26 Interrupt Block Diagram

Table 11 Interrupt sources

Interrupt sources	INT Activation	SPI bit	State
Temperature			
Over temperature pre-warning $V_{CC1\mu C}$	Rising	OTP $V_{CC1\mu C}$	Event / State
Over temperature V_{CC2}	Rising	OT V_{CC2}	
Over temperature HS CAN	Rising	OT HSCAN	
Communication failure			
CAN Failure	Rising	CAN Failure 1..0 CAN Bus	Event/ State
LIN Failure	Rising	LINx Failure 1..0	
Voltage regulator			

Table 11 Interrupt sources

Interrupt sources	**INT Activation**	**SPI bit**	**State**
Undervoltage at V_{CC2} (except during switch off[1])	Rising and falling	$UV_{\_VCC2}$	Event / State
Undervoltage at V_{CC3}(except during switch off[1])	Rising and falling	$UV_{\_VCC3}$	
Over current at V_{CC3} (except during inhibition)	Rising	$I_{CC3} > I_{CC3MAX}$	
Voltage at V_{CC2} (during switch on[1])	Rising	$UV_{\_VCC2}$	Event
Voltage at V_{CC3} (during switch on[1])	Rising	$UV_{\_VCC3}$	
SBC Failure			
SPI data corrupted	Rising	SPI Fail	Event
Reset (SBC SW Development only)	Rising	Reset	
Wrong watchdog setting	Rising	Wrong WD set	
Wake			
Wake at CAN	Rising	WK CAN	Event
Wake at LIN	Rising	WK LINx	
Wake at WK	Rising	WK WK pin 1..0	
Cyclic WK	Rising	Cyclic WK	

1) When $V_{CC2/3}$ is switched off no interrupt is generated due to the undervoltage at $V_{CC2/3}$. When switching on $V_{CC2/3}$ an interrupt is generated when the command is sent to the SBC via SPI.

12.1.1 Interrupt for switching on Vcc2 and Vcc3

The Interrupt for Vcc2 and Vcc3 are generated when the SPI command for switching on the voltage regulator is executed. The interrupt bit is set to "1" and can be cleared with a Read Only command after the under voltage threshold is reached. If the Read Only is done before the reset threshold is reached, the interrupt bit can not be cleared as the undervoltage condition is still present. In this case a second interrupt can be issued for releasing the undervoltage condition.

In case of a short to GND on Vcc2 or Vcc3 the interrupt for switching on the voltage regulator is issued, but the µC can not clear the interrupt bit as the voltage regulator does not reach the undervoltage threshold.

12.1.2 Example of Interrupt Events and Read-out

The examples show single interrupt events. SPI read is done with "Read Only". The shown interrupts are not masked. Watchdog trigger is not shown in the examples.

The interrupt UV_Vcc2 that is generated by switching on V_{CC2} is shown in **Figure 27**. The interrupt is sensitive on rising event only.

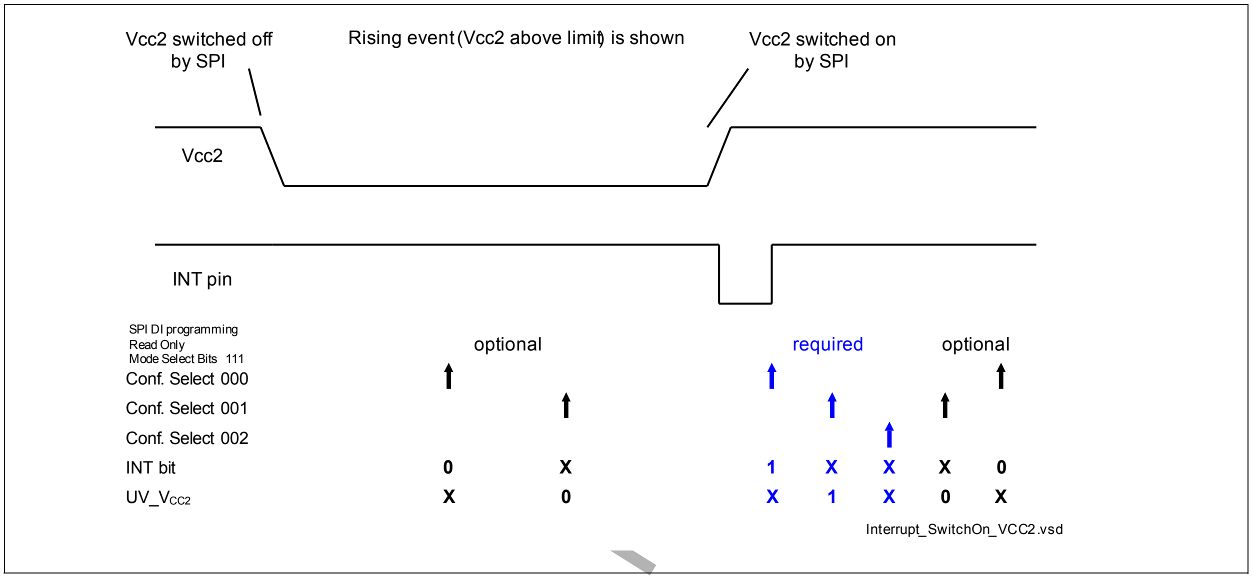


Figure 27 Interrupt Vcc2 switch-on.

The interrupt UV_Vcc2 that is generated by an under-voltage on V_{CC2} is shown in **Figure 28**. The interrupt is sensitive on rising and falling event and the interrupt bit also shows the state of the device and function.

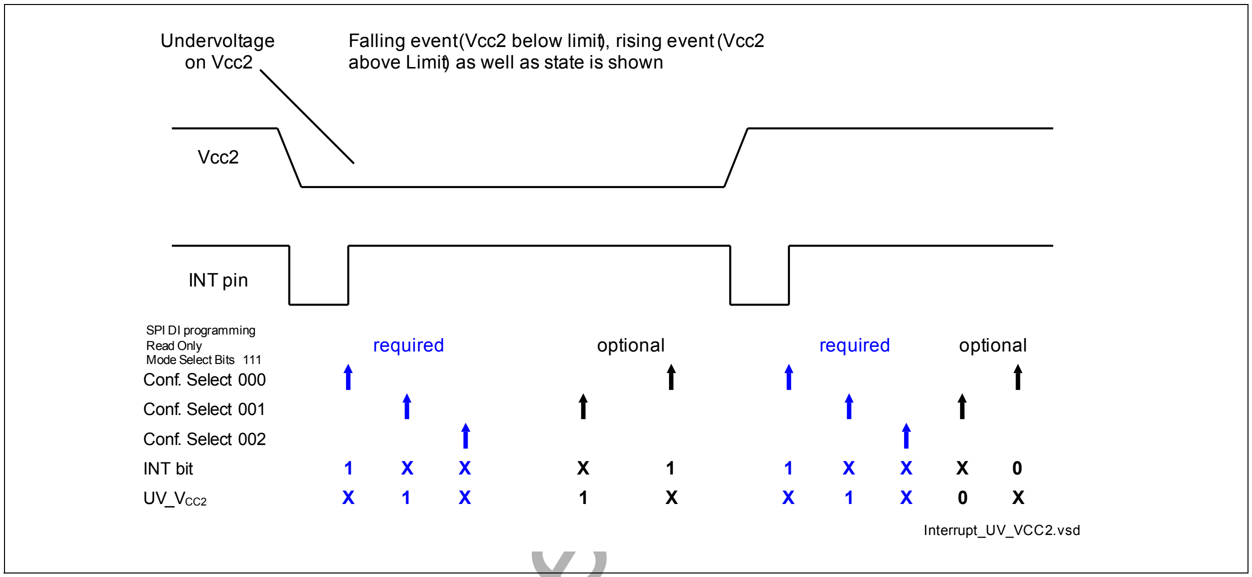


Figure 28 Interrupt V_{CC2} under-voltage.

The interrupt OT_Vcc2 that is generated by an over temperature on V_{CC2} is shown in **Figure 29**. The interrupt is sensitive on rising event and the interrupt bit also shows the state of the device and function.

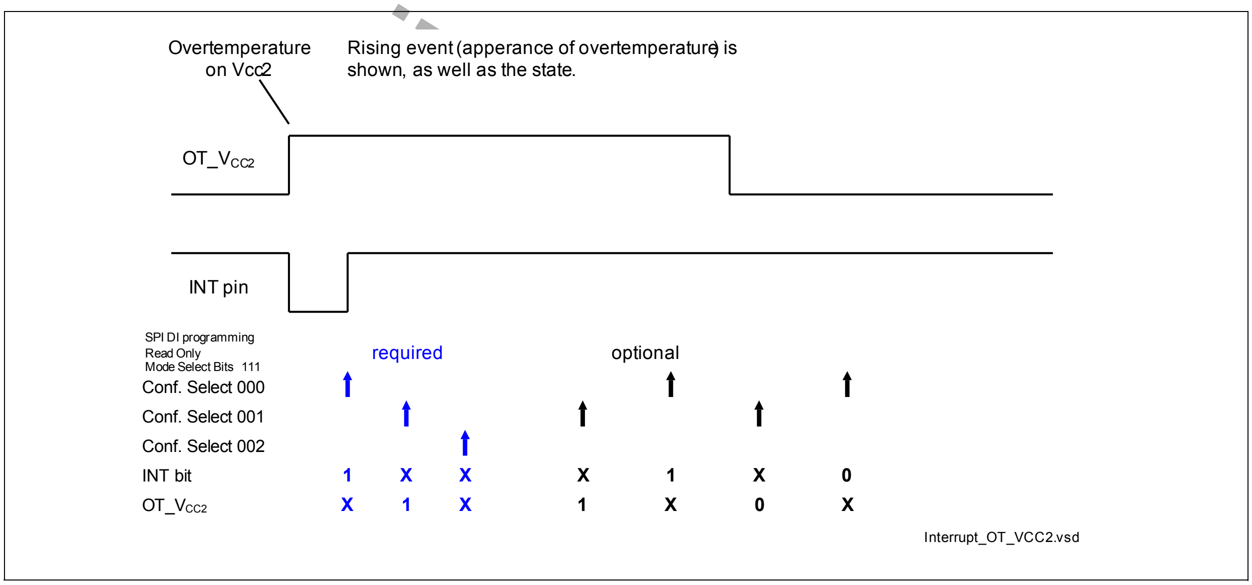


Figure 29 Interrupt Vcc2 Over Temperature.

12.2 Interrupt Timing

Figure 30 illustrates the interrupt timing. The INT output is set LOW as soon as an interrupt condition occurs. The INT pin is released after a SPI interrupt buffer read out command, that is performed with a Read Only command (111) to register (000). In case consecutive interrupt sources are indicated before the SPI read out, only one INT LOW will be raised but the SPI read out will indicate the interrupt sources. A time-out feature is implemented. The INT pin can be active LOW only for the time t_{INTTO}. Afterwards, the INT pin is released but the INT source is still valid or present in the SPI register. Between two activations of the INT, there is at least a delay of t_{INTTO}. If an interrupt occurs in the meantime, the information is stored and the INT will go LOW after t_{INTO}. The INT pulse width is at minimum t_{INT}.

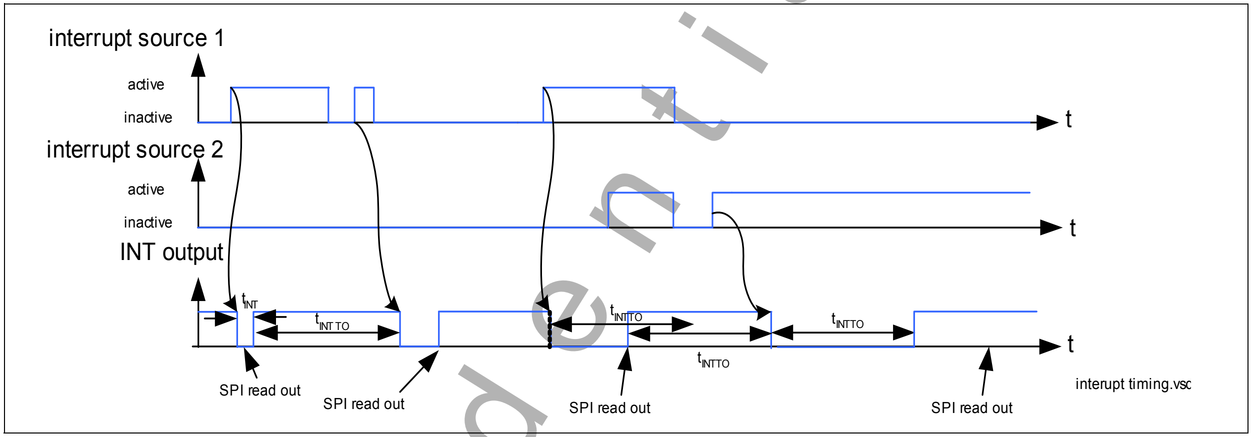


Figure 30 Interrupt Timing

12.3 Interrupt Modes with SBC Modes

The interrupt function is possible only in SBC Normal and Stop Mode.

After an SBC Restart Mode, all interrupt sources are enabled.

12.4 Interrupt Application Information

By default, all interrupt sources are activated. Please refer to the dedicated chapter for the definition of the interrupt.

The INT output is active for at least t_{INT}, even if the corresponding interrupt register is read out immediately after the interrupt event occurs.

If no SPI read is done after the interrupt is generated (INT pin low) the INT output becomes active (INT pin high) again after t_{INTTO}.

If two interrupt cases occur after each other and the SPI read (with read-only) is done after the second interrupt case, both interrupt bits are cleared. Although the interrupt bits for both interrupt cases are cleared the second interrupt will be issued by INT pin Low. This can lead to an interrupt where all interrupt bits are read as “0”.

12.5 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
Interrupt output; Pin INT							
12.5.1	Interrupt delay Time-out	t_{INTTO}	5.4	6	6.6	ms	–
12.5.2	INT pulse width	t_{INT}	10	–	–	µs	[1]
12.5.3	INT Low Output Voltage	V_{INTOL}	–	0.2	0.4	V	I_{INT} = 1 mA
12.5.4	INT High Output Voltage	V_{INTOH}	0.7 x $V_{\mathrm{CC1\mu C}}$	–	$V_{\mathrm{CC1\mu C}}$ + 0.3 V	V	I_{INT} = -20µA
12.5.5	INT Pull-up Resistor	R_{INT}	10	20	40	kΩ	V_{INT} = 0 V
Configuration select; Pin INT							
12.5.6	INT Config LOW input voltage	V_{CFGLO}	0.3 x $V_{\mathrm{cc1\mu C}}$	–	–	V	–
12.5.7	INT Config HIGH input voltage	V_{CFGHI}	–	–	0.7 x $V_{\mathrm{cc1\mu C}}$	V	–
12.5.8	INT Config pull down	R_{CFG}	–	250	–	kΩ	–

[1] Not subject to production test, specified by design.

13 Limp Home

13.1 Description

The Limp Home outputs are a very useful way to control safety critical functions independent of the microcontroller, such as turning on or off critical load during a microcontroller failure.

13.2 Limp Home output

The Limp Home output is an active LOW open drain transistor, please refer to **Figure 31**; therefore, it is necessary to connect at least an external pull-up resistor at.

The Limp Home output is activated due to a failure condition or via SPI, see **Chapter 13.3**. If V_s is below V_{LHUV}, the Limp Home cannot be activated and remains as a high impedance.

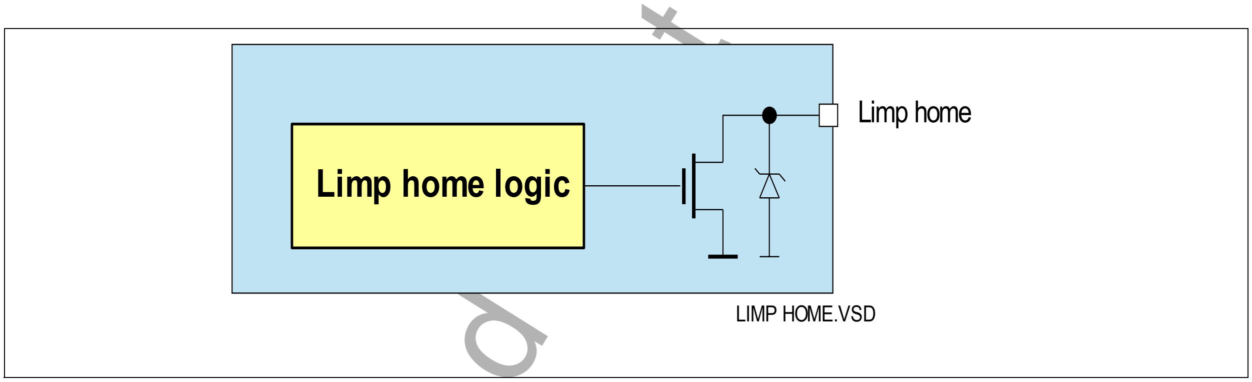


Figure 31 Limp Home block diagram

13.2.1 Limp Home side indicators output

The LH_SI output is similar to the Limp Home output. The output is pulsed to f_{LHSI} frequency with d_{SI} and designed to provide the side indicators frequency. The LH_SI function is active when the Limp Home is active.

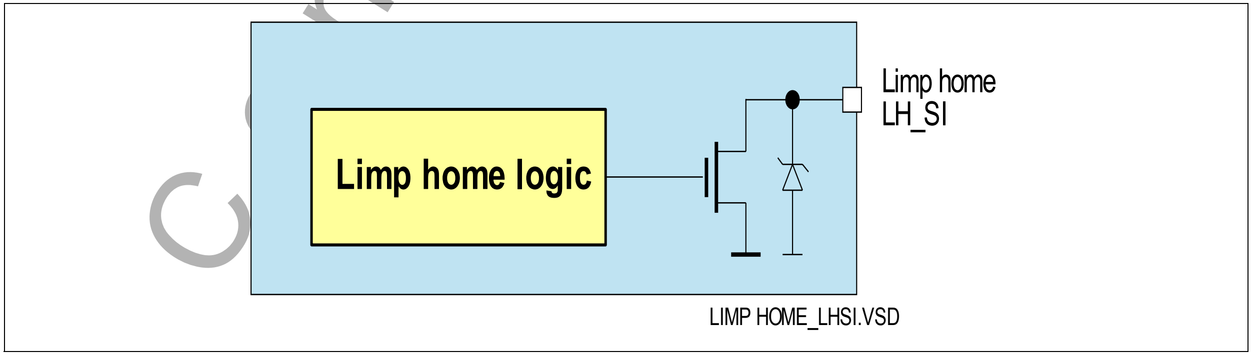


Figure 32 Limp Home LH_SI block diagram

13.2.2 LH_PL (Pulsed Light) output

The LH_PL/Test pin is an output pin shared with the Test pin function. During SBC Init Mode, the pin is used as an input, in all other modes, the pin is an output.

The output is pulsed to f_{LHPL} frequency with a duty cycle of d_{PL} (20% LOW, 80% high impedance), designed to dim the 27W stop lights into an 5W rear light. Refer to **Figure 33**. The LH_PL function is activated when the Limp Home is active. In SBC Init Mode, the LH_PL is inhibited, to avoid a wrong set of the SBC into SBC Software development Mode.

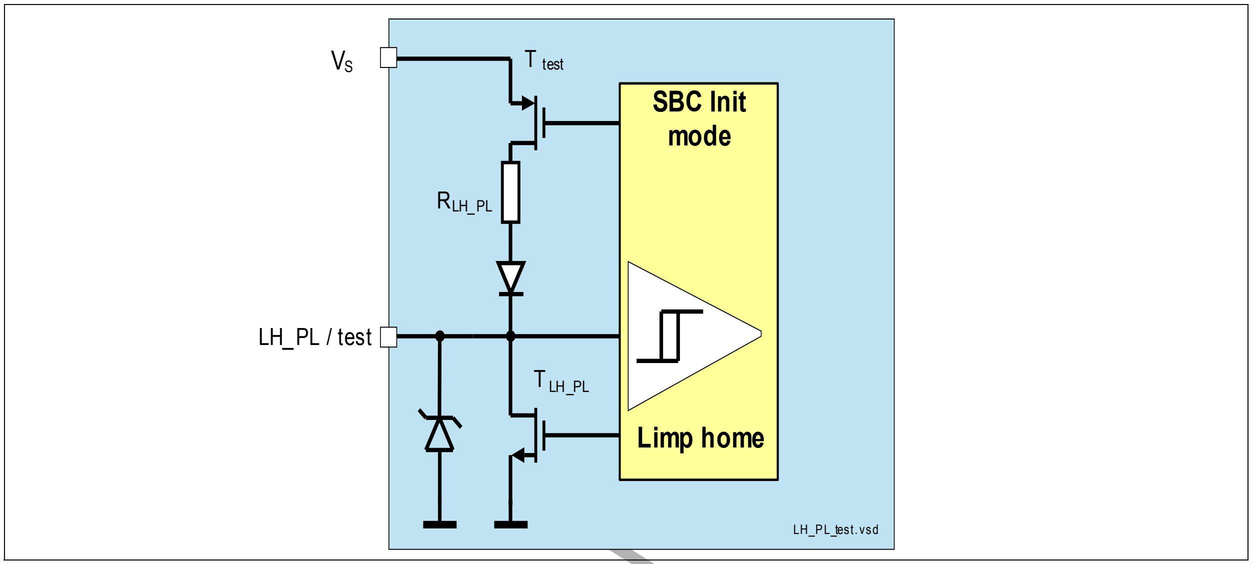


Figure 33 LH_PL/ Test block diagram

13.2.3 Test Pin

The Test pin is used to set the SBC chip into SBC Software Development Mode. When the Test pin is connected to GND, the SBC starts in SBC Software Development Mode. When the pin is left open, or connected to V_s the SBC starts into normal operation. Please refer to **Figure 3**. The LH_PL/Test pin has an integrated pull-up resistor (switched ON only during SBC Init Mode) to prevent the SBC device from starting in SBC Software Development Mode during normal life of the vehicle, as for example when the battery has been disconnected. To avoid disturbance, the Test pin is monitored during the Init Mode (from the time $V_S > V_{UVON}$ until Init Mode is left). If the pin is low for the Init Mode time, Software Development Mode is reached. The mode is stored during the complete time where V_S is above V_{UVOFF}. It means to leave Software Development Mode, the SBC must go back to SBC OFF mode.

13.3 Activation of the Limp Home Output

The reason to activate the Limp Home pins and the consequences are listed in **Table 12** and **Table 13**.

Table 12 Limp Home, Function of the SBC Mode

SBC Mode	Limp Home Outputs		
INIT Mode	OFF		
Normal Mode	OFF	ON via SPI	ON if it was ON until the successful Watchdog setting and deactivation via SPI.
Stop Mode	Unchanged		
Sleep Mode	Unchanged		
Restart Mode	Unchanged		
Fail-Safe Mode	ON		
SW Flash Mode	Unchanged		

Table 13 Automatic Activation of Limp Home Output

SBC Mode	Reason
INIT Mode	INIT time-out (t_{INITTO})
Normal Mode	1st Watchdog failure (config 1/2) 2nd Watchdog failure (config 3/4)
Restart Mode	Reset output permanent short circuit to $V_{cc1\mu C}$
	Reset output permanent short circuit to GND
	$V_{cc1\mu C}$ undervoltage time-out
Any mode	If previously turned ON in SBC Normal Mode, via SPI command
	$V_{cc1\mu C}$ thermal shutdown

13.4 Release of the Limp Home Output

When Limp Home is activated via SPI command, then it is released via SPI command. This is useful for diagnosis purpose for example.

Otherwise, the Limp Home outputs are released only in SBC Normal Mode with the following conditions: After the device has been set to SBC Restart Mode, automatically entering SBC Normal Mode, a successful Watchdog trigger must be sent via SPI. At this point, the Limp Home outputs remain active. Then the microcontroller needs to send by SPI command the deactivation of the Limp Home.

13.5 $V_{cc1\mu C}$ undervoltage time-out

A $V_{cc1\mu C}$ undervoltage time-out condition is given, when

1) the $V_{cc1\mu C}$ output voltage is below the reset threshold (V_{RT1}, V_{RT2}, V_{RT3}),

2) V_S is higher then the threshold (V_{SthUV1}, V_{SthUV2}, V_{SthUV3}) and

3) the condition is valid longer then the $V_{cc1\mu C}$ under voltage time-out ($t_{Vcc1UVTO}$).

A $V_{cc1\mu C}$ undervoltage time-out will sent the device into Fail-Safe Mode. Limp Home output stag will be activated (for $V_s > V_{LHUV}$)

Figure 34 gives an example of the Limp Home output activation, due to a $V_{cc1\mu C}$ undervoltage time-out.

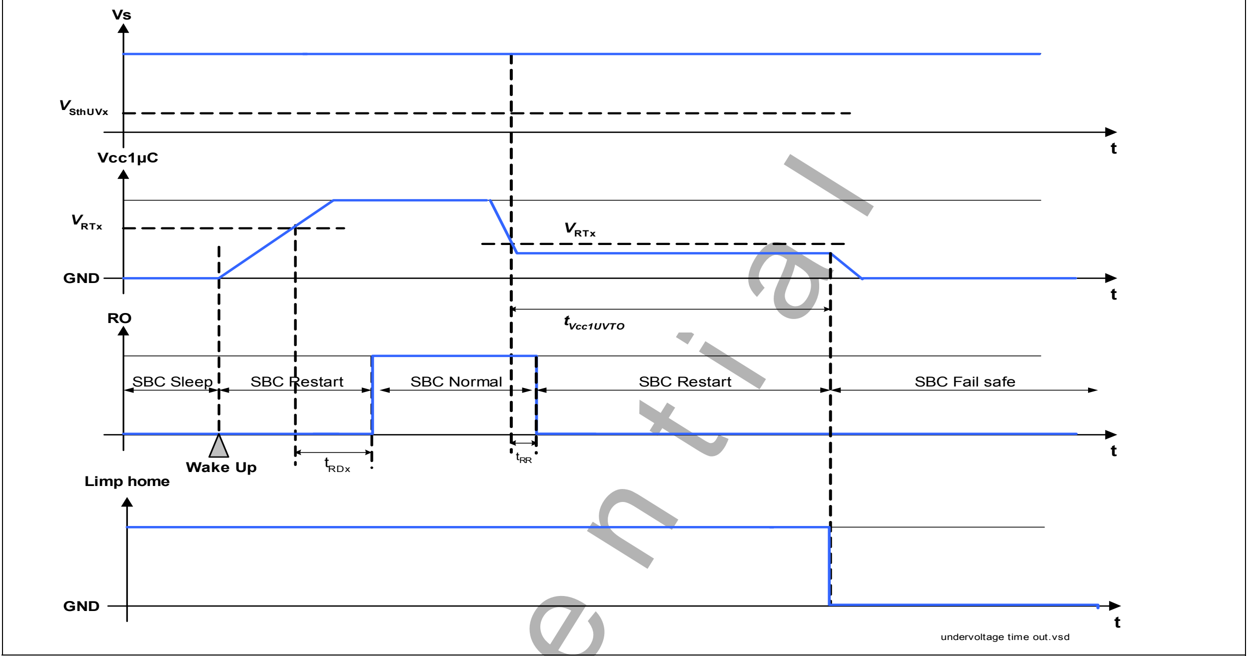


Figure 34 $V_{cc1\mu C}$ undervoltage time-out timing

13.6 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
Limp Home;							
13.6.1	Watchdog edge count difference to set Limp Home activated	n_{LH}	–	1 2	–	–	With SPI set. Default Setting
13.6.2	Limp Home low output voltage (active)	V_{LHLO}	–	0.2	0.4	V	I_{LH} = 1mA
13.6.3	Limp Home high output current (inactive)	I_{LHHI}	0	–	2	µA	V_{LH} = 28V
13.6.4	INIT Time-out	t_{INITTO}	–	256	–	ms	[1]
13.6.5	$V_{cc1\mu C}$ under voltage Time-out	$t_{Vcc1UVTO}$	900	1024	1150	ms	
13.6.6	V_s threshold for $V_{cc1\mu C}$ under voltage Time-out (V_s needs to be above, to activate $V_{cc1\mu C}$ under voltage Time-out)	V_{SthUV1}	5.3	–	6.3	V	V_{RT1} default setting
		V_{SthUV2}	4.3	–	5.3	V	V_{RT2} SPI option
		V_{SthUV3}	4.0	–	5.0	V	V_{RT3} SPI option
13.6.7	Threshold for Limp Home minimum V_s	V_{LHUV}	4.5	–	5.5	V	–
13.6.8	Limp Home V_s voltage hysteresis	$V_{LHUVhys}$	–	0.2	–	V	–
;							
13.6.9	Limp Home side indicator frequency	f_{LHSI}	1.125	1.25	1,375	Hz	–
13.6.10	Limp Home side indicator duty cycle	d_{SI}	–	50	–	%	–
LH_PL/Test							
13.6.11	HIGH Level Input Voltage Threshold	$V_{Test,HI}$	–	–	3	V	–
13.6.12	Input Hysteresis	$V_{Test,hys}$	100	300	700	mV	–
13.6.13	LOW Level Input Voltage Threshold	$V_{Test,LO}$	1	–	–	V	–
13.6.14	Pull-up Resistor	R_{Test}	20	40	80	kΩ	$V_{LH\_PL/Test}$ = 0V SBC Init Mode
13.6.15	Limp Home pulsed light frequency	f_{LH_PL}	90	100	110	Hz	–
13.6.16	Limp Home pulsed light duty cycle	d_{PL}	-	20	-	%	–

1) Not subject to production test, specified by design.

14 Configuration Select

14.1 Configuration select

The Configuration select is used to set the device for two different SBC behaviors; please refer to **Chapter 4.2.1** for detailed information. Depending on the requirements of the application, the $V_{cc1\mu C}$ is switched off and the device goes to Fail-Safe Mode in case of watchdog fail (1 or 2 fail) or reset clamped. To turn $V_{cc1\mu C}$ OFF (Config 2/4), the INT pin is not connected to a pull up resistor externally. In case the $V_{cc1\mu C}$ is not switched off (Config 1/3) the INT pin is connected to $V_{cc1\mu C}$ with a pull up resistor. The configuration is only read during Init Mode, after that the configuration is stored.

14.2 Config Hardware Descriptions

In Init Mode before the RO pin goes high the INT pin is pulled to low with a weak pull down resistor R_{CFG}, the pull up resistor R_{INT} is switched off. When $V_{cc1\mu C}$ is high, above the reset threshold V_{RT1} and before the RO pin goes high the level on the INT pin is monitored to select the configuration. With RO going high in Init Mode the pull up resistor R_{INT} is switched on.

Figure 35 gives the electrical equivalents to the configuration function of the INT pin.

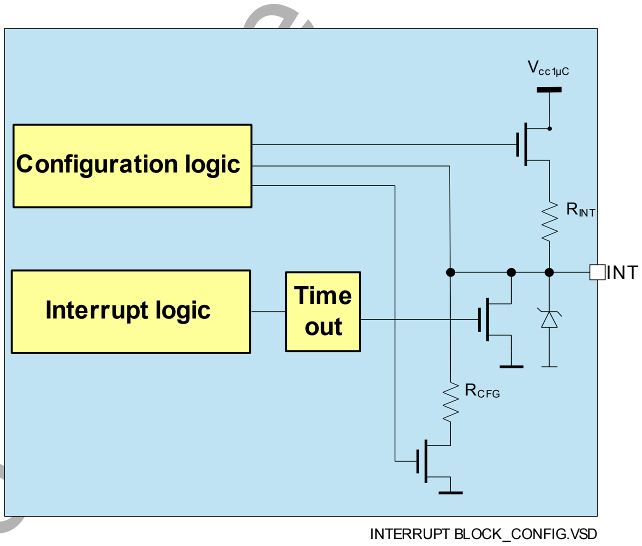


Figure 35 Config Logic Diagram

Electrical characteristics are listed in chapter **Chapter 12.5**

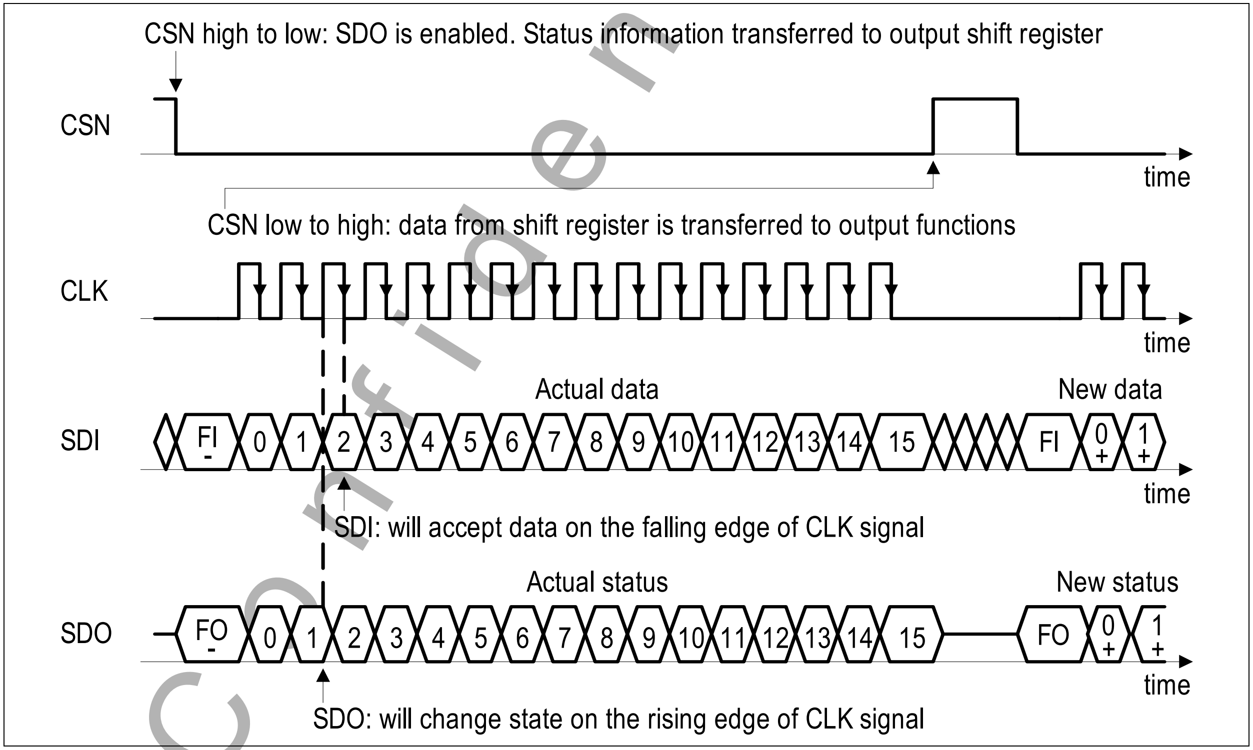
15 Serial Peripheral Interface

15.1 SPI Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK supplied by the microcontroller. The output word appears synchronously at the data output SDO (see **Figure 36**).

The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read in becomes the new control word. The SDO output switches to tri-state status (high impedance) at this point, thereby releasing the SDO bus for other use.

The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The number of received input clocks is supervised by a modulo-16 operation and the Input / Control Word is discarded in case of a mismatch. This error is flagged in the following SPI output by a “HIGH” at the data output (SDO pin, bit FO) before the first rising edge of the clock is received. The SPI of the SBC is not daisy chain capable.



CSN high to low: SDO is enabled. Status information transferred to output shift register

CSN low to high: data from shift register is transferred to output functions

SDI: will accept data on the falling edge of CLK signal

SDO: will change state on the rising edge of CLK signal

Figure 36 SPI Data Transfer Timing

15.2 Corrupted data in the SPI data input

When the microcontroller send a wrong SPI command to the SBC, the SBC ignores the information. Wrong SPI command can be either a number of bits different of 16, the mode selection (MS2..0) = 000 or requesting to go to an SBC mode which is not allowed by the state machine, for example from SBC Stop Mode to SBC SW Flash Mode. In that case, an interrupt is generated (if not inhibited) and the bit SPI Fail is set. Since the SPI data is corrupted, the next SPI output data will remain the former one (the information is then repeated).

15.3 SPI Input Data

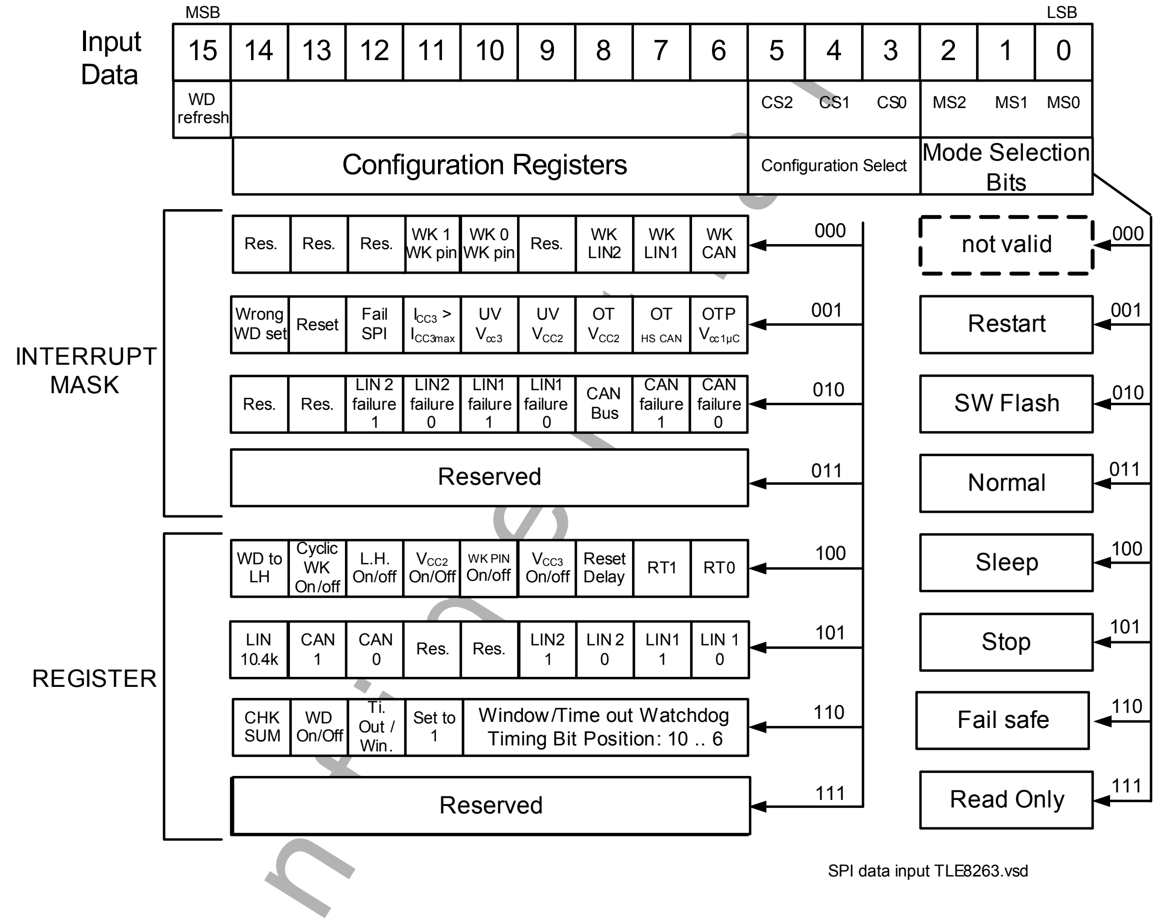


Figure 37 16-Bit SPI Input Data / Control Word

15.4 SPI Output Data

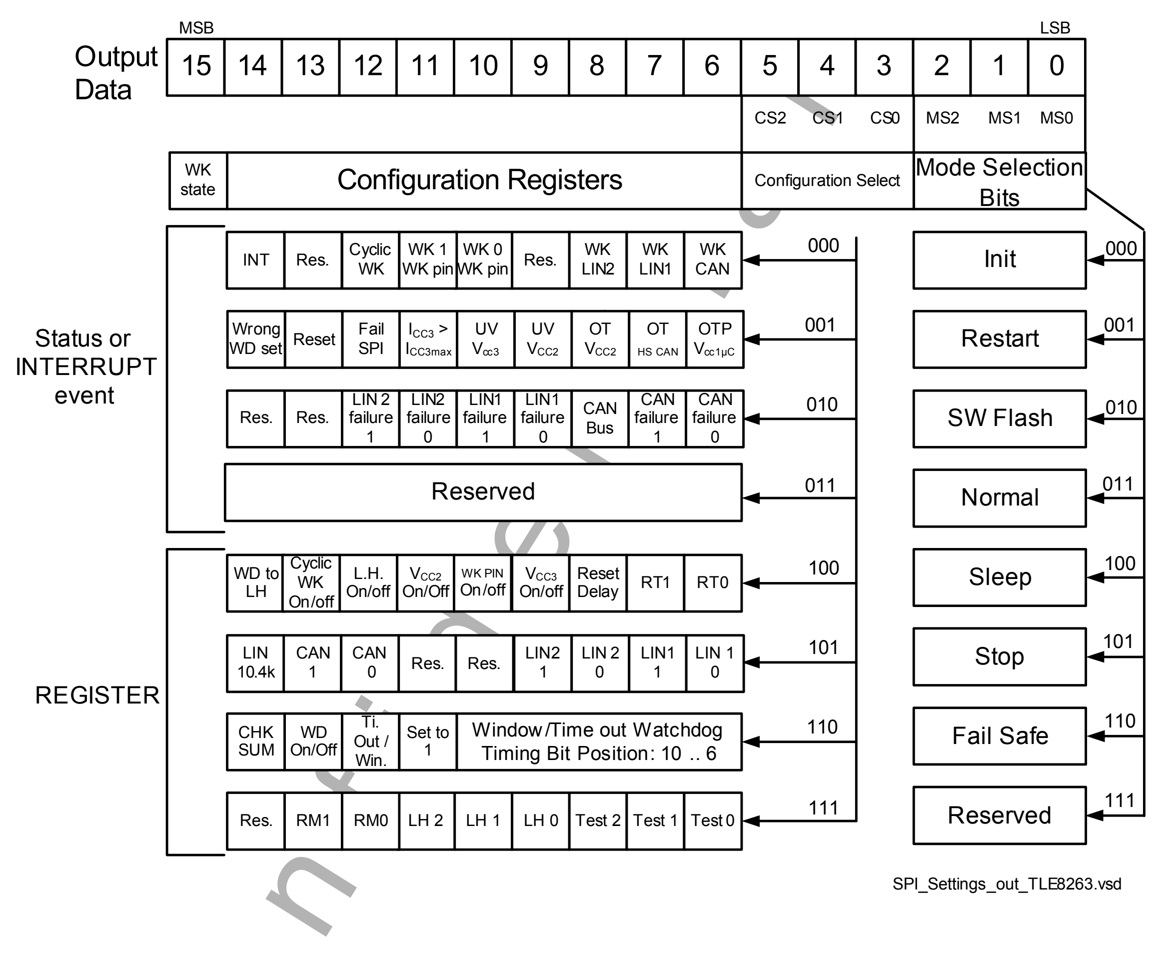


Figure 38 16-bit SPI Output Data / Control Word

15.5 SPI Data Encoding

15.5.1 WD Refresh bit / WK state

The WD Refresh bit is used to trigger the Watchdog. The first trigger should be a *1*, and then a *0*. For more details, please refer to **Chapter 11.2**.

The WK state bit gives the voltage level at the WK pin. A *1* indicates a high level, a *0* a low level.

15.5.2 SBC Configuration Setting and Read Out

15.5.2.1 Mode selection bits and configuration select

Table 14 lists the encoding of the possible SBC mode. Except SBC Restart and Init Mode which are most of time entered automatically, all others SBC mode are accessible on request of the microcontroller. The microcontroller should send the correct mode selection bits to set the SBC in the respective mode. The output indicates the SBC mode where the SBC currently is or was, depending on the situation.

Table 14 Mode Selection Bits

MS2	MS1	MS0	Data Input	Data Output
0	0	0	Not valid (the complete SPI word is ignored)	Show the device was in Init previous SPI data
0	0	1	Set the SBC to SBC Restart Mode. (In SW Flash mode only)	Show the device was in Restart previous SPI data
0	1	0	Set the SBC to Software Flash Mode	Show the device is SBC Software Flash Mode
0	1	1	Set the SBC to SBC Normal Mode	Show the device is in SBC Normal Mode
1	0	0	Set the SBC to SBC Sleep Mode	Show the device was in SBC Sleep Mode
1	0	1	Set the SBC to SBC Stop Mode	Show the device is in SBC Stop Mode
1	1	0	Set the SBC to SBC Fail-Safe Mode (In SBC Software Development mode only)	Show the device was in SBC Fail-Safe Mode
1	1	1	Set the SBC to Read Only SPI access. The configuration register needs to be selected. The SPI information on SDO is provided in the same SPI frame. No write access is done in this mode. Bit 15 (Watchdog) has to be served correctly.	Reserved

Table 15 lists the eight possible configuration selection. Some are related to event or state of the different part of the SBC, others are used to configure the SBC in the application specific set up.

Table 15 Configuration Select Encoder (for Data Input and Output)

CS2	CS1	CS0	Configuration Register Select
0	0	0	Wake Register Interrupt
0	0	1	SBC Failure Interrupt
0	1	0	Communication Failure Interrupt
0	1	1	Reserved
1	0	0	SBC Configuration Register
1	0	1	Communication Setup Register
1	1	0	Watchdog Configuration Register
1	1	1	Limp Home / Diagnosis Register

15.5.2.2 Interrupt Register Encoder

Table 16 lists all interrupts the SBC can generates. The microcontroller should read the correct register to release the INT pin. By default, all interrupt sources are enabled. The microcontroller can decide to inhibit a specific interrupt source.

Table 16 Interrupt Register encoder [1)]

CS	Bit Name	Default Value (INPUT)	Default Value (OUT)	Data Input	Data Output
Configuration select 000 (Wake register interrupt)					
000	WK CAN	1	0	Interrupt enabled (1) disabled (0) for wake event on CAN	Wake on CAN (1)
	WKLINx	1	0	Interrupt enabled (1) disabled (0) for wake event on LIN	Wake on LINx (1)
	WK 1 WK pin WK 0 WK pin	11	00	Interrupt enabled (1) disabled (0) for wake pin event. 00 No interrupt 10 Interrupt for a LOW to HIGH transition on WK 01 Interrupt for HIGH to LOW transition on WK 11 Interrupt for both HIGH to LOW and LOW to HIGH on WK	Wake on WK pin 00 No wake 10 Interrupt for a LOW to HIGH transition on WK 01 Interrupt for HIGH to LOW transition on WK 11 Interrupt for both HIGH to LOW and LOW to HIGH on WK
	Cyclic WK	n.a	0	n.a	Cyclic WK (1)
	INT	n.a	0	n.a	Indicates that there is a status bit or uncleared event in configuration select 001 and/or 010. If set read the two register

Table 16 Interrupt Register encoder (cont'd)[1]

CS	Bit Name	Default Value (INPUT)	Default Value (OUT)	Data Input	Data Output
Configuration select 001 (SBC Failure interrupt)					
001	OTP_$V_{cc1\mu C}$	1	0	Interrupt enabled (1) disabled (0) for temperature pre-warning	$V_{cc1\mu C}$ temperature pre warning (1)
	OT_HSCAN	1	0	Interrupt enabled (1) disabled (0) for temperature shutdown	HS CAN temperature shutdown (1)
	OT_V_{cc2}	1	0	Interrupt enabled (1) disabled (0) for temperature shutdown	V_{cc2} temperature shutdown (1)
	UV_V_{cc3}	1	0	Interrupt enabled (1) disabled (0) for undervoltage detection or due to back to normal voltage	Undervoltage detection on Vcc3 (1)
	SPI Fail	1	0	Interrupt enabled (1) disabled (0) for SPI corrupted data.	SPI input corrupted data (1)
	Reset	1	0	Interrupt enabled (1) disabled (0) for reset information (only in SBC Software Development Mode)	Reset (1) (only in SBC Software Development Mode)
	Wrong WD set	1	0	Interrupt enabled (1) disabled (0) for incorrect Watchdog setting	Incorrect WD programming for data output
	UV V_{cc2}	1	0	Interrupt enabled (1) disabled (0) for undervoltage detection at V_{cc2}	Under voltage detected at V_{cc2}
	$I_{CC3} > I_{CC3max}$	1	0	Interrupt enable (1) disabled (0) for over current at V_{cc3}	Over current detected at V_{cc3}
Configuration select 010 (Communication failure interrupt)					
010	CAN failure 1 CAN failure 0	n.a 1	0 0	Interrupt enabled (1) disabled (0) for CAN failure	CAN failure Refer to **Table 17**
	CAN Bus	1	0	Interrupt enabled (1) disabled (0) for CAN bus failure	CAN bus failure detected (1)
	LINx failure 1 LINx failure 0	n.a 1	0 0	Interrupt enabled (1) disabled (0) for LIN failure	LIN failure. Refer to **Table 17**

---

1) A value of 0 will set the SBC into the opposite state.

15.5.2.3 CAN / LIN failure encoder

Table 17 describes the encoding of the possible internal CAN and LIN failures.

Table 17 CAN / LIN Failure Encoder

CAN / LINx 1 Failure	CAN / LINx 0 Failure	Fault
0	0	No failure
0	1	TxD shorted to GND or bus dominant clamped
1	0	RxD shorted to V_{cc}
1	1	TxD shorted to RxD

15.5.2.4 Configuration encoder

Table 18 lists the configuration register of the SBC. The microcontroller can change the settings. If no settings are changed the default values are used. The current value can be read on the SPI Data Out.

Table 18 Configuration Encoder

Configuration Select	Bit Name	Default Value (INPUT)	Default Value (OUT)	State
Configuration select 100 (SBC Configuration Register)				
100	RT10	01	01	Reset threshold setting. Please refer to **Table 19**
	Reset delay	1	1	Long reset window
	V_{cc3} ON /OFF	0	0	V_{cc3} is activated (1)
	WK pin ON / OFF	1	1	The wake pin will wake the SBC
	V_{cc2} On / Off	0	0	V_{cc2} is activated (1)
	LH ON / OFF	0	0	Limp Home output state. Activated (1) when entry condition is met.
	Cyclic WK On / Off	0	0	Activation (1) of the cyclic wake
	WD to LH	1	1	Watchdog failure to Limp Home active. 0 = only one Watchdog failure brings to Limp Home activated. 1 = two consecutive Watchdog failures bring to Limp Home activated.

Table 18 Configuration Encoder

Configuration Select	Bit Name	Default Value (INPUT)	Default Value (OUT)	State
Configuration select 101 (SBC communication set up register)				
101	LIN 10.4k	1	1	LIN cells are in LIN Low slope Mode (1)
	CAN 1.0	00	00	The CAN cell is in: 00 = CAN OFF 01 = CAN is Wake Capable 10 = CAN Receive Only Mode 11 = CAN Normal Mode
	LINx 1.0	00	00	The LIN cell is in: 00 = LIN OFF 01 = LIN is Wake Capable 10 = LIN Receive Only Mode 11 = LIN Normal Mode
Configuration select 110 (SBC Watchdog register)				
110	Ti. Out / Win.	1	1	Time-out Watchdog is activated
	Set to 1	1	1	Bit is reserved and fix set to “1”. Set to 1 in SW.
	WD ON / OFF	1	1	Watchdog is activated
	CHK SUM	1	1	Check sum of the bit 13...6 In case the CHK SUM is wrong, the device remains in previous valid state. $\text{CHKSUM} = \text{Bit13} \oplus \ldots \oplus \text{Bit6}$
Configuration select 111 (Limp Home / Diagnosis register)				
111	-			Reserved for input For output, refer to **Table 21**, **Table 22** and **Table 23**

15.5.2.5 Reset encoder

Table 19 lists the three possible reset thresholds. Please also refer to **Chapter 11.3** to get the exact voltage threshold.

Table 19 Reset Encoder

RT1	RT0	Threshold Selected
0	0	Not Valid. Device remains at previous threshold
0	1	VRT1 (default setting at SBC Init),
1	0	VRT2
1	1	VRT3

15.5.2.6 SBC Watchdog encoder

Table 20 list the 32 possible watchdog timer.

Table 20 Watchdog Encoder

Bit 10...6	Decimal	calculation (ms)	Timer (ms)
00000	0	(n+1) × 16 n = decimal value of setting	16
00001	1		32
00010	2		48
...	...		...
01111	15		256 (default setting)
10000	16	n × 48 - 464	304
10001	17		352
...	...		...
11110	30		976
11111	31		1024

15.5.3 SBC Diagnostic encoder

The SBC offers diagnostics information. The encoding of the different possible failures are listed in the following table. The description apply only to data output.

15.5.3.1 Reason for restart and reset

Reason for reset, without activation of the Limp Home and the way it is encoded are summed up in **Table 21**. The bits are cleared by reading the register with Read-Only command. When coming from Sleep Mode or Fail Safe Mode the bits are cleared.

Table 21 Reason to Enter SBC Restart Mode without Limp HomeLimp Home activation

RM1	RM0	Cause for entering SBC Restart Mode
0	0	No reset has occurred or Limp Home activated
0	1	Undervoltage on $V_{cc1\mu C}$
1	0	First Watchdog failure (config 3 and 4) or no acknowledge of the Cyclic Wake-up
1	1	SPI command in SBC Software Flash Mode or reset low from outside

15.5.3.2 Limp Home failure encoder

Table 22 describes the encoding of all possible reason to activate automatically the Limp Home output. Bits are set back to “000” when switching Limp Home off via SPI.

Table 22 Limp Home Failure Diagnosis

LH2	LH1	LH0	Failure[1]
0	0	0	No failure
0	0	1	$V_{cc1\mu C}$ undervoltage Time-out
0	1	0	One Watchdog failure (config 1 and 2)
0	1	1	Two consecutive Watchdog failures (config 3 and 4)
1	0	0	INIT Mode Time-out
1	0	1	Temperature shutdown at $V_{cc1\mu C}$
1	1	0	Reset clamped
1	1	1	Reserved

15.5.3.3 Test pin and failure to Limp Home configuration read out

The SBC allows to read the hardware setting of the configuration that is done via the INT pin, as well as the test pin and the WD to LH bit. **Table 23** describes the encoding of these informations.

Table 23 Test pin and SBC Configuration

Test2	Test1	Test0	Test Read Out[1]
0	0	0	$V_{cc1\mu C}$ remains ON in SBC Restart Mode after one Watchdog failure (config 1)
0	0	1	$V_{cc1\mu C}$ is OFF in SBC Fail-Safe Mode after one Watchdog failure (config 2)
0	1	0	$V_{cc1\mu C}$ remains ON in SBC Restart Mode after two Watchdog failures (config 3)
0	1	1	$V_{cc1\mu C}$ is OFF in SBC Fail-Safe Mode after two Watchdog failures (config 4)
1	0	0	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.
1	0	1	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.
1	1	0	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.
1	1	1	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.

[1] Refer also to **Chapter 4.2.1**

15.6 SPI Output Data

15.6.1 First SPI output data

Since the SPI output data is sent when the SBC is receiving data, the output data are dependent of the previous SPI command, if no Read Only command is used. Under some conditions there is no “previous command”. **Table 24** gives the first SPI output data that is sent to the microcontroller when entering SBC Normal Mode, depending on the mode where the SBC was before receiving the first SPI command.

Table 24 First SPI output data frame

Previous SBC mode	Mode selection bits (MS2...0)	Configuration select (CS 2..0)
Sleep mode	Sleep mode	Wake Register interrupt(1)
Fail-Safe mode	Fail-Safe mode	Limp Home register(1)
Restart mode when failure and config 1 / 3	Restart mode	Limp Home register(1)
Restart mode when microcontroller has sent to Restart mode	Restart mode	SBC Configuration Register
SBC Init mode	Init mode	SBC Configuration Register

1) This does not clear the bits. It will be reset when the microcontroller requests the read out

15.6.2 Read Only command

In the Mode Selection Bits a Read Only can be selected. The Read Only access clears the INT bits that are selected in the Configuration Select (some interrupt bits show a state, and can not be cleared with a SPI read). With this SPI command no write access is done to the SBC, and the mode of the SBC is not changed. The watchdog can also be triggered with a Read Only command.

The Read Only command delivers the information requested with the Configuration Select in the same SPI command on the SDO pin. As all other SPI commands deliver the requested information with the next SPI command.

Figure 39 shows an example of a Read Only access. The bits are shown with LSB first, on the left side in difference to the register description.

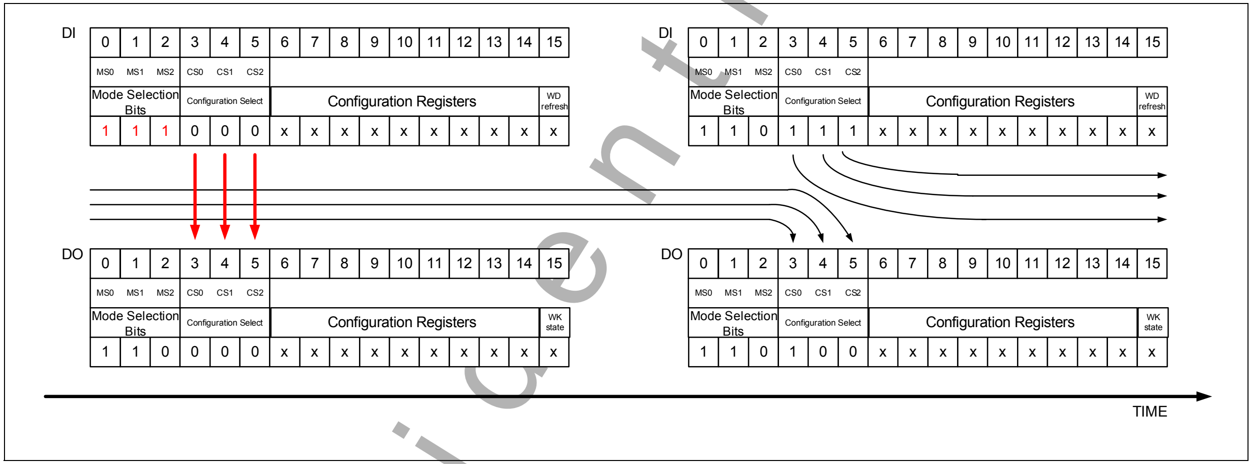


Figure 39 Read Only Command

Figure 40 shows an example of an SPI write access in normal mode for comparison. The requested information is sent out with the next SPI command.

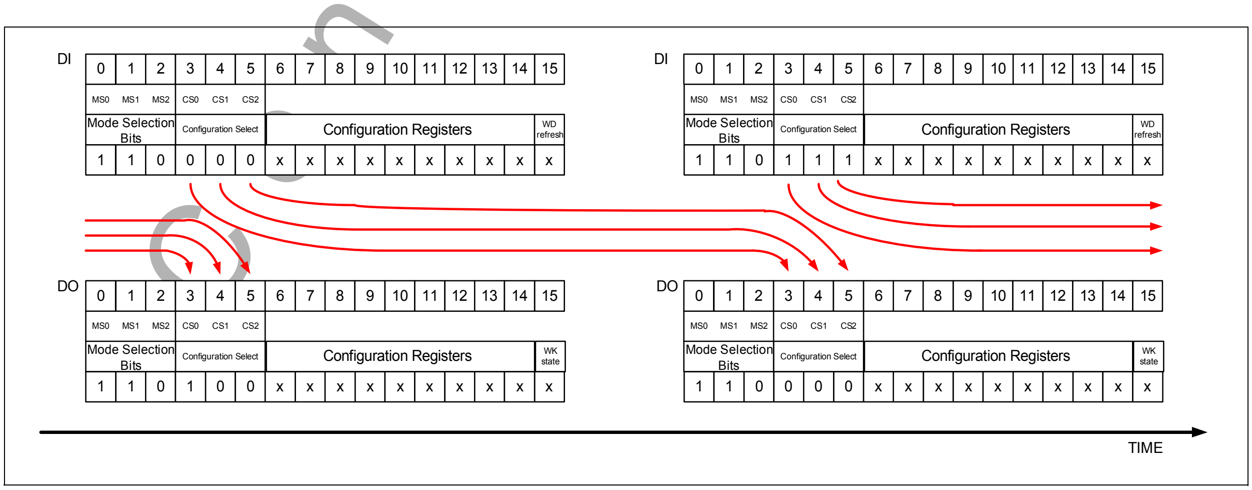


Figure 40 Write Command

15.7 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
SPI Interface; Logic Inputs SDI, CLK and CSN							
15.7.1	H-input Voltage Threshold	V_{IH}	–	–	0.7 x $V_{\mathrm{CC1\mu C}}$	V	–
15.7.2	L-input Voltage Threshold	V_{IL}	0.3 x $V_{\mathrm{CC1\mu C}}$	–	–	V	–
15.7.3	Hysteresis of input Voltage	V_{IHY}		0.12 x $V_{\mathrm{CC1\mu C}}$		V	–1)
15.7.4	Pull-up Resistance at pin CSN	R_{ICSN}	20	40	80	kΩ	$V_{\mathrm{CSN}} = 0.7 \times V_{\mathrm{CC1\mu C}}$
15.7.5	Pull-down Resistance at pin SDI and CLK	$R_{\mathrm{ICLK/SDI}}$	20	40	80	kΩ	$V_{\mathrm{SDI/CLK}} = 0.2 \times V_{\mathrm{CC1\mu C}}$
15.7.6	Input Capacitance at pin CSN, SDI or CLK	C_{I}	–	10	-	pF	-1)
Logic Output SDO							
15.7.7	H-output Voltage Level	V_{SDOH}	$V_{\mathrm{CC1\mu C}}$ - 0.4	$V_{\mathrm{CC1\mu C}}$ - 0.2	–	V	I_{DOH} = -1.6 mA
15.7.8	L-output Voltage Level	V_{SDOL}	–	0.2	0.4	V	I_{DOL} = 1.6 mA
15.7.9	Tri-state Leakage Current	I_{SDOLK}	-10	–	10	µA	$V_{\mathrm{CSN}} = V_{\mathrm{CC1\mu C}}$; 0 V < V_{DO} < V_{CC1}
15.7.10	Tri-state Input Capacitance	C_{SDO}	–	10	15	pF	1)
Data Input Timing1)							
15.7.11	Clock Period	t_{pCLK}	250	–	–	ns	–
15.7.12	Clock High Time	t_{CLKH}	125	–	–	ns	–
15.7.13	Clock Low Time	t_{CLKL}	125	–	–	ns	–
15.7.14	Clock Low before CSN Low	t_{bef}	125	–	–	ns	–
15.7.15	CSN Setup Time	t_{lead}	250	–	–	ns	–
15.7.16	CLK Setup Time	t_{lag}	250	–	–	ns	–
15.7.17	Clock Low after CSN High	t_{beh}	125	–	–	ns	–
15.7.18	SDI Set-up Time	t_{DISU}	100	–	–	ns	–
15.7.19	SDI Hold Time	t_{DIHO}	50	–	–	ns	–

15.7 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
15.7.20	Input Signal Rise Time at pin SDI, CLK and CSN	t_{rIN}	–	–	50	ns	–
15.7.21	Input Signal Fall Time at pin SDI, CLK and CSN	t_{fIN}	–	–	50	ns	–
15.7.22	Delay Time for Mode Change from Normal Mode to Sleep Mode	t_{fIN}	–	–	10	µs	–
15.7.23	CSN High Time	$t_{CSN(high)}$	10	–	–	µs	-
Data Output Timing 1)							
15.7.24	SDO Rise Time	t_{rSDO}	–	30	80	ns	C_L = 100 pF
15.7.25	SDO Fall Time	t_{fSDO}	–	30	80	ns	C_L = 100 pF
15.7.26	SDO Enable Time	t_{ENSDO}	–	–	50	ns	low impedance
15.7.27	SDO Disable Time	t_{DISSDO}	–	–	50	ns	high impedance
15.7.28	SDO Valid Time	t_{VASDO}	–	–	60	ns	C_L = 100 pF

1) Not subject to production test; specified by design

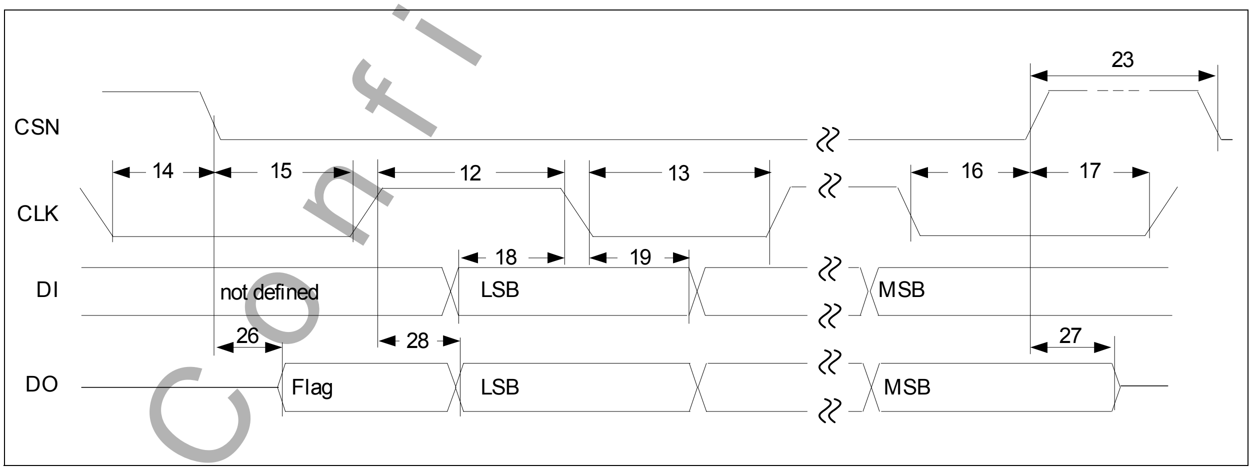


Figure 41 SPI Timing Diagram

Note: Numbers in drawing correlate to the last 2 digits of the Pos. number in the Electrical Characteristics table.

16 Application Information

Note: The following information is given only as a hint for the implementation of the device and should not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

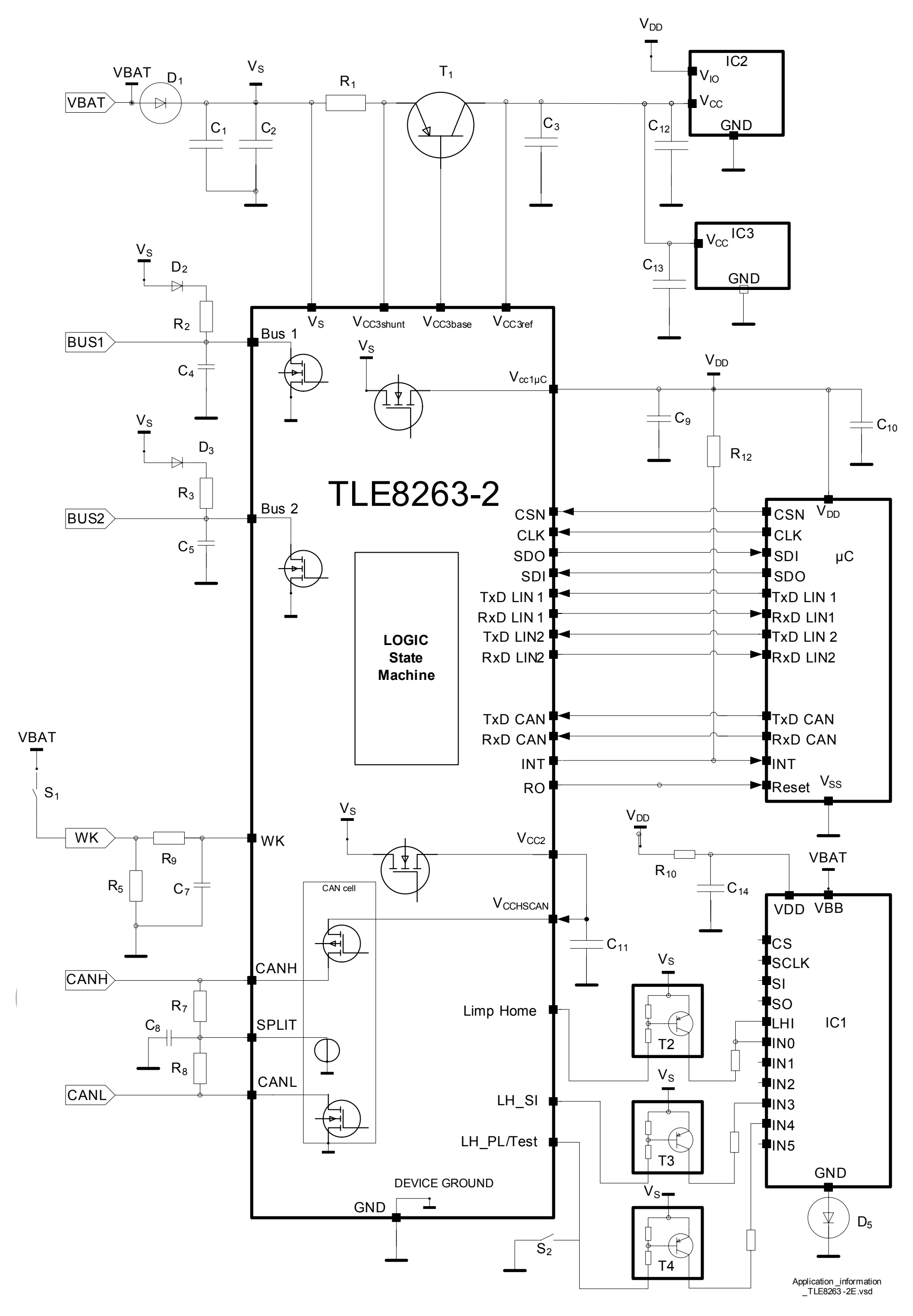


Figure 42 Application Example for a Body Controller Module

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

Table 25 Bills of material

Ref.	Option	Vendor	Value	Purpose
Capacitance				
C1	Y	Kemet	68µF optional depending on application	Cut off battery spike
C2	Y		100nF	EMC
C3	N	Murata	10µF ceramic cap low ESR	Stability of the V_{CC3}
C4	N		1nF OEM dependent	LIN Master Termination
C5	N		1nF OEM dependent	LIN Master Termination
C7	Y		22nF 50V	EMC
C8	Y		47nF OEM dependent	Improve SPLIT pin stability
C9	Y		10µF	Buffer of the $V_{CC1µC}$ depending on load. (µC)
C10	N		100nF	Stability of the $V_{CC1µC}$
C11	N		10µF CAN transceiver dependent	Buffering of the V_{CC2} for CAN Transceiver
C12	Y		100nF	Improve stability of the logic
C13	Y		100nF	Improve stability of the logic
C14	Y		100nF	Improve stability of the logic
Resistance				
R1	N		220mΩ	V_{CC3} current measurement for I_{CC3} 400mA max
R2	Y		1kΩ / OEM dependent	LIN master termination
R3	Y		1kΩ / OEM dependent	LIN master termination
R5	Y		1kΩ	Wetting current of the switch
R7	Y		60Ω / OEM dependent	CAN bus termination
R8	Y		60Ω / OEM dependent	CAN bus termination
R9	Y		10kΩ	Limit the WK pin current in ISO pulses
R10	Y		500Ω	Insulation of the VDD supply
R12	Y		47kΩ	Set config 1/3. If not connected config 2/4 is selected

Table 25 Bills of material

Ref.	Option	Vendor	Value	Purpose
Active components				
T1	N	ON Semi	MJD253	Power element of V_{CC3}
		Infineon	BCP52-16	Alternative power element of $V_{CC3,}$ current limit to be adapted R1 to be changed.
T2	N	Infineon	BCR191W	High active Limp Home
T3	N	Infineon	BCR191W	High active Limp Home
T4	N	Infineon	BCR191W	High active Limp Home
D1	N	Infineon	BAS 3010A	Reverse polarity protection
D2	N	Infineon	BAS70 06 (dual) BAS70 (single)	Requested by LIN norm. Protect the application in reverse polarity.
D3	N	Infineon	BAS70 06 (dual) BAS70 (single)	Requested by LIN norm. Protect the application in reverse polarity.
µC	N	Infineon	XC2xxx	micro-controller
IC1	Y	Infineon	SPOC - BTS5672E	high side switches
IC2	Y	Infineon	TLE 6254-3G	Low speed CAN
IC3	Y	Infineon	TLE 6251DS	High speed CAN

16.1 ZthJA Curve

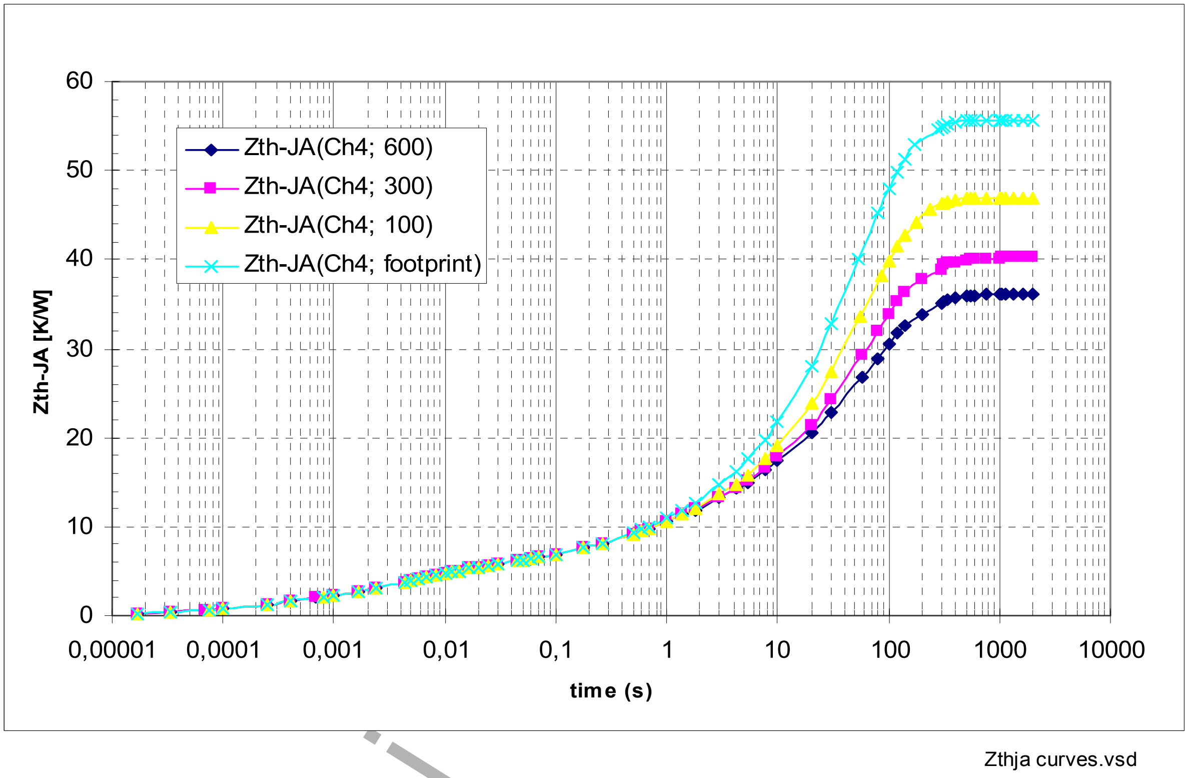


Figure 43 ZthJA Curve, Function of Cooling Area

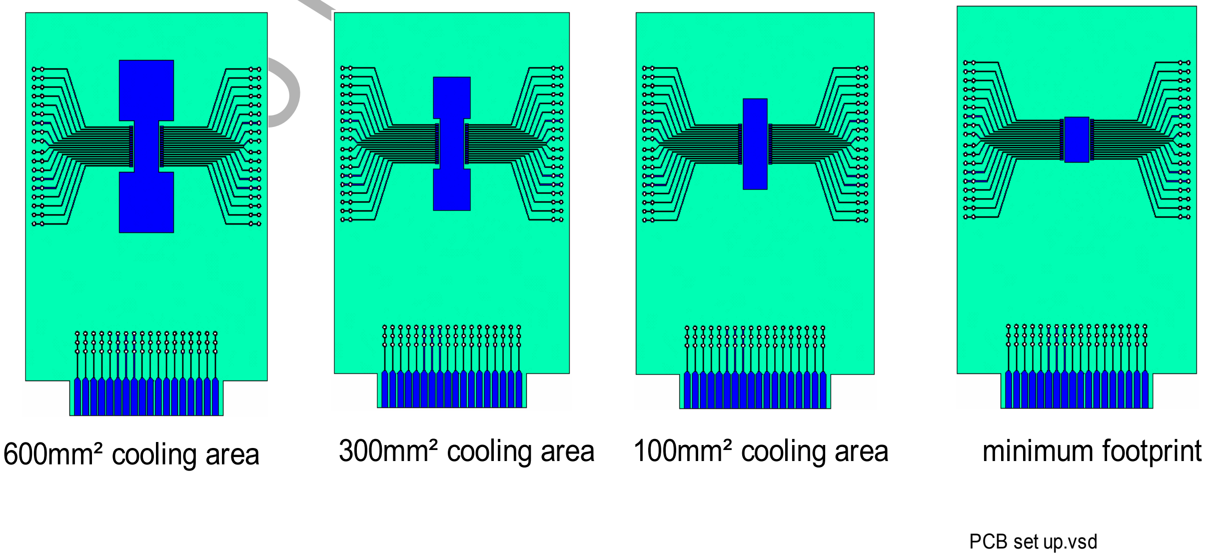


Figure 44 Board Set-up

Board set-up is done according to JESD 51-3, single layer FR4 PCB 70 µm.

16.2 Hints for SBC Factory Flash Mode

The mode is used during production of the module to flash the µC. The idea is that the µC is not supplied from the SBC but from an external 5V power supply. The reset of the µC that is connected to the RO pin of the SBC can be driven from an external source and the SBC does not give a reset signal. Also no interrupt at the pin INT and no signal on the SPI SDO pin is generated by the SBC. The SPI pins can be driven externally.

The mode is reached by applying 5V to the $V_{CC1\mu C}$ pin and no voltage to the Vs pin. The Vs pin will show a voltage of about 4.5V because of the internal diode from $V_{CC1\mu C}$ to V_s. The current drawn at Vs must not exceed the maximum rating of $I_{vs,max}$ = -500mA. The function is designed for ambient temperature.

In case the V_s was supplied before going to FF Mode, the voltage on pin V_s must be set below 3 V before applying 5V to $V_{CC1\mu C}$ (discharging the C)

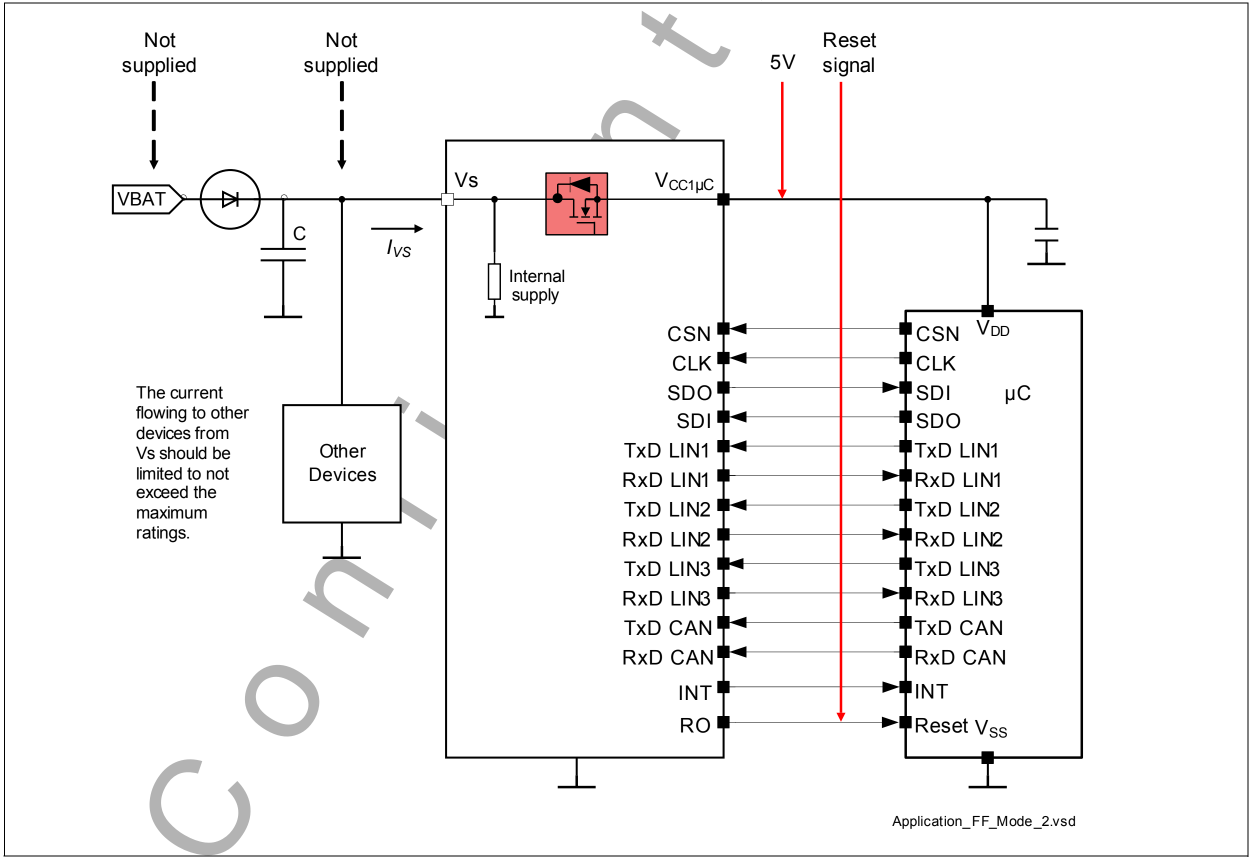


Figure 45 Application Hint for Factor Flash Mode

Table 26 PIN in Factory Flash Mode

Pin	Level	Comment
Vs	typ. 4.5V	Voltage output from SBC. No voltage applied from external.
Vcc1µC	5V ± 2%	To be applied from external
RO	Pull-up resistor	Can be driven from external
INT	Pull-up resistor	Can be driven from external if required
LH	High impedance	Can be driven from external if required
SDO	High impedance	Can be driven from external if required
CLK, SDI	Pull-down resistor	Can be driven from external if required
CSN	Pull-up resistor	Can be driven from external if required
TxDCAN, TxDLIN1, TxDLIN2, TxDLIN3	Pull-up resistor	Can be driven from external if required
RxDCAN, RxDLIN1, RxDLIN2, RxDLIN3	High impedance	Can be driven from external if required

16.3 ESD Tests

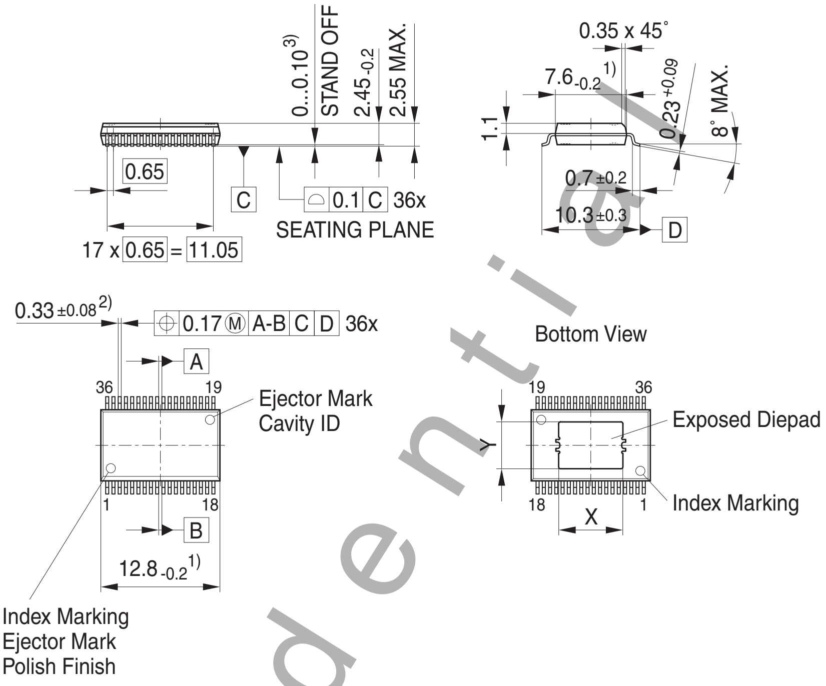
Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) have been performed. The results and test condition is available in a test report. The values for the test are listed in **Table 27** below.

Table 27 ESD “Gun test”

Performed Test	Result	Unit	Remarks
ESD at pin CANH, CANL, BUSx, Vs versus GND	> 8	kV	positive pulse[1]
ESD at pin CANH, CANL, BUSx, Vs versus GND	< -8	kV	negative pulse

[1] ESD susceptibility “ESD GUN” contact discharge (R=330Ohm C=150pF) (DIN EN 61000-4-2) tested according LIN EMC 1.3 Test Specification and ICT EMC Evaluation of CAN Transceiver. Tested by external test house (IBEE Zwickau, EMC Test report Nr. 06-02-09a)

17 Package Outline



Exposed Diepad Dimensions 4)

Package	Leadframe	X	Y
PG-DSO-36-24, -41, -42	A6901-C001	7	5.1
PG-DSO-36-38	A6901-C003	7	5.1
PG-DSO-36-38	A6901-C007	5.2	4.6
PG-DSO-36-24	A6901-C008	6.0	5.4

1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side
3) Distance from leads bottom (= seating plane) to exposed diepad
4) Excluding the mold flash allowance of 0.3mm MAX per side

PG-DSO-36-24, -38, -41, -42-PO V08

Figure 46 PG-DSO-36-38 (Leadframe A6901-003);)

Note: For the SBC product family the package PG-DSO-36-38 with the leadframe A6901-C003 is used.

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the Universal System Basis Chip is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For information about packages and types of packing, refer to the Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

18 Revision History

Version	Date	Parameter	Changes
1.0	2009-02-06		First Rev. after Preliminary Data Sheet
1.0	2009-03-31		Editorial changes

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