

# TLE8261-2E

Universal System Basis Chip  
HERMES  
Rev. 1.0

Automotive Power



Never stop thinking

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## 1 HERMES Overview

### Scalable System Basis Chip Family

- Eight products for complete scalable application coverage
- Complete compatibility (hardware and software) across the family
- TLE8264-2E (3LIN), TLE8263-2E (2LIN) - 3 Limp Home outputs
- TLE8264E (3LIN), TLE8263E (2LIN) - 1 Limp Home output
- TLE8262-2E (1LIN), TLE8261-2E (no LIN) - 3 Limp Home outputs
- TLE8262E (1LIN), TLE8261E (no LIN) - 1 Limp Home output

### Basic Features

- Very low quiescent current in Stop and Sleep Modes
- Reset input, output
- Power on and scalable undervoltage reset generator
- Standard 16-bit SPI interface
- Overtemperature and short circuit protection
- Short circuit proof to GND and battery
- One universal wake-up input
- Wide input voltage and temperature range
- Cyclic wake in Stop Mode
- Green Product (RoHS compliant)
- AEC Qualified

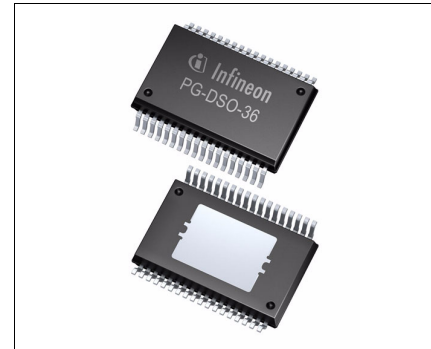
### Description

The devices of the SBC family are monolithic integrated circuits in an enhanced power package with identical software functionality and hardware features except for the number of LIN cells. The devices are designed for CAN-LIN automotive applications e.g. body controller, gateway applications.

To support these applications, the System Basis Chip (SBC) provides the main functions, such as HS-CAN transceiver for data transmission, low dropout voltage regulators (LDO) for an external 5 V supply, and a 16-bit Serial Peripheral Interface (SPI) to control and monitor the device. Also implemented are a Time-out or a Window Watchdog circuit with a reset feature, Limp Home circuitry output, and an undervoltage reset feature.

The devices offer low power modes in order to support application that are connected permanent to the battery. A wake-up from the low power mode is possible via a message on the buses or via the bi-level sensitive monitoring/wake-up input as well as from the SPI command. Each wake-up source can be inhibited.

The device is designed to withstand the severe conditions of automotive applications.



PG-DSO-36-38

Type	Package	Marking
TLE8261-2E	PG-DSO-36-38	TLE8261-2E

### HS CAN Transceiver

- Compliant to ISO 11898-2 and 11898-5 as well as SAE J2284
- CAN data transmission rate up to 1 Mbaud
- Supplied by dedicated input  $V_{ccHSCAN}$
- Low power mode management
- Bus wake-up capability via CAN message
- Excellent EMC performance (very high immunity and very low emission)
- Bus pins are short circuit proof to ground and battery voltage
- 8 kV ESD gun test on CANH / CANL / SPLIT
- Bus failure detection

### Voltage Regulators

- Low-dropout voltage regulator
- $V_{cc1\mu C}$ , 200 mA, 5 V  $\pm 2\%$  for external devices, such as microcontroller and RF receiver
- $V_{cc2}$ , 200 mA, 5 V  $\pm 2\%$  for external devices or the internal HS CAN cell
- $V_{cc3}$ , current limitation by shunt resistor (up to 400 mA with 220 m $\Omega$  shunt resistor), 5 V  $\pm 4\%$  with external PNP transistor; for example: to supply additional external CAN transceivers
- $V_{cc1\mu C}$ , undervoltage Time-out

### Supervision

- Reset output with integrated pull-up resistor
- Time-out or Window Watchdog, SPI configured
- Watchdog Timer from 16 ms to 1024 ms
- Check sum bit for Watchdog configuration
- Reset due to Watchdog failure can be inhibited with Test pin (SBC SW Development Mode)

### Interrupt Management

- Complete enabling / disabling of interrupt sources
- Timing filter mechanism to avoid multiple / infinite Interrupt signals

### Limp Home

- Open drain Limp Home outputs
- Dedicated internal logic supply
- Maximum safety architecture for Safety Operation Mode
- Configurable Fail-Safe behavior
- Dedicated side indicators signal 1.25Hz 50% duty cycle
- Dedicated PWM signal 100Hz 20% duty cycle

## 2 Block Diagram

The simplified block diagram illustrates only the basic elements of the SBC devices. Please refer to the information for each device in the product family for more specific hardware configurations.

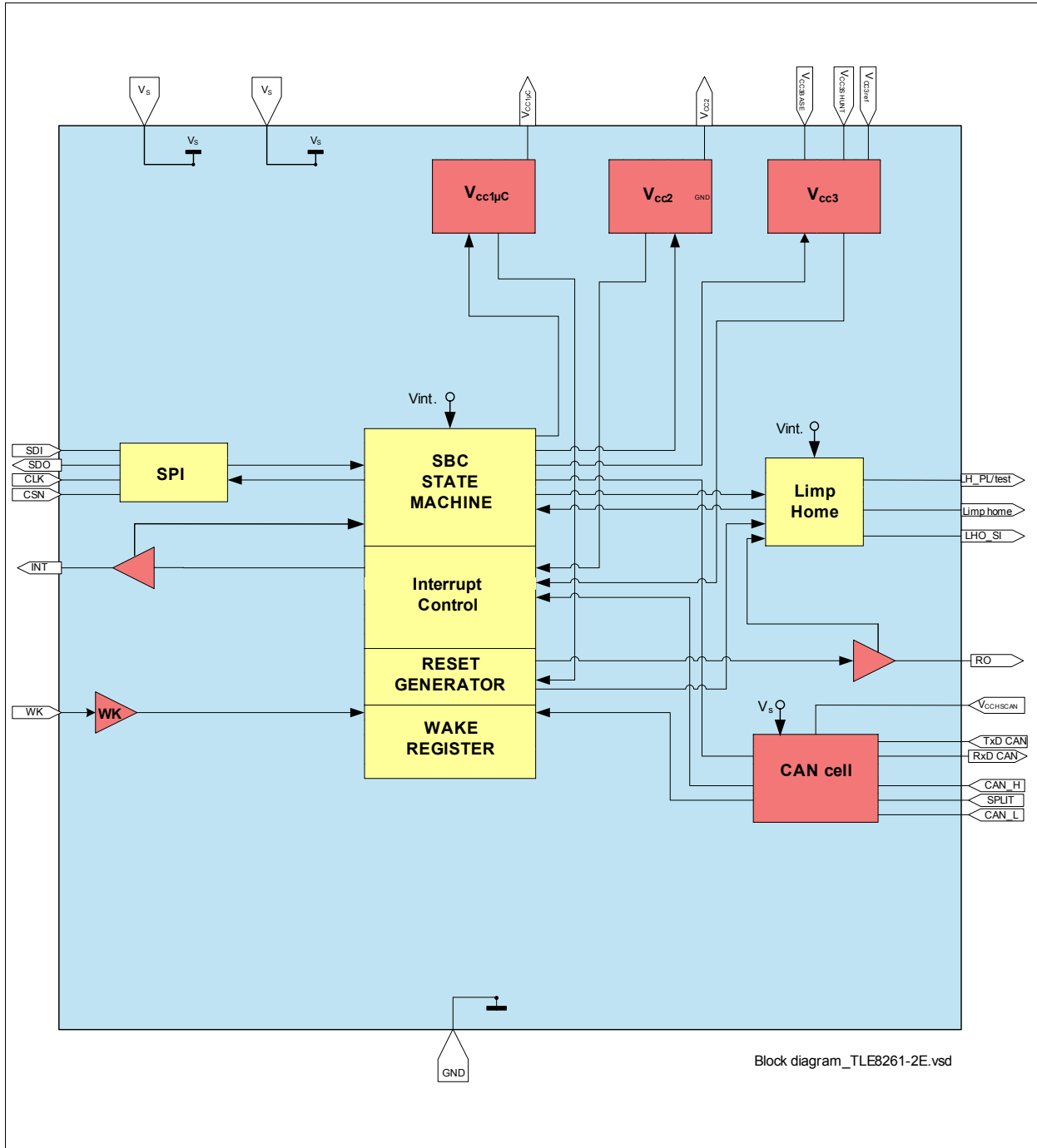


Figure 1 Simplified Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignments

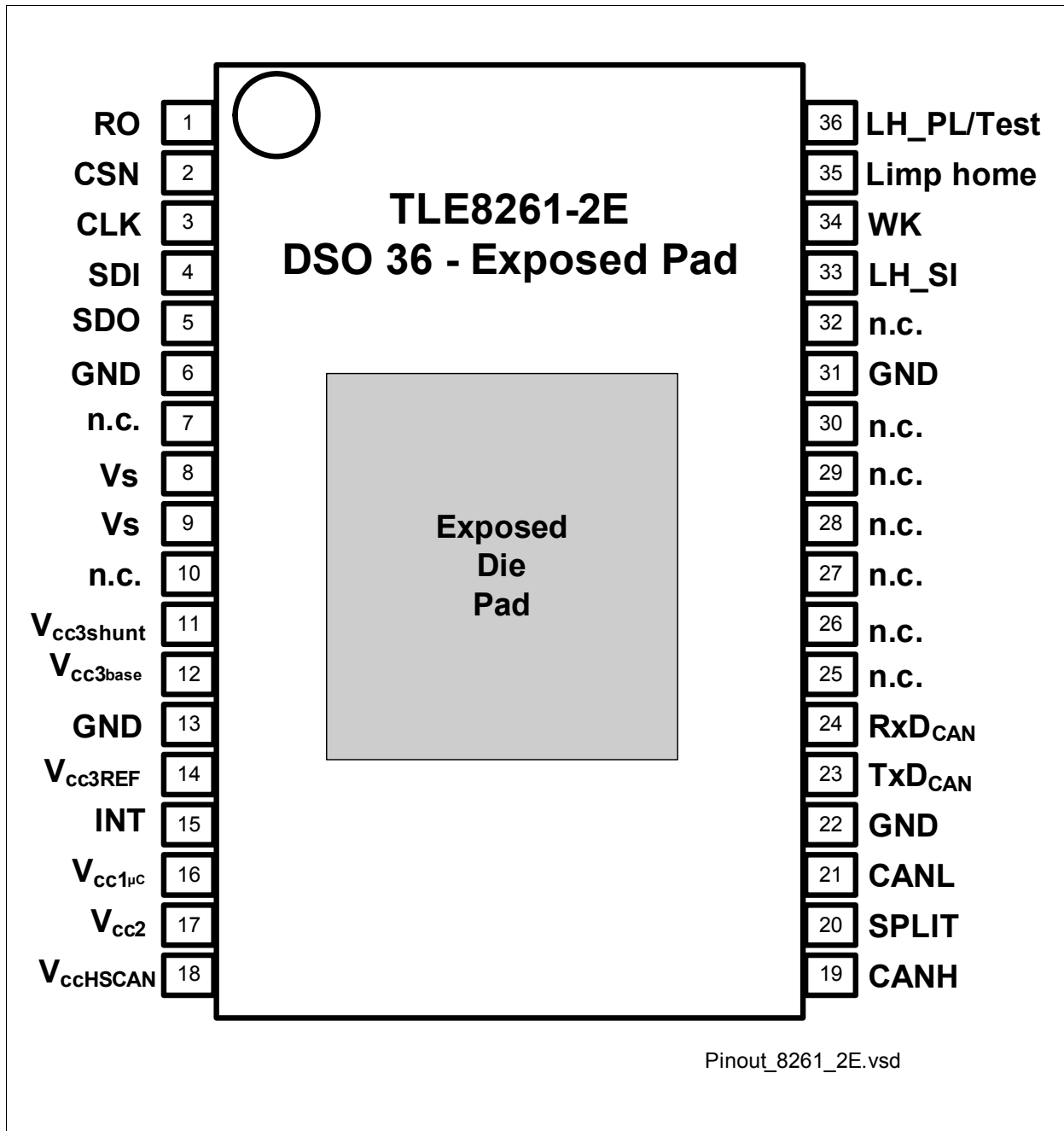


Figure 2 Pin Configuration

### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	RO	<b>Reset Input/Output</b> ; open drain output, integrated pull-up resistor; active low.
2	CSN	<b>SPI Chip Select Not Input</b> ; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should be set to low only when CLK is low; CSN has an internal pull-up resistor and requires CMOS logic level inputs.
3	CLK	<b>SPI Clock Input</b> ; clock input for shift register; CLK has an internal pull-down resistor and requires CMOS logic level inputs.
4	SDI	<b>SPI Data Input</b> ; receives serial data from the control device; serial data transmitted to SDI is a 16-bit control word with the Least Significant Bit (LSB) transferred first; the input has a pull-down resistor and requires CMOS logic level inputs; SDI will accept data on the falling edge of the CLK signal.
5	SDO	<b>SPI Data Output</b> ; this tri-state output transfers diagnostic data to the control device; the output will remain tri-stated unless the device is selected by a low on Chip Select Not (CSN).
6	GND	<b>Ground</b>
7	n.c.	<b>Not connected</b>
8	$V_s$	<b>Power Supply Input</b> ; block to GND directly at the IC with ceramic capacitor. Ensure to have no current flow from PIN8 to PIN9. PIN8 and PIN9 can be directly connected.
9	$V_s$	<b>Power Supply Input</b> ; block to GND directly at the IC with ceramic capacitor. Ensure to have no current flow from PIN8 to PIN9. PIN8 and PIN9 can be directly connected.
10	n.c.	<b>Not connected</b>
11	$V_{cc3\ shunt}$	<b>PNP Shunt</b> ; External PNP emitter voltage.
12	$V_{cc3\ base}$	<b>PNP Base</b> ; External PNP base voltage.
13	GND	<b>Ground</b>
14	$V_{cc3REF}$	External PNP Output Voltage
15	INT	<b>Interrupt Output, configuration Input</b> ; used as wake-up flag from SBC Stop Mode and indicating failures. Active low. Integrated pull up. During start-up used to set the SBC configuration. External Pull-up sets config 1/3, no external Pull-up sets config 2/4.
16	$V_{cc1\ \mu c}$	<b>Voltage Regulator Output</b> ; 5 V supply; to stabilize block to GND with an external capacitor.
17	$V_{cc2}$	<b>Voltage Regulator Output</b> ; 5 V supply; to stabilize block to GND with an external capacitor.
18	$V_{ccHSCAN}$	<b>Supply Input</b> ; for the internal HS CAN cell.
19	CANH	<b>CAN High Line</b> ; High in dominant state.
20	SPLIT	<b>Termination Output</b> ; to support recessive voltage level of the bus lines.
21	CANL	<b>CAN Low Line</b> ; Low in dominant state.
22	GND	<b>Ground</b>
23	$TxD_{CAN}$	<b>CAN Transmit Data Input</b> ; integrated pull-up resistor.
24	$RxD_{CAN}$	<b>CAN Receive Data Output</b>
25	n.c.	<b>Not connected</b>
26	n.c.	<b>Not connected</b>



**Pin Configuration**

Pin	Symbol	Function
27	n.c.	<b>Not connected</b>
28	n.c.	<b>Not connected</b>
29	n.c.	<b>Not connected</b>
30	n.c.	<b>Not connected</b>
31	GND	<b>Ground</b>
32	n.c.	<b>Not connected</b>
33	LH_SI	<b>Limp Home side indicator</b> ; Side indicators 1.25Hz 50% duty cycle output; Open drain. Active LOW.
34	WK	<b>Monitoring / Wake-Up Input</b> ; bi-level sensitive input used to monitor signals coming from, for example, an external switch panel; also used as wake-up input;
35	Limp Home	<b>Fail-Safe Function Output</b> ; Open drain. Active LOW.
36	LH_PL/Test	<b>SBC SW Development Mode entry</b> ; Connect to GND for activation; Integrated pull-up resistor. Connect to $V_S$ or leave open for normal operation. <b>Limp Home Pulsed Light output</b> : Brake/rear light 100Hz 20% duty cycle output; Open drain. Active LOW.
EDP	-	<b>Exposed Die Pad</b> ; For cooling purposes only, do not use it as an electrical ground. <sup>1)</sup>

- 1) The exposed die pad at the bottom of the package allows better dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC and can be left floating or it can be connected to GND for the best EMC performance.

## 4 State Machine

### 4.1 Block Description

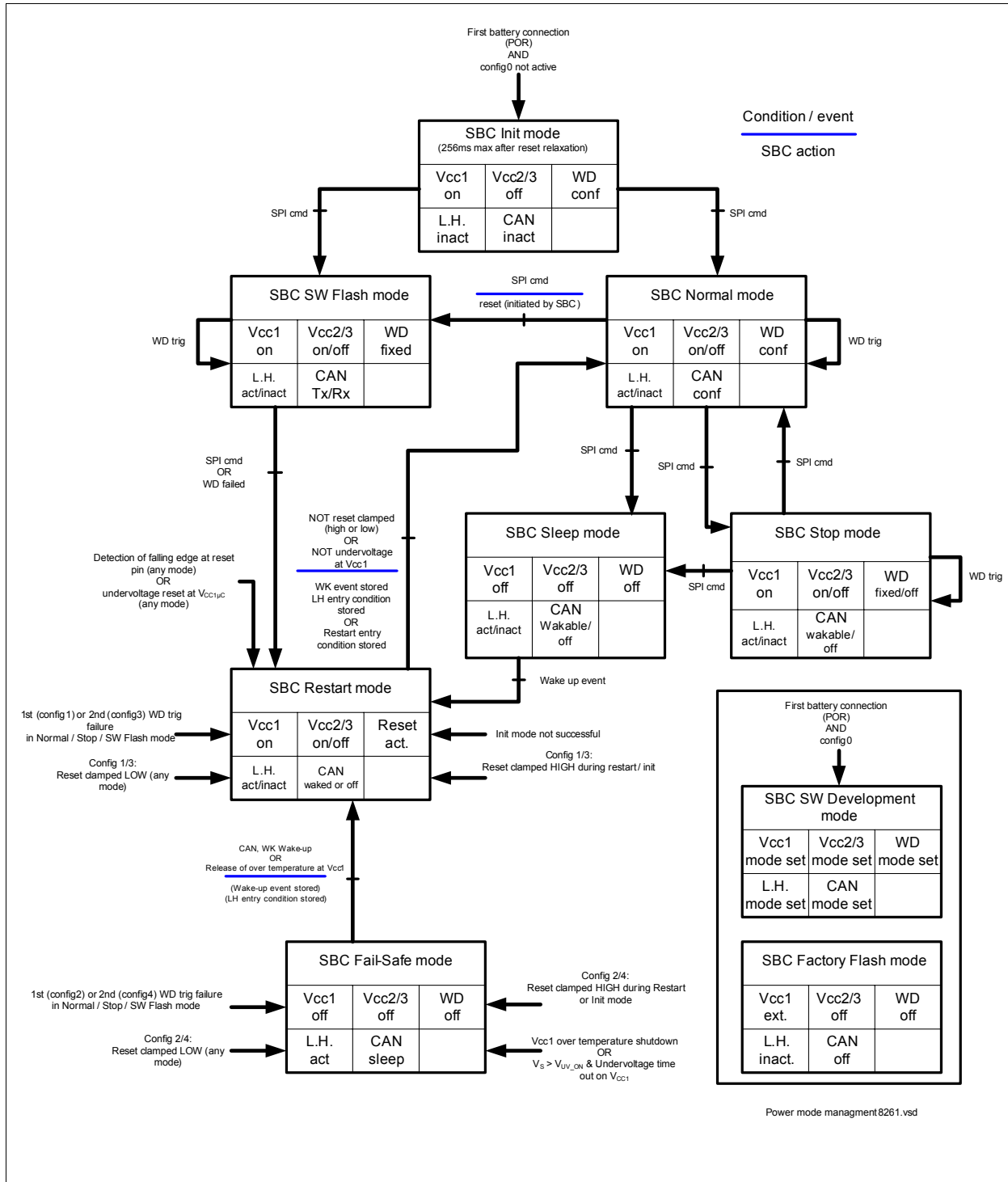


Figure 3 Power Mode Management

## 4.2 State Machine Description

The System Basis Chip (SBC) offers ten operating modes: Power On Reset, Init, Normal, Restart, Software Flash, Sleep, Stop, Fail-Safe, Software Development, and Factory Flash Mode. The modes are controlled with one test pin and via three mode select bits MS2..0, within the SPI. Additionally, the SBC allows five configurations, accessed via two external pins and one SPI bit.

### 4.2.1 Configuration Description

**Table 1** provides descriptions and conditions for entry to the different configurations of the SBC.

**Table 1 SBC Configuration**

Configuration	Description	Test pin	INT Pin	WD to LH bit
config 0	Software Development Mode	0V	n.a	n.a
config 1	After missing the WD trigger for the first time, the state of $V_{cc1\mu C}$ remain unchanged, LH pin is active, SBC in Restart Mode	Open / $V_S$	External pull-up	0
config 2	After missing the WD trigger for the first time, $V_{cc1\mu C}$ turns OFF, LH pin is active, SBC in Fail-Safe Mode		No ext. pull-up	0
config 3	After missing the WD trigger for the second time, the state of $V_{cc1\mu C}$ remain unchanged, LH pin is active, SBC in Restart Mode		External pull-up	1
config 4	After missing the WD trigger for the second time, $V_{cc1\mu C}$ turns OFF, LH pin is active, SBC in Fail-Safe Mode		No ext. pull-up	1

In SBC SW Development Mode, Config 1 to 4 are accessible.

### 4.2.2 SBC Power ON Reset (POR)

At  $V_S > V_{UVON}$ , the SBC starts to operate, by reading the test pin and then by turning ON  $V_{cc1\mu C}$ . When  $V_{cc1\mu C}$  reaches the reset threshold  $V_{RT1}$ , the reset output remains activated for  $t_{RD1}$  and the SBC enters then the Init Mode.

In the event that  $V_S$  decreases below  $V_{UVOFF}$ , the device is completely disabled. For more details on the disable behavior of the SBC blocks, please refer to the chapter specific to each block.

### 4.2.3 SBC Init Mode

At entering the SBC Init Mode, the SBC starts to read the Test pin. The SBC starts-up in SBC Init Mode, and, after powering-up, waits for the microcontroller to finish its startup and initialization sequences.  $V_{cc2/3}$  are OFF and the Watchdog is configurable but not active. CAN is inactive and Limp Home output is inactive. From this transition mode, the SBC can be switched via SPI command to the desired operating mode, SBC Normal or Software Flash Mode. If the SBC does not receive any SPI command, or receive wrong SPI command (i.e. not send the device to SBC Normal or SBC SW Flash Mode) within a 256 ms time frame after the reset relaxation, it will enter into SBC Restart Mode and activate the Limp Home output.

*Note: In Init Mode it is recommended to send one SPI command that sets the device to Normal Mode, triggers the watchdog the first time and sets the required watchdog settings.*

#### 4.2.4 SBC Normal Mode

SBC Normal Mode is used to transmit and receive CAN messages. In this mode,  $V_{cc1\mu C}$  is always "ON"  $V_{cc2}$  and  $V_{cc3}$  can be turned-on or off by SPI command. In Normal Mode the watchdog needs to be triggered. It can be configured via SPI, window watchdog and time-out watchdog is possible (default value is time-out 256 ms). All the wake-up sources can be inhibited in this mode. The Limp Home output can be enabled or disabled via SPI command. Via SPI command, the SBC can enter Sleep, Stop or Software Flash Mode. A reset is triggered by the SBC when entering the Software Flash Mode. It is recommended to send at first SPI command the watchdog setting. Please refer to [Chapter 12.4](#).

#### 4.2.5 SBC Sleep Mode

During SBC Sleep Mode, the lowest power consumption is achieved by having the main and external voltage regulators switched-off. As the microcontroller is not supplied, the integrated Watchdog is disabled in Sleep Mode. The last Watchdog configuration is not stored. The CAN module is in Wake-capable or OFF modes and the Limp Home output is unchanged, as before entering the Sleep Mode. If a wake-up appears in this mode, the SBC goes into Restart Mode automatically. In Sleep Mode, not all wake-up sources should be inhibited, this is required to not program the device in a mode where it can not wake up. If all wake sources are inhibited when sending the SBC to Sleep Mode, the SBC does not go to Sleep Mode, the microcontroller is informed via the INT output, and the SPI bit "Fail SPI" is set. The first SPI output data when going to SBC Normal Mode will always indicate the wake up source, as well as the SBC Sleep Mode to indicate where the device comes from and why it left the state.

*Note: Do not change the transceiver settings in the same SPI command that sends the SBC to Sleep Mode.*

#### 4.2.6 SBC Stop Mode

The Stop Mode is used as low power mode where the  $\mu C$  is supplied. In this mode the voltage regulator  $V_{cc1\mu C}$  remains active. The other voltage regulator ( $V_{cc2/3}$ ) can be switched on or off.

The watchdog can be used or switched off. If the watchdog is used the settings made in Normal Mode are also valid in Stop Mode and can not be changed.

The CAN is not active. It can be selected to be off or used as wake-up source. If all wake up sources are disabled, (CAN, WK, cyclic wake) the watchdog can not be disabled, the SBC stays in Normal Mode and the watchdog continues with the old settings.

If a wake-up event occurs the INT pin is set to low. The  $\mu C$  can react on the interrupt and set the device into Normal Mode via SPI. There is no automatic transition to SBC Normal Mode.

There are 4 Options for SBC Stop Mode

- WD on (the watchdog needs to be served as in Normal Mode)
- WD off (special sequence required see [Chapter 10.2.4](#))
- Cyclic Wake up with acknowledge (interrupt is sent after set time and needs to be acknowledged by SPI read)
- Cyclic Wake-up, Watchdog off (interrupt is sent after set time)

#### Cyclic Wake-Up Feature

SBC Stop Mode supports the cyclic wake-up feature. By default, the function is OFF. It is possible to activate the cyclic wake-up via "Cyclic WK on/off" SPI bit. This feature is useful to monitor battery voltage, for example, during parking of the vehicle or for tracking RF data coming via the RF receiver. The Cyclic Wake-up feature sends an interrupt via the pin INT to the  $\mu C$  after the set time. The cyclic wake-up feature shares the same clock as the Watchdog. The time base set in the SPI for the Watchdog will be used for the cyclic wake-up. The timer has to be set before activating the function. With the cyclic wake-up feature the watchdog is not working as known from the other modes. In the case that both functions (Watchdog and cyclic wake-up) are selected, the cyclic wake-up is activated and each interrupt has to be acknowledged by reading the SPI Wake register before the next Cyclic Wake-Up comes. Otherwise, the SBC goes to SBC Restart Mode.

#### 4.2.7 SBC Software Flash Mode

SBC Software Flash Mode is similar to SBC Normal Mode regarding voltage regulators. In this mode, the Limp Home output can be set to active LOW via SPI and the communication on CAN is activated to receive flash data. The Watchdog configuration is fixed to the settings used before entering the SBC SW Flash Mode. When the device comes from SBC Normal Mode, a reset is generated at the transition.

From the SBC Software Flash Mode, the SBC goes into SBC Restart Mode, the config setting has no influence on the behavior. A mode change to SBC Restart Mode can be caused by a SPI command, a time-out or Window Watchdog failure or an undervoltage reset. When leaving the SBC Software Flash Mode a reset is generated.

#### 4.2.8 SBC Restart Mode

They are multiple reasons to enter the SBC Restart Mode and multiple SBC behaviors described in [Table 2](#).

In any case, the purpose of the SBC Restart Mode is to reset the microcontroller.

- From SBC SW Flash Mode, it is used to start the new downloaded code.
- From SBC Normal, SBC Stop Mode and SBC SW Flash Mode it is reached in case of undervoltage on  $V_{cc1\mu C}$ , or due to incorrect Watchdog triggering.
- From SBC Sleep Mode it is used to ramp up  $V_{cc1\mu C}$  after wake
- From SBC Init Mode, it is used to avoid the system to remain undefined.
- From SBC Fail-safe Mode it is used to ramp up  $V_{cc1\mu C}$  after wake or cool down of  $V_{cc1\mu C}$ .

From SBC Restart Mode, the SBC goes automatically to SBC Normal Mode. The delay time  $t_{RDx}$  is programmable by the “Reset delay” SPI bit. The Reset output (RO) is released at the transition. SBC Restart Mode is left automatically by the SBC without any microcontroller influence. The first SPI output data will provide information about the reason for entering Restart Mode. The reason for entering Restart Mode is stored and kept until the microcontroller reads the corresponding “LH0..2” or “RM0..1” SPI bits. In case of a wake up from Sleep Mode the wake source is seen at the interrupt bits (Configuration select 000), an interrupt is not generated.

Entering or leaving the SBC Restart Mode will not result in deactivation of the Limp Home output (if activated).

The first SPI output data when going to SBC Normal Mode will always indicate the reason for the SBC Restart event.

**Table 2 SBC Restart Mode Entry Reasons and Actions**

SBC Mode and Configuration		Entering reason	Actions			
Mode	Config		LH output	$V_{cc1\mu C}$	RO	SPI Out Bits
Init Mode	n.a	Init Mode time-out	ON	remains ON	LOW	LH 0..2
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Normal <sup>1)</sup>	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	config 1	WD trigger failure	ON	remains ON	LOW	LH 0..2
	config 3		OFF after 1st ON after 2nd			RM 0..1 after 1st LH 0..2 after 2nd
	config 4		OFF after 1st			RM 0..1 after 1st <sup>2)</sup>
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Software Flash	n.a	undervoltage reset	unchanged	remains ON	LOW	RM 0..1
	n.a	SPI cmd	unchanged	remains ON	LOW	RM 0..1
	n.a	WD trigger failure	unchanged	remains ON	LOW	RM 0..1
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Sleep	n.a	Wake-up event	unchanged	ramping up	LOW	WK bits register
Stop <sup>1)</sup>	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	config 1	WD trigger failure	ON	remains ON	LOW	LH 0..2
	config 3		OFF after 1st ON after 2nd			RM 0..1 after 1st LH 0..2 after 2nd
	config 4		OFF after 1st			RM 0..1 after 1st <sup>2)</sup>
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Fail-Safe	n.a.	Wake-up event	ON	ramping up	LOW	LH 0..2
Software Development Mode	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2

1) Config 2 will never enter Restart Mode in case of WD failure but directly Fail-Safe Mode

2) Goes to Fail-Safe Mode after the second consecutive failure

#### 4.2.9 SBC Fail-Safe Mode

In SBC Fail-Safe Mode, all voltage regulators are OFF and the transceivers are in Wake-Capable Mode. The Limp Home output is active.

Conditions to enter the SBC Fail-Safe Mode are:

- Watchdog trigger failure in configuration 2 or 4
- $V_{CC1\mu C}$  undervoltage time-out in any configuration if  $V_S$  is above  $V_{LHUV}$  range.
- Temperature shutdown of  $V_{CC1\mu C}$  in any configuration.
- Reset clamped in Config. 2/4

In case of  $V_{CC1\mu C}$  overtemperature shutdown, the SBC will latch and wait to cool down below the thermal hysteresis, and will go back to SBC Restart Mode.

In case of a wake-up event, the SBC will go to SBC Restart Mode (not in case of  $V_{CC1\mu C}$  overtemperature shutdown), storing the wake-up event and resetting the Watchdog trigger failure counter. The first SPI output data when going to SBC Normal Mode will always indicate the reason for the SBC Fail-Safe Mode.

#### 4.2.10 SBC Software Development Mode

If the Test pin is connected to GND (Config 0 active) during powering-up, the SBC enters SBC Software Development Mode. SBC Software Development Mode is a super set of the other modes so it is possible to use all the modes of the SBC with the following difference. In SBC Software Development Mode, no reset is generated and  $V_{CC1\mu C}$  is not switched off due to Watchdog trigger failure. If a Watchdog trigger failure occurs, it will be indicated by the INT output (reset bit). The SBC Fail-Safe Mode or SBC Restart Mode are not reached in case of wrong Watchdog trigger but the other reasons to enter these modes are still valid.

#### 4.2.11 SBC Factory Flash Mode

In this mode, the SBC is completely powered OFF and the microcontroller is supplied externally. The mode is detected when  $V_{CC1\mu C}$  is powered from external and the voltage on  $V_S$  is not powered from external. The current flow out of  $V_S$  must be limited to the maximum rating. The external supply voltage should be below the absolute maximum rating stated in [Chapter 5.1](#). The reset can be driven by an external circuit, or pulled high with a pull-up resistor.

*Note: Please respect the absolute maximum ratings when the device is in SBC Factory Flash Mode.*

## 5 General Product Characteristics

### 5.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			Min.	Max.		
<b>Voltages</b>						
5.1.1	Supply Voltage	$V_S$	-0.3	40	V	–
5.1.2	Supply Voltage Slew Rate	$dV_{S/dt}$	-0.5	5	V/ $\mu$ s	–
5.1.3	Regulator Output Voltage	$V_{cc1\mu C/2/3}$	-0.3	5.5	V	–
5.1.4	CAN Bus Voltage (CANH, CANL)	$V_{CANH/L}$	-27	40	V	–
5.1.5	Differential Voltage CANH, CANL, SPLIT	$V_{diffESD}$	-40	40	V	CANH-CANL <  40 V ; CANH-SPLIT <  40 V  CANL-SPLIT <  40 V ;
5.1.6	Input Voltage at $V_{CCHSCAN}$	$V_{CCHSCAN}$	-0.3	5.5	V	–
5.1.7	Voltage at SPLIT, WK	$V_{SPLIT}$	-27	40	V	–
5.1.8	Voltage at LH_PL/Test	$V_{Test,max}$	-0.3	40	V	–
5.1.9	Voltage at $V_{cc3base}$ , $V_{cc3shunt}$ , $V_{cc3REF}$	$V_{cc3base}$	-0.3	40	V	–
5.1.10	Voltage at Limp Home (LH, LH_SI pin)	$V_{LH}$	-0.3	40	V	–
5.1.11	Logic Voltages Input Pin (SDI, CLK, CSN, TxDCAN)	$V_I$	-0.3	$V_{CC1\mu C} + 0.3V$	V	$0\text{ V} < V_S < 28\text{ V}$ $0\text{ V} < V_{CC1\mu C} < 5.5\text{ V}$
5.1.12	Logic Voltage Output PIN (SDO, RO, INT, RxDCAN)	$V_{DRI, RD}$	-0.3	$V_{CC1\mu C} + 0.3V$	V	$0\text{ V} < V_S < 28\text{ V}$ $0\text{ V} < V_{CC1\mu C} < 5.5\text{ V}$
<b>Currents</b>						
5.1.13	Reverse current on pin Vs	$I_{VS}$	-500	–	mA	$V_S < V_{CC}$
<b>Temperatures</b>						
5.1.14	Junction Temperature	$T_j$	-40	150	°C	–
5.1.15	Storage Temperature	$T_{stg}$	-55	150	°C	–
<b>ESD Susceptibility</b>						
5.1.16	Electrostatic Discharge Voltage at CANH, CANL, SPLIT versus GND	$V_{ESD}$	-6	6	kV	<sup>2)</sup> HBM (100 pF via 1.5 k $\Omega$ )
5.1.17	Electrostatic Discharge Voltage	$V_{ESD}$	-2	2	kV	<sup>2)</sup> HBM (100 pF via 1.5 k $\Omega$ )
5.1.18	Electrostatic Discharge CDM Corner Pins (Pin 1, 18, 19, 36)	$V_{ESD\_CDM\_C}$	-750	750	V	<sup>3)</sup>
	Electrostatic Discharge CDM	$V_{ESD\_CDM}$	-500	500	V	<sup>3)</sup>

1) Not subject to production test; specified by design

2) ESD susceptibility Human Body Model "HBM" according to JESD22-A114

3) ESD susceptibility Charged Device Model "CDM" according to ESDA STM5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



**General Product Characteristics**

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

**5.2 Functional Range**

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			Min.	Max.		
5.2.1	Supply Voltage	$V_S$	$V_{UV\ OFF}$	28	V	After $V_S$ rising above $V_{UV\ ON}$ , <sup>1)</sup>
5.2.2	Supply Voltage	$V_S$	$V_{UV\ OFF}$	40	V	<sup>2)</sup> $t_{pulse} = 400\ ms$ 40 V load dump; $R_i = 2\ \Omega$
5.2.3	SPI Clock Frequency	$f_{clkSPI}$	–	4	MHz	<sup>3)</sup> $V_S > 5.5\ V$
5.2.4	SPI Clock Frequency	$f_{clkSPI}$	–	1	MHz	If $V_{UV\ ON} > V_S > V_{UV\ OFF}$ ;
5.2.5	Junction Temperature	$T_j$	-40	150	°C	–
5.2.6	Undervoltage "OFF"	$V_{UV\ OFF}$	3	4	V	- <sup>1)</sup>
5.2.7	Undervoltage "ON"	$V_{UV\ ON}$	4.5	5.5	V	- <sup>1)</sup>
5.2.8	Supply Voltage for Limp Home Output Active	$V_{S\_LH}$	5.5	40	V	Pull up to $V_S$ $R_{LHO} = 40k\ \Omega$

- 1) In the case  $V_S < V_{UV\ OFF}$ , the SBC is switched OFF and will restart in INIT Mode at next  $V_S$  rising.
- 2) During load dump, the others pins remains in their absolute maximum ratings
- 3) Not subject to production test, specified by design

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

**5.3 Thermal Characteristics**

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
5.3.1	Junction Ambient	$R_{thJA\_1L}$	–	40		K/W	1) 3) 300 mm <sup>2</sup> cooling area
	Junction Ambient	$R_{thJA\_4L}$	–	25		K/W	2) 3) 2s2p + 600 mm <sup>2</sup> cooling area
5.3.2	Junction to Soldering Point	$R_{thJSP}$	–	5	–	K/W	3)

**Thermal Prewarning and Shutdown Junction Temperatures;**

5.3.3	$V_{CC1\mu C}$ , Thermal Pre-warning ON Temperature	$T_{JPW}$	120	145	170	°C	3)
5.3.4	$V_{CC1\mu C}$ , Thermal Prewarning Hysteresis	$\Delta T_{PW}$	–	25	–	K	3)
5.3.5	$V_{CC1\mu C}$ , $V_{CC2}$ Thermal Shutdown Temperature	$T_{jSDVcc}$	150	185	200	°C	3)
5.3.6	$V_{CC1\mu C}$ , $V_{CC2}$ Thermal Shutdown Hysteresis	$\Delta T_{SDVcc}$	–	35	–	K	3)
5.3.7	$V_{CC1\mu C}$ , Ratio of SD to PW Temperature	$\frac{T_{jSDVcc}}{T_{JPW}}$	–	1.20	–	–	3)
5.3.8	CAN Transmitter Thermal Shutdown Temperature	$T_{jSDCAN}$	150	–	200	°C	3)
5.3.9	CAN Transmitter Thermal Shutdown Hysteresis	$\Delta T_{CAN}$	–	10	–	K	3)

1) Specified Rthja value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 single layer. The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board.

2) According to Jedec JESD51-2,-5,-7 at natural convection on 2s2p board for 2W. Board: 76.2x114.3x1.5mm<sup>3</sup> with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacted the first inner copper layer and 600mm<sup>2</sup> cooling are on the top layer (70µm)

3) Not subject to production test; specified by design;

**5.4 Current Consumption**

$V_S = 5.5 \text{ V to } 28 \text{ V}$ ; all outputs open; Without  $V_{CC3}$ ;  $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Normal Mode;</b>							
5.4.1	Current Consumption for Internal Logic	$I_{VS\_logic}$	–	–	2	mA	SBC Normal Mode $I_{CC1\mu C} = I_{CC2} = 0\text{mA}$ ; CAN OFF mode;
5.4.2	Additional current Consumption for CAN Cell	$I_{VS\_CAN}$	–	–	10	mA	CAN Normal Mode; Recessive state; $V_{CC2}$ connected to $V_{CCHSCAN}$ $V_{TXD} = V_{CC1\mu C}$ ; without $R_L$
			–	–	12	mA	CAN Normal Mode; dominant state; $V_{CC2}$ connected to $V_{CCHSCAN}$ $V_{TXD} = \text{low}$ ; without $R_L$ ;
<b>Stop Mode</b>							
5.4.3	Current Consumption	$I_{VS}$	–	58	75	$\mu\text{A}$	SBC Stop Mode; $V_S = 13.5 \text{ V}$ ; $V_{CC1\mu C}$ "ON"; $V_{CC2/3}$ "OFF" CAN wake capable; $T_j = 25^\circ\text{C}$
				65	85		
			–	70	90	$\mu\text{A}$	SBC Stop Mode; $V_S = 13.5 \text{ V}$ ; $V_{CC1\mu C/2}$ "ON"; $V_{CC3}$ "OFF" CAN wake capable; $T_j = 25^\circ\text{C}$
			–	78	100	$\mu\text{A}$	$T_j = 85^\circ\text{C}^{1)}$

### 5.4 Current Consumption (cont'd)

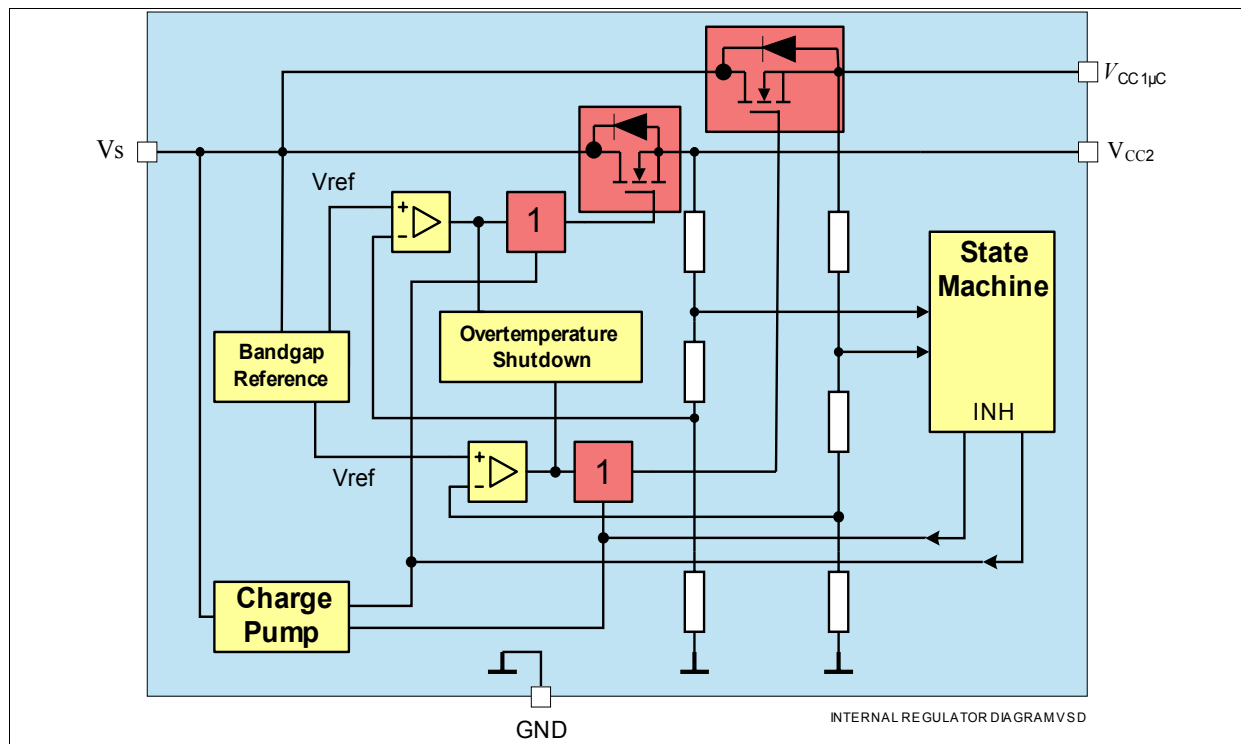
$V_S = 5.5\text{ V to }28\text{ V}$ ; all outputs open; Without  $V_{CC3}$ ;  $T_j = -40\text{ °C to }+150\text{ °C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Sleep Mode</b>							
5.4.4	Current consumption, all Wake Up Sources available.	$I_{VS\_sleep\_SBC}$	–	28	40	$\mu\text{A}$	SBC Sleep Mode; $T_j = 25\text{ °C}$ $V_S = 13.5\text{ V}$ ; $V_{CC1\mu C/2/3}$ "OFF" CAN wake capable;
				32	50		$T_j = 85\text{ °C}^{1)}$
5.4.5	Quiescent Current Reduction when Wake Capable CAN Cell Disabled	$I_{VS\_sleep\_CAN}$	5	12	–	$\mu\text{A}$	<sup>1)</sup> SBC Sleep Mode; $T_j = 25\text{ °C}$ ; $V_S = 13.5\text{ V}$ ; $V_{CC1\mu C/2/3}$ "OFF" CAN OFF

1) Not subject to production test; specified by design

## 6 Internal Voltage Regulator

### 6.1 Block Description



**Figure 4 Functional Block Diagram**

The internal voltage regulators are dual low-drop voltage regulators that can supply loads up to  $I_{CC1\mu C/2\_max}$ . An input voltage up to  $V_{S\_MAX}$  is regulated to  $V_{CC1\mu C/2\_nom} = 5.0\text{ V}$  with a precision of  $\pm 2\%$ . Due to its integrated reset circuitry, featuring two SPI configurable power-on timing ( $t_{RDx}$ ) and three SPI configurable output voltages ( $V_{RTx}$ ) monitoring, the device is well suited for microcontroller supply. The design enables stable operation even with ceramic output capacitors down to 470nF, with  $ESR < 1\ \Omega @ f = 10\text{ kHz}$ . The device is designed for automotive applications, therefore it is protected against overload, short circuit, and overtemperature conditions. **Figure 4** shows the functional block diagram. If the  $V_S$  voltage is lower than  $V_{UV\_OFF}$ , the DMOS of the voltage regulator is switched to high impedance. The body diodes of the DMOS might go into conduction when  $V_{CC1\mu C}$  or  $V_{CC2} > V_S$  (no reverse protection).

### 6.2 Internal Voltage Regulator Modes

It is possible to turn  $V_{CC1\mu C}$  via SBC Modes and  $V_{CC2}$  activity ON or OFF via SPI command or by entering SBC modes. The limiting current for the both regulators is  $I_{CC1\mu C\_max}/I_{CC2}$ .

### 6.3 Internal Voltage Regulator Modes with SBC Mode

Depending on the SBC Mode in use,  $V_{CC1\mu C}$  and  $V_{CC2}$  can be either ON or OFF by definition,  $V_{CC2}$  can be also turned ON or OFF, via SPI. **Table 3** identifies the possible states of the voltage regulators, based on the various SBC modes.

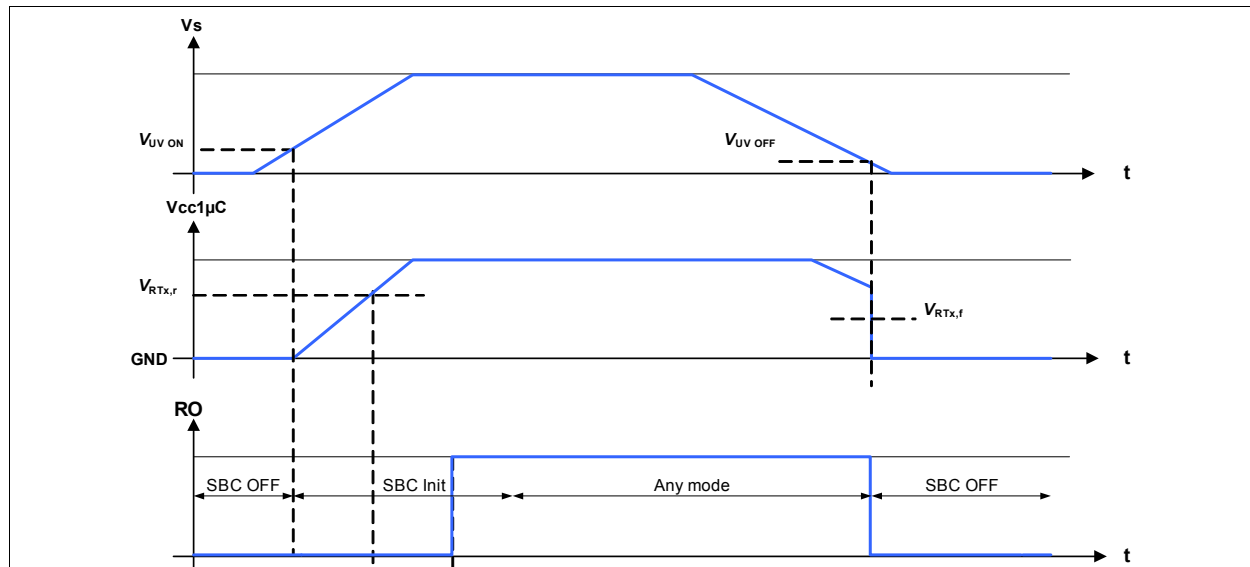
**Table 3 Internal Voltage Regulators States**

SBC Mode	Vcc1 $\mu$ C	Vcc2	
INIT Mode	ON	OFF	
Normal Mode	ON	ON	OFF
Sleep Mode	OFF	OFF	
Restart Mode	ON	unchanged	
Software Flash Mode	ON	ON	OFF
Stop Mode	ON	ON	OFF
Fail-Safe Mode	OFF	OFF	

## 6.4 Application information

### 6.4.1 Timing Diagram

**Figure 5** shows the ramp up and down of the  $V_S$ , and the dependency of  $V_{cc1\mu C}$ . At the first ramp up from SBC Init Mode, the reset threshold  $V_{RT}$  and time  $t_{RO}$  are set to the default value. See [Chapter 10.1](#)



**Figure 5 Ramp up / Down of Main Voltage Regulator**

An undervoltage time-out on  $V_{cc1\mu C}$  is implemented. Refer to [Chapter 12](#) for more information on this function.

### 6.4.2 Under voltage detection at $V_{cc2}$

The  $V_{cc2}$  voltage regulator integrates an under voltage detection. When  $V_{cc2}$  voltage goes below  $V_{UV\_VCC2}$ , the failure is indicated by an interrupt and the failure is reported into the diagnosis frame of the SPI.

## 6.5 Electrical Characteristics

$V_S = 5.5 \text{ V to } 28 \text{ V}$ ;  $C_{CC1\mu C} = C_{CC2} = 470 \text{ nF}$ ; all outputs open; SBC Normal Mode;

$T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Voltage Regulator; Pin <math>V_{CC1\mu C}</math></b>							
6.5.1	Output Voltage	$V_{CC1\mu C}$	4.9	5.0	5.1	V	$0 \text{ mA} < I_{CC1\mu C} < 200 \text{ mA}$ ; $5.5 \text{ V} < V_S < 28 \text{ V}$ ;
6.5.2	Line Regulation	$\Delta V_{CC1\mu C, Li}$	–	–	20	mV	$6 \text{ V} < V_S < 16 \text{ V}$ ; $I_{CC1\mu C} = 0 \text{ A}$
6.5.3	Load Regulation	$\Delta V_{CC1\mu C, Lo}$	–	–	50	mV	$5 \text{ mA} < I_{CC1\mu C} < 200 \text{ mA}$ ; $V_S = 6 \text{ V}$
6.5.4	Power Supply Ripple Rejection	PSRR	–	40	–	dB	$V_r = 1 \text{ Vpp}$ ; $f_r = 100 \text{ Hz}$ ; <sup>1)</sup>
6.5.5	Output Current Limit	$I_{CC1\mu C \text{ max}}$	200	–	500	mA	$V_{CC1\mu C} = 4.5 \text{ V}$ ; power transistor thermally monitored;
6.5.6	Drop Voltage	$V_{DR_{VCC1\mu C}}$	–	–	0.5	V	$I_{CC1\mu C} = 150 \text{ mA}$ ; <sup>2)</sup>
<b>Voltage Regulator; Pin <math>V_{CC2}</math></b>							
6.5.7	Output Voltage	$V_{CC2}$	4.9	5.0	5.1	V	$0 < I_{CC2} < 200 \text{ mA}$ ; $5.5 \text{ V} < V_S < 28 \text{ V}$ ;
6.5.8	Line Regulation	$\Delta V_{CC2, Li}$	–	–	20	mV	$6 \text{ V} < V_S < 16 \text{ V}$ ; $I_{CC2} = 0 \text{ A}$ ;
6.5.9	Load Regulation	$\Delta V_{CC2, Lo}$	–	–	50	mV	$5 \text{ mA} < I_{CC2} < 200 \text{ mA}$ ; $V_S = 6 \text{ V}$
6.5.10	Power Supply Ripple Rejection	PSRR	–	40	–	dB	$V_r = 1 \text{ Vpp}$ ; $f_r = 100 \text{ Hz}$ ; <sup>1)</sup>
6.5.11	Output Current Limit	$I_{CC2}$	200	–	500	mA	$V_{CC2} = 4.5 \text{ V}$ ; power transistor thermally monitored;
6.5.12	Drop Voltage	$V_{DR_{VCC2}}$	–	–	0.5	V	$I_{CC2} = 150 \text{ mA}$ ; <sup>2)</sup>
6.5.13	Under voltage detection on $V_{CC2}$	$V_{UV_{VCC2}}$	4.5	4.65	4.8	V	$V_{CC2}$ falls until INT = LOW

1) specified by design; not subject to production test.

2) Measured when the output voltage has dropped 100 mV from the nominal Value obtained at  $V_S = 13.5 \text{ V}$ . Specified drop voltage for  $V_S > 4 \text{ V}$ .

## 7 External Voltage Regulator

### 7.1 Block Description

$V_{cc3}$  is activated via SPI. The external voltage regulator circuitry is designed to drive an external PNP transistor to increase output current flexibility. Four pins are used:  $V_S$ ,  $V_{cc3base}$ ,  $V_{cc3shunt}$  and  $V_{cc3ref}$ . One transistor is tested during production. An input voltage up to  $V_{SMAX}$  is regulated to  $V_{Q,nom} = 5.0\text{ V}$  with a precision of  $\pm 4\%$ . The output current of the transistor is monitored via an external shunt resistor. The state of  $V_{cc3}$  is reported in the diagnostic SPI register. When battery voltage is below the minimum operating battery voltage  $V_S < V_{VextUV}$ , the external voltage regulator switches off. **Figure 7** shows the behavior during this phase. The shunt is used for overcurrent limitation. If this feature is not needed, connect pins  $V_{cc3shunt}$  and  $V_S$  together.

Since the junction temperature of the external PNP transistor cannot be read, it cannot be protected against over temperature by the SBC, and so the thermal behavior has to be checked by the application.

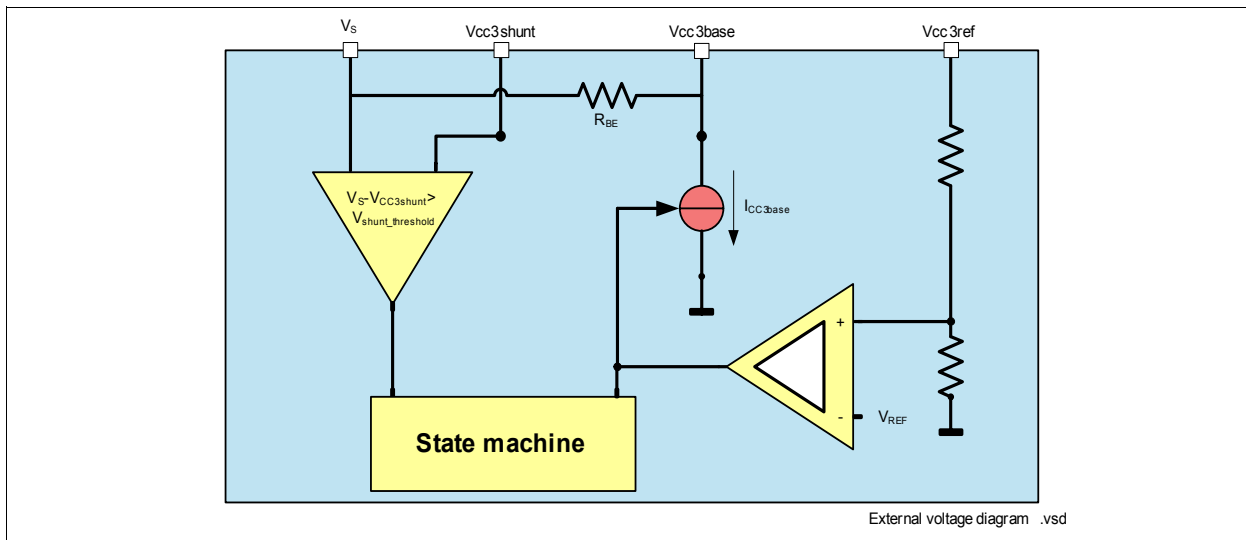


Figure 6 Functional Block Diagram

### 7.2 External Voltage Regulator Mode

It is possible to turn the  $V_{cc3}$  ON or OFF via SPI command, depending on the SBC modes. **Table 4** identifies the possible states, based on the different SBC modes.

### 7.3 External Voltage Regulator State by SBC Mode

**Table 4** shows the possible states of the  $V_{cc3}$  external voltage regulator as a function of the SBC mode.

Table 4 External Voltage Regulator State by SBC Mode

SBC Mode	$V_{cc3}$
INIT Mode	OFF
Normal Mode	ON
Sleep Mode	OFF
Restart Mode	Unchanged
SW Flash Mode	ON
Stop Mode	ON
Fail-Safe Mode	OFF



## 7.4 Application Information

### 7.4.1 Timing information

Figure 7 shows the typical timing, ramp up and ramp down of the External Voltage Regulator, in regards to the  $V_S$  pin.

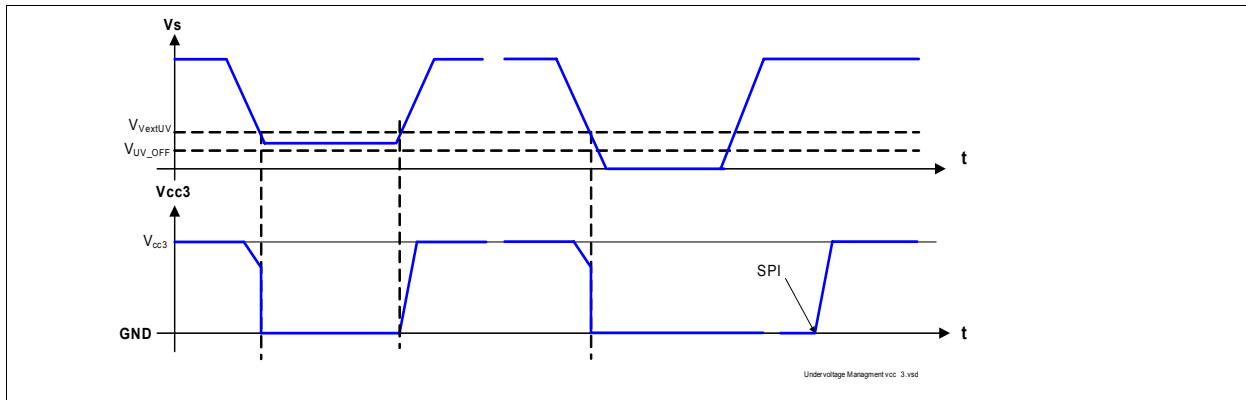


Figure 7 Supply Voltage Management

### 7.4.2 External Components

During production test, the listed parameter are tested with the PNP transistor MJD253 from ON semi. Characterization is done with the BCP52-16 from Infineon ( $I_{CC3} < 200$  mA). Other PNP transistors can be used. Function must be checked in the application.

Figure 8 shows the hardware set up used.

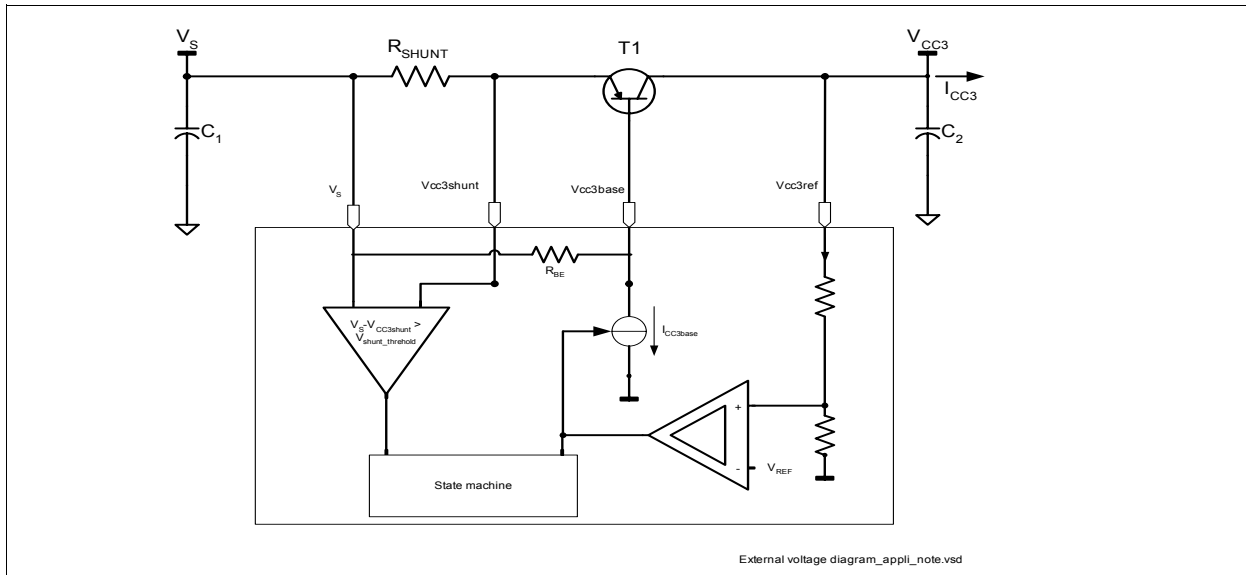


Figure 8 Hardware Set Up

**Table 5 Bills of material for the  $V_{CC3}$  function**

Device	Vendor	Reference / Value
C <sub>2</sub>	Murata	10μF/10V GCM31CR71AA106K
R <sub>SHUNT</sub>	-	220mΩ
T <sub>1</sub>	ON semi	MJD253

### 7.4.3 Calculation of R<sub>SHUNT</sub>

The maximum current  $I_{CC3max}$  where the limit starts and the bit  $I_{CC3} > I_{CC3max}$  is set is determined by the shunt resistor  $R_{shunt}$  and the Output Current Shunt Voltage Threshold  $V_{shunt\_threshold}$ .

The resistor can be calculated as following

$$R_{SHUNT} = \frac{U_{shunt\_threshold}}{I_{CC3max}}$$

### 7.4.4 Unused Pins

In case the Vcc3 is not used in the application, it is recommended to connect the unused pins of Vcc3 as followed.

Connect Vcc1shunt to Vs. (It is also possible to leave the pin open)

Leave Vcc3base open

Leave Vcc3ref open

Do not enable the Vcc3 via SPI as this leads to increased current consumption.

## 7.5 Electrical Characteristics

$V_S = 5.5 \text{ V to } 28 \text{ V}$ ; SBC Normal Mode; all outputs open;

$T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Parameters independent from test set-up</b>							
7.5.1	External Regulator Control Drive Current Capability	$I_{CC3base}$	20		70	mA	$V_{CC3base} = 28\text{V}$
7.5.2	Input Current $V_{CC3ref}$	$I_{CC3ref}$	10	25	50	$\mu\text{A}$	$V_{CC3ref} = 5 \text{ V}$
7.5.3	Input Current $V_{CC3}$ Shunt Pin	$I_{CC3shunt}$	10	25	50	$\mu\text{A}$	$V_{CC3shunt} = V_S$
7.5.4	$V_{CC3}$ Undervoltage Detection	$V_{CC3,UV}$	4.0	4.25	4.5	V	–
7.5.5	$V_{CC3}$ Undervoltage detection hysteresis	$V_{CC3,UV,hys}$	20	100	250	mV	
7.5.6	Output Current Shunt Voltage Threshold	$V_{shunt\_threshold}$	88	110	130	mV	<sup>1)</sup>
7.5.7	Current increase regulation reaction time	$t_{rlinc}$	-	-	5	$\mu\text{s}$	$V_{CC3} = 6\text{V to } 0\text{V}$ ; $I_{CC3base,50\%} = 20\text{mA}$ <b>Figure 9</b>
7.5.8	Current decrease regulation reaction time	$t_{rldec}$	-	-	5	$\mu\text{s}$	$V_{CC3} = 0\text{V to } 6\text{V}$ ; $I_{CC3base,50\%} = 20\text{mA}$ <b>Figure 9</b>
7.5.9	Leakage current of $V_{CC3base}$ when Vcc3 disabled	$I_{CC3base\_lk}$	-	-	5	$\mu\text{A}$	$V_{CC3base} = V_S$ $T_j = 25^\circ\text{C}$
7.5.10	Leakage current of $V_{CC3ref}$ when Vcc3 disabled	$I_{CC3ref\_lk}$	-2	0	2	$\mu\text{A}$	$V_{CC3ref} = 5\text{V}$ $T_j = 25^\circ\text{C}$
7.5.11	Leakage current of $V_{CC3shunt}$ when Vcc3 disabled	$I_{CC3shunt\_lk}$	-	-	5	$\mu\text{A}$	$V_{CC3shunt} = V_S$ $T_j = 25^\circ\text{C}$
7.5.12	Base to emitter resistor	$R_{BE}$	50	100	200	k $\Omega$	$V_{CC3base} = V_S - 0.3\text{V}$ $V_{CC3}$ OFF
7.5.13	External regulator minimum $V_S$ voltage	$V_{VextUV}$	4.5	-	5.5	V	
7.5.14	External regulator minimum $V_S$ voltage hysteresis	$V_{VextUVhys}$	-	0.2	-	V	

### Parameters dependent on the test set-up, according to the **Figure 8**

7.5.15	External Regulator Output Voltage	$V_{CC3}$	4.8	5	5.2	V	$0 \text{ mA} < I_{CC3} < 400 \text{ mA}$ ; $5.5 \text{ V} < V_S < 28 \text{ V}$ ; <sup>2)</sup>
7.5.16	Load Regulation	$\Delta V_{CC3,Lo}$	-	-	50	mV	$2 \text{ mA} < I_{CC3} < 200 \text{ mA}$ ;
7.5.17	Line Regulation	$\Delta V_{CC3,Li}$	-	-	50	mV	$6 \text{ V} < V_S < 16 \text{ V}$ ;

1) Threshold at which the current limitation starts to operate.

2) Tolerance includes load regulation and line regulation.

External Voltage Regulator

Timing diagram for regulator reaction time “current increase regulation reaction time” and “current decrease regulation reaction time”

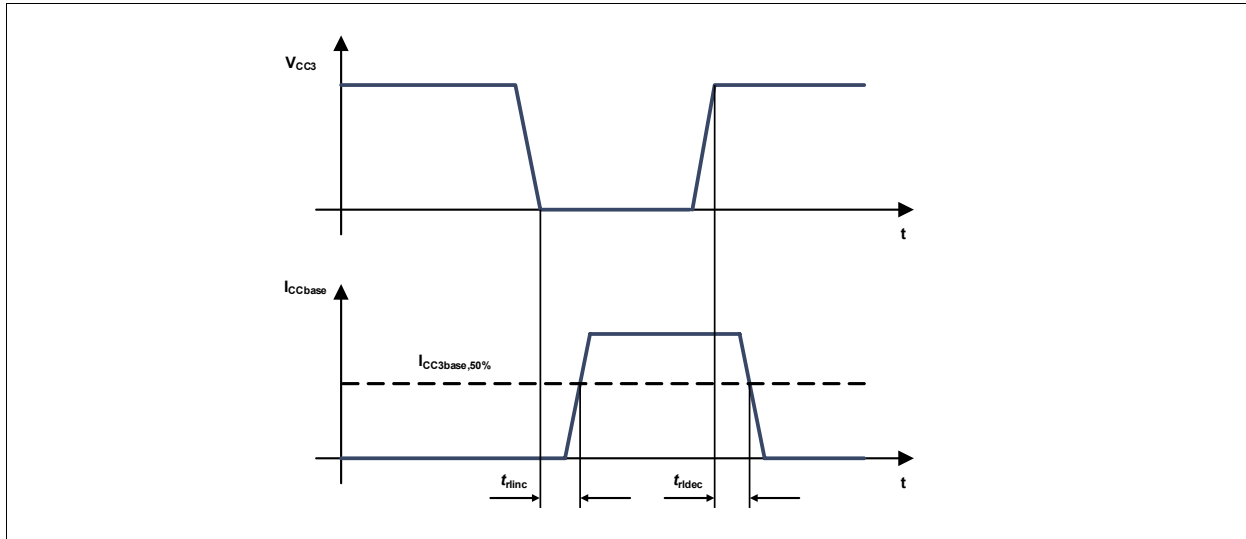


Figure 9 Regulator Reaction Time

## 8 High Speed CAN Transceiver

### 8.1 Block Description

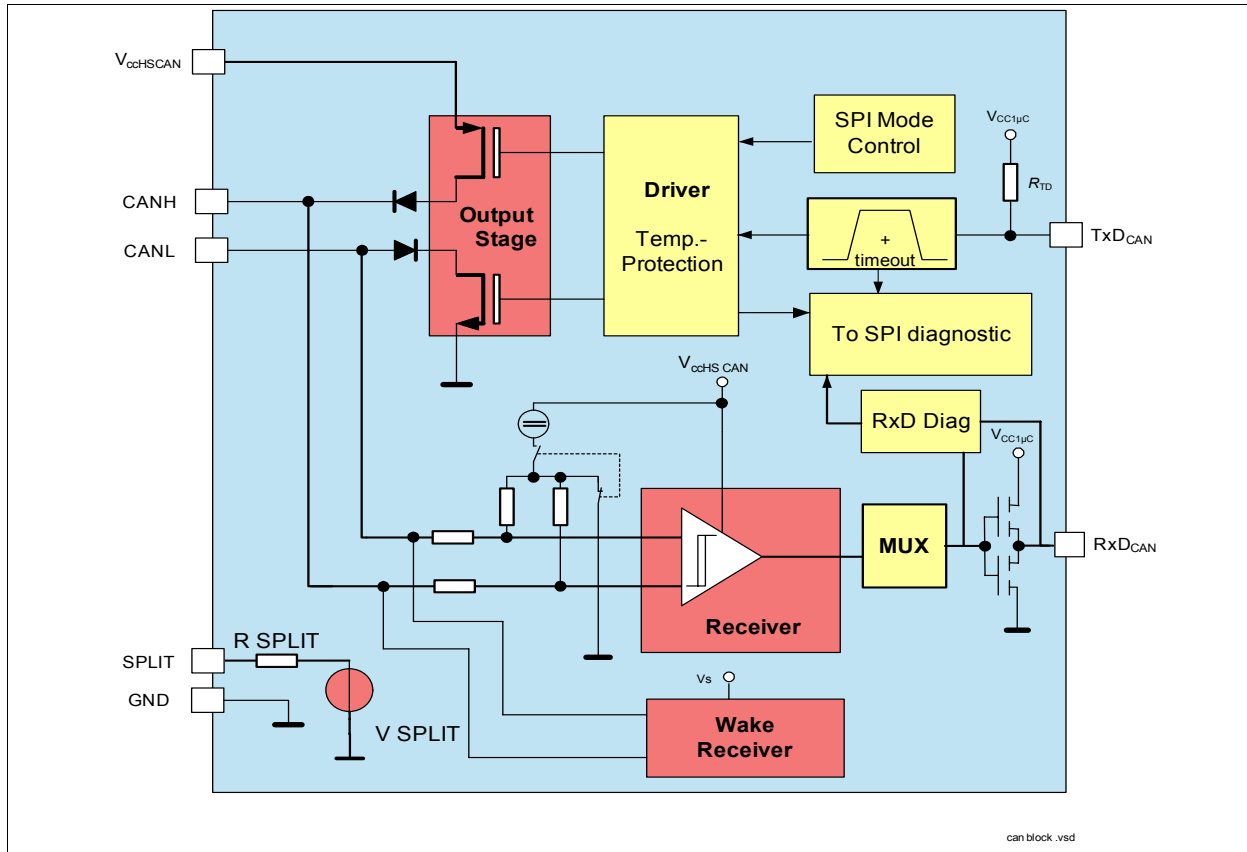


Figure 10 Functional Block Diagram

### 8.2 High-speed CAN Description

The Controller Area Network (CAN) transceiver part of the SBC provides high-speed (HS) differential mode data transmission (up to 1 Mbaud) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible to ISO/DIS 11898-2 and 11898-5 as well as SAE J2284.

The CAN transceiver offers low power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive-only Mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp15/30 applications).

A wake-up from the CAN Wake capable Mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and will be woken up by the CAN bus activities.

Refer to [Figure 11](#) for a description of the matching of the transceiver modes with the SBC mode.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

### 8.2.1 CAN Normal Mode

To transfer the CAN transceiver into the CAN Normal Mode, an SPI word must be sent. This mode is designed for normal data transmission/reception within the HS CAN network. It can be accessed in Normal Mode of the SBC, as well as in SBC Software Flash Mode, and SBC Software Development Mode.

#### Transmission

The signal from the microcontroller is applied to the TxDCAN input of the SBC. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

#### Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

#### Reception

Analog CAN bus signals are converted into digital signals at RxD via the differential input receiver. In CAN Normal and CAN Receive Only Mode, the split pin is used to stabilize the Recessive Common Mode signal. The RxD pin is diagnosed and the detected failure is reported to the SPI diagnostic register.

### 8.2.2 CAN Wake Capable Mode

This mode, which can be used in SBC Stop, Sleep, Restart and Normal Modes by programming via SPI and is automatically accessed in SBC Fail-Safe Mode, is used to monitor bus activities. A wake up signal on the bus results in different behavior of the SBC, as described in [Table 6](#). After wake-up the transceiver can be switched to CAN Normal Mode for communication. To enable the CAN wakeable mode after a wake via CAN, the CAN transceiver must be switched to CAN Normal Mode, CAN Receive Only Mode or CAN Off, before switching to CAN Wakeable Mode again.

**Table 6 Action Due to a CAN Wake Up**

SBC Mode	SBC Mode after wake	Vcc1 $\mu$ C	INT	RxD	Int. Bit WK CAN
Sleep Mode	Restart Mode	Ramping up	HIGH	LOW	1
Stop Mode	Stop Mode	ON	LOW <sup>1)</sup>	LOW	1
Restart Mode	Restart Mode	Ramping up / ON	HIGH	LOW	1
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW	1
Normal Mode	Normal Mode	ON	LOW <sup>1)</sup>	LOW	1

1) When not masked via SPI

#### Wake-Up in SBC Sleep Mode

Wake-up is possible via a CAN message (filtering time  $t > t_{WU}$ ), it automatically transfers the SBC into the SBC Restart Mode and from there to Normal Mode the RxD pins in set to LOW, see [Figure 11](#). The microcontroller is able to detect the low signal on RxD and to read the wake source out of the "Wake Register Interrupt" register (000) via SPI. No Interrupt is generated when coming out of Sleep Mode.

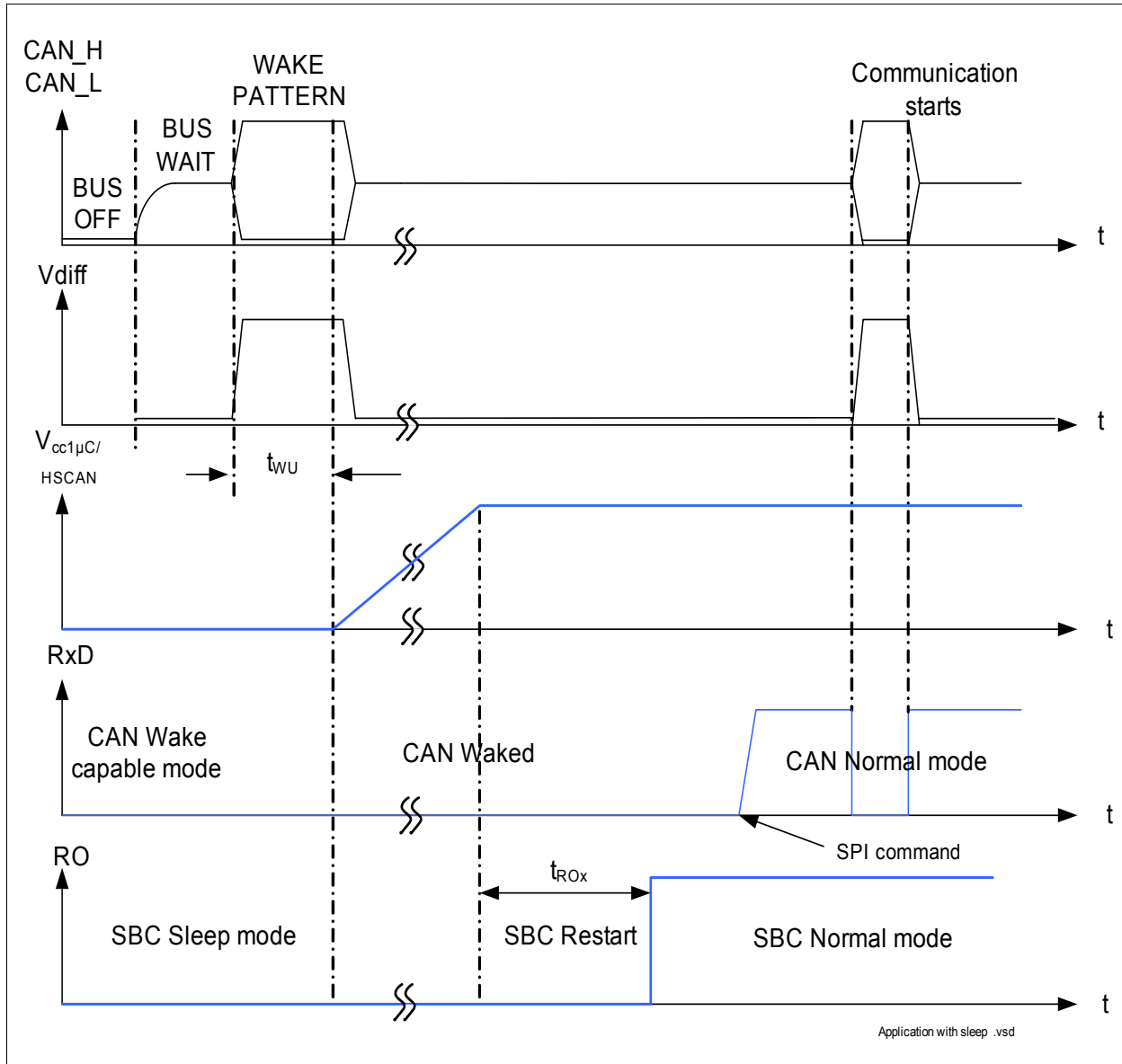


Figure 11 Timing during Transition from Sleep to Normal Mode

### Wake-Up in SBC Stop Mode

In SBC Stop Mode, if a wake-up is detected, it is signaled by the INT output and by the “WK CAN” SPI bit. It is also signaled by RxD<sub>CAN</sub> put to low. The microcontroller should set the device to SBC Normal Mode, there is no automatic transition to Normal Mode. In Normal Mode the transceiver can be enabled via SPI.

### Wake-Up in SBC Restart or SBC Fail-Safe Mode

In SBC Restart or SBC Fail-Safe Mode, if a wake-up is detected, it is signaled by the “WK CAN” SPI bit.

### Wake-Up in SBC Normal Mode

In SBC Normal Mode, if a wake-up is detected, it is signaled by the “WK CAN” SPI bit and INT output, and RxD remains LOW.

### 8.2.3 CAN OFF Mode

CAN OFF Mode, which can be accessed in the SBC Stop, Sleep, Restart and Normal modes, and automatically accessed in SBC Init and Factory Flash modes, is used to completely stop CAN activities. In CAN OFF Mode, a wake up event on the bus will be ignored.

### 8.2.4 CAN Receive Only Mode

In CAN Receive Only Mode (RxD only), the driver stage is de-activated but reception is still operational. This mode is accessible by an SPI command.

### 8.2.5 CAN Cell in Disabled State

During disable state, when  $V_s < V_{UV\_OFF}$ , the CAN cell does not have enough supply voltage. In this state, the CANH and CANL pins are set to high impedance, to guarantee passive behavior. The maximum current that can flow in the CANH and CANL pins in this mode are specified by  $I_{CANH,IK}$  and  $I_{CANL,IK}$ .

## 8.3 CAN Cell Mode with SBC Mode

**Table 7** shows all the CAN modes accessible to the current SBC Mode. Automatic transition from one CAN mode to an other is only allowed in the same column.

**Table 7 HS CAN States, Based on SBC modes**

SBC Mode	CAN Mode			
INIT Mode	OFF			
Normal Mode	OFF	Wake capable	Normal	Receive only
Stop Mode	OFF	Wake capable		
Sleep Mode	OFF	Wake capable		
Restart Mode	OFF	Wake capable		
Fail-Safe Mode	Wake capable			
SW Flash Mode	Normal			

### 8.3.1 SBC Normal Transition to Sleep or Stop Mode

During the transition from SBC Normal to Sleep or Stop Modes, the receiver module is deactivated and replaced by the low power mode receiver for wake-up capability. The next message can be only a wake-up call. It is possible to set the SBC directly from SBC Normal Mode (with CAN Normal Mode) to SBC Sleep or Stop Mode, but this is not recommended, because a wake pattern on the CAN network that could occurs during SPI communication could get lost. It is preferable, in SBC Normal Mode to first send the CAN transceiver into CAN Wake Capable Mode, and then set the entire device to SBC Sleep or Stop Mode. In the unlikely case that the device would see a wake up call during the transmission order “SBC go to sleep”, the device will store this event and bypass the “SBC go to sleep” command to go back into SBC Restart Mode.

Do not change the Transciever setting with the same SPI command that is used to sent the device to Sleep Mode.

### 8.3.2 Transition from SBC Sleep to other Modes

In SBC Sleep Mode, a wake-up on the CAN cell will set the SBC to Restart Mode automatically if the CAN Wake Capable Mode of the SBC is selected via SPI. **Figure 11** shows the typical timing.



## 8.4 Failure Detection

All failures are reported in the SPI diagnostic encoder, the TxD time-out is reported as TxD shorted to GND. In case of local failure and Bus Dominant Clamped failure, the transceiver is automatically switched to the CAN Receive only Mode.

### 8.4.1 TxD Time-out Feature

If the TxD signal is dominant for a time  $t > t_{TxD}$ , the TxD time-out function deactivates the transmission of the signal at the bus. This is implemented to prevent the bus from being blocked permanently due to an error. The transmission is released after switching the CAN to Active Mode via SPI. Refer to [Figure 12](#).

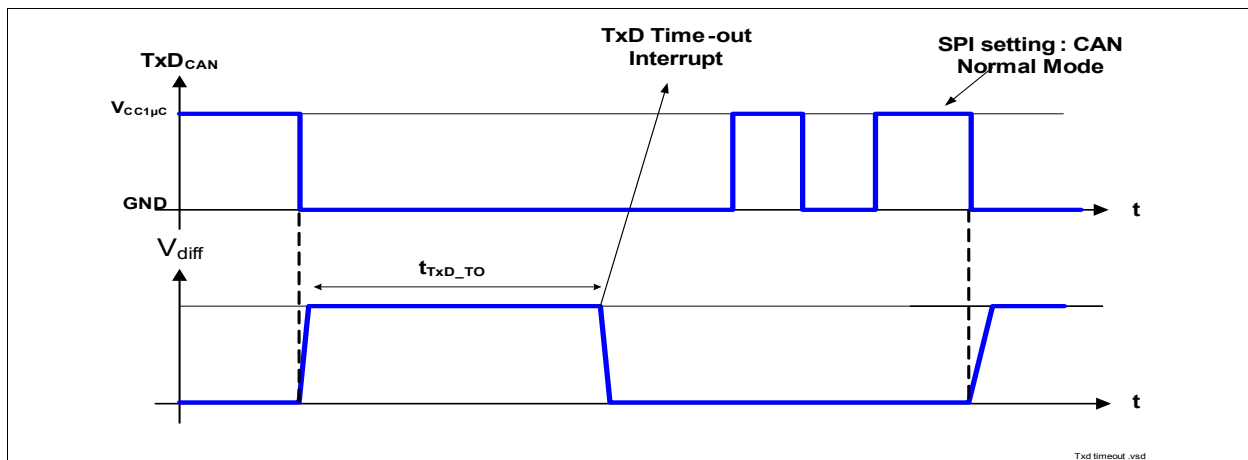


Figure 12 TxD Time-out diagram

### 8.4.2 Bus Dominant Clamping

If the HS CAN bus signal is dominant for a time  $t > t_{BUS\_TO}$ , a bus dominant clamping is detected. The CAN transceiver is switched to Receive Only Mode. The failure is signaled via SPI. If the bits are not masked the INT pin is set to low. For operation the transceiver needs to be switched back to Normal Mode via SPI.

### 8.4.3 TxD to RxD Short Circuit Feature

Similar to the TxD time-out, a TxD to RxD short circuit would also block the bus communication. To avoid this, the CAN transceiver provides TxD to RxD short circuit detection. In this case, it is recommended to switch OFF the SBC HS CAN supply (e.g.  $V_{cc2}$ ) via SPI command to prevent disturbances on the CAN bus. This failure is reported into the diagnostic frame of the SPI. The INT pin is set LOW if not disabled via SPI. The transmitter is automatically inhibited and goes back to normal operation after a SPI command.

### 8.4.4 Overtemperature

The driver stages are protected against overtemperature. Exceeding the shutdown temperature results in deactivation of the CAN transceiver. The CAN transceiver is activated again after cooling down, the device stays in CAN Active Mode. To avoid a bit failure after cooling down, the signals can be transmitted again only after a dominant to recessive edge at TxD.

[Figure 13](#) shows how the transmission stage is deactivated and activated again. First, an overtemperature condition causes the CAN transceiver to be deactivated. After the overtemperature condition is no longer present, the transmission is released automatically after the TxD bus signal has changed to recessive level.

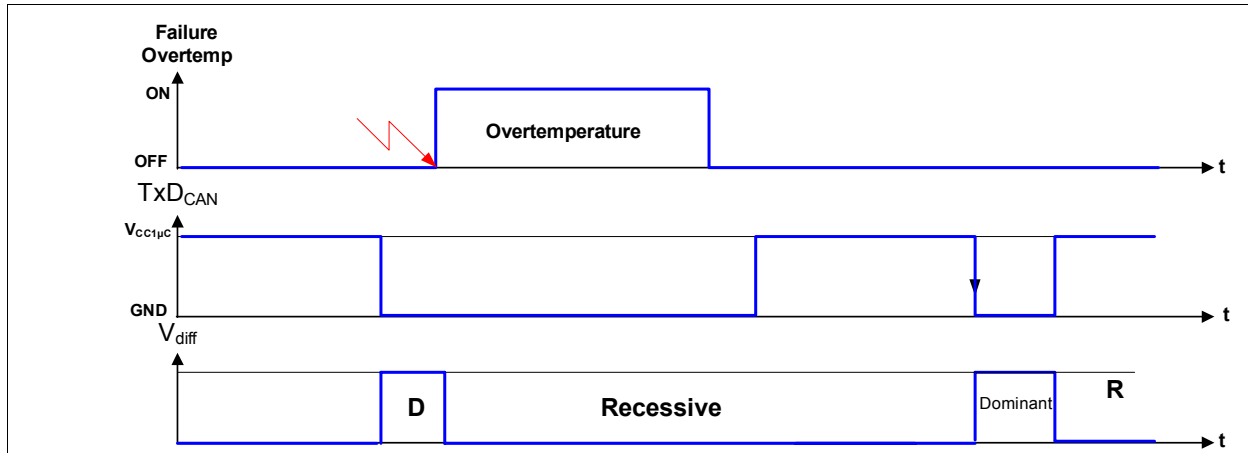


Figure 13 Release of the Transmission after Overtemperature

### 8.4.5 Permanent RxD Recessive Clamping

If the RxD signal is permanently recessive (such as shorted to  $V_{cc1\mu C}$ ), although there is a message sent on the bus, the host microcontroller of this transceiver could start a message at any time because the bus appears to be idle. To prevent this node from disturbing communication on the bus, the SBC offers permanent RxD recessive clamping. If the RxD signal is permanently recessive, the failure is diagnosed and the transmitter is deactivated as long as the error occurs. The transmitter is reactivated after an SPI command.

### 8.4.6 $V_{ccHSCAN}$ Undervoltage

The CAN transceiver cell has no dedicated under voltage detection and use the  $V_{cc2}$  or  $V_{cc3}$  under voltage circuitry. The  $\mu C$  can switch of the CAN in case of undervoltage.

### 8.4.7 Bus failures

In case one of the following bus failures is detected by the SBC the interrupt bit CAN BUS is set to “1” and an interrupt is generated, if not masked. The CAN transceiver does not change the mode due to a detected bus failure.

Bus Failures

- CANH short to GND
- CANH short to Vs
- CANH short to Vcc
- CANL short to GND
- CANL short to Vs
- CANL short to Vcc

A short of CANH to CANL is detected by the microcontroller as the signal sent on TxD is not received on RxD.

## 8.5 SPLIT Circuit

SPLIT circuitry is activated during CAN Normal and Receive Only Mode and de-activated (SPLIT pin high ohmic) during CAN Wake Capable and OFF Modes. The SPLIT pin is used to stabilize the recessive common mode signal in Normal Mode and RxD Only Mode. This is achieved with a stabilized voltage of  $0.5 \times V_{ccHSCAN}$  typical at SPLIT.

A correct application of the SPLIT pin is shown in [Figure 14](#). The SPLIT termination for the left and right nodes is implemented with two 60  $\Omega$  resistors and one 10 nF capacitor. The center node in this example is a stub node and the recommended value for the split resistances is 1.5 k $\Omega$ .

In the case the application doesn't request the SPLIT pin feature, the pin has to be left open.

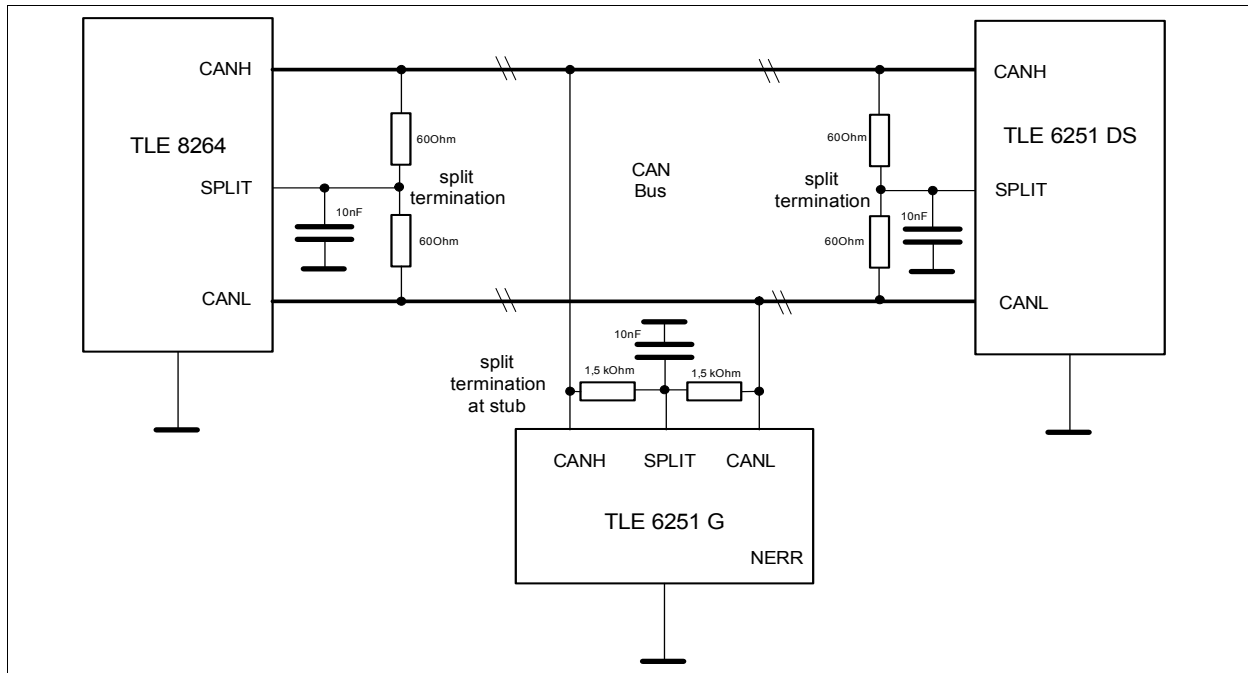


Figure 14 Application example for the SPLIT Pin

## 8.6 Electrical Characteristics

4.75 V <  $V_{ccHSCAN}$  < 5.25 V;  $V_S = 5.5$  V to 28 V;  $R_L = 60 \Omega$ ; CAN Normal Mode;  $T_j = -40$  °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>CAN Bus Receiver</b>							
8.6.1	Differential Receiver Threshold Voltage, recessive to dominant edge	$V_{diff,rd\_N}$	–	0.80	0.90	V	$V_{diff} = V_{CANH} - V_{CANL}$ CAN Normal Mode
8.6.2	Differential Receiver Threshold Voltage, dominant to recessive edge	$V_{diff,dr\_N}$	0.50	0.60	–	V	$V_{diff} = V_{CANH} - V_{CANL}$ CAN Normal Mode
8.6.3	Common Mode Range	CMR	-12	–	12	V	–
8.6.4	Differential Receiver Hysteresis	$V_{diff,hys\_N}$	–	110	–	mV	CAN Normal Mode
8.6.5	CANH, CANL Input Resistance	$R_i$	10	20	30	k $\Omega$	Recessive state
8.6.6	Differential Input Resistance	$R_{diff}$	20	40	60	k $\Omega$	Recessive state
8.6.7	Wake-up Receiver Threshold Voltage, recessive to dominant edge	$V_{diff,rd\_W}$	–	0.8	1.15	V	CAN Wake Capable Mode
8.6.8	Wake-up Receiver Threshold Voltage, dominant to recessive edge	$V_{diff,dr\_W}$	0.4	0.7	–	V	CAN Wake Capable Mode
8.6.9	Wake-up Receiver Differential Receiver Hysteresis	$V_{diff,hys\_W}$	–	120	–	mV	CAN Wake Capable Mode

**8.6 Electrical Characteristics (cont'd)**

4.75 V <  $V_{ccHSCAN}$  < 5.25 V;  $V_S = 5.5$  V to 28 V;  $R_L = 60$   $\Omega$ ; CAN Normal Mode;  $T_j = -40$  °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>CAN Bus Transmitter</b>							
8.6.10	CANH/CANL Recessive Output Voltage	$V_{CANL/H}$	2.0	–	3.0	V	CAN Normal Mode no load
8.6.11	CANH, CANL Recessive Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff_r_N}$	-500	–	50	mV	CAN Normal Mode $V_{TxD} = V_{cc1\mu C}$ ; no load
8.6.12	CANL Dominant Output Voltage	$V_{CANL}$	0.5	–	2.25	V	CAN Normal Mode $V_{TxD} = 0$ V; $V_{ccHSCAN} = 5$ V
8.6.13	CANH Dominant Output Voltage	$V_{CANH}$	2.75	–	4.5	V	CAN Normal Mode $V_{TxD} = 0$ V; $V_{ccHSCAN} = 5$ V
8.6.14	CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff_d_N}$	1.5	–	3.0	V	CAN Normal Mode $V_{TxD} = 0$ V; $V_{ccHSCAN} = 5$ V
8.6.15	CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff_d_N}$	1.5	–	3.0	V	CAN Normal Mode $V_{TxD} = 0$ V; $V_{ccHSCAN} = 5$ V $R_L = 50$ $\Omega$
8.6.16	CANH Short Circuit Current	$I_{CANHsc}$	-200	-80	-50	mA	CAN Normal Mode $V_{CANHshort} = 0$ V
8.6.17	CANL Short Circuit Current	$I_{CANLsc}$	50	80	200	mA	CAN Normal Mode $V_{CANLshort} = 18$ V
8.6.18	Leakage Current	$I_{CANH,ik}$ $I_{CANL,ik}$	–	2	–	$\mu$ A	$V_S = V_{ccHSCAN} = 0$ V; $0$ V < $V_{CANH,L} < 5$ V
<b>SPLIT Termination Output; Pin SPLIT</b>							
8.6.20	SPLIT Output Voltage	$V_{SPLIT}$	$0.3 \times V_{ccHSCAN}$	$0.5 \times V_{ccHSCAN}$	$0.7 \times V_{ccHSCAN}$	V	CAN Normal Mode $-500$ $\mu$ A < $I_{SPLIT} < 500$ $\mu$ A
8.6.21	Leakage Current	$I_{SPLIT}$	-5	0	5	$\mu$ A	CAN Wake capable Mode; $-27$ V < $V_{SPLIT} < 40$ V
8.6.22	SPLIT Output Resistance	$R_{SPLIT}$	–	600	–	$\Omega$	– <sup>1)</sup>
<b>Receiver Output RxD</b>							
8.6.23	HIGH level Output Voltage	$V_{RxD,H}$	$0.8 \times V_{CC1\mu C}$	–	–	V	CAN Normal Mode $I_{RxD(CAN)} = -2$ mA;
8.6.24	LOW Level Output Voltage	$V_{RxD,L}$	–	–	$0.2 \times V_{cc1\mu C}$	V	CAN Normal Mode $I_{RxD(CAN)} = 2$ mA;
<b>Transmission Input TxD</b>							
8.6.26	HIGH Level Input Voltage Threshold	$V_{TD,H}$	–	–	$0.7 \times V_{cc1\mu C}$	V	CAN Normal Mode recessive state
8.6.27	LOW Level Input Voltage Threshold	$V_{TD,L}$	$0.3 \times V_{cc1\mu C}$	–	–	V	CAN Normal Mode dominant state

**8.6 Electrical Characteristics (cont'd)**

4.75 V <  $V_{ccHSCAN}$  < 5.25 V;  $V_S = 5.5$  V to 28 V;  $R_L = 60 \Omega$ ; CAN Normal Mode;  $T_j = -40$  °C to +150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
8.6.28	TxD Input Hysteresis	$V_{TD,hys}$	–	$0.12 \times V_{cc1\mu C}$	–	mV	1)
8.6.29	TxD Pull-up Resistance	$R_{TD}$	20	40	80	k $\Omega$	–

**Dynamic CAN-Transceiver Characteristics**

8.6.30	Min. Dominant Time for Bus Wake-up	$t_{WU}$	0.75	3	5	$\mu$ s	CAN Wake capable Mode
8.6.31	Propagation Delay TxD-to-RxD LOW (recessive to dominant)	$t_{d(L),TR}$	–	150	255	ns	CAN Normal Mode $C_L = 47$ pF; $R_L = 60 \Omega$ ; $V_{ccHSCAN} = 5$ V; $C_{RxD} = 15$ pF
8.6.32	Propagation Delay TxD-to-RxD HIGH (dominant to recessive)	$t_{d(H),TR}$	–	150	255	ns	CAN Normal Mode $C_L = 47$ pF; $R_L = 60 \Omega$ ; $V_{ccHSCAN} = 5$ V; $C_{RxD} = 15$ pF
8.6.33	Propagation Delay TxD LOW to bus dominant	$t_{d(L),T}$	–	50	120	ns	CAN Normal Mode $C_L = 47$ pF; $R_L = 60 \Omega$ ; $V_{ccHSCAN} = 5$ V
8.6.34	Propagation Delay TxD HIGH to bus recessive	$t_{d(H),T}$	–	50	120	ns	CAN Normal Mode $C_L = 47$ pF; $R_L = 60 \Omega$ ; $V_{ccHSCAN} = 5$ V
8.6.35	Propagation Delay bus dominant to RxD LOW	$t_{d(L),R}$	–	100	135	ns	CAN Normal Mode $C_L = 47$ pF; $R_L = 60 \Omega$ ; $V_{ccHSCAN} = 5$ V; $C_{RxD} = 15$ pF
8.6.36	Propagation Delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	100	135	ns	CAN Normal Mode $C_L = 47$ pF; $R_L = 60 \Omega$ ; $V_{ccHSCAN} = 5$ V; $C_{RxD} = 15$ pF
8.6.37	TxD Permanent Dominant Time-out	$t_{TxD\_TO}$	0.3	0.6	1.0	ms	CAN Normal Mode
8.6.38	Bus Dominant Time-out	$t_{BUS\_TO}$	0.3	0.6	1.0	ms	CAN Normal Mode <sup>1)</sup>

1) Not subject to production test; specified by design.

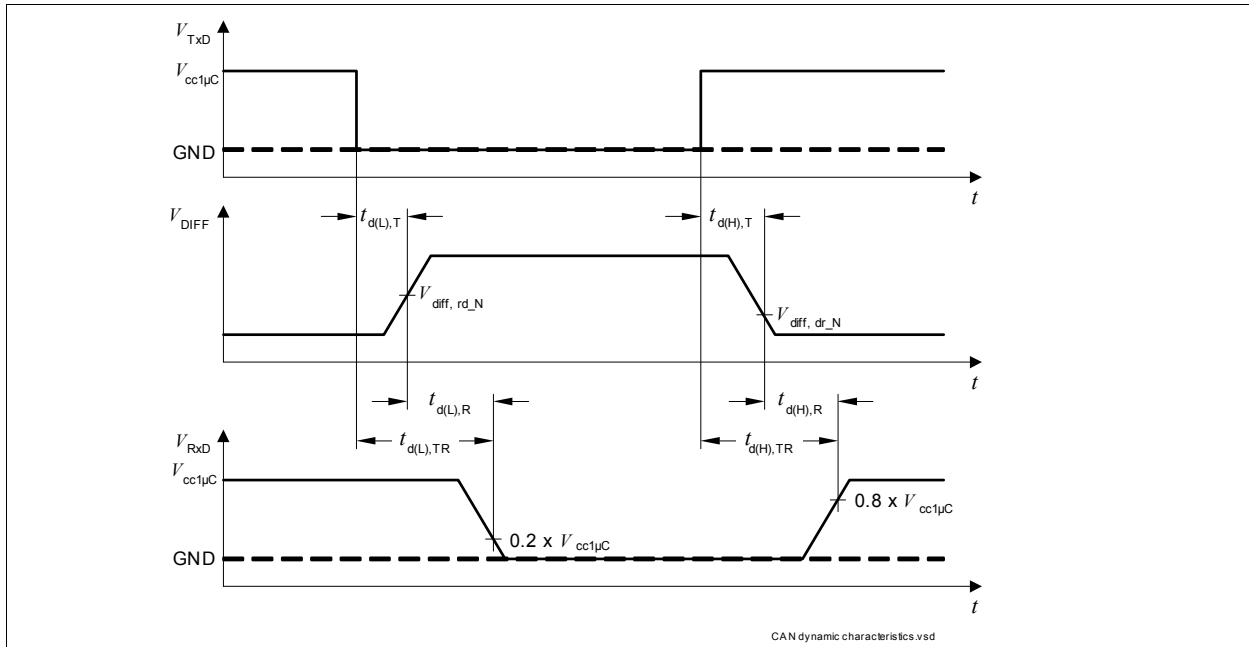
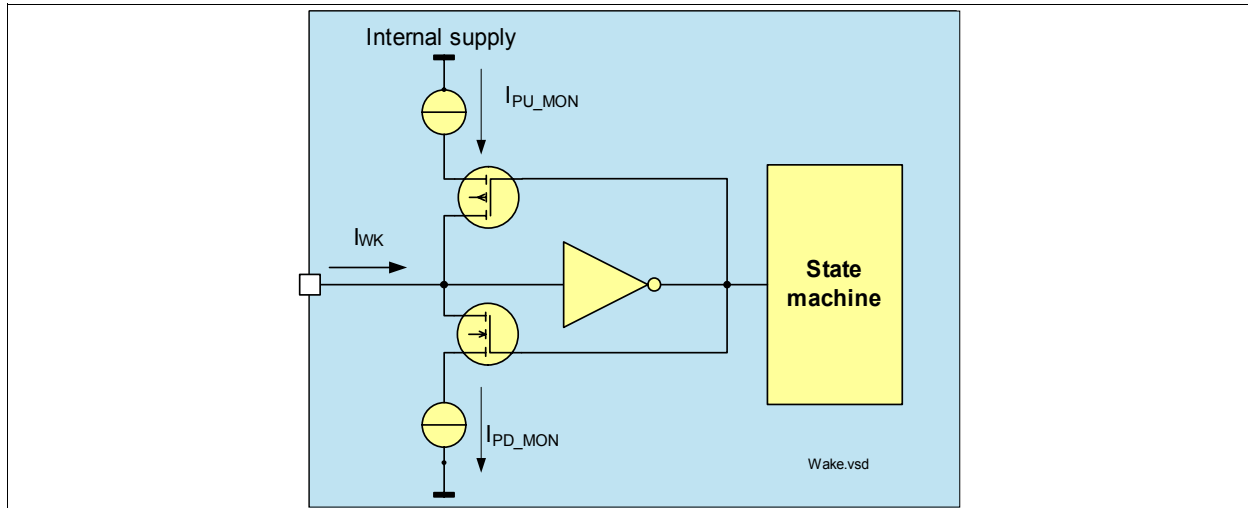


Figure 15 Timing Diagrams for Dynamic Characteristics

## 9 WK Pin

### 9.1 Block Description



**Figure 16 Functional Block Diagram**

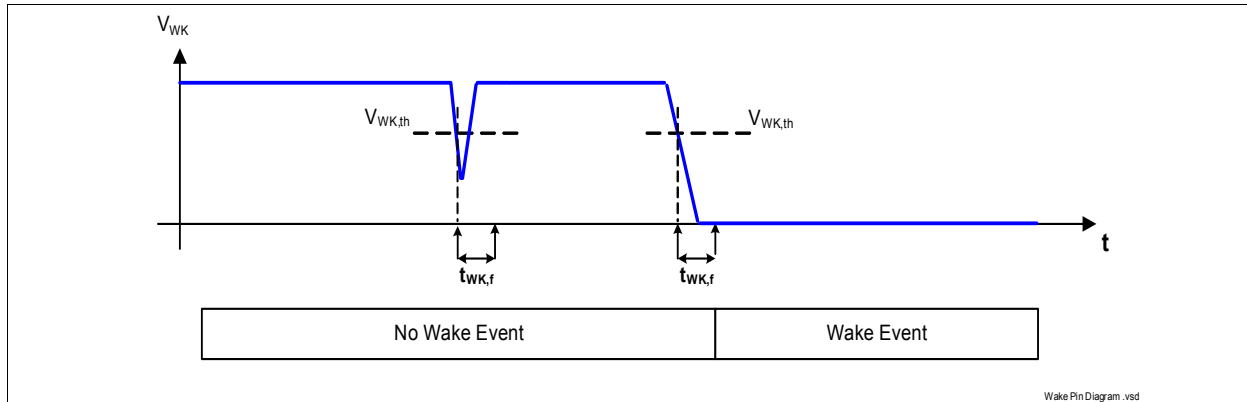
The internal voltage regulator ( $V_{cc1\mu C}$ ) and the entire SBC can wake up by changing the wake input voltage. The WK input pin is a bi-level sensitive input. This means that both transitions, HIGH to LOW and LOW to HIGH, result in a wake-up. The filtering time is  $t_{WK, f}$ . The wake-up capability can be enabled or disabled via SPI command. In case of reverse polarity, no special protection must be set if the absolute maximum rating is respected. When the SBC is below the minimum  $V_{UVOFF}$ , (SBC OFF Mode) the pin WK is at high impedance; a wake event will be ignored.

The state of the WK pin (low or high) can always be read in Normal Mode, Stop Mode and SW Flash Mode at the bit WK State. When setting the bit "WK PIN on/off" to 1, the device wakes up from Sleep Mode with a high to low or low to high transition. From Fail-Safe Mode the device will always go to Restart Mode with a high to low or low to high transition. If the bit "WK PIN on/off" is set to 1 in Normal, Stop or SBC SW Flash Mode the interrupt bits "WK 0 WK pin" and/or "WK 1 WK pin" are set in case of a change on the WK pin and an interrupt is generated if not masked. With the bits "WK 0 WK pin" and "WK 1 WK pin" the interrupt for low to high transition and high to low transition can be masked separately.

### 9.2 Wake-Up Timing

**Figure 17** shows typical wake-up timing and parasitic filtering. The filtering time is  $t_{WK, f}$ . This is used to avoid a parasitic wake-up due to EMC disturbances. Specifically, the voltage transition on pin WK must be higher than the  $V_{WK, TH}$  and longer than  $t_{WK, f}$  to be understood as a wake-up signal.





**Figure 17** Wake-up Timing

### 9.2.1 Transition from Normal to Sleep Mode.

The SBC can not be sent from Normal Mode to Sleep Mode with uncleared interrupt in the WK interrupt bits “WK 0 WK pin” and “WK 1 WK pin”. This is implemented to avoid that a wake information from the WK pin gets lost during the transition from Normal to Sleep Mode. If a wake up appears during the  $\mu$ C sets the SBC to Sleep Mode, the SBC will wake up directly after going to Sleep Mode. There is no difference if the bits “WK 0 WK pin” or “WK 1 WK pin” bit were set during the transition or were just not cleared before sending the SPI command for Sleep Mode, the SBC will wake-up after entering the Sleep Mode. Therefore it always needs to be ensured that the bits are cleared before sending the SBC to Sleep Mode.

### 9.3 Electrical Characteristics

$V_S = 5.5\text{ V to }28\text{ V}$ ;  $T_j = -40\text{ °C to }+150\text{ °C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
9.3.1	WK Input Threshold Voltage	$V_{WK,th}$	2	3	4	V	–
9.3.2	Input Hysteresis	$V_{I,hys.}$	0.1	–	0.7	V	
9.3.3	WK Filter Time	$t_{WK,f}$	10	–	25	μs	–
9.3.4	Input Current	$I_{WK}$	-2	–	2	μA	$V_{WK} = 0\text{ V};$ $V_{WK} > 5\text{ V}$
9.3.5	WK pin pull up current	$I_{PU\_MON}$	-30	–	-3	μA	$V_{WK} = 3.8\text{ V}$
9.3.6	WK pin pull down current	$I_{PD\_MON}$	3	–	30	μA	$V_{WK} = 2\text{ V}$

## 10 Supervision Functions

### 10.1 Reset Function

#### 10.1.1 Description

The reset output pin RO provides information to the microcontroller, for example, in the event that the output voltage has fallen below the undervoltage threshold  $V_{RT1/2/3}$ . When connecting the SBC to battery voltage, the reset signal remains LOW initially. When the output voltage  $V_{CC1\mu C}$  has reached the reset threshold  $V_{RT1,r}$ , the reset output RO remains LOW for the reset delay time  $t_{rd1}$ . After that the RO is released to HIGH. A reset can also occur due to faulty Watchdog refresh. See [Chapter 10.2](#). The reset threshold as well as the reset delay time can be adjusted via SPI. The RO pin has an integrated pull-up resistor.

#### 10.1.2 Reset diagnosis

The RO pin is diagnosed for both short circuit to  $V_{CCx}$  and GND. Depending on the configuration, in case of RO failure, the SBC goes to SBC Fail-Safe or Restart Mode and activate the Limp Home output.

In case of short circuit to GND, it is detected in any SBC mode except SBC Restart Mode. At the falling edge of the RO, when supposed to be HIGH, the SBC enters automatically the SBC Restart Mode. If after the  $t_{rd}$  and RO relaxation, the RO pin is still LOW, then the SBC detects the clamping to LOW failure. The microcontroller is in permanent reset.

In case of short circuit to  $V_{CCx}$ , the SBC cannot detect the short circuit before a reset should occur. So reset clamped is detected when the SBC goes to SBC Restart Mode or during Init Mode.

#### 10.1.3 Reset Timing

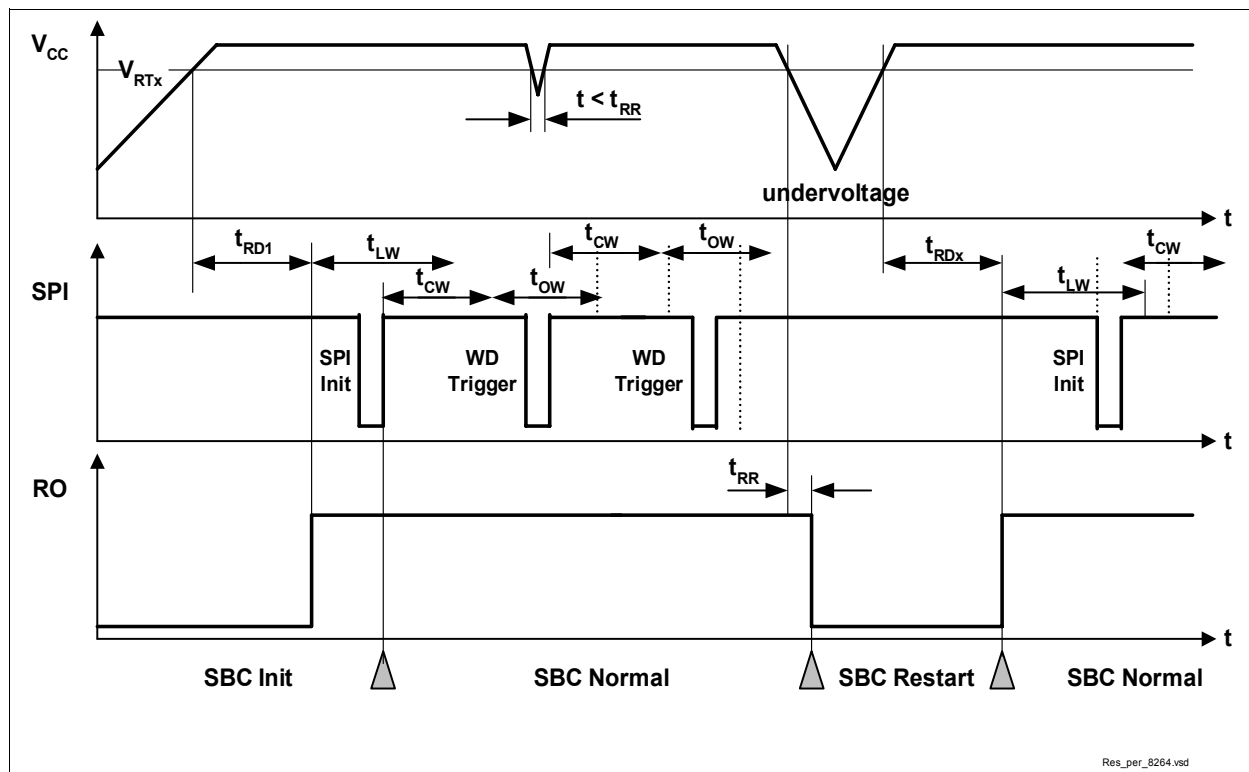


Figure 18 Reset Timing Diagram

### 10.1.4 Reset from Outside

If the reset pin RO is pulled to low from outside while no reset low is issued by the SBC, the device goes to Restart Mode. In Restart Mode an reset is issued by the SBC, the RO pin is set to low for the time  $t_{RD1}$  or  $t_{RD2}$ . If the RO pin is pulled to low for longer time Reset clamped is detected.

## 10.2 Watchdog

Two different Watchdogs are possible in the SBC. It can be either a Window Watchdog or a Time-out Watchdog. The Watchdog can also be inhibited in SBC Stop Mode and SBC SW Flash Mode via SPI. The Watchdog timing is programmed via SPI command. As soon as the Watchdog is activated, the timer starts running and the Watchdog must be served. Please refer to [Table 8](#) to match the SBC Modes with the Watchdog Modes.

The default setting for the Watchdog is Time-out Watchdog with a 256 ms timer. The long open window allows the microcontroller to run its initialization sequences and then to trigger the Watchdog via the SPI.

The Watchdog is served by a SPI bit and should toggle with the correct frequency. The default value is a 0, so the first trigger bit must be a 1.

In case of a Watchdog reset, the Watchdog immediately starts with a long open window when entering SBC Normal Mode. With the reset the watchdog bit is set to 0, so the first watchdog trigger after reset is a change to 1.

In SBC Software Development Mode, no reset is generated due to watchdog failure, if a watchdog failure occurs it is indicated by the SPI Reset bit and via INT pin. All watchdog modes are accessible in regards to the normal operation modes.

**Table 8 Watchdog Functionality by SBC Modes**

SBC Mode	Watchdog Mode	Remarks
INIT Mode	Watchdog Programmable; Watchdog is not active.	INIT Mode should be left in less than 256 ms (see <a href="#">Chapter 12</a> )
Normal Mode	WD Programmable; Time-out or Window Watchdog	–
Software Flash Mode	Mode is fixed	SBC retains the set-up as in the mode before entering the Software Flash Mode
Stop Mode	Mode is fixed	SBC retains the set up as in the mode before entering the Stop Mode
Sleep Mode	OFF	SBC does not retain the set-up.
Fail-Safe Mode	OFF	SBC does not retain the set-up
Restart Mode	OFF	SBC will start default Watchdog setting (256ms Time-out Watchdog) when entering Normal Mode.

### 10.2.1 Time-out Watchdog

The Time-out Watchdog is an easier and less secure type of watchdog. Compared to the Window Watchdog there is no closed window existing. The watchdog trigger can be done any time within the watchdog time.

A watchdog trigger is detected as a write access to the “WD Refresh” within the SPI control word. The bit needs to be toggle (transition HIGH to LOW or LOW to HIGH) within the watchdog window. The trigger is accepted when the CSN input becomes HIGH.

A correct watchdog trigger starts a new window. The period is selected via the Window Watchdog timing bit field in the range of 16 ms to 1024 ms. For the safe trigger area the tolerance of the oscillator has to be taken into consideration, so the safe trigger time is below 90% of the programmed Watchdog time. It is possible to refresh the Watchdog with any SPI programming with the mode selection Normal, Stop, SW Flash or Read Only.

Should the trigger signal not meet the window, depending on the configuration, the SBC will go to SBC Restart Mode or to Fail-Safe Mode. A watchdog reset is created by setting the reset output RO low. In config 1 and config 3 the watchdog starts again in Normal Mode with the default watchdog setting (256ms Time-out Watchdog). The watchdog failure can be read at the bits RM0, RM1, LH0, LH1, LH2 via SPI.

### 10.2.2 Window Watchdog

A Watchdog trigger is detected as a write access to the “WD Refresh” within the SPI control word. The bit needs to be toggle (transition HIGH to LOW or LOW to HIGH) in the open window. The trigger is accepted when the CSN input becomes HIGH.

A correct Watchdog trigger results in starting the Window Watchdog by a closed window with a width of typically 50% of the selected Window Watchdog reset period. This period, selected via the Window Watchdog timing bit field, is in the range of 16 ms to 1024 ms. This closed window is followed by an open window, with a width of typical 50% of the selected period. From now on, the microcontroller must serve the Watchdog by periodically toggling the Watchdog bit. This bit toggling access must meet the open window. The tolerance of the oscillator has to be taken into consideration, so the safe window to trigger the Watchdog is from 55% to 90% of the programmed Window Watchdog time. It is possible to refresh the Watchdog with any SPI programming with the mode selection Normal, Stop, SW Flash or Read Only. A correct Watchdog service immediately results in starting the next closed window (see [Figure 19](#), safe trigger area).

Should the trigger signal not meet the open window, depending on the configuration the SBC will go to SBC Restart Mode or to Fail-Safe Mode. A watchdog reset is created by setting the reset output RO low (see [Figure 20](#)). In config 1 and config 3 the watchdog starts again in Normal Mode with the default watchdog setting (256ms Time-out Watchdog). The watchdog failure can be read at the bits RM0, RM1, LH0, LH1, LH2 via SPI.

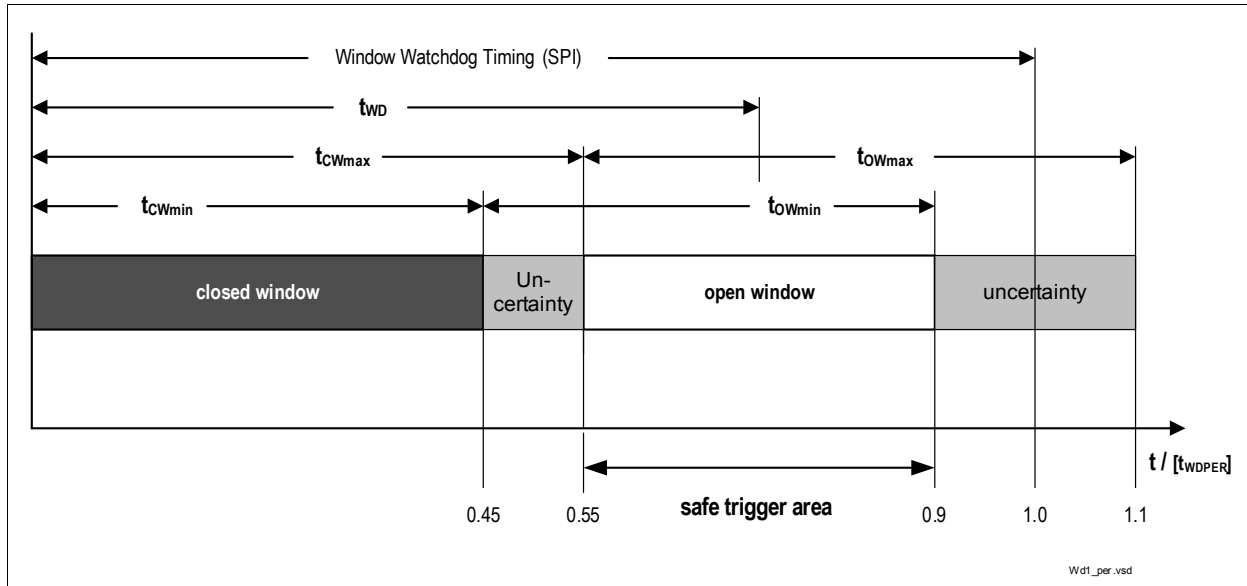


Figure 19 Window Watchdog Definitions

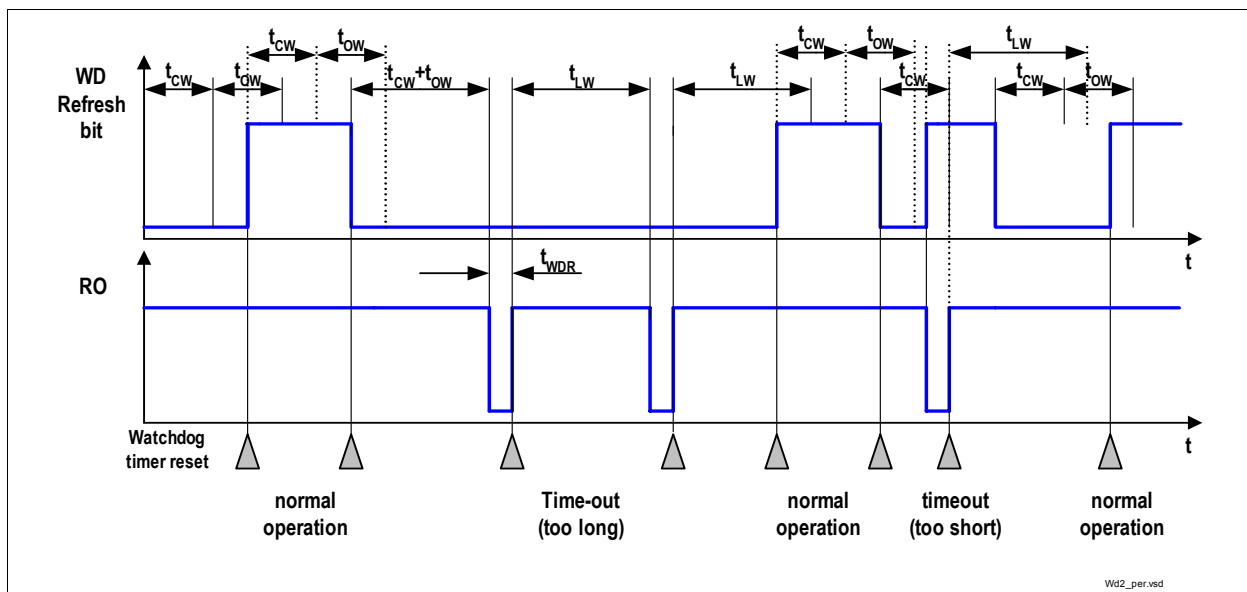


Figure 20 Window Watchdog Timing Diagram for config 1 and config 3

### 10.2.3 Changing the Watchdog Settings

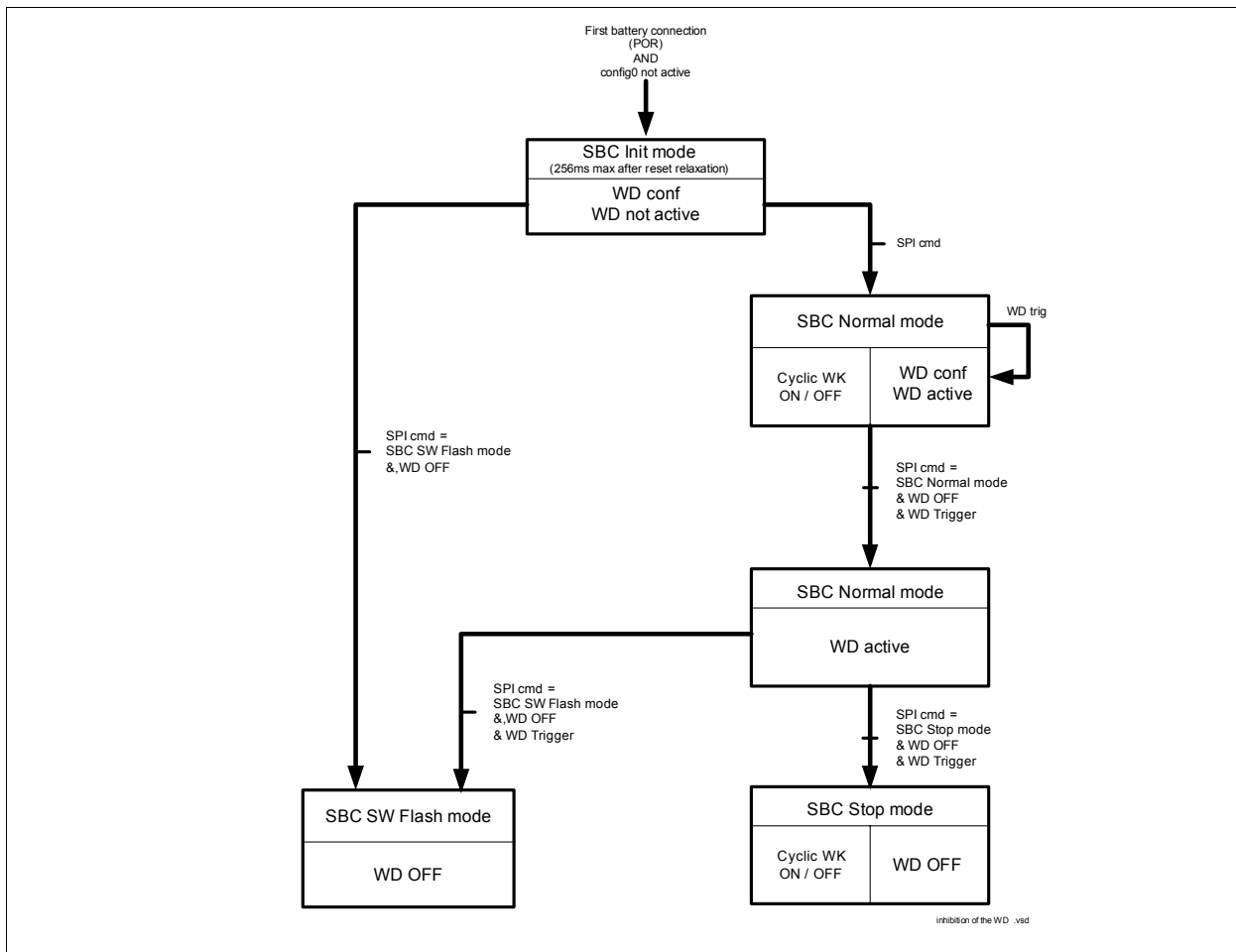
The settings of the watchdog can be changed during the operation of the watchdog. The change is done with a SPI programming into the Watchdog Configuration Register. The new setting is programmed together with a valid watchdog trigger according to the old settings. The timer with the new settings starts with this SPI command. The toggling of the “WD Refresh” bit needs to be continued (transition HIGH to LOW or LOW to HIGH) with the new settings.

If the new settings were not valid, the watchdog will continue with the old settings and generate a “Wrong WD Set” interrupt.

### 10.2.4 Inhibition of the watchdog

During SBC Stop Mode and SBC SW Flash Mode, it is possible to deactivate the watchdog. To avoid unwished deactivation of the watchdog, a special protocol has to be followed, prior deactivating the watchdog. Please refer to **Figure 21**. In the case the exact process below is not respected, the SBC remains in the previous state, and an interrupt is generated (if not inhibited), and the *Wrong WD set* bit in the SPI is set.

When the microcontroller requests the SBC to go back to SBC Normal Mode, the Watchdog is reactivated. The watchdog settings that were valid before entering Stop Mode with watchdog off are valid. The watchdog timer starts with entering Normal Mode. In case window watchdog was selected the watchdog starts with a closed window. When setting the WD Refresh bit to 0 for the command that sends the device to Normal Mode the first watchdog trigger is a change to 1. As in Stop Mode the watchdog settings can not be changed, it is also not possible to change the watchdog settings with the command that sets the SBC from Stop Mode into Normal Mode.



**Figure 21 Inhibition of the watchdog**

During SBC Stop Mode, when the cyclic wake feature is used and the watchdog is not disabled, it is necessary that the microcontroller acknowledges the interrupt by reading the SPI Wake register before the next Cyclic Wake occurs. Otherwise, a reset is performed by setting the SBC to SBC Restart Mode.

### 10.3 Electrical Characteristics

$V_S = 5.5\text{ V to }28\text{ V}$ ;  $T_j = -40\text{ °C to }+150\text{ °C}$ ; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Reset Generator; Pin RO</b>							
10.3.1	Reset Threshold Voltage,	$V_{RT1,f}$	4.5	4.65	4.75	V	default setting, Vcc falling
		$V_{RT1,r}$	4.6	4.75	4.85	V	default setting, Vcc rising
		$V_{RT2,f}$	3.5	3.65	3.75	V	SPI option; Vcc falling
		$V_{RT2,r}$	3.6	3.75	3.85	V	SPI option; Vcc rising
		$V_{RT3,f}$	3.2	3.35	3.45	V	SPI option; $V_S \geq 4\text{ V}$ ; Vcc falling
		$V_{RT3,r}$	3.3	3.45	3.55	V	SPI option; $V_S \geq 4\text{ V}$ , Vcc rising
	Reset Threshold Voltage Headroom	$V_{RT1\_HR}$	250	–	–	mV	default setting <sup>1)</sup>
		$V_{RT2\_HR}$	1.25	–	–	V	SPI option; <sup>1)</sup>
		$V_{RT3\_HR}$	1.55	–	–	V	SPI option; $V_S \geq 4\text{ V}$ <sup>1)</sup>
10.3.2	Reset Threshold Hysteresis	$V_{RT,hys}$	20	100	200	mV	-
10.3.3	Reset Low Output Voltage	$V_{RO}$	–	0.2	0.4	V	$I_{RO} = 1\text{ mA}$ for $V_{CC1\mu C} = V_{RT1/2/3}$ ; $I_{RO} = 200\text{ }\mu\text{A}$ for $V_{RT1/2/3} > V_{CC1\mu C} \geq 1\text{ V}$
10.3.4	Reset High Output Voltage	$V_{RO}$	$0.7 \times V_{CC1\mu C}$	–	$V_{CC1\mu C} + 0.3\text{ V}$	V	$I_{RO} = -20\text{ }\mu\text{A}$
10.3.5	Reset Pull-up Resistor	$R_{RO}$	10	20	40	k $\Omega$	$V_{RO} = 0\text{ V}$
10.3.6	Reset Reaction Time	$t_{RR}$	4	10	26	$\mu\text{s}$	$V_{CC1\mu C} < V_{RT1/2}$ to RO = L
10.3.7	Reset Delay Time	$t_{RD1}$	4.5	5.0	5.5	ms	default SPI setting; after Power-On-Reset
		$t_{RD2}$	450	500	550	$\mu\text{s}$	SPI setting option
<b>Watchdog Generator</b>							
10.3.8	Long Open Window	$t_{LW}$	–	256	–	ms	<sup>2)</sup> default setting
<b>Internal Oscillator</b>							
10.3.9	Internal Oscillator tolerance	$f_{CLKSBC}$	-10	0	10	%	–

1) Headroom between actual output voltage on  $V_{CC1\mu C}$  and Reset Threshold Voltage for falling Vcc.

2) Specified by design; not subject to production test. Tolerance defined by internal oscillator tolerance  $f_{CLKSBC}$ .



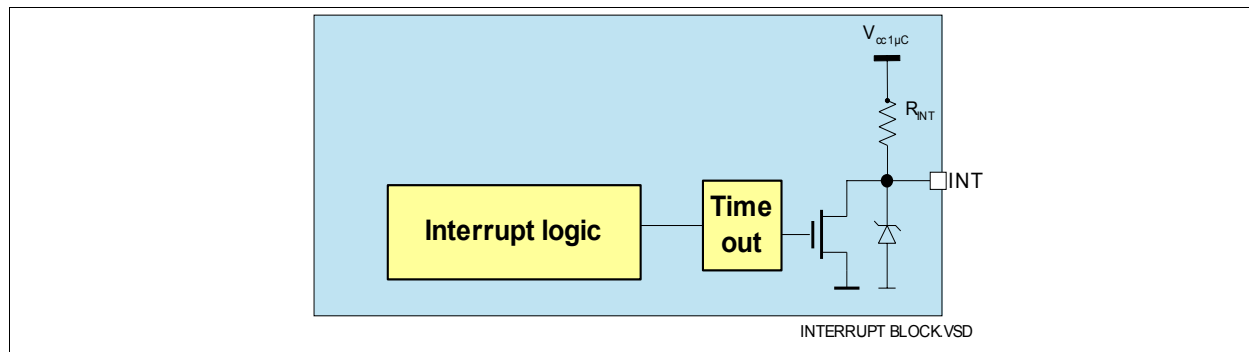
## 11 Interrupt Function

### 11.1 Interrupt Description

The interrupt pin has a general purpose function to point out to the microcontroller either a wake up, a failure condition or the switch on of a voltage regulator. **Table 9** shows the possible interrupt sources in the device, and **Figure 22** gives the hardware set-up. The interrupt function is designed to inform the microcontroller of any wake-up event, overtemperature or overtemperature pre-warning as well as other failures. These events turn the INT pin to active LOW. All interrupt sources can be masked via a SPI bit, then no interrupt is generated for this event. For failures on under-voltage the interrupt is dual-sensitive. This means that an interrupt is generated when the failure appears, as well as when the failure disappears. For failures on over-temperature, communication failures and voltage regulator over current and undervoltage, the dedicated SPI interrupt bit indicated first the interrupt source and then the state of the device. So, the bit is set to failure 1 at the event, and remains latched at least until the microcontroller reads the bit. For the SBC failure (Wrong WD Setting, Reset, Fail SPI) and wake events, the INT indicates only an event and the bit is cleared with a dedicated SPI read.

The INT pin is released when an SPI read is done to Interrupt Register 000 with a “Read Only” command, or after interrupt time out  $t_{INTTO}$ . If the interrupt cause was a wake event, the interrupt bit can be read in Interrupt Register 000 and the bit is cleared. If it was an other interrupt source the bit INT is set, and interrupt register 001 and 010 need to be read. With a “Read Only” command the event triggered interrupt bits are cleared. The INT bit will be set to “0” when all bits in interrupt register 001 and 010 are set to “0”. If an interrupt is masked (bit set to “0”) only the interrupt does not occur, the interrupt bit in the SPI is shown.

**Figure 22** shows a simplified diagram of the INT output. In Init Mode before RO goes high the INT pin is used to set the configuration of the device to config 1/3 or config 2/4, see **Chapter 13**.



**Figure 22** Interrupt Block Diagram

**Table 9** Interrupt sources

Interrupt sources	INT Activation	SPI bit	State
<b>Temperature</b>			
Over temperature pre-warning $V_{CC1\mu C}$	Rising	OTP $V_{CC1\mu C}$	Event / State
Over temperature $V_{CC2}$	Rising	OT $V_{CC2}$	
Over temperature HS CAN	Rising	OT HSCAN	
<b>Communication failure</b>			
CAN Failure	Rising	CAN Failure 1..0 CAN Bus	Event/ State
<b>Voltage regulator</b>			

**Table 9 Interrupt sources**

Interrupt sources	INT Activation	SPI bit	State
Undervoltage at $V_{CC2}$ (except during switch off <sup>1)</sup> )	Rising and falling	$UV_{VCC2}$	Event / State
Undervoltage at $V_{CC3}$ (except during switch off <sup>1)</sup> )	Rising and falling	$UV_{VCC3}$	
Over current at $V_{CC3}$ (except during inhibition)	Rising	$I_{CC3} > I_{CC3MAX}$	
Voltage at $V_{CC2}$ (during switch on <sup>1)</sup> )	Rising	$UV_{VCC2}$	Event
Voltage at $V_{CC3}$ (during switch on <sup>1)</sup> )	Rising	$UV_{VCC3}$	
<b>SBC Failure</b>			
SPI data corrupted	Rising	SPI Fail	Event
Reset (SBC SW Development only)	Rising	Reset	
Wrong watchdog setting	Rising	Wrong WD set	
<b>Wake</b>			
Wake at CAN	Rising	WK CAN	Event
Wake at WK	Rising	WK WK pin 1..0	
Cyclic WK	Rising	Cyclic WK	

1) When  $V_{CC2/3}$  is switched off no interrupt is generated due to the undervoltage at  $V_{CC2/3}$ . When switching on  $V_{CC2/3}$  an interrupt is generated when the command is sent to the SBC via SPI.

### 11.1.1 Interrupt for switching on Vcc2 and Vcc3

The Interrupt for Vcc2 and Vcc3 are generated when the SPI command for switching on the voltage regulator is executed. The interrupt bit is set to “1” and can be cleared with a Read Only command after the under voltage threshold is reached. If the Read Only is done before the reset threshold is reached, the interrupt bit can not be cleared as the undervoltage condition is still present. In this case a second interrupt can be issued for releasing the undervoltage condition.

In case of a short to GND on Vcc2 or Vcc3 the interrupt for switching on the voltage regulator is issued, but the  $\mu$ C can not clear the interrupt bit as the voltage regulator does not reach the undervoltage threshold.

### 11.1.2 Example of Interrupt Events and Read-out

The examples show single interrupt events. SPI read is done with “Read Only”. The shown interrupts are not masked. Watchdog trigger is not shown in the examples.

The interrupt  $UV_{Vcc2}$  that is generated by switching on  $V_{CC2}$  is shown in [Figure 23](#). The interrupt is sensitive on rising event only.

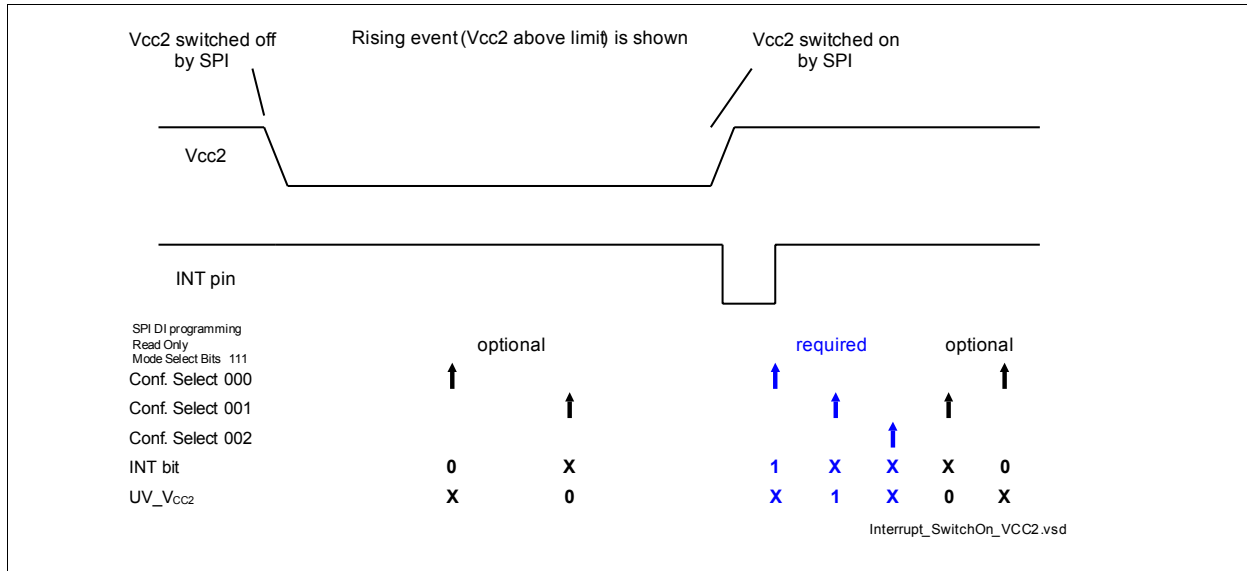
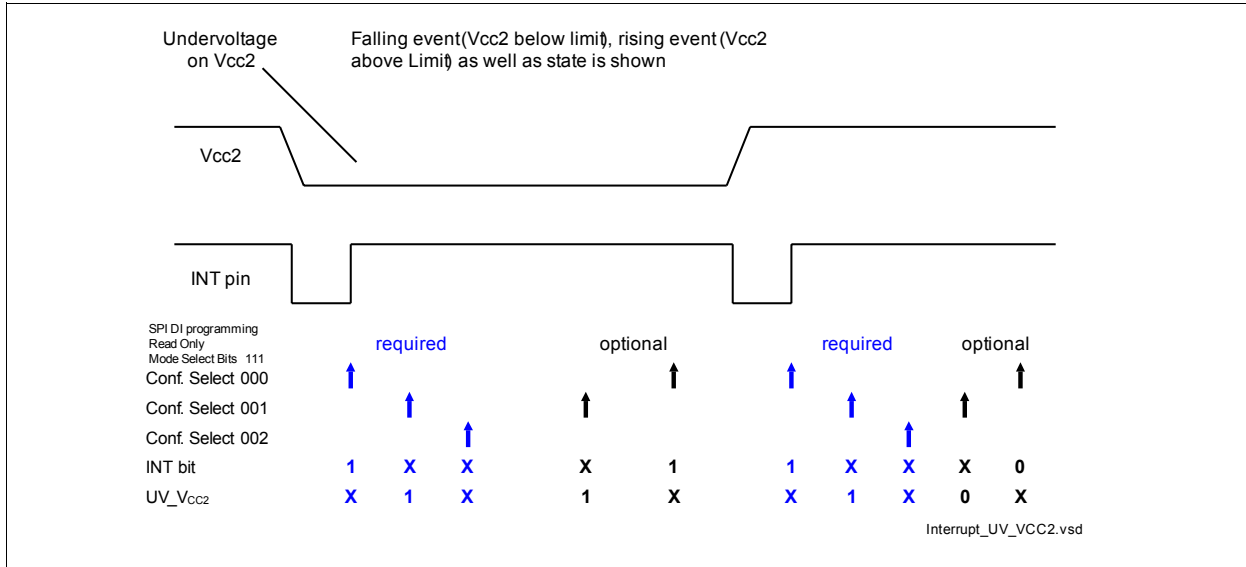


Figure 23 Interrupt Vcc2 switch-on.

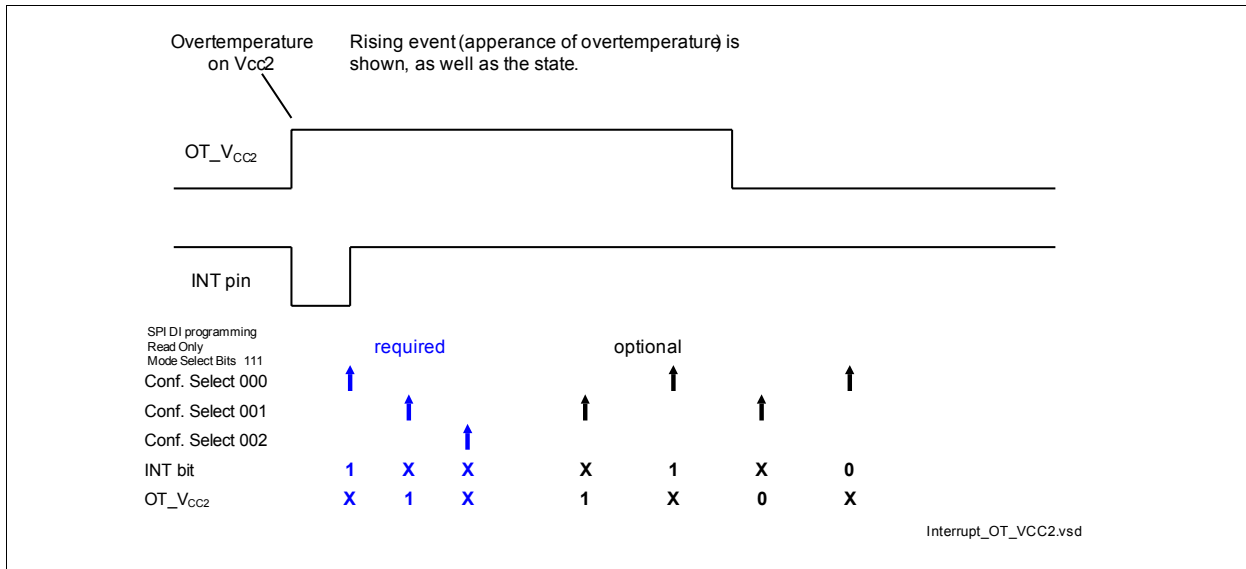
Interrupt Function

The interrupt UV\_Vcc2 that is generated by an under-voltage on  $V_{CC2}$  is shown in **Figure 24**. The interrupt is sensitive on rising and falling event and the interrupt bit also shows the state of the device and function.



**Figure 24** Interrupt  $V_{CC2}$  under-voltage.

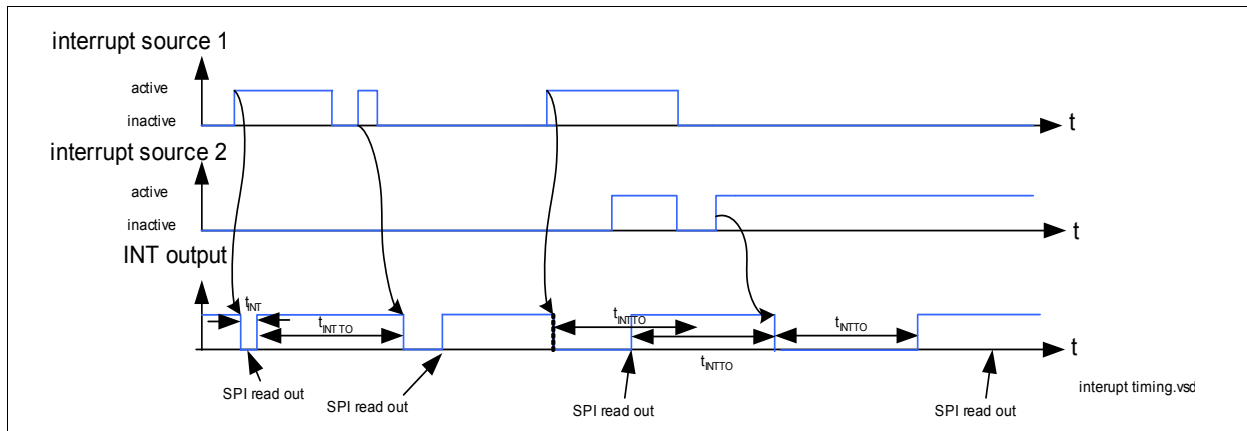
The interrupt OT\_Vcc2 that is generated by an over temperature on  $V_{CC2}$  is shown in **Figure 25**. The interrupt is sensitive on rising event and the interrupt bit also shows the state of the device and function.



**Figure 25** Interrupt  $V_{CC2}$  Over Temperature.

## 11.2 Interrupt Timing

**Figure 26** illustrates the interrupt timing. The INT output is set LOW as soon as an interrupt condition occurs. The INT pin is released after a SPI interrupt buffer read out command, that is performed with a Read Only command (111) to register (000). In case consecutive interrupt sources are indicated before the SPI read out, only one INT LOW will be raised but the SPI read out will indicate the interrupt sources. A time-out feature is implemented. The INT pin can be active LOW only for the time  $t_{INTTO}$ . Afterwards, the INT pin is released but the INT source is still valid or present in the SPI register. Between two activations of the INT, there is at least a delay of  $t_{INTTO}$ . If an interrupt occurs in the meantime, the information is stored and the INT will go LOW after  $t_{INTO}$ . The INT pulse width is at minimum  $t_{INT}$ .



**Figure 26** Interrupt Timing

## 11.3 Interrupt Modes with SBC Modes

The interrupt function is possible only in SBC Normal and Stop Mode. After an SBC Restart Mode, all interrupt sources are enabled.

## 11.4 Interrupt Application Information

By default, all interrupt sources are activated. Please refer to the dedicated chapter for the definition of the interrupt.

The INT output is active for at least  $t_{INT}$ , even if the corresponding interrupt register is read out immediately after the interrupt event occurs.

If no SPI read is done after the interrupt is generated (INT pin low) the INT output becomes active (INT pin high) again after  $t_{INTTO}$ .

If two interrupt cases occur after each other and the SPI read (with read-only) is done after the second interrupt case, both interrupt bits are cleared. Although the interrupt bits for both interrupt cases are cleared the second interrupt will be issued by INT pin Low. This can lead to an interrupt where all interrupt bits are read as "0".

## 11.5 Electrical Characteristics

$V_S = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Interrupt output; Pin INT</b>							
11.5.1	Interrupt delay Time-out	$t_{INTTO}$	5.4	6	6.6	ms	–
11.5.2	INT pulse width	$t_{INT}$	10	–	–	$\mu\text{s}$	1)
11.5.3	INT Low Output Voltage	$V_{INTOL}$	–	0.2	0.4	V	$I_{INT} = 1 \text{ mA}$
11.5.4	INT High Output Voltage	$V_{INTOH}$	$0.7 \times V_{CC1\mu\text{C}}$	–	$V_{CC1\mu\text{C}} + 0.3 \text{ V}$	V	$I_{INT} = -20\mu\text{A}$
11.5.5	INT Pull-up Resistor	$R_{INT}$	10	20	40	$\text{k}\Omega$	$V_{INT} = 0 \text{ V}$
<b>Configuration select; Pin INT</b>							
11.5.6	INT Config LOW input voltage	$V_{CFGLO}$	$0.3 \times V_{CC1\mu\text{C}}$	–	–	V	–
11.5.7	INT Config HIGH input voltage	$V_{CFGHI}$	–	–	$0.7 \times V_{CC1\mu\text{C}}$	V	–
11.5.8	INT Config pull down	$R_{CFG}$	–	250	–	$\text{k}\Omega$	–

1) Not subject to production test, specified by design.

## 12 Limp Home

### 12.1 Description

The Limp Home outputs are a very useful way to control safety critical functions independent of the microcontroller, such as turning on or off critical load during a microcontroller failure.

### 12.2 Limp Home output

The Limp Home output is an active LOW open drain transistor, please refer to [Figure 27](#); therefore, it is necessary to connect at least an external pull-up resistor at.

The Limp Home output is activated due to a failure condition or via SPI, see [Chapter 12.3](#). If  $V_s$  is below  $V_{LHUV}$ , the Limp Home cannot be activated and remains as a high impedance.

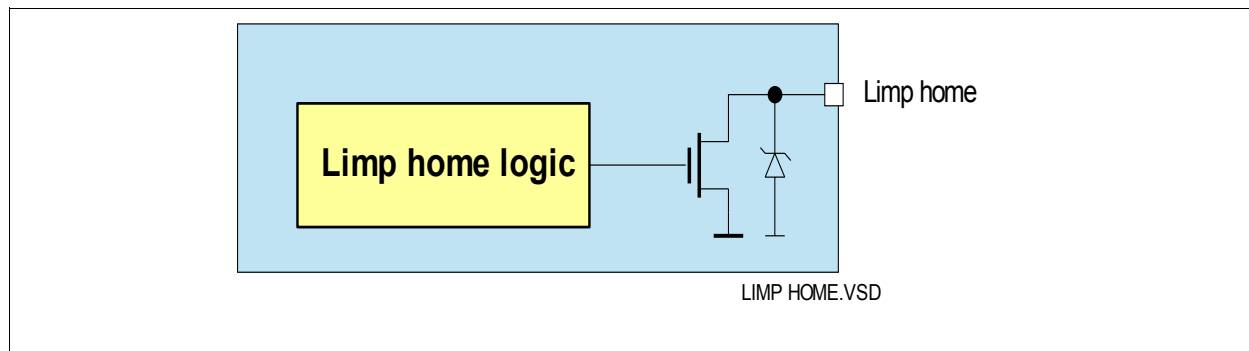


Figure 27 Limp Home block diagram

#### 12.2.1 Limp Home side indicators output

The LH\_SI output is similar to the Limp Home output. The output is pulsed to  $f_{LHSI}$  frequency with  $d_{SI}$  and designed to provide the side indicators frequency. The LH\_SI function is active when the Limp Home is active.

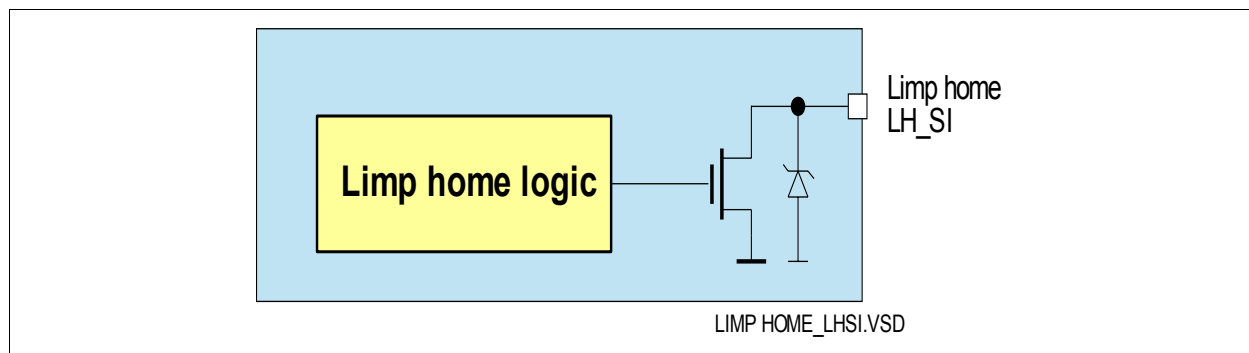


Figure 28 Limp Home LH\_SI block diagram

#### 12.2.2 LH\_PL (Pulsed Light) output

The LH\_PL/Test pin is an output pin shared with the Test pin function. During SBC Init Mode, the pin is used as an input, in all other modes, the pin is an output.

The output is pulsed to  $f_{LHPL}$  frequency with a duty cycle of  $d_{PL}$  (20% LOW, 80% high impedance), designed to dim the 27W stop lights into an 5W rear light. Refer to [Figure 29](#). The LH\_PL function is activated when the Limp Home is active. In SBC Init Mode, the LH\_PL is inhibited, to avoid a wrong set of the SBC into SBC Software development Mode.

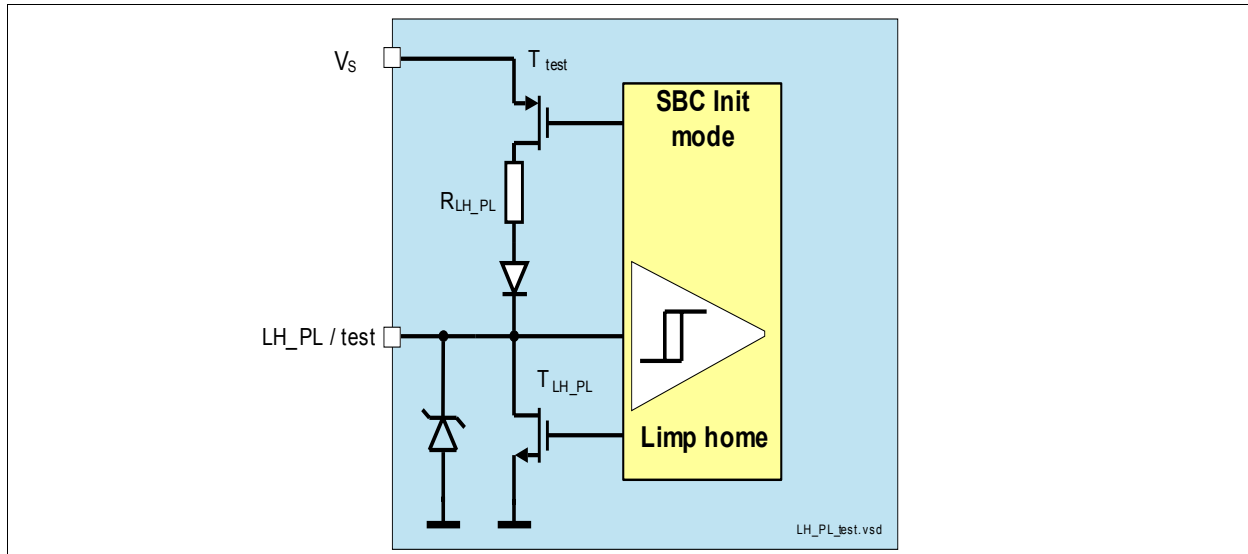


Figure 29 LH\_PL/ Test block diagram

### 12.2.3 Test Pin

The Test pin is used to set the SBC chip into SBC Software Development Mode. When the Test pin is connected to GND, the SBC starts in SBC Software Development Mode. When the pin is left open, or connected to  $V_S$  the SBC starts into normal operation. Please refer to [Figure 3](#). The Test pin has an integrated pull-up resistor (switched ON only during SBC Init Mode) to prevent the SBC device from starting in SBC Software Development Mode during normal life of the vehicle, as for example when the battery has been disconnected. To avoid disturbance, the Test pin is monitored during the Init Mode (from the time  $V_S > V_{UVON}$  until Init Mode is left). If the pin is low for the Init Mode time, Software Development Mode is reached. The mode is stored during the complete time where  $V_S$  is above  $V_{UVOFF}$ . It means to leave Software Development Mode, the SBC must go back to SBC OFF mode.



### 12.3 Activation of the Limp Home Output

The reason to activate the Limp Home pins and the consequences are listed in [Table 10](#) and [Table 11](#).

**Table 10 Limp Home, Function of the SBC Mode**

SBC Mode	Limp Home Outputs		
INIT Mode	OFF		
Normal Mode	OFF	ON via SPI	ON if it was ON until the successful Watchdog setting and deactivation via SPI.
Stop Mode	Unchanged		
Sleep Mode	Unchanged		
Restart Mode	Unchanged		
Fail-Safe Mode	ON		
SW Flash Mode	Unchanged		

**Table 11 Automatic Activation of Limp Home Output**

SBC Mode	Reason
INIT Mode	INIT time-out ( $t_{\text{INITTO}}$ )
Normal Mode	1st Watchdog failure (config 1/2) 2nd Watchdog failure (config 3/4)
Restart Mode	Reset output permanent short circuit to $V_{\text{cc}1\mu\text{C}}$
	Reset output permanent short circuit to GND
	$V_{\text{cc}1\mu\text{C}}$ undervoltage time-out
Any mode	If previously turned ON in SBC Normal Mode, via SPI command
	$V_{\text{cc}1\mu\text{C}}$ thermal shutdown

### 12.4 Release of the Limp Home Output

When Limp Home is activated via SPI command, then it is released via SPI command. This is useful for diagnosis purpose for example.

Otherwise, the Limp Home outputs are released only in SBC Normal Mode with the following conditions: After the device has been set to SBC Restart Mode, automatically entering SBC Normal Mode, a successful Watchdog trigger must be sent via SPI. At this point, the Limp Home outputs remain active. Then the microcontroller needs to send by SPI command the deactivation of the Limp Home.

### 12.5 $V_{\text{cc}1\mu\text{C}}$ undervoltage time-out

A  $V_{\text{cc}1\mu\text{C}}$  undervoltage time-out condition is given, when

- 1) the  $V_{\text{cc}1\mu\text{C}}$  output voltage is below the reset threshold ( $V_{\text{RT}1}$ ,  $V_{\text{RT}2}$ ,  $V_{\text{RT}3}$ ),
- 2)  $V_{\text{S}}$  is higher then the threshold ( $V_{\text{StHUV}1}$ ,  $V_{\text{StHUV}2}$ ,  $V_{\text{StHUV}3}$ ) and
- 3) the condition is valid longer then the  $V_{\text{cc}1\mu\text{C}}$  under voltage time-out ( $t_{\text{Vcc}1\mu\text{C}UVTO}$ ).

A  $V_{\text{cc}1\mu\text{C}}$  undervoltage time-out will sent the device into Fail-Safe Mode. Limp Home output stag will be activated (for  $V_{\text{S}} > V_{\text{LHUV}}$ )

[Figure 30](#) gives an example of the Limp Home output activation, due to a  $V_{\text{cc}1\mu\text{C}}$  undervoltage time-out.

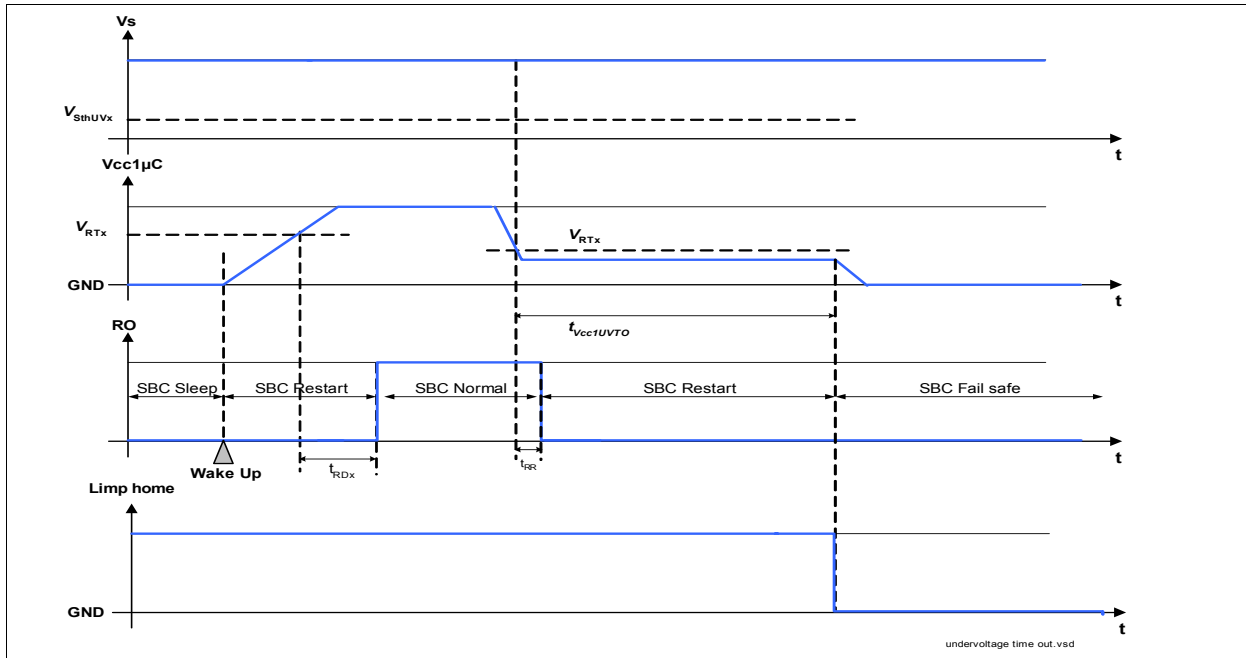


Figure 30  $V_{cc1\mu C}$  undervoltage time-out timing

## 12.6 Electrical Characteristics

$V_S = 5.5\text{ V to }28\text{ V}$ ;  $T_j = -40\text{ °C to }+150\text{ °C}$ ; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Limp Home;</b>							
12.6.1	Watchdog edge count difference to set Limp Home activated	$n_{LH}$	–	1 2	–	–	With SPI set. Default Setting
12.6.2	Limp Home low output voltage (active)	$V_{LHLO}$	–	0.2	0.4	V	$I_{LH} = 1\text{ mA}$
12.6.3	Limp Home high output current (inactive)	$I_{LHHI}$	0	–	2	$\mu\text{A}$	$V_{LH} = 28\text{ V}$
12.6.4	INIT Time-out	$t_{INITTO}$	–	256	–	ms	1)
12.6.5	$V_{CC1\mu C}$ under voltage Time-out	$t_{VCC1UVTO}$	900	1024	1150	ms	
12.6.6	$V_S$ threshold for $V_{CC1\mu C}$ under voltage Time-out ( $V_S$ needs to be above, to activate $V_{CC1\mu C}$ under voltage Time-out)	$V_{SthUV1}$	5.3	–	6.3	V	$V_{RT1}$ default setting
		$V_{SthUV2}$	4.3	–	5.3	V	$V_{RT2}$ SPI option
		$V_{SthUV3}$	4.0	–	5.0	V	$V_{RT3}$ SPI option
12.6.7	Threshold for Limp Home minimum $V_S$	$V_{LHUV}$	4.5	–	5.5	V	–
12.6.8	Limp Home $V_S$ voltage hysteresis	$V_{LHUVhys}$	–	0.2	–	V	–
<b>LH_SI;</b>							
12.6.9	Limp Home side indicator frequency	$f_{LHSI}$	1.125	1.25	1,375	Hz	–
12.6.10	Limp Home side indicator duty cycle	$d_{SI}$	–	50	–	%	–
<b>LH_PL/Test</b>							
12.6.11	HIGH Level Input Voltage Threshold	$V_{Test,HI}$	–	–	3	V	–
12.6.12	Input Hysteresis	$V_{Test,hys}$	100	300	700	mV	–
12.6.13	LOW Level Input Voltage Threshold	$V_{Test,LO}$	1	–	–	V	–
12.6.14	Pull-up Resistor	$R_{Test}$	20	40	80	k $\Omega$	$V_{LH\_PL/Test} = 0\text{ V}$ SBC Init Mode
12.6.15	Limp Home pulsed light frequency	$f_{LH\_PL}$	90	100	110	Hz	–
12.6.16	Limp Home pulsed light duty cycle	$d_{PL}$	–	20	–	%	–

1) Not subject to production test, specified by design.

## 13 Configuration Select

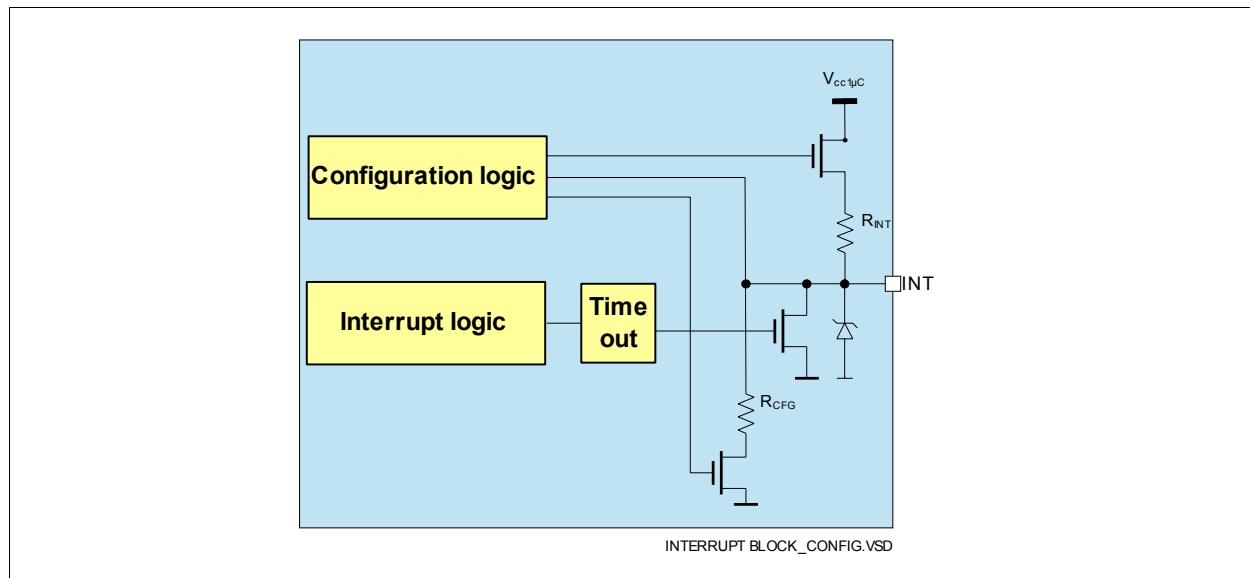
### 13.1 Configuration select

The Configuration select is used to set the device for two different SBC behaviors; please refer to [Chapter 4.2.1](#) for detailed information. Depending on the requirements of the application, the  $V_{cc1\mu C}$  is switched off and the device goes to Fail-Safe Mode in case of watchdog fail (1 or 2 fail) or reset clamped. To turn  $V_{cc1\mu C}$  OFF (Config 2/4), the INT pin is not connected to a pull up resistor externally. In case the  $V_{cc1\mu C}$  is not switched off (Config 1/3) the INT pin is connected to  $V_{cc1\mu C}$  with a pull up resistor. The configuration is only read during Init Mode, after that the configuration is stored.

### 13.2 Config Hardware Descriptions

In Init Mode before the RO pin goes high the INT pin is pulled to low with a weak pull down resistor  $R_{CFG}$ , the pull up resistor  $R_{INT}$  is switched off. When  $V_{cc1\mu C}$  is high, above the reset threshold  $V_{RT1}$  and before the RO pin goes high the level on the INT pin is monitored to select the configuration. With RO going high in Init Mode the pull up resistor  $R_{INT}$  is switched on.

[Figure 31](#) gives the electrical equivalents to the configuration function of the INT pin.



**Figure 31** Config Logic Diagram

Electrical characteristics are listed in chapter [Chapter 11.5](#)

## 14 Serial Peripheral Interface

### 14.1 SPI Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK supplied by the microcontroller. The output word appears synchronously at the data output SDO (see [Figure 32](#)).

The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read in becomes the new control word. The SDO output switches to tri-state status (high impedance) at this point, thereby releasing the SDO bus for other use.

The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The number of received input clocks is supervised by a modulo-16 operation and the Input / Control Word is discarded in case of a mismatch. This error is flagged in the following SPI output by a "HIGH" at the data output (SDO pin, bit FO) before the first rising edge of the clock is received. The SPI of the SBC is not daisy chain capable.

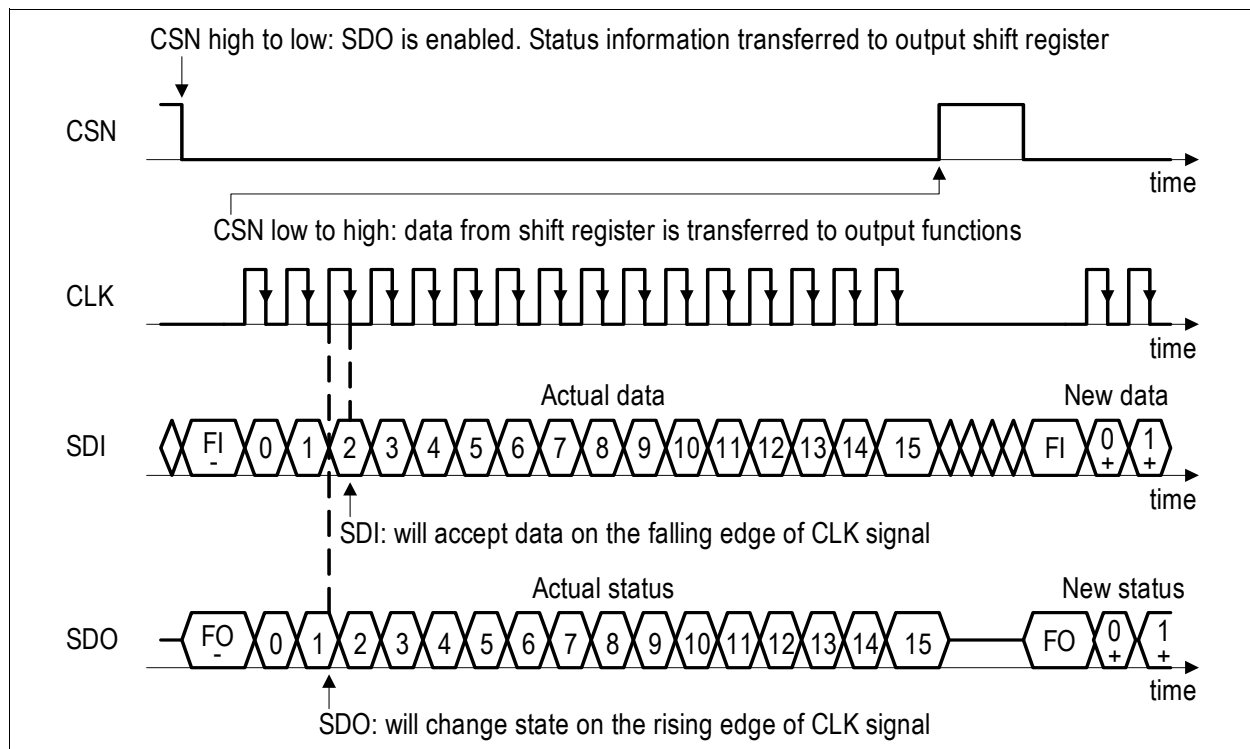


Figure 32 SPI Data Transfer Timing

### 14.2 Corrupted data in the SPI data input

When the microcontroller send a wrong SPI command to the SBC, the SBC ignores the information. Wrong SPI command can be either a number of bits different of 16, the mode selection (MS2..0) = 000 or requesting to go to an SBC mode which is not allowed by the state machine, for example from SBC Stop Mode to SBC SW Flash Mode. In that case, an interrupt is generated (if not inhibited) and the bit SPI Fail is set. Since the SPI data is corrupted, the next SPI output data will remain the former one (the information is then repeated).

14.3 SPI Input Data

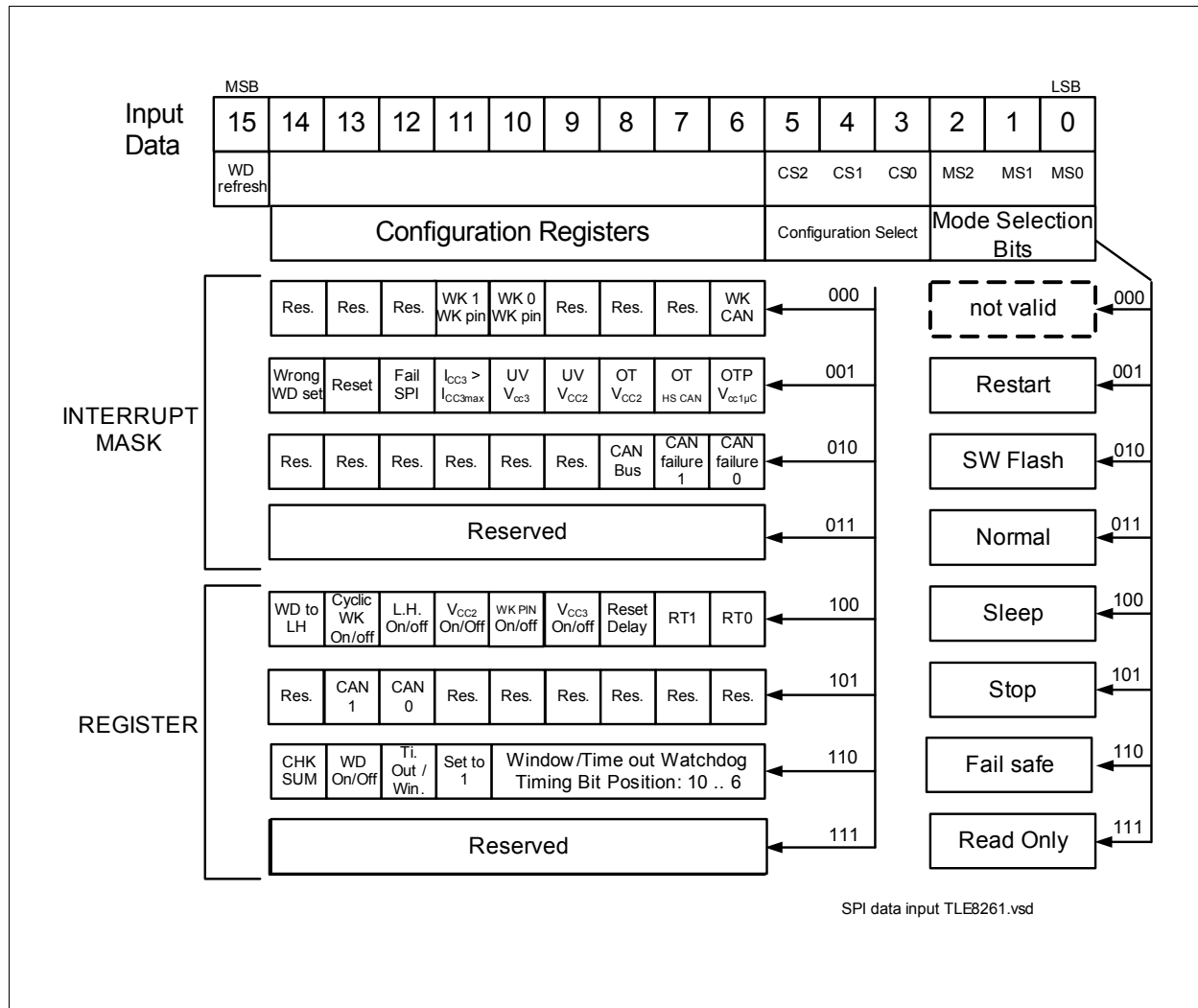
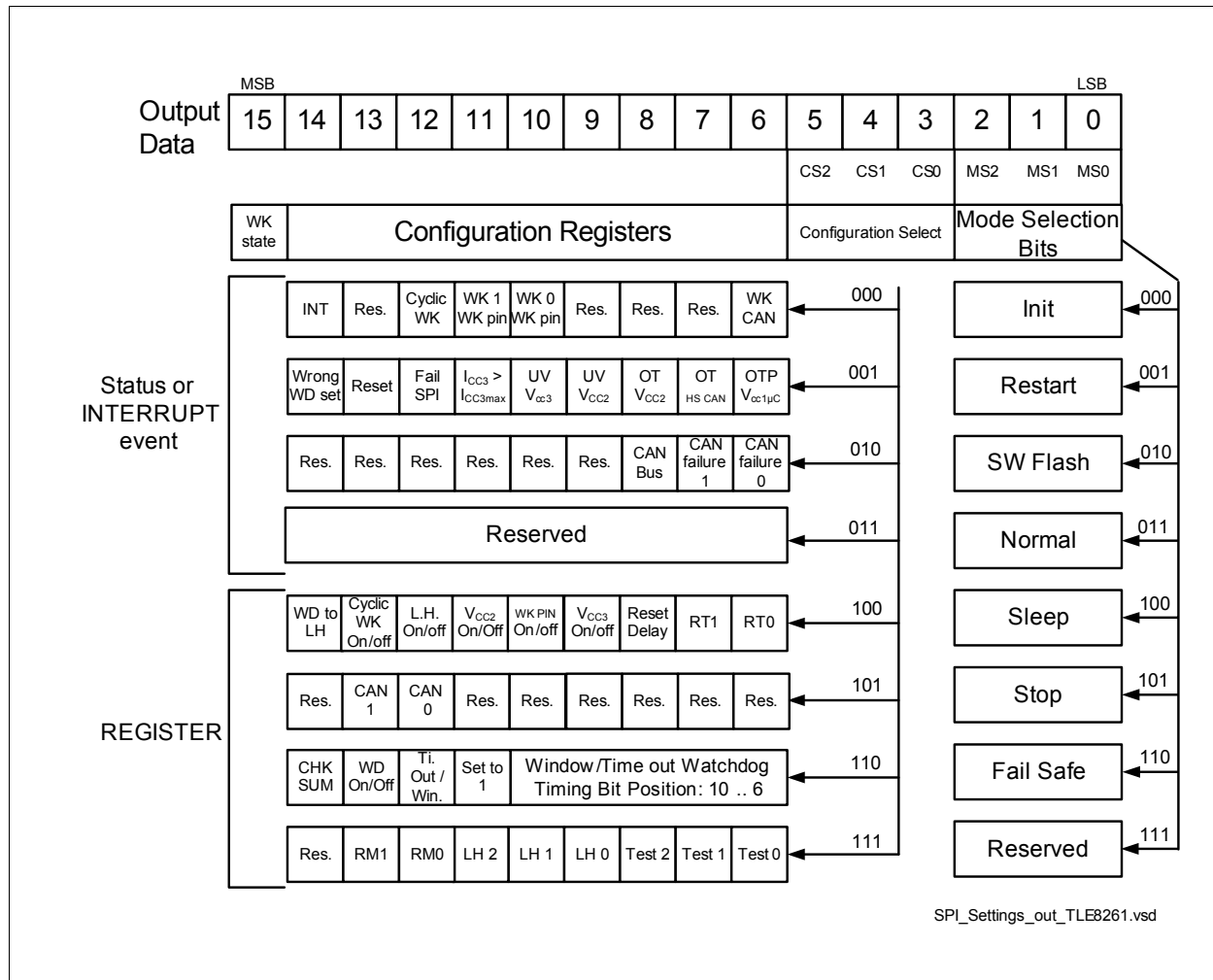


Figure 33 16-Bit SPI Input Data / Control Word

### 14.4 SPI Output Data



### 14.5 SPI Data Encoding

#### 14.5.1 WD Refresh bit / WK state

The WD Refresh bit is used to trigger the Watchdog. The first trigger should be a 1, and then a 0. For more details, please refer to [Chapter 10.2](#).

The WK state bit gives the voltage level at the WK pin. A 1 indicates a high level, a 0 a low level.

## 14.5.2 SBC Configuration Setting and Read Out

### 14.5.2.1 Mode selection bits and configuration select

**Table 12** lists the encoding of the possible SBC mode. Except SBC Restart and Init Mode which are most of time entered automatically, all others SBC mode are accessible on request of the microcontroller. The microcontroller should send the correct mode selection bits to set the SBC in the respective mode. The output indicates the SBC mode where the SBC currently is or was, depending on the situation.

**Table 12 Mode Selection Bits**

MS2	MS1	MS0	Data Input	Data Output
0	0	0	Not valid (the complete SPI word is ignored)	Show the device was in Init previous SPI data
0	0	1	Set the SBC to SBC Restart Mode. (In SW Flash mode only)	Show the device was in Restart previous SPI data
0	1	0	Set the SBC to Software Flash Mode	Show the device is SBC Software Flash Mode
0	1	1	Set the SBC to SBC Normal Mode	Show the device is in SBC Normal Mode
1	0	0	Set the SBC to SBC Sleep Mode	Show the device was in SBC Sleep Mode
1	0	1	Set the SBC to SBC Stop Mode	Show the device is in SBC Stop Mode
1	1	0	Set the SBC to SBC Fail-Safe Mode (In SBC Software Development mode only)	Show the device was in SBC Fail-Safe Mode
1	1	1	Set the SBC to Read Only SPI access. The configuration register needs to be selected. The SPI information on SDO is provided in the same SPI frame. No write access is done in this mode. Bit 15 (Watchdog) has to be served correctly.	Reserved

**Table 13** lists the eight possible configuration selection. Some are related to event or state of the different part of the SBC, others are used to configure the SBC in the application specific set up.

**Table 13 Configuration Select Encoder (for Data Input and Output)**

CS2	CS1	CS0	Configuration Register Select
0	0	0	Wake Register Interrupt
0	0	1	SBC Failure Interrupt
0	1	0	Communication Failure Interrupt
0	1	1	Reserved
1	0	0	SBC Configuration Register
1	0	1	Communication Setup Register
1	1	0	Watchdog Configuration Register
1	1	1	Limp Home / Diagnosis Register



### 14.5.2.2 Interrupt Register Encoder

**Table 14** lists all interrupts the SBC can generate. The microcontroller should read the correct register to release the INT pin. By default, all interrupt sources are enabled. The microcontroller can decide to inhibit a specific interrupt source.

**Table 14** Interrupt Register encoder <sup>1)</sup>

CS	Bit Name	Default Value (INPUT)	Default Value (OUT)	Data Input	Data Output
<b>Configuration select 000 (Wake register interrupt)</b>					
000	WK CAN	1	0	Interrupt enabled (1) disabled (0) for wake event on CAN	Wake on CAN (1)
	WK 1 WK pin WK 0 WK pin	11	00	Interrupt enabled (1) disabled (0) for wake pin event. 00 No interrupt 10 Interrupt for a LOW to HIGH transition on WK 01 Interrupt for HIGH to LOW transition on WK 11 Interrupt for both HIGH to LOW and LOW to HIGH on WK	Wake on WK pin 00 No wake 10 Interrupt for a LOW to HIGH transition on WK 01 Interrupt for HIGH to LOW transition on WK 11 Interrupt for both HIGH to LOW and LOW to HIGH on WK
	Cyclic WK	n.a	0	n.a	Cyclic WK (1)
	INT	n.a	0	n.a	Indicates that there is a status bit or uncleared event in configuration select 001 and/or 010. If set read the two register

**Table 14 Interrupt Register encoder (cont'd)<sup>1)</sup>**

CS	Bit Name	Default Value (INPUT)	Default Value (OUT)	Data Input	Data Output
<b>Configuration select 001 (SBC Failure interrupt)</b>					
001	OTP_V <sub>cc1μC</sub>	1	0	Interrupt enabled (1) disabled (0) for temperature pre-warning	V <sub>cc1μC</sub> temperature pre warning (1)
	OT_HSCAN	1	0	Interrupt enabled (1) disabled (0) for temperature shutdown	HS CAN temperature shutdown (1)
	OT_V <sub>cc2</sub>	1	0	Interrupt enabled (1) disabled (0) for temperature shutdown	V <sub>cc2</sub> temperature shutdown (1)
	UV_V <sub>cc3</sub>	1	0	Interrupt enabled (1) disabled (0) for undervoltage detection or due to back to normal voltage	Undervoltage detection on V <sub>cc3</sub> (1)
	SPI Fail	1	0	Interrupt enabled (1) disabled (0) for SPI corrupted data.	SPI input corrupted data (1)
	Reset	1	0	Interrupt enabled (1) disabled (0) for reset information (only in SBC Software Development Mode)	Reset (1) (only in SBC Software Development Mode)
	Wrong WD set	1	0	Interrupt enabled (1) disabled (0) for incorrect Watchdog setting	Incorrect WD programming for data output
	UV V <sub>cc2</sub>	1	0	Interrupt enabled (1) disabled (0) for undervoltage detection at V <sub>cc2</sub>	Under voltage detected at V <sub>cc2</sub>
	I <sub>CC3</sub> > I <sub>CC3max</sub>	1	0	Interrupt enable (1) disabled (0) for over current at V <sub>cc3</sub>	Over current detected at V <sub>cc3</sub>
<b>Configuration select 010 (Communication failure interrupt)</b>					
010	CAN failure 1	n.a	0	Interrupt enabled (1) disabled (0) for CAN failure	CAN failure Refer to <a href="#">Table 15</a>
	CAN failure 0	1	0		
	CAN Bus	1	0	Interrupt enabled (1) disabled (0) for CAN bus failure	CAN bus failure detected (1)

1) A value of 0 will set the SBC into the opposite state.

### 14.5.2.3 CAN failure encoder

Table 15 describes the encoding of the possible internal CAN failures.

Table 15 CAN Failure Encoder

CAN 1 Failure	CAN 0 Failure	Fault
0	0	No failure
0	1	TxD shorted to GND or bus dominant clamped
1	0	RxD shorted to $V_{cc}$
1	1	TxD shorted to RxD

### 14.5.2.4 Configuration encoder

Table 16 lists the configuration register of the SBC. The microcontroller can change the settings. If no settings are changed the default values are used. The current value can be read on the SPI Data Out.

Table 16 Configuration Encoder

Configuration Select	Bit Name	Default Value (INPUT)	Default Value (OUT)	State
<b>Configuration select 100 (SBC Configuration Register)</b>				
100	RT10	01	01	Reset threshold setting. Please refer to <a href="#">Table 17</a>
	Reset delay	1	1	Long reset window
	$V_{cc3}$ ON / OFF	0	0	$V_{cc3}$ is activated (1)
	WK pin ON / OFF	1	1	The wake pin will wake the SBC
	$V_{cc2}$ On / Off	0	0	$V_{cc2}$ is activated (1)
	LH ON / OFF	0	0	Limp Home output state. Activated (1) when entry condition is met.
	Cyclic WK On / Off	0	0	Activation (1) of the cyclic wake
	WD to LH	1	1	Watchdog failure to Limp Home active. 0 = only one Watchdog failure brings to Limp Home activated. 1 = two consecutive Watchdog failures bring to Limp Home activated.

**Table 16 Configuration Encoder**

Configuration Select	Bit Name	Default Value (INPUT)	Default Value (OUT)	State
<b>Configuration select 101 (SBC communication set up register)</b>				
	CAN 1.0	00	00	The CAN cell is in: 00 = CAN OFF 01 = CAN is Wake Capable 10 = CAN Receive Only Mode 11 = CAN Normal Mode
<b>Configuration select 110 (SBC Watchdog register)</b>				
110	Ti. Out / Win.	1	1	Time-out Watchdog is activated
	Set to 1	1	1	Bit is reserved and fix set to "1". Set to 1 in SW.
	WD ON / OFF	1	1	Watchdog is activated
	CHK SUM	1	1	Check sum of the bit 13...6 In case the CHK SUM is wrong, the device remains in previous valid state. $\text{CHKSUM} = \text{Bit13} \oplus \dots \oplus \text{Bit6}$
<b>Configuration select 111 (Limp Home / Diagnosis register)</b>				
111	-			Reserved for input For output, refer to <a href="#">Table 19</a> , <a href="#">Table 20</a> and <a href="#">Table 21</a>

### 14.5.2.5 Reset encoder

[Table 17](#) lists the three possible reset thresholds. Please also refer to [Chapter 10.3](#) to get the exact voltage threshold.

**Table 17 Reset Encoder**

RT1	RT0	Threshold Selected
0	0	Not Valid. Device remains at previous threshold
0	1	VRT1 (default setting at SBC Init),
1	0	VRT2
1	1	VRT3

### 14.5.2.6 SBC Watchdog encoder

[Table 18](#) list the 32 possible watchdog timer.

**Table 18 Watchdog Encoder**

Bit 10...6	Decimal	calculation (ms)	Timer (ms)
00000	0	$(n+1) \times 16$	16
00001	1	n = decimal value of setting	32
00010	2		48
...	...		...
01111	15		256 (default setting)

**Table 18 Watchdog Encoder**

Bit 10...6	Decimal	calculation (ms)	Timer (ms)
10000	16	n × 48 - 464	304
10001	17		352
...	...		...
11110	30		976
11111	31		1024

### 14.5.3 SBC Diagnostic encoder

The SBC offers diagnostics information. The encoding of the different possible failures are listed in the following table. The description apply only to data output.

#### 14.5.3.1 Reason for restart and reset

Reason for reset, without activation of the Limp Home and the way it is encoded are summed up in [Table 19](#). The bits are cleared by reading the register with Read-Only command. When coming from Sleep Mode or Fail Safe Mode the bits are cleared.

**Table 19 Reason to Enter SBC Restart Mode without Limp HomeLimp Home activation**

RM1	RM0	Cause for entering SBC Restart Mode
0	0	No reset has occurred or Limp Home activated
0	1	Undervoltage on $V_{cc1\mu C}$
1	0	First Watchdog failure (config 3 and 4) or no acknowledge of the Cyclic Wake-up
1	1	SPI command in SBC Software Flash Mode or reset low from outside

### 14.5.3.2 Limp Home failure encoder

**Table 20** describes the encoding of all possible reason to activate automatically the Limp Home output. Bits are set back to “000” when switching Limp Home off via SPI.

**Table 20 Limp Home Failure Diagnosis**

LH2	LH1	LH0	Failure <sup>1)</sup>
0	0	0	No failure
0	0	1	$V_{cc1\mu C}$ undervoltage Time-out
0	1	0	One Watchdog failure (config 1 and 2)
0	1	1	Two consecutive Watchdog failures (config 3 and 4)
1	0	0	INIT Mode Time-out
1	0	1	Temperature shutdown at $V_{cc1\mu C}$
1	1	0	Reset clamped
1	1	1	Reserved

### 14.5.3.3 Test pin and failure to Limp Home configuration read out

The SBC allows to read the hardware setting of the configuration that is done via the INT pin, as well as the test pin and the WD to LH bit. **Table 21** describes the encoding of these informations.

**Table 21 Test pin and SBC Configuration**

Test2	Test1	Test0	Test Read Out <sup>1)</sup>
0	0	0	$V_{cc1\mu C}$ remains ON in SBC Restart Mode after one Watchdog failure (config 1)
0	0	1	$V_{cc1\mu C}$ is OFF in SBC Fail-Safe Mode after one Watchdog failure (config 2)
0	1	0	$V_{cc1\mu C}$ remains ON in SBC Restart Mode after two Watchdog failures (config 3)
0	1	1	$V_{cc1\mu C}$ is OFF in SBC Fail-Safe Mode after two Watchdog failures (config 4)
1	0	0	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.
1	0	1	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.
1	1	0	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.
1	1	1	Software Development Mode. In case of watchdog failure $V_{cc1\mu C}$ remains ON, no reset is generated and Restart Mode or Fail-Safe Mode are not entered.

1) Refer also to [Chapter 4.2.1](#)

## 14.6 SPI Output Data

### 14.6.1 First SPI output data

Since the SPI output data is sent when the SBC is receiving data, the output data are dependent of the previous SPI command, if no Read Only command is used. Under some conditions there is no “previous command”. **Table 22** gives the first SPI output data that is sent to the microcontroller when entering SBC Normal Mode, depending on the mode where the SBC was before receiving the first SPI command.

**Table 22 First SPI output data frame**

Previous SBC mode	Mode selection bits (MS2...0)	Configuration select (CS 2..0)
Sleep mode	Sleep mode	Wake Register interrupt <sup>1)</sup>
Fail-Safe mode	Fail-Safe mode	Limp Home register <sup>1)</sup>
Restart mode when failure and config 1 / 3	Restart mode	Limp Home register <sup>1)</sup>
Restart mode when microcontroller has sent to Restart mode	Restart mode	SBC Configuration Register
SBC Init mode	Init mode	SBC Configuration Register

1) This does not clear the bits. It will be reset when the microcontroller requests the read out

### 14.6.2 Read Only command

In the Mode Selection Bits a Read Only can be selected. The Read Only access clears the INT bits that are selected in the Configuration Select (some interrupt bits show a state, and can not be cleared with a SPI read). With this SPI command no write access is done to the SBC, and the mode of the SBC is not changed. The watchdog can also be triggered with a Read Only command.

The Read Only command delivers the information requested with the Configuration Select in the same SPI command on the SDO pin. As all other SPI commands deliver the requested information with the next SPI command.

Figure 34 shows an example of a Read Only access. The bits are shown with LSB first, on the left side in difference to the register description.

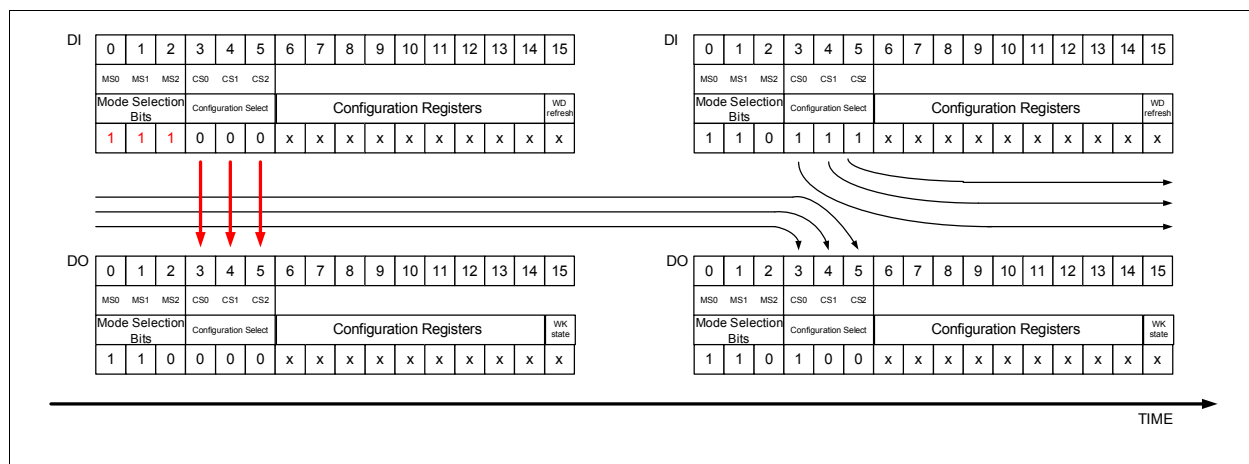


Figure 34 Read Only Command

Figure 35 shows an example of an SPI write access in normal mode for comparison. The requested information is sent out with the next SPI command.



Figure 35 Write Command



### 14.7 Electrical Characteristics

$V_S = 5.5 \text{ V to } 28 \text{ V}$ ;  $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		

#### SPI Interface; Logic Inputs SDI, CLK and CSN

14.7.1	H-input Voltage Threshold	$V_{IH}$	–	–	$0.7 \times V_{CC1\mu C}$	V	–
14.7.2	L-input Voltage Threshold	$V_{IL}$	$0.3 \times V_{CC1\mu C}$	–	–	V	–
14.7.3	Hysteresis of input Voltage	$V_{IH\Delta}$	–	$0.12 \times V_{CC1\mu C}$	–	V	-1)
14.7.4	Pull-up Resistance at pin CSN	$R_{ICSN}$	20	40	80	k $\Omega$	$V_{CSN} = 0.7 \times V_{CC1\mu C}$
14.7.5	Pull-down Resistance at pin SDI and CLK	$R_{ICLK/SDI}$	20	40	80	k $\Omega$	$V_{SDI/CLK} = 0.2 \times V_{CC1\mu C}$
14.7.6	Input Capacitance at pin CSN, SDI or CLK	$C_1$	–	10	–	pF	-1)

#### Logic Output SDO

14.7.7	H-output Voltage Level	$V_{SDOH}$	$V_{CC1\mu C} - 0.4$	$V_{CC1\mu C} - 0.2$	–	V	$I_{DOH} = -1.6 \text{ mA}$
14.7.8	L-output Voltage Level	$V_{SDOL}$	–	0.2	0.4	V	$I_{DOL} = 1.6 \text{ mA}$
14.7.9	Tri-state Leakage Current	$I_{SDOLK}$	-10	–	10	$\mu\text{A}$	$V_{CSN} = V_{CC1\mu C}$ ; $0 \text{ V} < V_{DO} < V_{CC1}$
14.7.10	Tri-state Input Capacitance	$C_{SDO}$	–	10	15	pF	1)

#### Data Input Timing<sup>1)</sup>

14.7.11	Clock Period	$t_{pCLK}$	250	–	–	ns	–
14.7.12	Clock High Time	$t_{CLKH}$	125	–	–	ns	–
14.7.13	Clock Low Time	$t_{CLKL}$	125	–	–	ns	–
14.7.14	Clock Low before CSN Low	$t_{bef}$	125	–	–	ns	–
14.7.15	CSN Setup Time	$t_{lead}$	250	–	–	ns	–
14.7.16	CLK Setup Time	$t_{lag}$	250	–	–	ns	–
14.7.17	Clock Low after CSN High	$t_{beh}$	125	–	–	ns	–
14.7.18	SDI Set-up Time	$t_{DISU}$	100	–	–	ns	–
14.7.19	SDI Hold Time	$t_{DIHO}$	50	–	–	ns	–

### 14.7 Electrical Characteristics (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C to }+150\text{ }^\circ\text{C}$ ; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
14.7.20	Input Signal Rise Time at pin SDI, CLK and CSN	$t_{rIN}$	–	–	50	ns	–
14.7.21	Input Signal Fall Time at pin SDI, CLK and CSN	$t_{fIN}$	–	–	50	ns	–
14.7.22	Delay Time for Mode Change from Normal Mode to Sleep Mode	$t_{flIN}$	–	–	10	$\mu\text{s}$	–
14.7.23	CSN High Time	$t_{CSN(\text{high})}$	10	–	–	$\mu\text{s}$	–

#### Data Output Timing 1)

14.7.24	SDO Rise Time	$t_{rSDO}$	–	30	80	ns	$C_L = 100\text{ pF}$
14.7.25	SDO Fall Time	$t_{fSDO}$	–	30	80	ns	$C_L = 100\text{ pF}$
14.7.26	SDO Enable Time	$t_{ENSDO}$	–	–	50	ns	low impedance
14.7.27	SDO Disable Time	$t_{DISSDO}$	–	–	50	ns	high impedance
14.7.28	SDO Valid Time	$t_{VASDO}$	–	–	60	ns	$C_L = 100\text{ pF}$

1) Not subject to production test; specified by design

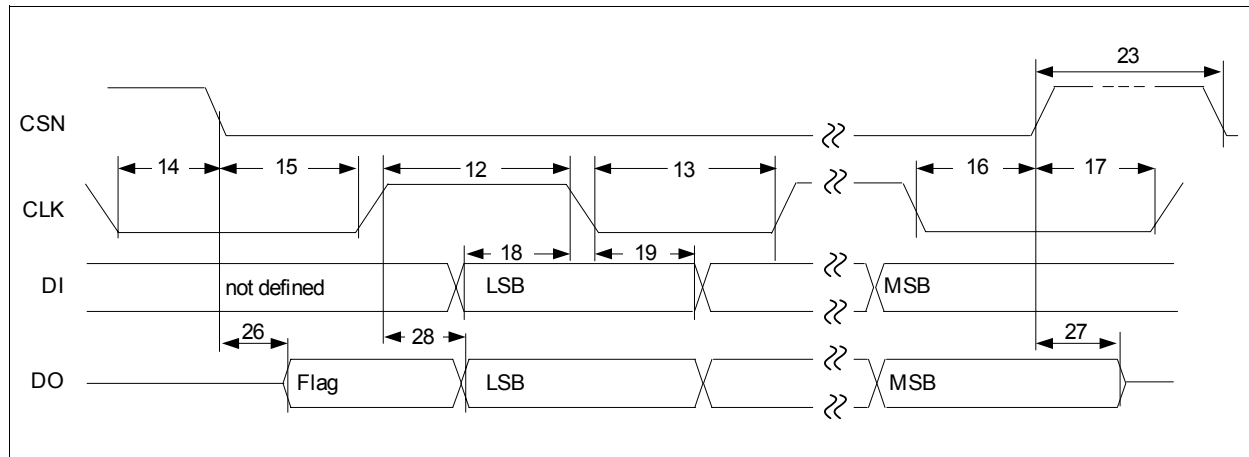


Figure 36 SPI Timing Diagram

Note: Numbers in drawing correlate to the last 2 digits of the Pos. number in the Electrical Characteristics table.



**Application Information**

*Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.*

**Table 23 Bills of material**

Ref.	Option	Vendor	Value	Purpose
<b>Capacitance</b>				
C1	Y	Kemet	68 $\mu$ F optional depending on application	Cut off battery spike
C2	Y		100nF	EMC
C3	N	Murata	10 $\mu$ F ceramic cap low ESR	Stability of the $V_{CC3}$
C7	Y		22nF 50V	EMC
C8	Y		47nF OEM dependent	Improve SPLIT pin stability
C9	Y		10 $\mu$ F	Buffer of the $V_{CC1\mu C}$ depending on load. ( $\mu$ C)
C10	N		100nF	Stability of the $V_{CC1\mu C}$
C11	N		10 $\mu$ F CAN transceiver dependent	Buffering of the $V_{CC2}$ for CAN Transceiver
C12	Y		100nF	Improve stability of the logic
C13	Y		100nF	Improve stability of the logic
C14	Y		100nF	Improve stability of the logic
<b>Resistance</b>				
R1	N		220m $\Omega$	$V_{CC3}$ current measurement for $I_{CC3}$ 400mA max
R5	Y		1k $\Omega$	Wetting current of the switch
R7	Y		60 $\Omega$ / OEM dependent	CAN bus termination
R8	Y		60 $\Omega$ / OEM dependent	CAN bus termination
R9	Y		10k $\Omega$	Limit the WK pin current in ISO pulses
R10	Y		500 $\Omega$	Insulation of the VDD supply
R12	Y		47k $\Omega$	Set config 1/3. If not connected config 2/4 is selected

**Table 23 Bills of material**

Ref.	Option	Vendor	Value	Purpose
<b>Active components</b>				
T1	N	ON Semi	MJD253	Power element of $V_{CC3}$
		Infineon	BCP52-16	Alternative power element of $V_{CC3}$ , current limit to be adapted R1 to be changed.
T2	N	Infineon	BCR191W	High active Limp Home
T3	N	Infineon	BCR191W	High active Limp Home
T4	N	Infineon	BCR191W	High active Limp Home
D1	N	Infineon	BAS 3010A	Reverse polarity protection
$\mu$ C	N	Infineon	XC2xxx	micro-controller
IC1	Y	Infineon	SPOC - BTS5672E	high side switches
IC2	Y	Infineon	TLE 6254-3G	Low speed CAN
IC3	Y	Infineon	TLE 6251DS	High speed CAN

15.1 ZthJA Curve

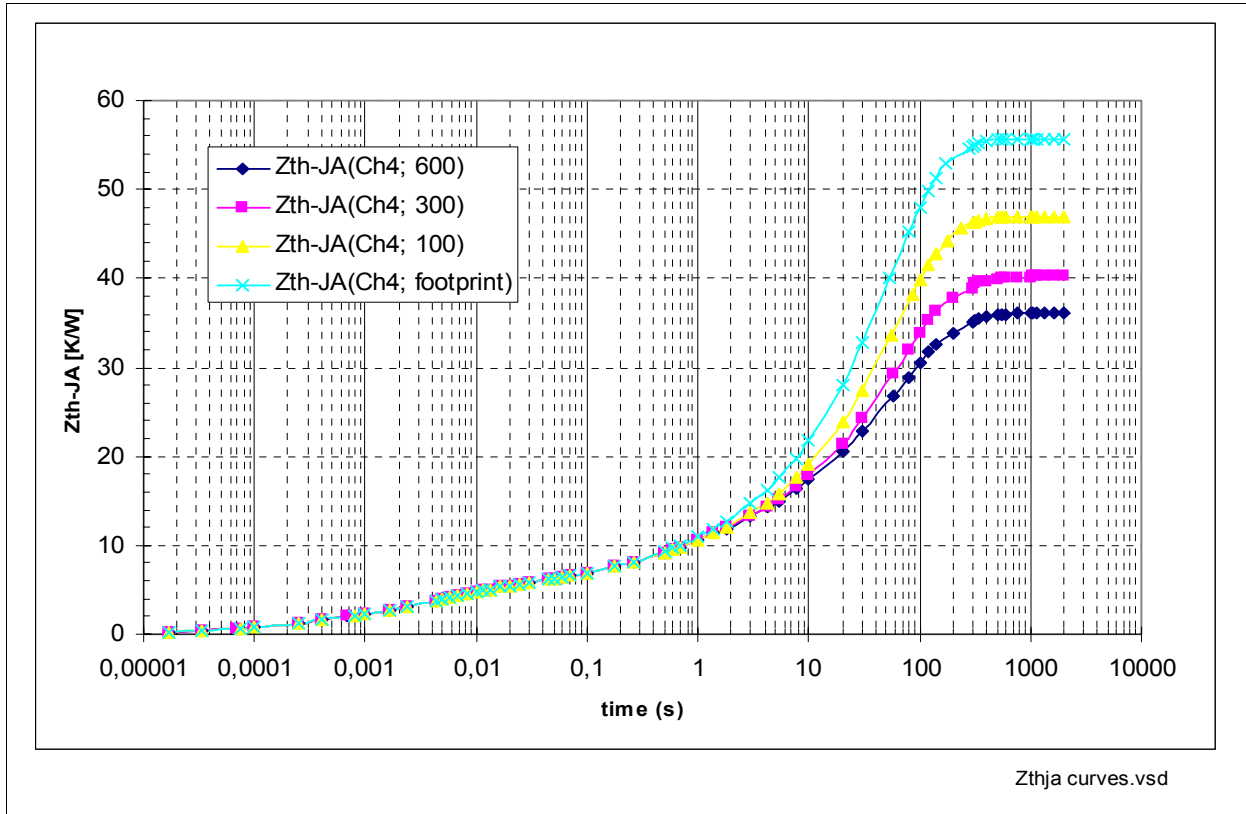


Figure 38 ZthJA Curve, Function of Cooling Area

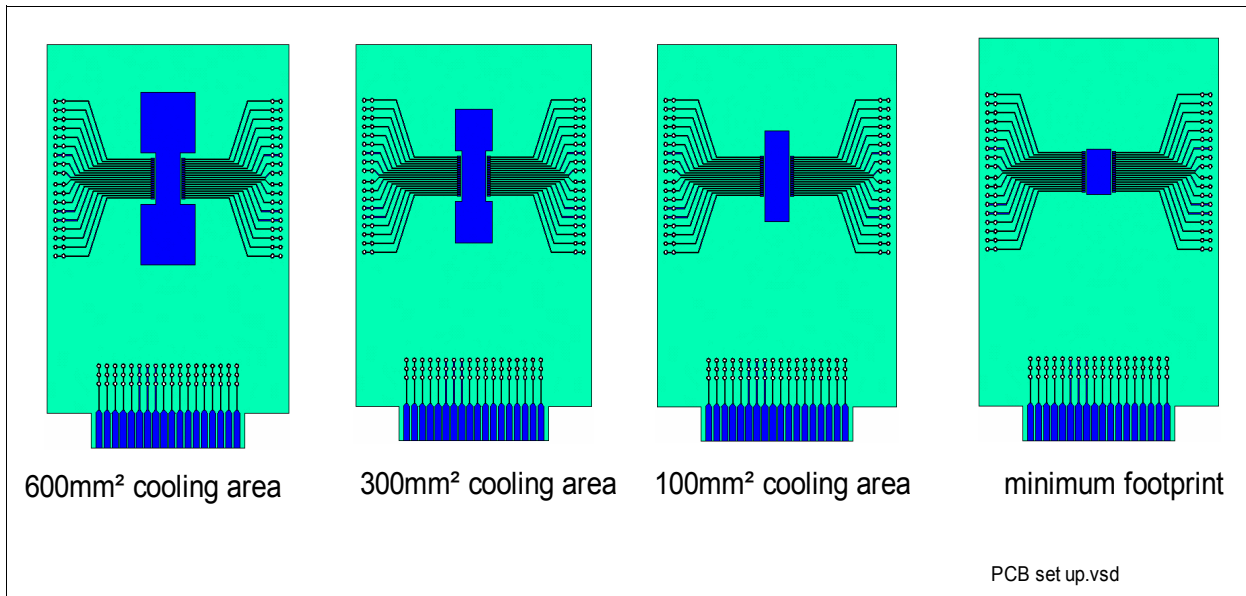


Figure 39 Board Set-up

Board set-up is done according to JESD 51-3, single layer FR4 PCB 70 μm.

### 15.2 Hints for SBC Factory Flash Mode

The mode is used during production of the module to flash the  $\mu\text{C}$ . The idea is that the  $\mu\text{C}$  is not supplied from the SBC but from an external 5V power supply. The reset of the  $\mu\text{C}$  that is connected to the RO pin of the SBC can be driven from an external source and the SBC does not give a reset signal. Also no interrupt at the pin INT and no signal on the SPI SDO pin is generated by the SBC. The SPI pins can be driven externally.

The mode is reached by applying 5V to the  $V_{\text{CC1}\mu\text{C}}$  pin and no voltage to the  $V_{\text{s}}$  pin. The  $V_{\text{s}}$  pin will show a voltage of about 4.5V because of the internal diode from  $V_{\text{CC1}\mu\text{C}}$  to  $V_{\text{s}}$ . The current drawn at  $V_{\text{s}}$  must not exceed the maximum rating of  $I_{\text{vs,max}} = -500\text{mA}$ . The function is designed for ambient temperature.

In case the  $V_{\text{s}}$  was supplied before going to FF Mode, the voltage on pin  $V_{\text{s}}$  must be set below 3 V before applying 5V to  $V_{\text{CC1}\mu\text{C}}$  (discharging the C)

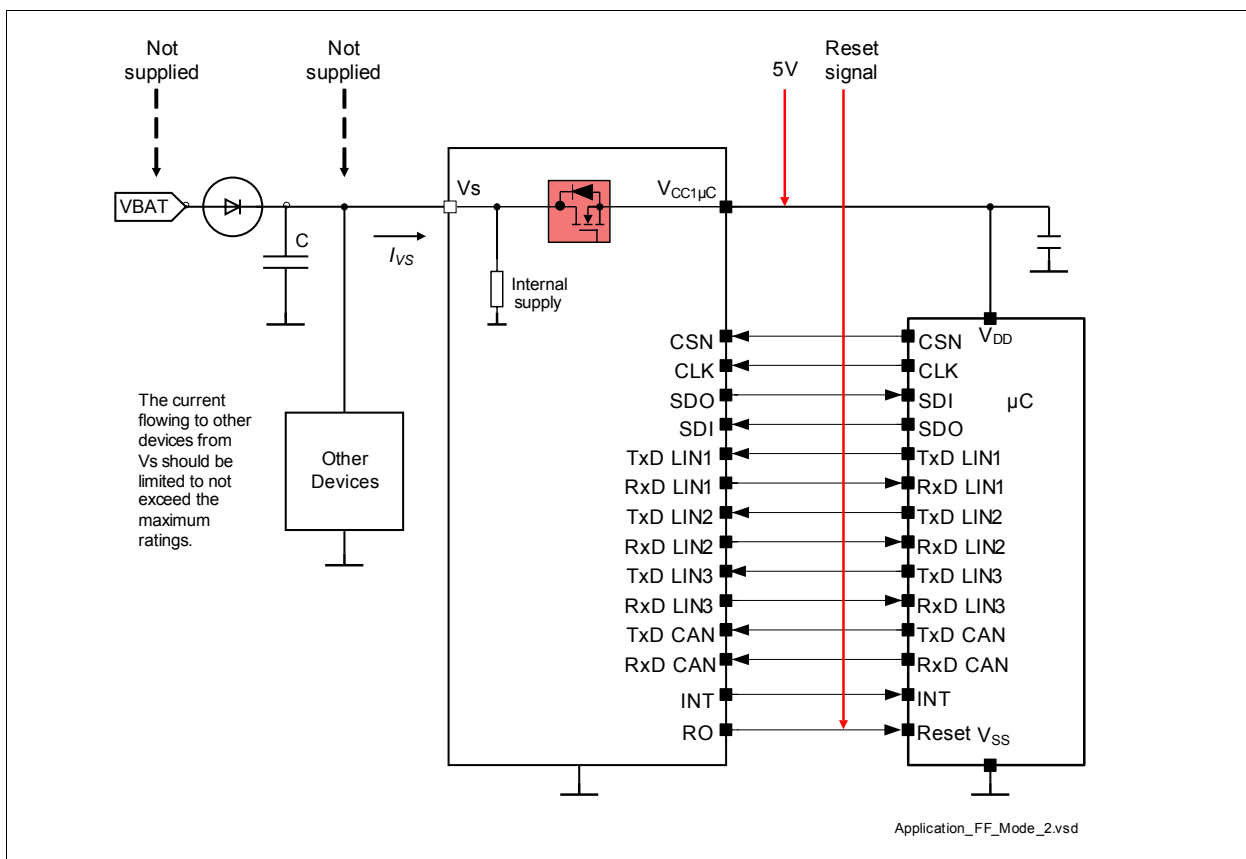


Figure 40 Application Hint for Factor Flash Mode

**Table 24 PIN in Factory Flash Mode**

Pin	Level	Comment
Vs	typ. 4.5V	Voltage output from SBC. No voltage applied from external.
Vcc1 $\mu$ C	5V $\pm$ 2%	To be applied from external
RO	Pull-up resistor	Can be driven from external
INT	Pull-up resistor	Can be driven from external if required
LH	High impedance	Can be driven from external if required
SDO	High impedance	Can be driven from external if required
CLK, SDI	Pull-down resistor	Can be driven from external if required
CSN	Pull-up resistor	Can be driven from external if required
TxDCAN, TxDLIN1, TxDLIN2, TxDLIN3	Pull-up resistor	Can be driven from external if required
RxDCAN, RxDLIN1, RxDLIN2, RxDLIN3	High impedance	Can be driven from external if required

### 15.3 ESD Tests

Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330 $\Omega$ ) have been performed. The results and test condition is available in a test report. The values for the test are listed in [Table 25](#) below.

**Table 25 ESD “Gun test”**

Performed Test	Result	Unit	Remarks
ESD at pin CANH, CANL, BUSx, Vs versus GND	> 8	kV	positive pulse <sup>1)</sup>
ESD at pin CANH, CANL, BUSx, Vs versus GND	< -8	kV	negative pulse

1) ESD susceptibility “ESD GUN” contact discharge (R=330 $\Omega$  C=150pF) (DIN EN 61000-4-2) tested according LIN EMC 1.3 Test Specification and ICT EMC Evaluation of CAN Transceiver. Tested by external test house (IBEE Zwickau, EMC Test report Nr. 06-02-09a)



16 Package Outline

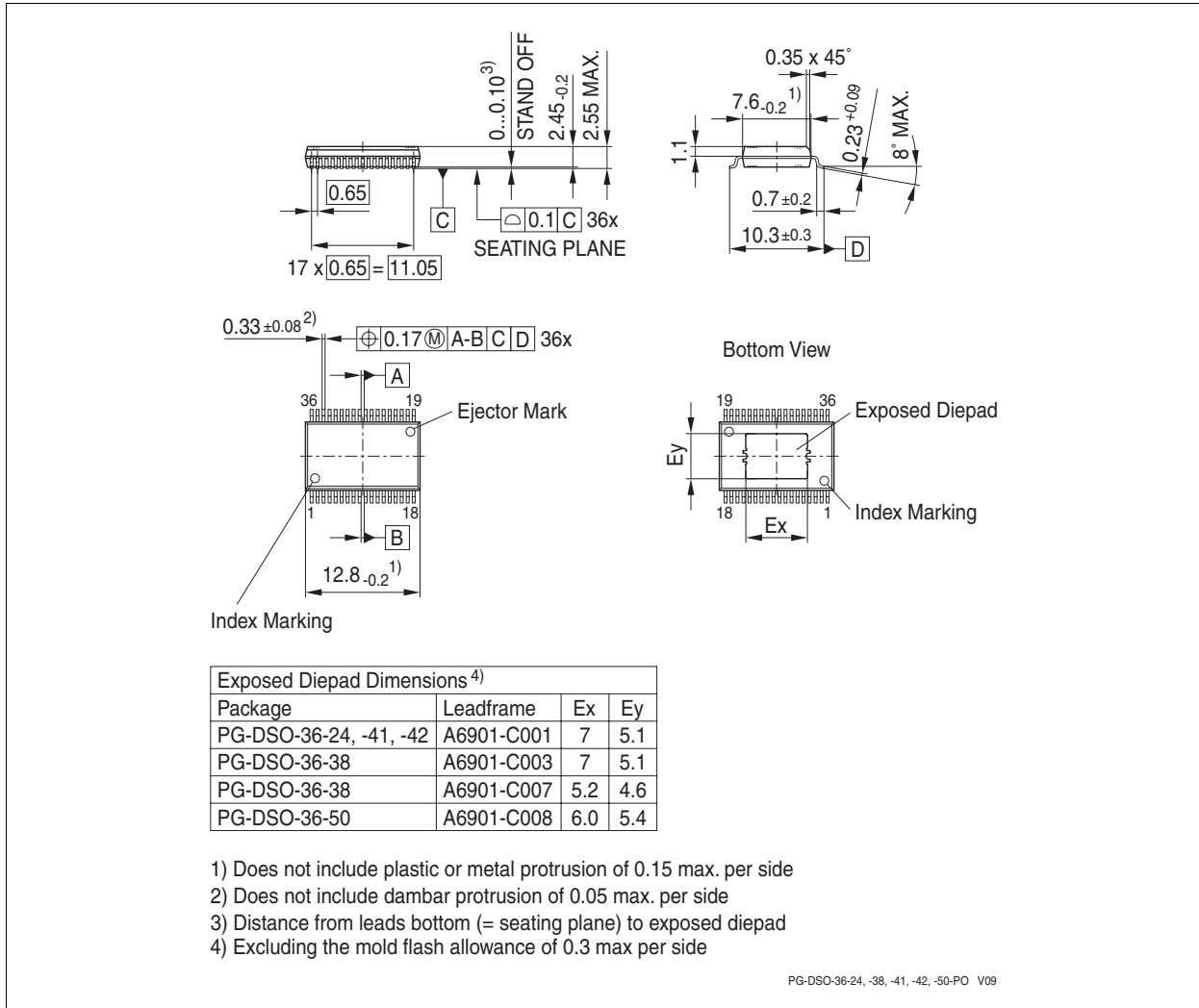


Figure 41 PG-DSO-36-38 (Leadframe A6901-003);

Note: For the SBC product family the package PG-DSO-36-38 with the leadframe A6901-C003 is used.

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the Universal System Basis Chip is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For information about packages and types of packing, refer to the Infineon Internet Page "Products": <http://www.infineon.com/products>.

Dimensions in mm

## 17 Revision History

Version	Date	Parameter	Changes
1.0	2009-05-25		First Rev. of Data Sheet

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