FAIRCHILD SEMICONDUCTOR®

March 2011

# FDT86113LZ

## N-Channel PowerTrench® MOSFET

### 100 V, 3.3 A, 100 mΩ

## Features

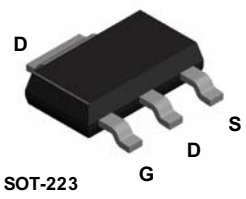
- Max $r_{DS(on)}$ = 100 mΩ at $V_{GS}$ = 10 V, $I_D$ = 3.3 A
- Max $r_{DS(on)}$ = 145 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 2.7 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- HBM ESD protection level > 3 KV typical (Note 4)
- 100% UIL tested
- RoHS Compliant

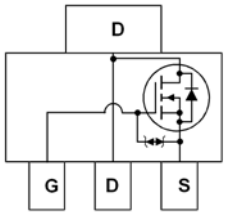
## General Description

This N-Channel logic Level MOSFETs are produced using Fairchild Semiconductor's advanced Power Trench® process that has been special tailored to minimize the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

## Application

- DC - DC Switch




## MOSFET Maximum Ratings $T_C$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 100 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous | | | 3.3 | A |
| | -Pulsed | | | 12 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 9 | mJ |
| $P_D$ | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.2 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1b) | 1.0 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 12 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 55 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 86113LZ | FDT86113LZ | SOT-223 | 13 ” | 12 mm | 2500 units |

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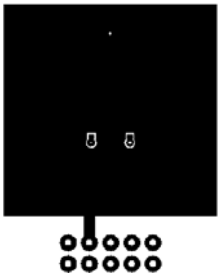
## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

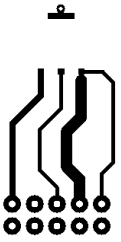
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 100 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 71 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.0 | 1.7 | 2.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -5 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.3 A | | 75 | 100 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 2.7 A | | 95 | 145 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 3.3 A, $T_J$ = 125 °C | | 140 | 189 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 3.3 A | | 8 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | | 234 | 315 | pF |
| $C_{oss}$ | Output Capacitance | | | 46 | 65 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 3.1 | 5 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 3.3 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 3.8 | 10 | ns |
| $t_r$ | Rise Time | | | 1.3 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 10 | 20 | ns |
| $t_f$ | Fall Time | | | 1.5 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 50 V, $I_D$ = 3.3 A | | 4.1 | 6.8 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 5 V; $V_{DD}$ = 50 V, $I_D$ = 3.3 A | | 2.3 | 3.9 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | $V_{DD}$ = 50 V, $I_D$ = 3.3 A | | 0.68 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 50 V, $I_D$ = 3.3 A | | 0.85 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 3.3 A (Note 2) | | 0.86 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 1 A (Note 2) | | 0.77 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 3.3 A, di/dt = 100 A/μs | | 31 | 49 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 21 | 34 | nC |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 55 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper



b) 118 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25°C, L = 0.3 mH, $I_{AS}$ = 8 A, $V_{DD}$ = 90 V, $V_{GS}$ = 10 V.

4. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.



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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

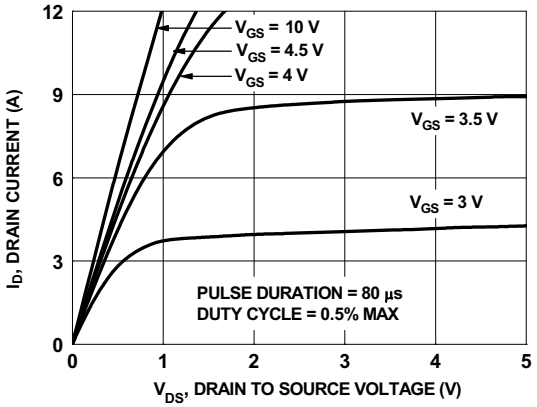


**Figure 1. On-Region Characteristics**

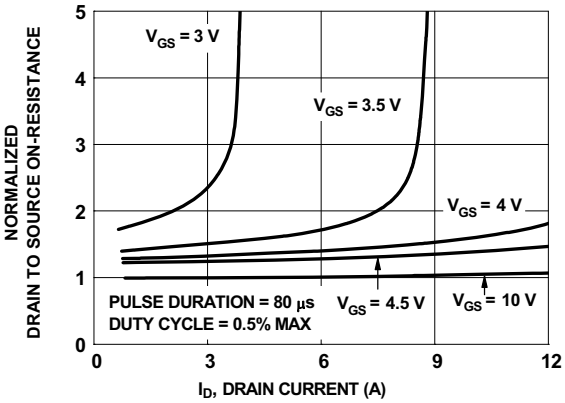


**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

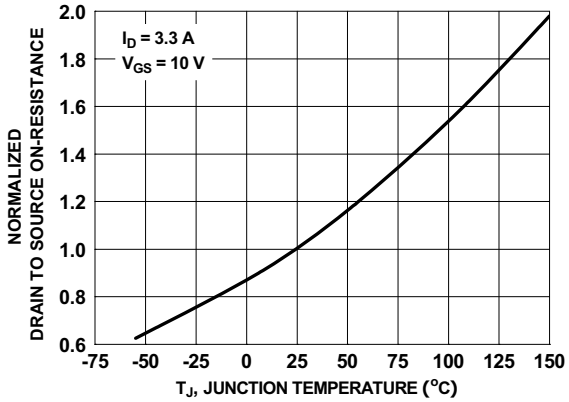


**Figure 3. Normalized On-Resistance vs Junction Temperature**

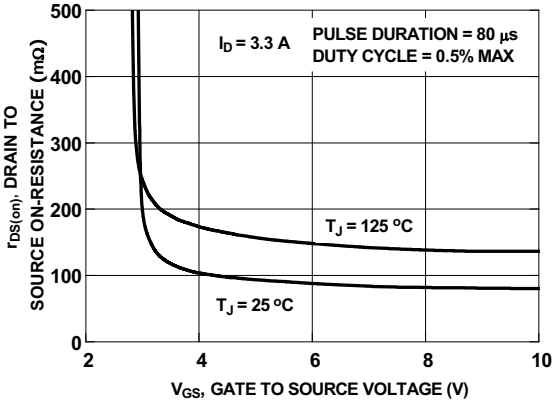


**Figure 4. On-Resistance vs Gate to Source Voltage**

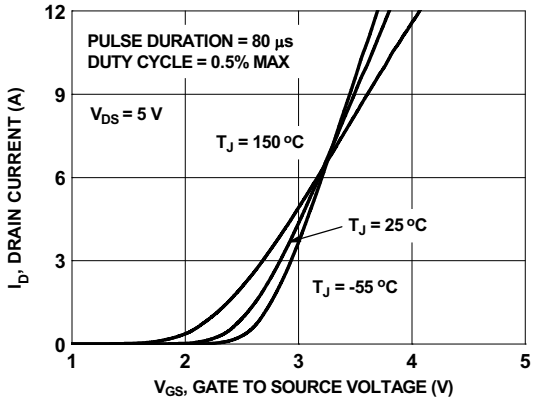


**Figure 5. Transfer Characteristics**

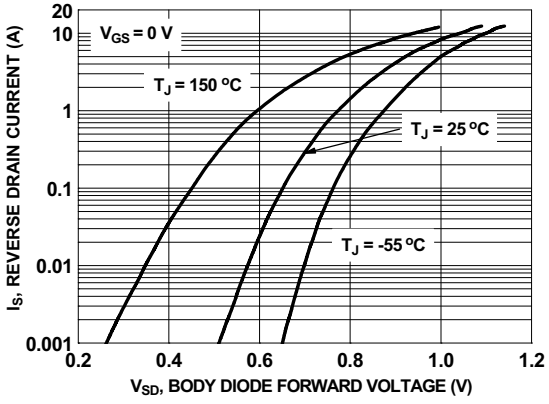


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**



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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

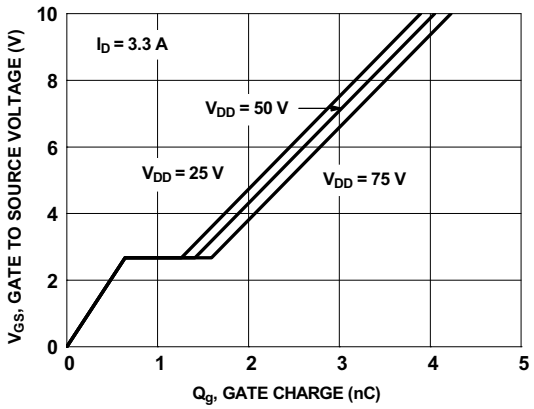


Figure 7. Gate Charge Characteristics

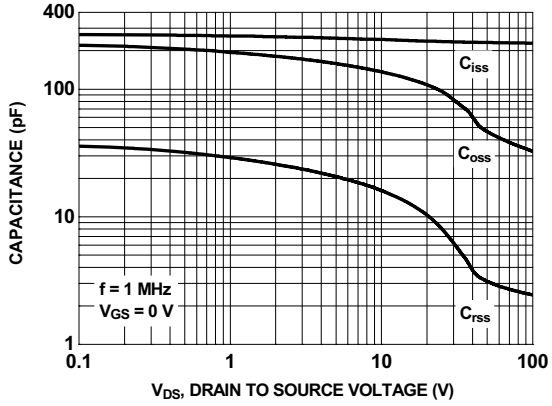


Figure 8. Capacitance vs Drain to Source Voltage

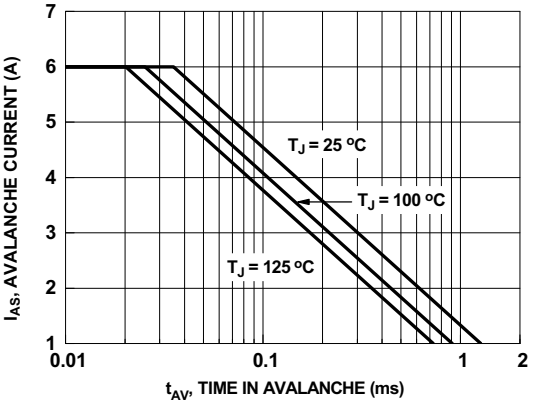


Figure 9. Unclamped Inductive Switching Capability

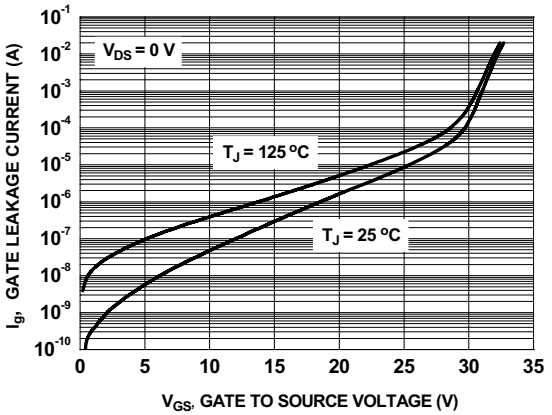


Figure 10. Gate Leakage Current vs Gate to Source Voltage

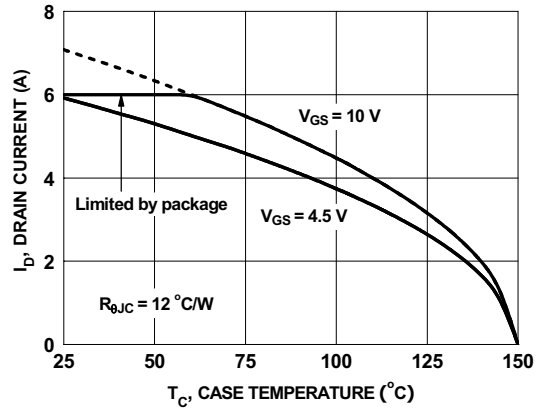


Figure 11. Maximum Continuous Drain Current vs Case Temperature

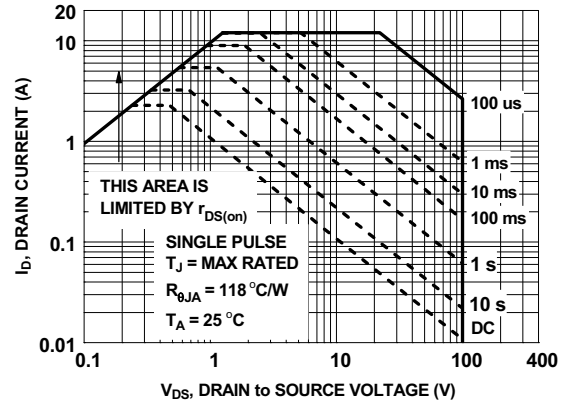


Figure 12. Forward Bias Safe Operating Area



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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

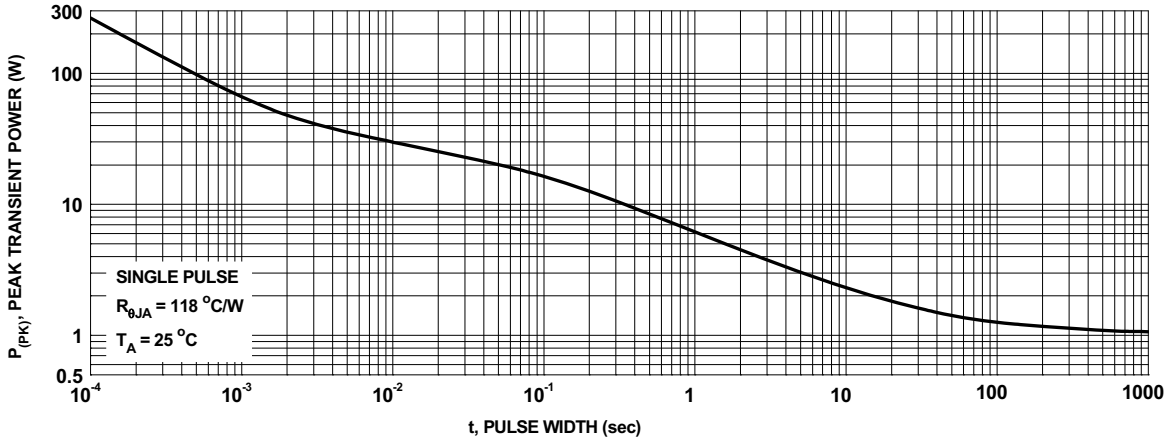


**Figure 13. Single Pulse Maximum Power Dissipation**

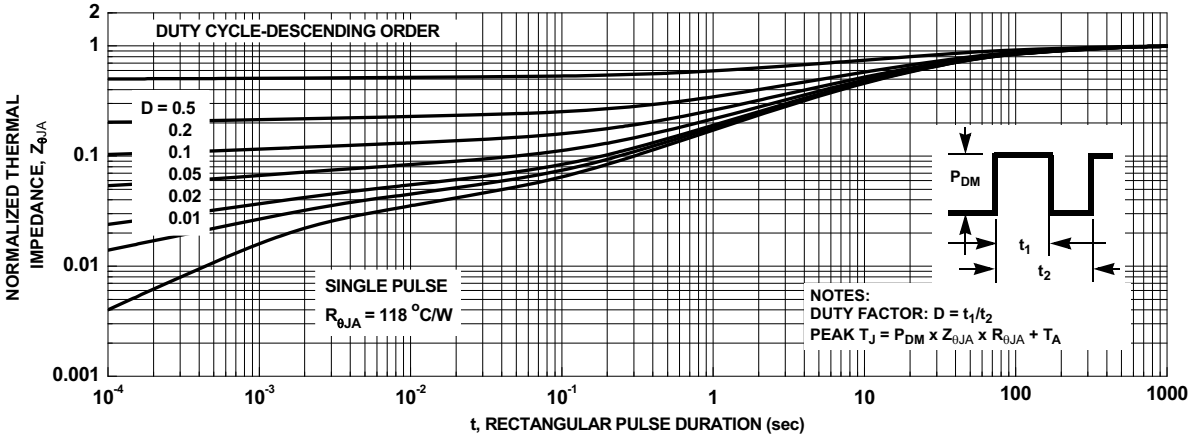


**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**



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