

# FDS86140

## N-Channel PowerTrench® MOSFET

100 V, 11.2 A, 9.8 mΩ

### Features

- Max  $r_{DS(on)}$  = 9.8 mΩ at  $V_{GS} = 10$  V,  $I_D = 11.2$  A
- Max  $r_{DS(on)}$  = 16 mΩ at  $V_{GS} = 6$  V,  $I_D = 9$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- RoHS Compliant

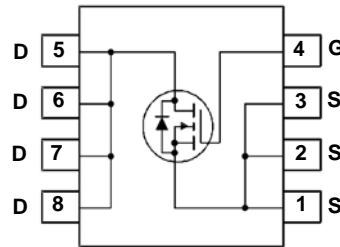
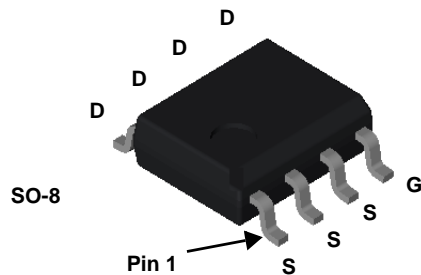


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Applications

- DC/DC Converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	11.2	A
	-Pulsed	50	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	264	mJ
$P_D$	Power Dissipation $T_C = 25$ °C (Note 1)	5.0	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS86140	FDS86140	SO-8	13"	12 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		70		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2	2.7	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-11		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 11.2\text{ A}$		8.1	9.8	m $\Omega$
		$V_{GS} = 6\text{ V}, I_D = 9\text{ A}$		10.8	16	
		$V_{GS} = 10\text{ V}, I_D = 11.2\text{ A}, T_J = 125\text{ }^\circ\text{C}$		13.1	17	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 11.2\text{ A}$		35		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1940	2580	pF
$C_{oss}$	Output Capacitance			440	585	pF
$C_{rss}$	Reverse Transfer Capacitance			20	30	pF
$R_g$	Gate Resistance			0.9		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 11.2\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		13.7	25	ns	
$t_r$	Rise Time			5.6	11	ns	
$t_{d(off)}$	Turn-Off Delay Time			23	38	ns	
$t_f$	Fall Time			4.8	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		29	41	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 5\text{ V}$		16.5	23	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50\text{ V}, I_D = 11.2\text{ A}$		8.0		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			6.5		nC	

### Drain-Source Diode Characteristics

$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 11.2\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 11.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		53	85	ns
$Q_{rr}$	Reverse Recovery Charge			59	94	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50\text{ }^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b)  $125\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 23\text{ A}$ ,  $V_{DD} = 90\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

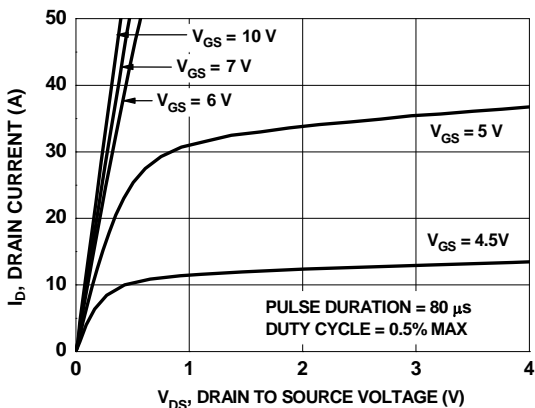


Figure 1. On Region Characteristics

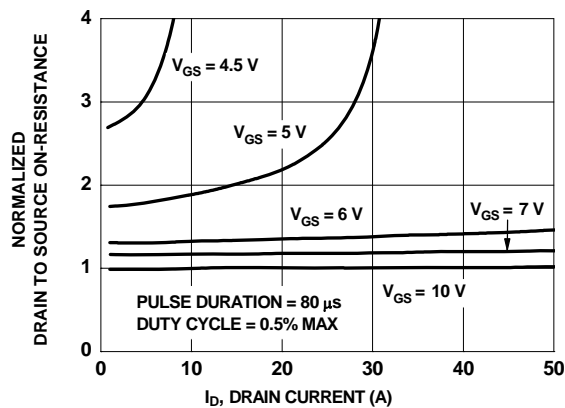


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

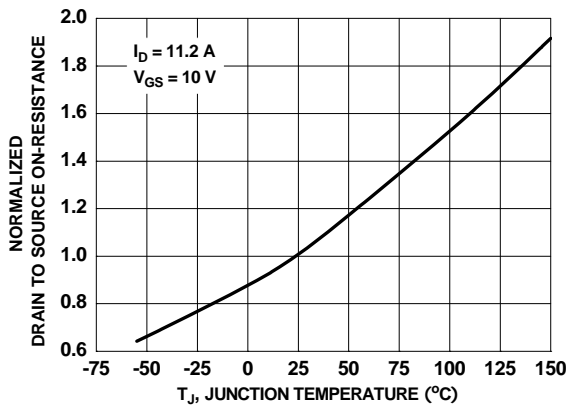


Figure 3. Normalized On Resistance vs Junction Temperature

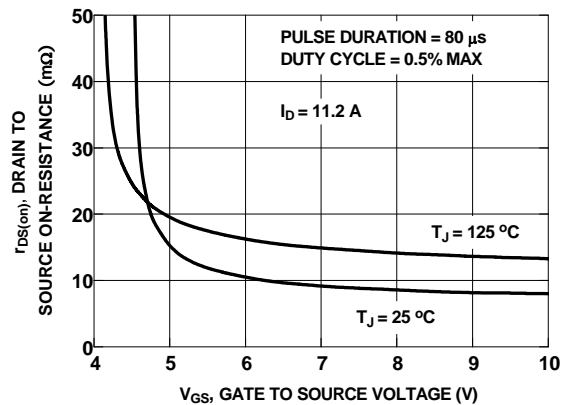


Figure 4. On-Resistance vs Gate to Source Voltage

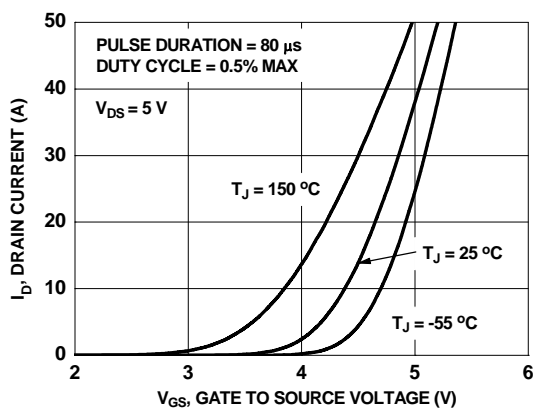


Figure 5. Transfer Characteristics

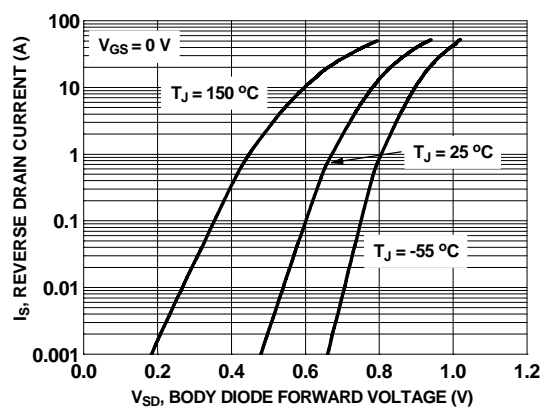
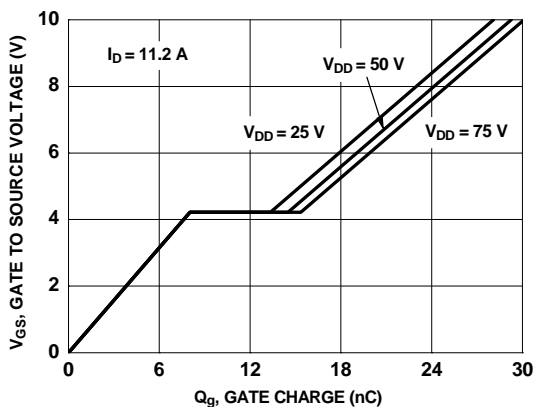
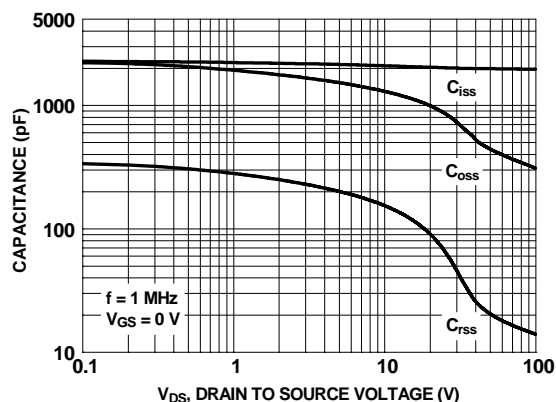


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

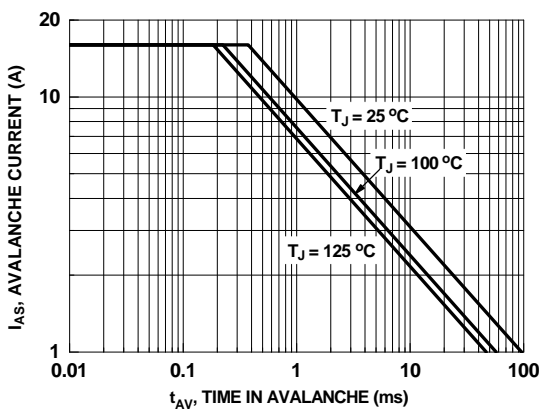
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



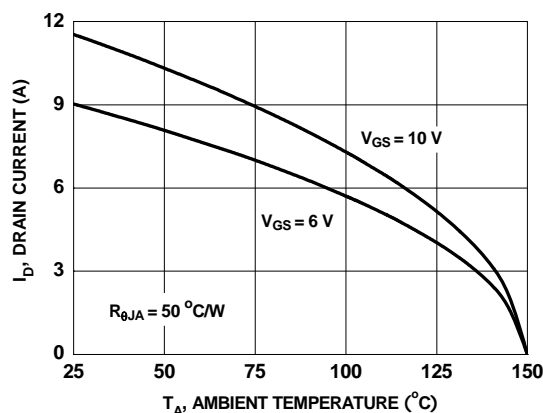
**Figure 7. Gate Charge Characteristics**



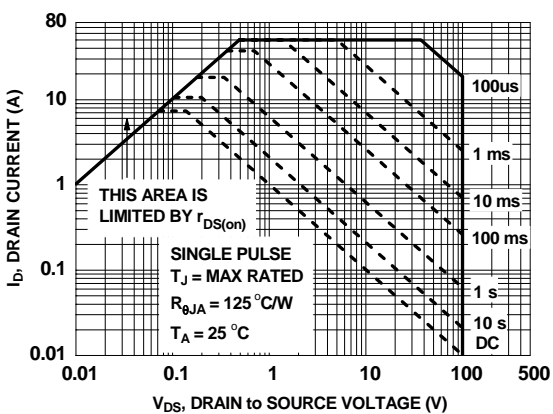
**Figure 8. Capacitance vs Drain to Source Voltage**



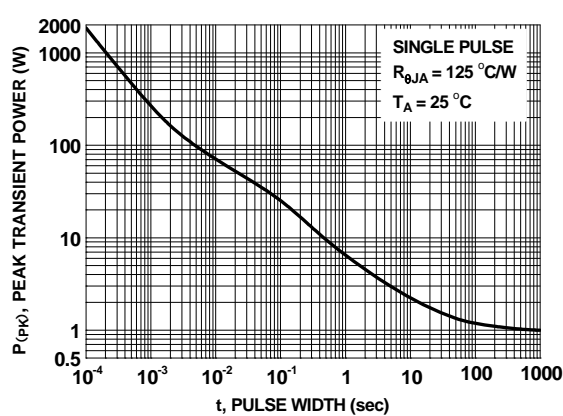
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

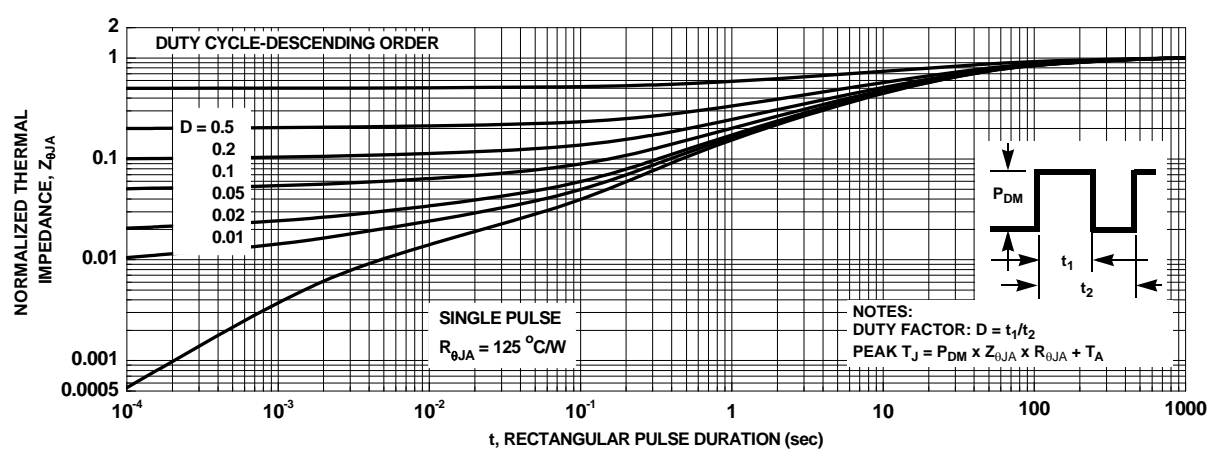


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



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