April 2011

FDMC86102LZ

N-Channel Power Trench® MOSFET

100 V, 22 A, 24 mΩ

Features

- Max $r_{DS(on)}$ = 24 mΩ at V_{GS} = 10 V, I_D = 6.5 A
- Max $r_{DS(on)}$ = 35 mΩ at V_{GS} = 4.5 V, I_D = 5.5 A
- HBM ESD protection level > 6 KV typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

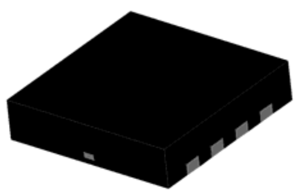
General Description

This N-Channel logic Level MOSFETs are produced using Fairchild Semiconductor's advanced Power Trench® process that has been special tailored to minimize the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

Application

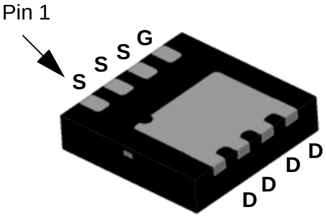
- DC - DC Switching

Top



Bottom

Pin 1



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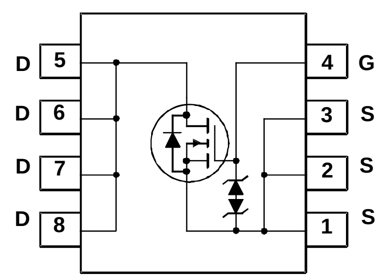


MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25 °C	22	A
	-Continuous (Silicon limited) T_C = 25 °C	29	
	-Continuous T_A = 25 °C (Note 1a)	7	
	-Pulsed	30	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	84	mJ
P_D	Power Dissipation T_C = 25 °C	41	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86102Z	FDMC86102LZ	Power 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		71		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	1.0	1.6	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6.5 A		19	24	mΩ
		V_{GS} = 4.5 V, I_D = 5.5 A		25	35	
		V_{GS} = 10 V, I_D = 6.5 A, T_J = 125 °C		31	40	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 6.5 A		24		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		969	1290	pF
C_{oss}	Output Capacitance			181	240	pF
C_{rss}	Reverse Transfer Capacitance			9	15	pF
R_g	Gate Resistance			0.4		Ω

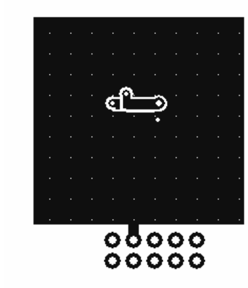
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 6.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		7.1	15	ns
t_r	Rise Time			2.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
t_f	Fall Time			2.5	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 6.5 A		15.3	22	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V		7.6	11	nC
Q_{gs}	Total Gate Charge			2.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.5		nC

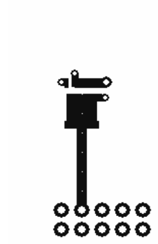
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 6.5 A (Note 2)		0.80	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)		0.72	1.2	
t_{rr}	Reverse Recovery Time	I_F = 6.5 A, di/dt = 100 A/μs		42	67	ns
Q_{rr}	Reverse Recovery Charge			40	64	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25 °C; N-ch: L = 1 mH, I_{AS} = 13 A, V_{DD} = 90 V, V_{GS} = 10 V.
4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

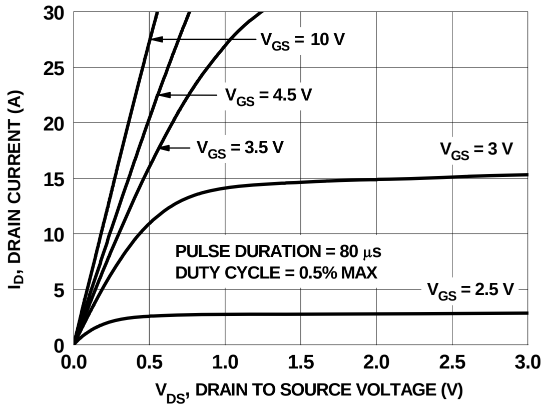


Figure 1. On-Region Characteristics

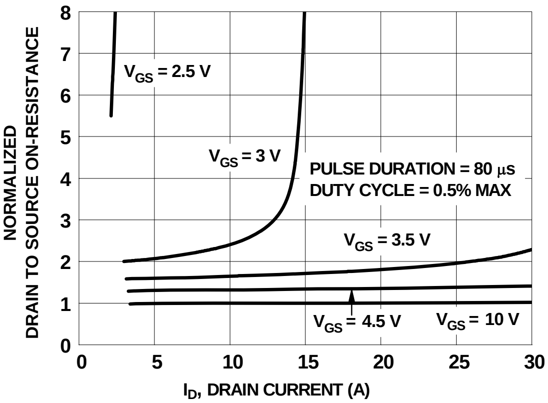


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

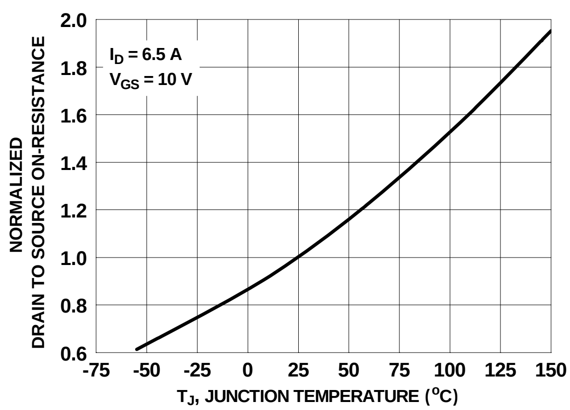


Figure 3. Normalized On-Resistance vs Junction Temperature

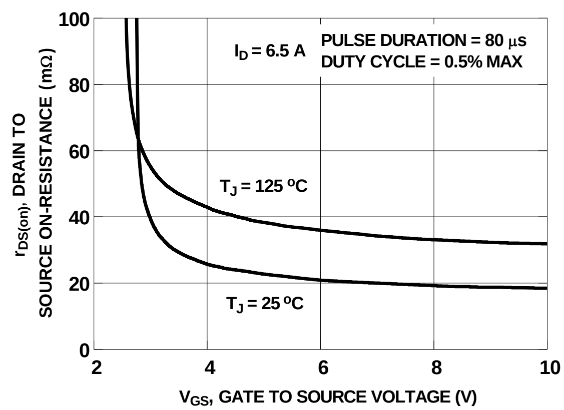


Figure 4. On-Resistance vs Gate to Source Voltage

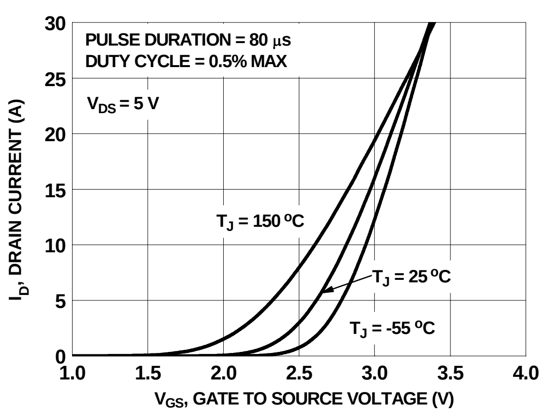


Figure 5. Transfer Characteristics

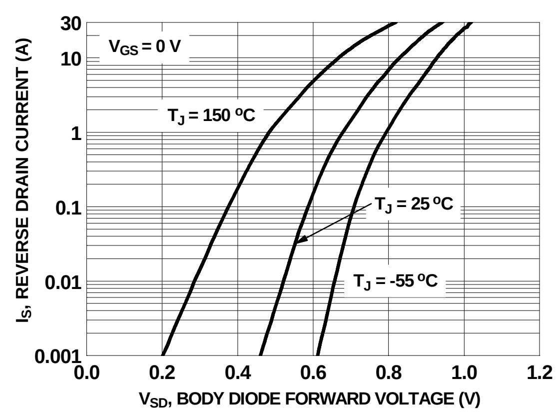


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

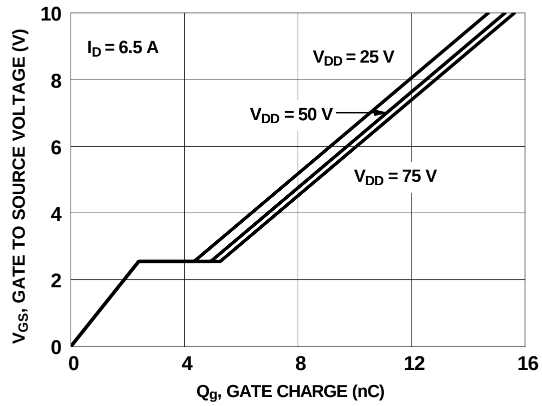


Figure 7. Gate Charge Characteristics

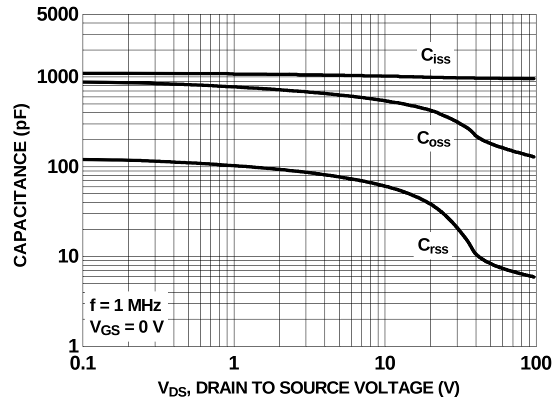


Figure 8. Capacitance vs Drain to Source Voltage

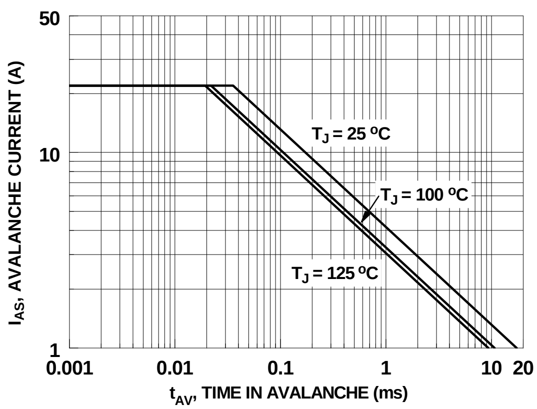


Figure 9. Unclamped Inductive Switching Capability

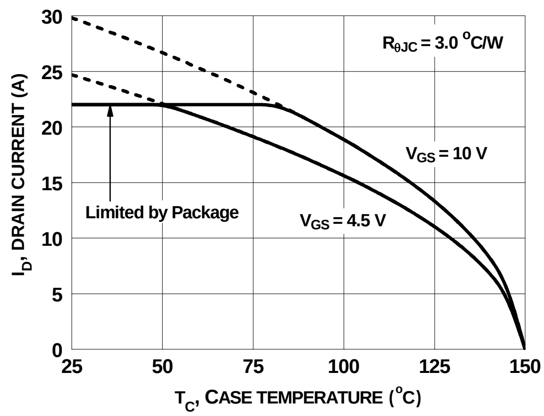


Figure 10. Maximum Continuous Drain Current vs Case Temperature

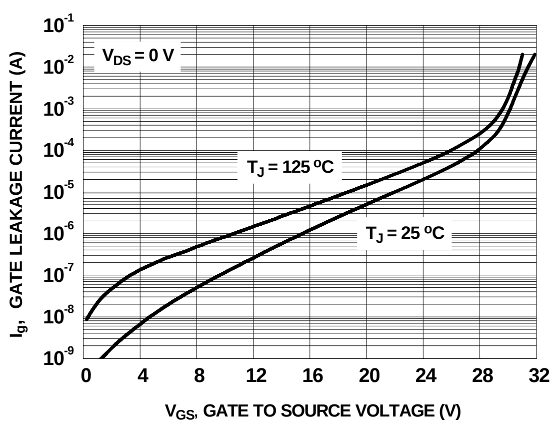


Figure 11. Gate Leakage Current vs Gate to Source Voltage

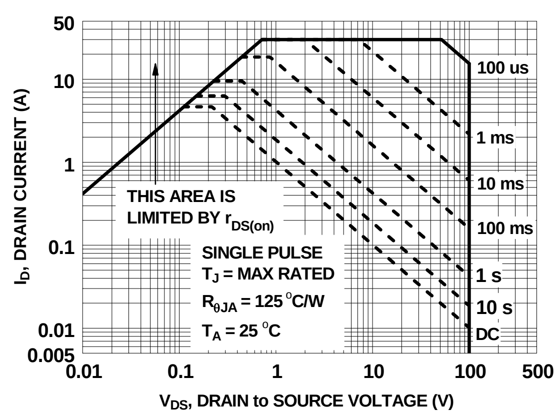


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25 °C unless otherwise noted

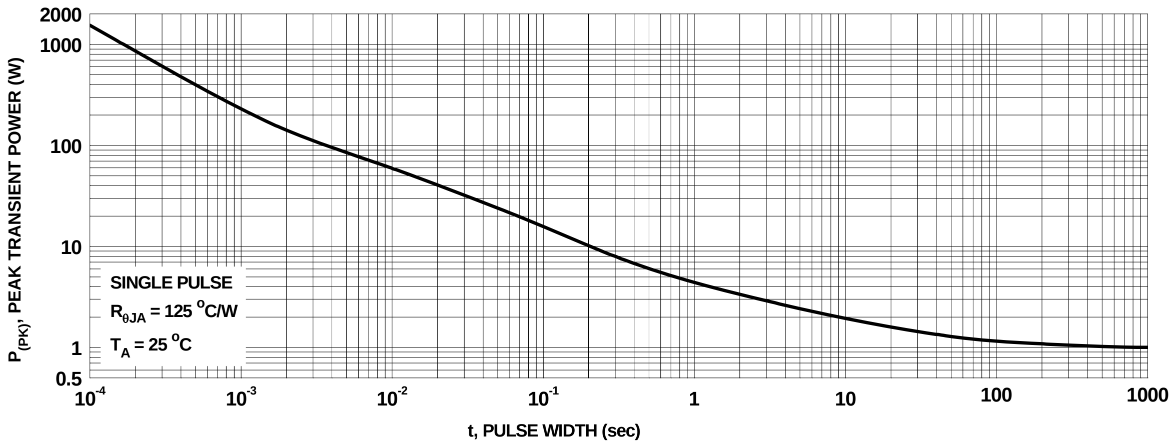


Figure 13. Single Pulse Maximum Power Dissipation

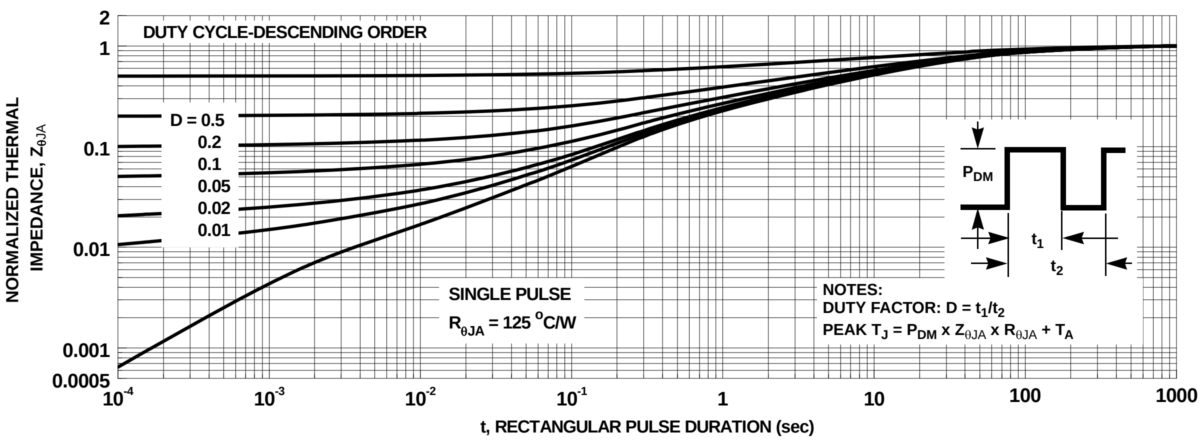
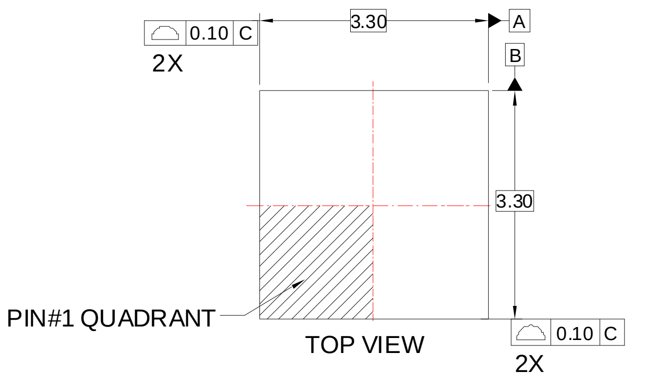
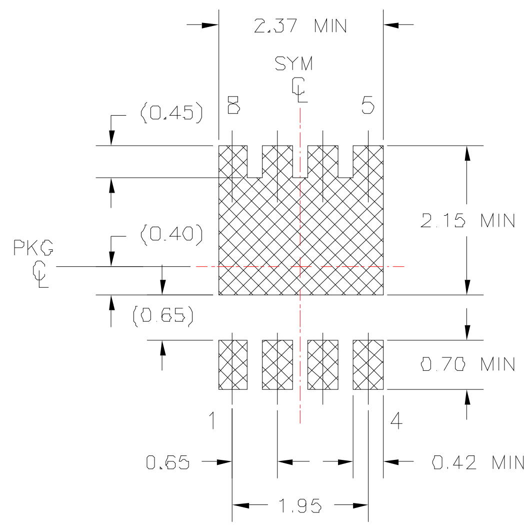


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

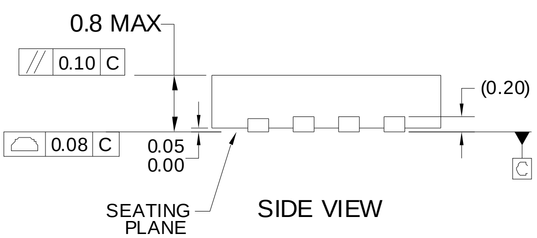
Dimensional Outline and Pad Layout



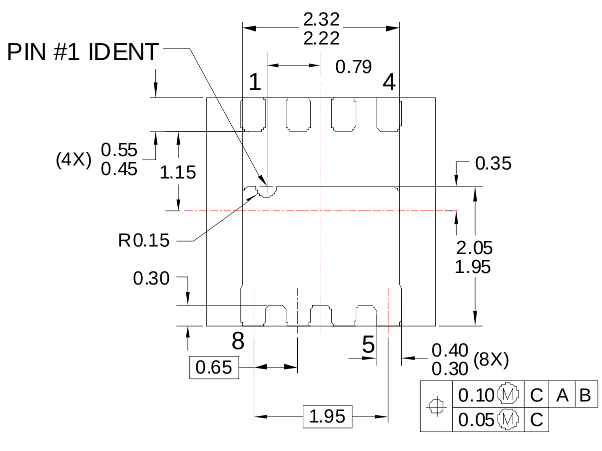
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY

E. DRAWING FILE NAME : MLP08Srev1

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I54