

FQD2N100/FQU2N100

1000V N-Channel MOSFET

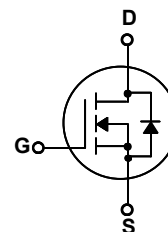
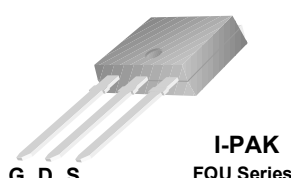
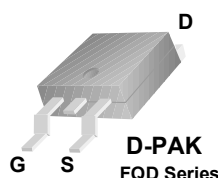
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp starter and ballast.

Features

- 1.6A, 1000V, $R_{DS(on)} = 9\Omega @ V_{GS} = 10V$
- Low gate charge (typical 12 nC)
- Low C_{rss} (typical 5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS Compliant



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | FQD2N100/FQU2N100 | Units |
|----------------|---|-------------------|---------------------|
| V_{DSS} | Drain-Source Voltage | 1000 | V |
| I_D | Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$) | 1.6 | A |
| | | 1.0 | A |
| I_{DM} | Drain Current - Pulsed (Note 1) | 6.4 | A |
| V_{GSS} | Gate-Source Voltage | ± 30 | V |
| E_{AS} | Single Pulsed Avalanche Energy (Note 2) | 160 | mJ |
| I_{AR} | Avalanche Current (Note 1) | 1.6 | A |
| E_{AR} | Repetitive Avalanche Energy (Note 1) | 5.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 5.5 | V/ns |
| P_D | Power Dissipation ($T_A = 25^\circ\text{C}$) * | 2.5 | W |
| | Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C | 50 | W |
| | | 0.4 | W/ $^\circ\text{C}$ |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |
| T_L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | 300 | $^\circ\text{C}$ |

Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|-----------------|---|-----|-----|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 2.5 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient * | -- | 50 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 110 | $^\circ\text{C}/\text{W}$ |

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------------------------------|---|---|------|-------|------|---------------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 1000 | -- | -- | V |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | -- | 0.976 | -- | $\text{V}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 1000\text{ V}, V_{GS} = 0\text{ V}$ | -- | -- | 10 | μA |
| | | $V_{DS} = 800\text{ V}, T_C = 125^\circ\text{C}$ | -- | -- | 100 | μA |
| I_{GSSF} | Gate-Body Leakage Current, Forward | $V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | 100 | nA |
| I_{GSSR} | Gate-Body Leakage Current, Reverse | $V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | -100 | nA |

On Characteristics

| | | | | | | |
|--------------|-----------------------------------|---|-----|-----|-----|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 3.0 | -- | 5.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 0.8\text{ A}$ | -- | 7.1 | 9 | Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = 50\text{ V}, I_D = 0.8\text{ A}$ (Note 4) | -- | 1.9 | -- | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|----|-----|-----|----|
| C_{iss} | Input Capacitance | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | -- | 400 | 520 | pF |
| C_{oss} | Output Capacitance | | -- | 40 | 52 | pF |
| C_{rss} | Reverse Transfer Capacitance | | -- | 5 | 6.5 | pF |

Switching Characteristics

| | | | | | | |
|--------------|---------------------|---|----|-----|------|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 500\text{ V}, I_D = 2.0\text{ A},$ $R_G = 25\ \Omega$ (Note 4, 5) | -- | 13 | 35 | ns |
| t_r | Turn-On Rise Time | | -- | 30 | 70 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 25 | 60 | ns |
| t_f | Turn-Off Fall Time | | -- | 35 | 80 | ns |
| Q_g | Total Gate Charge | $V_{DS} = 800\text{ V}, I_D = 2.0\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5) | -- | 12 | 15.5 | nC |
| Q_{gs} | Gate-Source Charge | | -- | 2.5 | -- | nC |
| Q_{gd} | Gate-Drain Charge | | -- | 6.5 | -- | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|---|---|----|-----|-----|---------------|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | -- | -- | 1.5 | A | |
| I_{SM} | Maximum Pulsed Drain-Source Diode Forward Current | -- | -- | 6.0 | A | |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 1.6\text{ A}$ | -- | -- | 1.4 | V |
| t_{rr} | Reverse Recovery Time | $V_{GS} = 0\text{ V}, I_S = 2.0\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4) | -- | 520 | -- | ns |
| Q_{rr} | Reverse Recovery Charge | | -- | 2.3 | -- | μC |

Notes:

1. Repetitive Rating ; Pulse width limited by maximum junction temperature
2. $L = 120\text{mH}, I_{AS} = 1.6\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 2.0\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

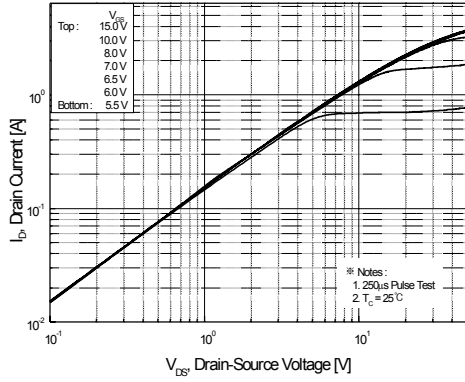


Figure 1. On-Region Characteristics

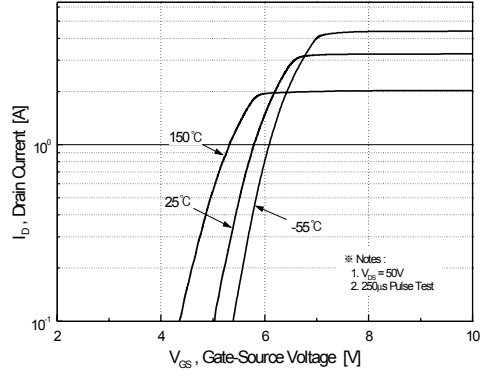


Figure 2. Transfer Characteristics

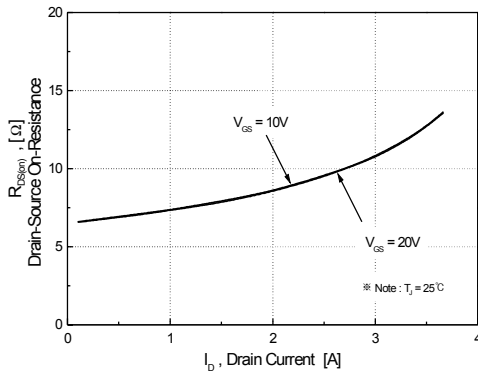


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

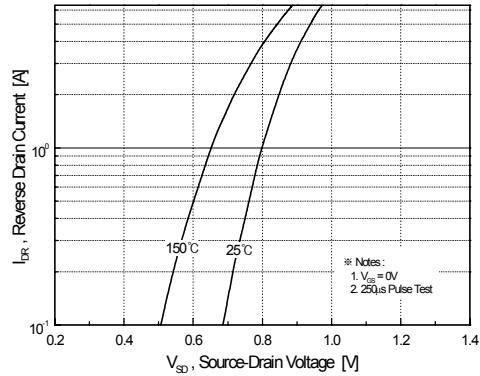


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

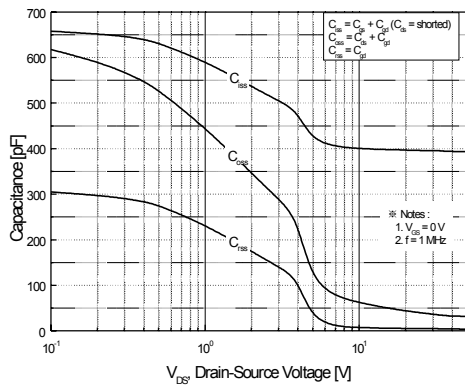


Figure 5. Capacitance Characteristics

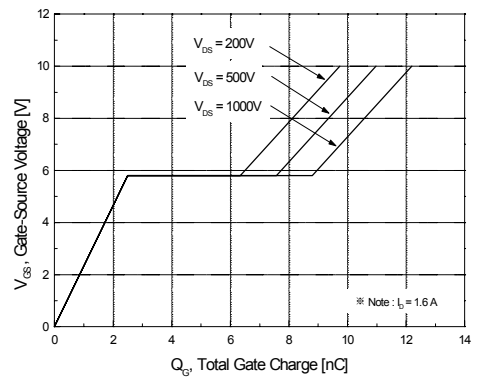


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

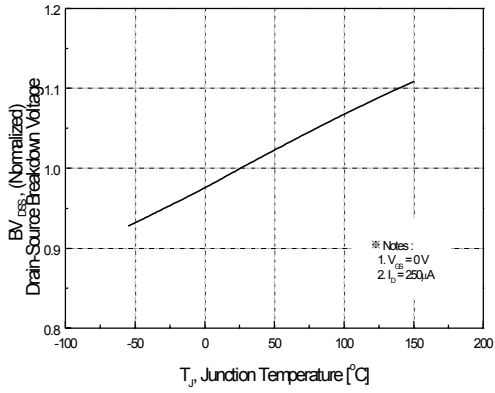


Figure 7. Breakdown Voltage Variation vs. Temperature

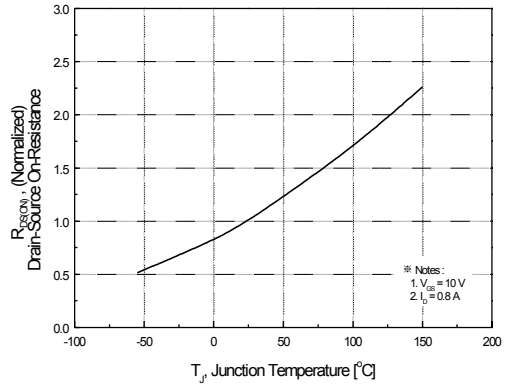


Figure 8. On-Resistance Variation vs. Temperature

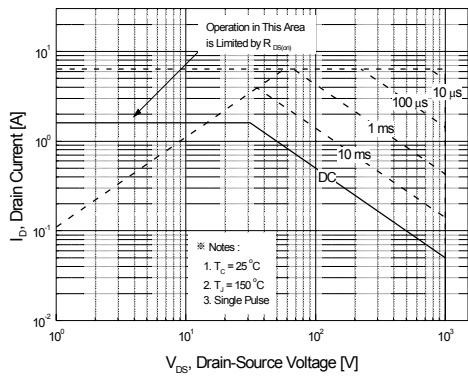


Figure 9. Maximum Safe Operating Area

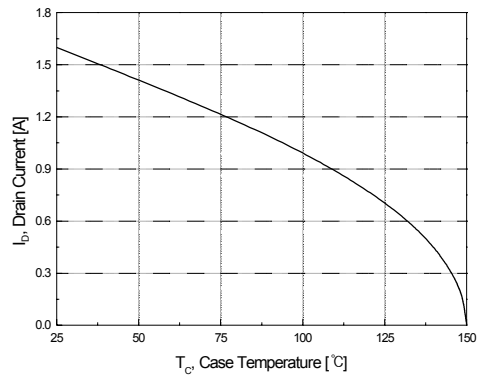


Figure 10. Maximum Drain Current vs. Case Temperature

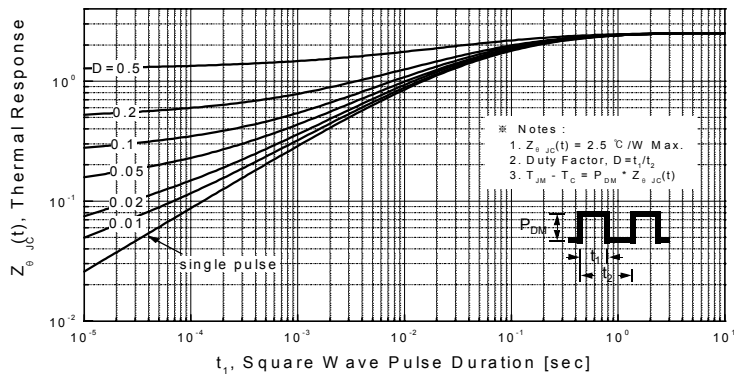
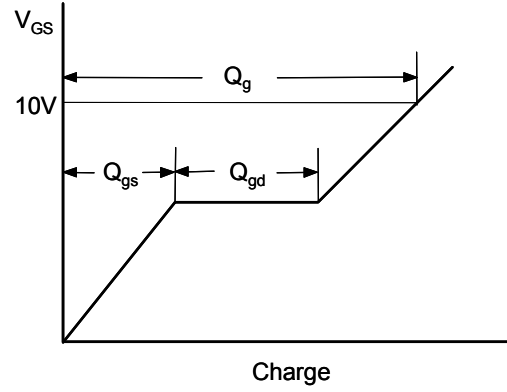
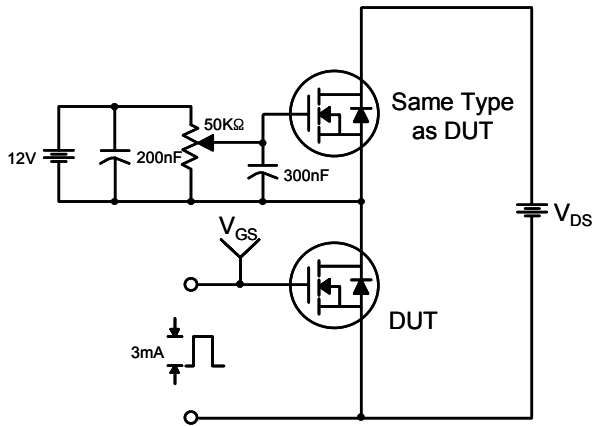
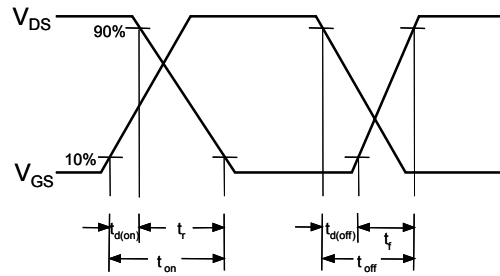
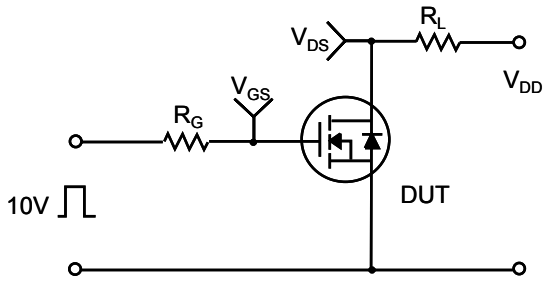


Figure 11. Transient Thermal Response Curve

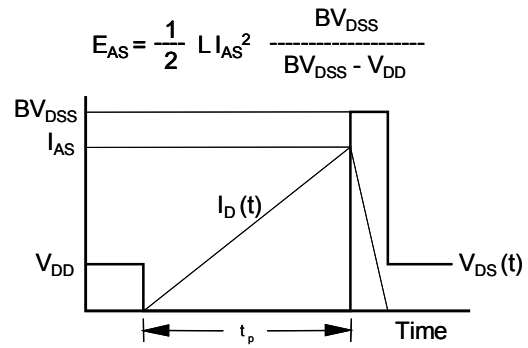
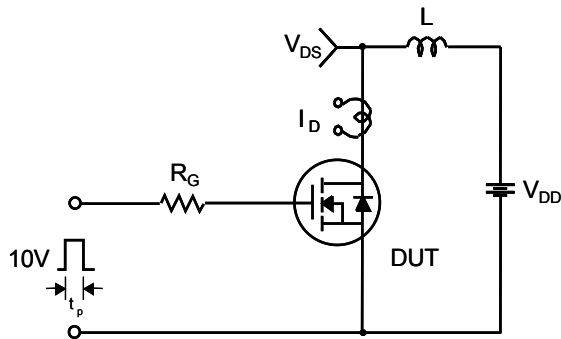
Gate Charge Test Circuit & Waveform



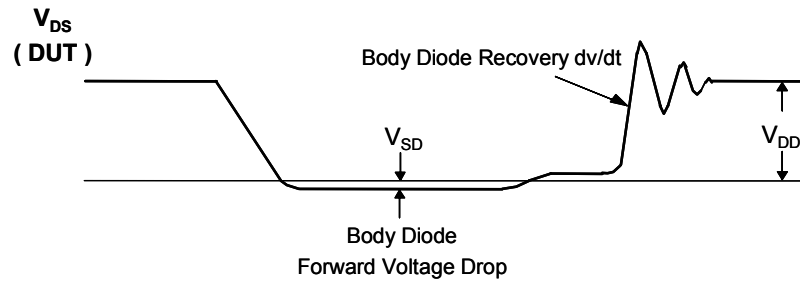
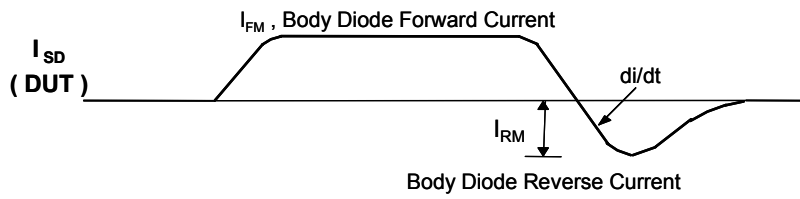
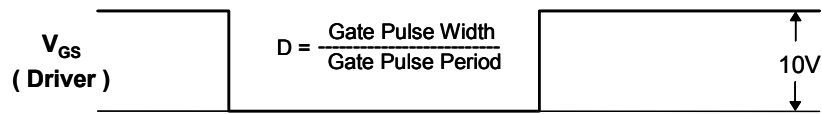
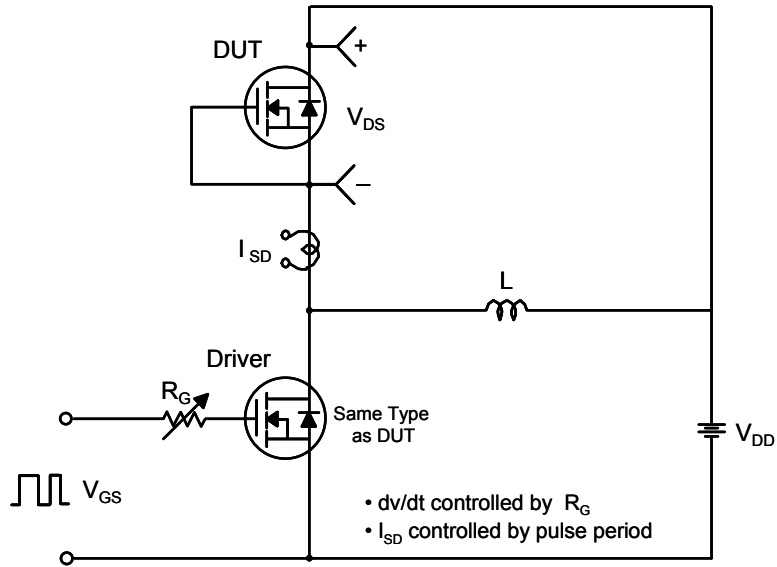
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

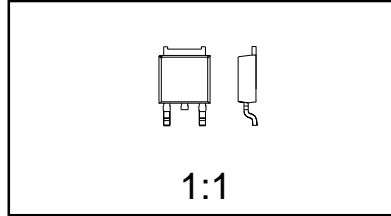
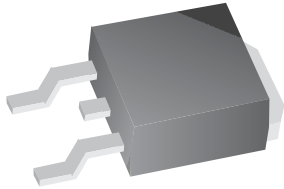


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-252 (DPAK) (FS PKG Code 36)

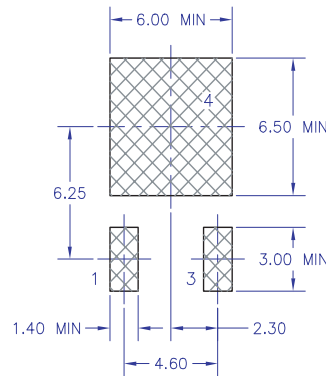
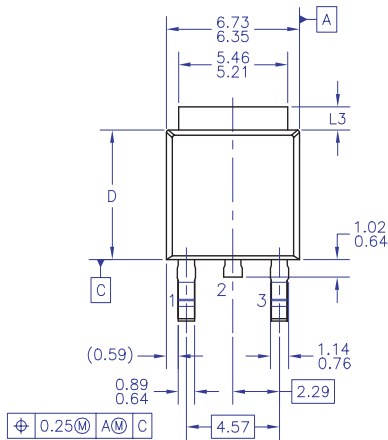


1:1

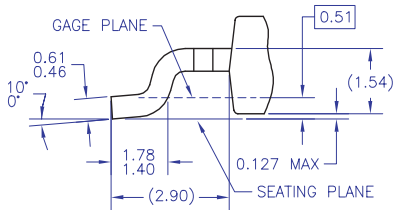
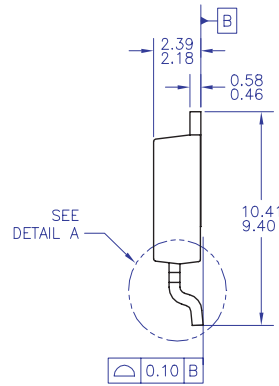
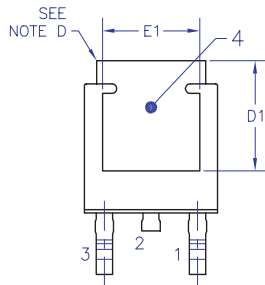
Scale 1:1 on letter size paper

Dimensions shown below are in millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



DETAIL A
(ROTATED -90°)
SCALE: 12X

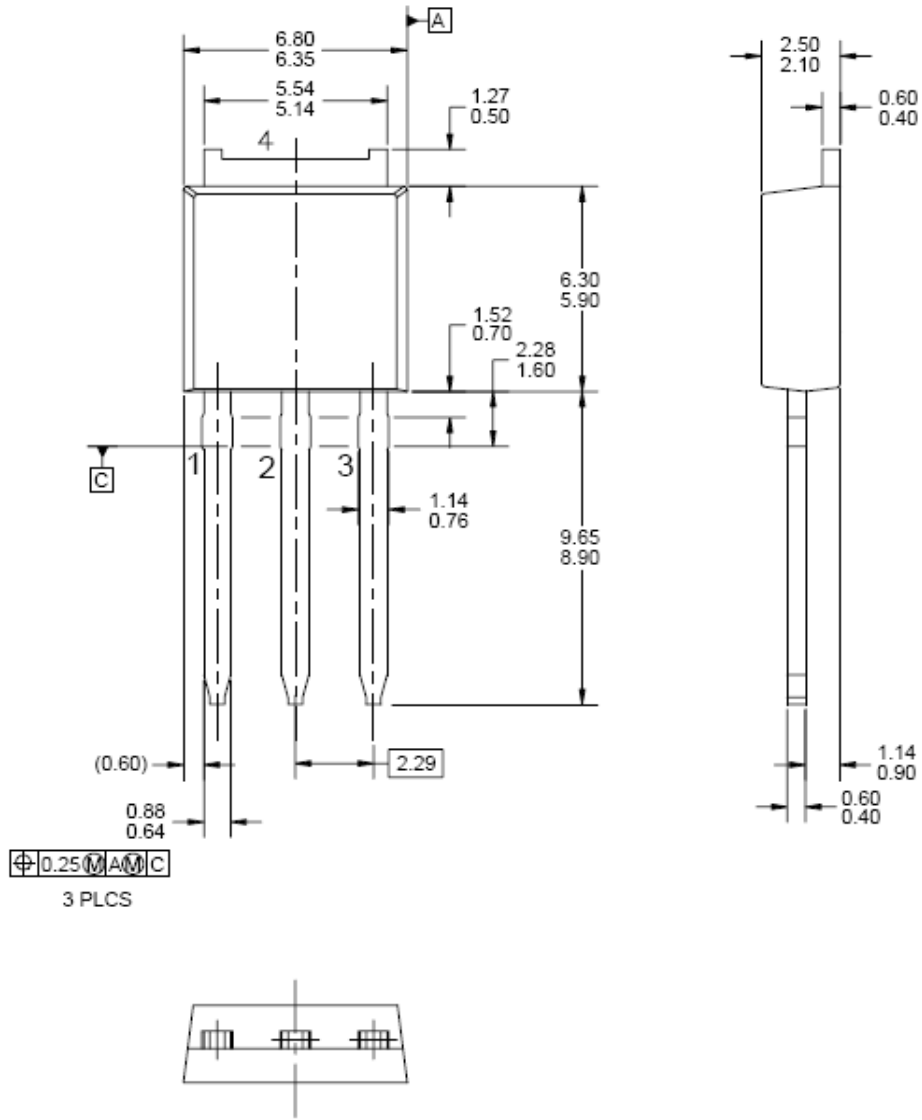
NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) DIMENSIONS L3,D,E1&D1 TABLE:

| | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |

Mechanical Dimensions

I - PAK



Dimensions in Millimeters


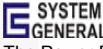


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