

## FDD3N40 / FDU3N40

### 400V N-Channel MOSFET

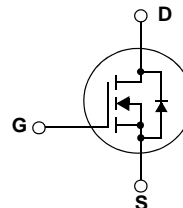
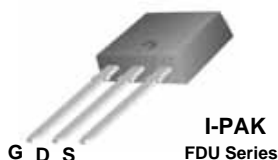
#### Features

- 2A, 400V,  $R_{DS(on)} = 3.4\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 4.5 nC)
- Low  $C_{rss}$  ( typical 3.7 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



#### Absolute Maximum Ratings

Symbol	Parameter	FDD3N40 / FDU3N40	Unit
$V_{DSS}$	Drain-Source Voltage	400	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	2.0 1.25	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	8.0	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	46	mJ
$I_{AR}$	Avalanche Current (Note 1)	2	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	30 0.24	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\* Drain current limited by maximum junction temperature

#### Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	4.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Case-to-Sink Typ.	--	110	$^\circ\text{C}/\text{W}$

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3N40	FDD3N40TM	D-PAK	380mm	16mm	2500
FDD3N40	FDD3N40TF	D-PAK	380mm	16mm	2000
FDU3N40	FDU3N40TU	I-PAK	-	-	70

### Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

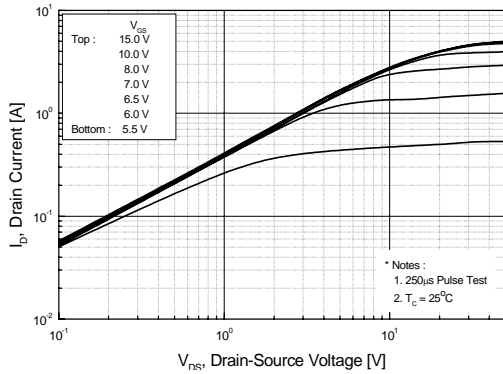
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	400	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.4	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 320V, T <sub>C</sub> = 125°C	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1A	--	2.8	3.4	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 1A (Note 4)	--	2	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	173	225	pF
C <sub>oss</sub>	Output Capacitance		--	30	40	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	3.7	6	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 200V, I <sub>D</sub> = 3A R <sub>G</sub> = 25Ω  (Note 4, 5)	--	10	30	ns
t <sub>r</sub>	Turn-On Rise Time		--	30	70	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	10	30	ns
t <sub>f</sub>	Turn-Off Fall Time		--	25	60	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 320V, I <sub>D</sub> = 3A V <sub>GS</sub> = 10V  (Note 4, 5)	--	4.5	6	nC
Q <sub>gs</sub>	Gate-Source Charge		--	1.2	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	2	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	2	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	8	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 3A di <sub>f</sub> /dt = 100A/μs (Note 4)	--	210	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.75	--	μC

**NOTES:**

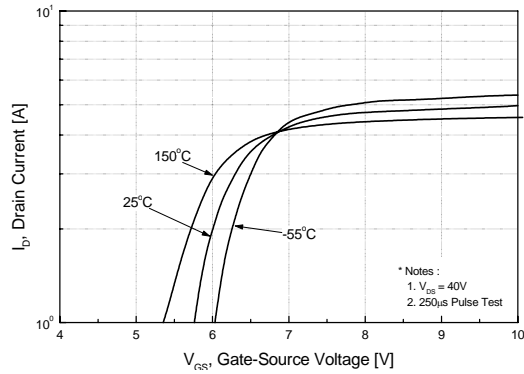
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 20mH, I<sub>AS</sub> = 2A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 2A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

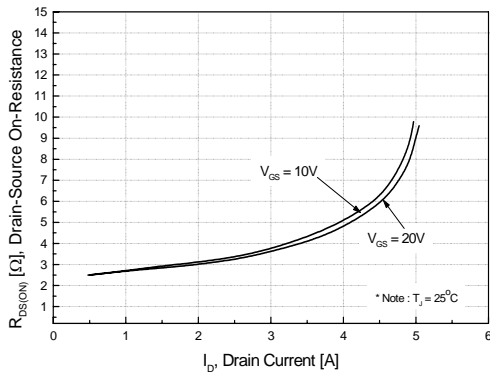
**Figure 1. On-Region Characteristics**



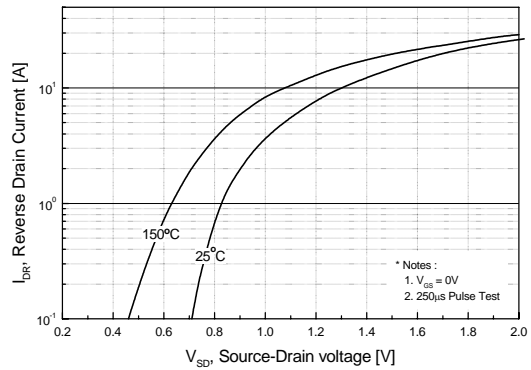
**Figure 2. Transfer Characteristics**



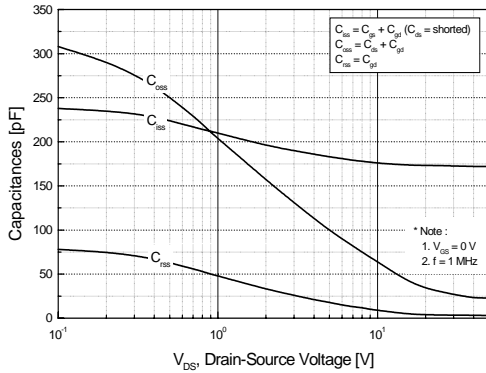
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



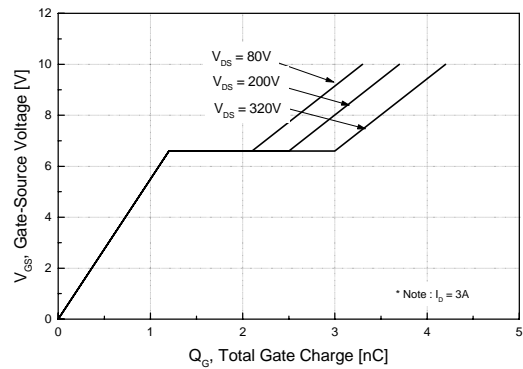
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

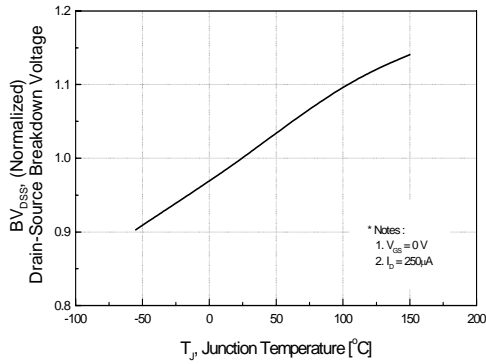


**Figure 6. Gate Charge Characteristics**

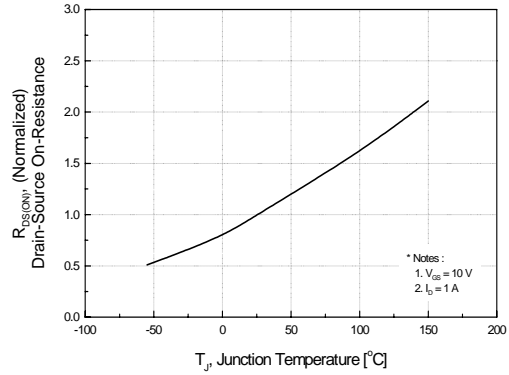


**Typical Performance Characteristics (Continued)**

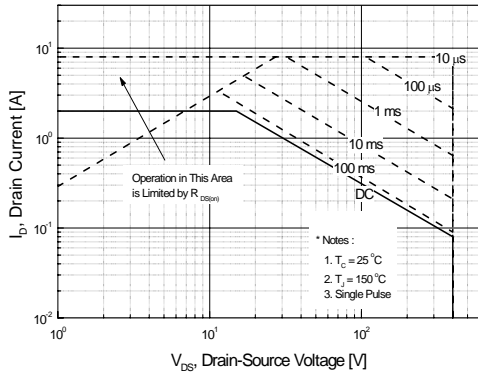
**Figure 7. Breakdown Voltage Variation vs. Temperature**



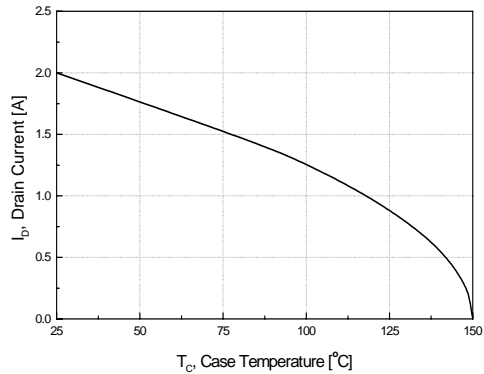
**Figure 8. On-Resistance Variation vs. Temperature**



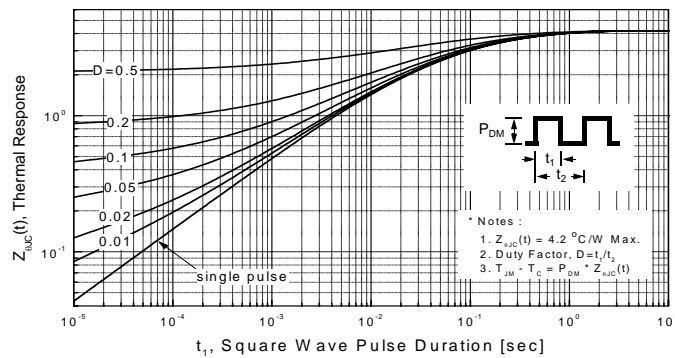
**Figure 9. Maximum Safe Operating Area**



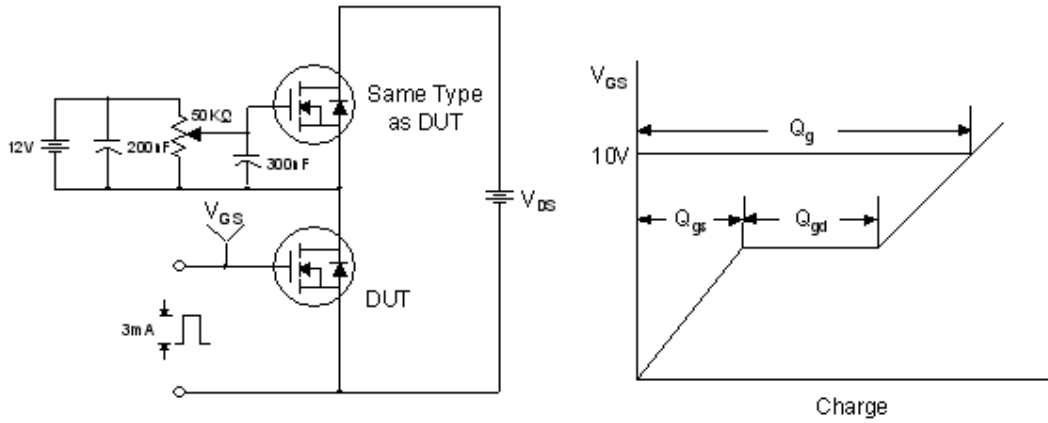
**Figure 10. Maximum Drain Current vs. Case Temperature**



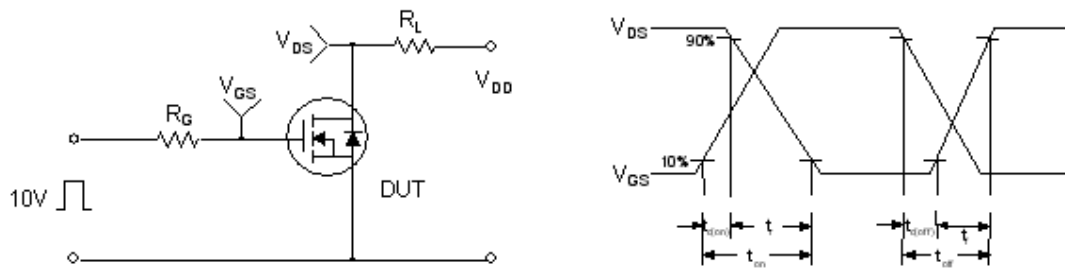
**Figure 11. Transient Thermal Response Curve**



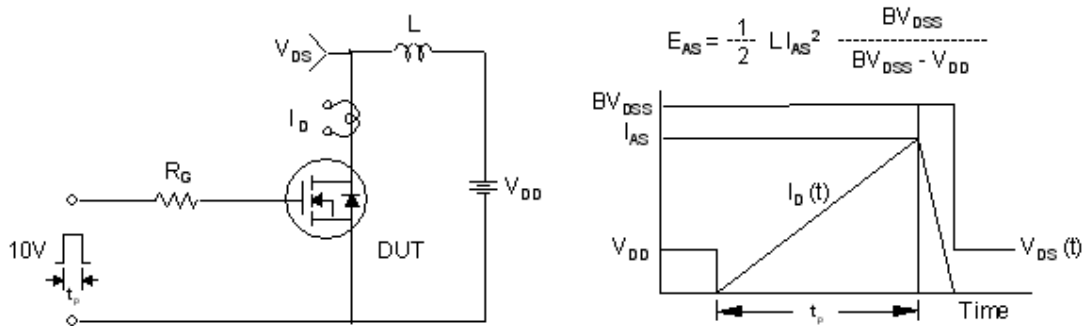
**Gate Charge Test Circuit & Waveform**



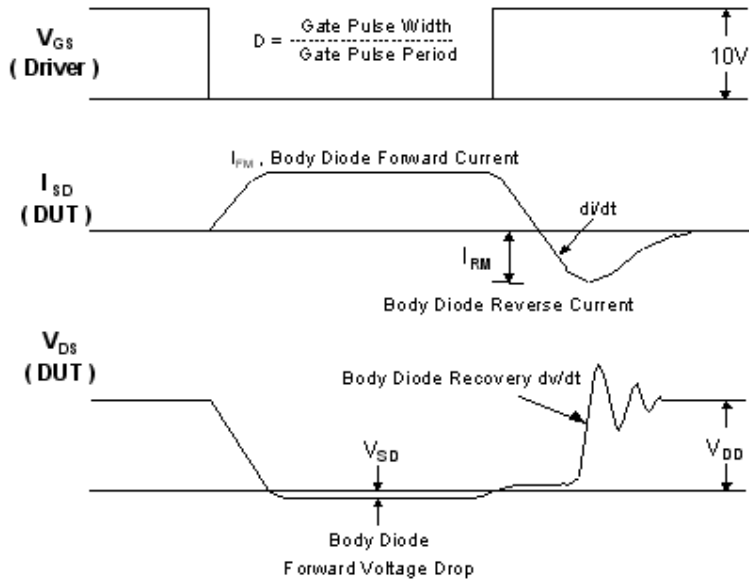
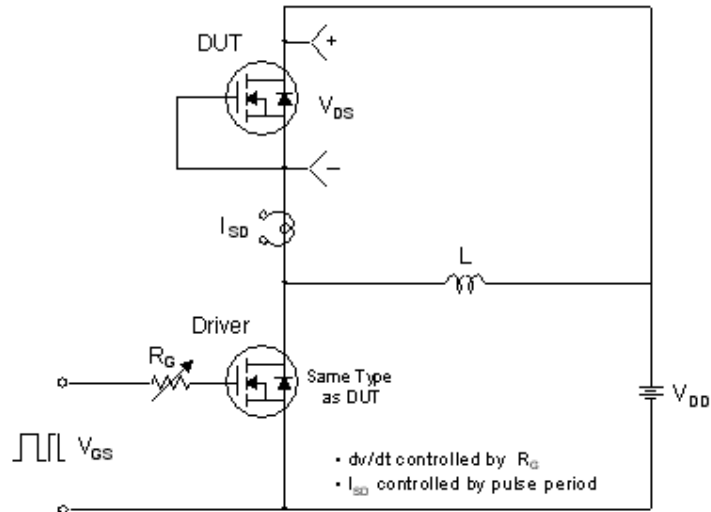
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

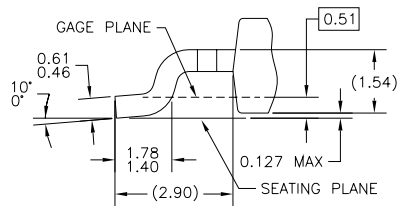
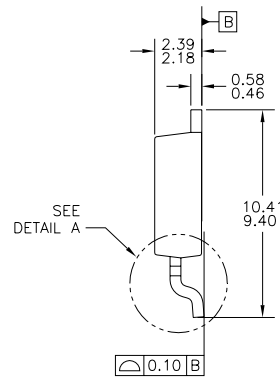
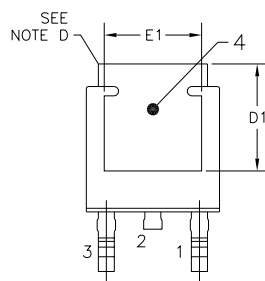
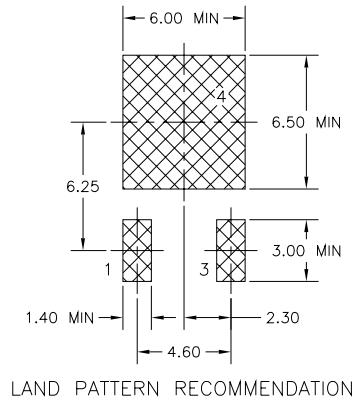
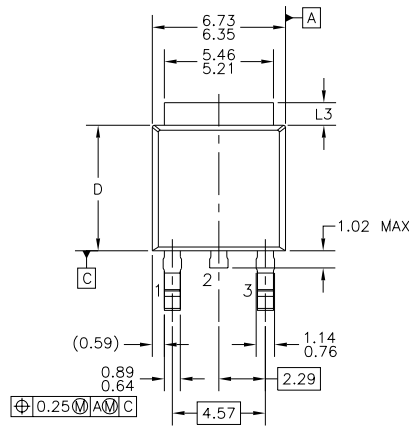


Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

### D-PAK

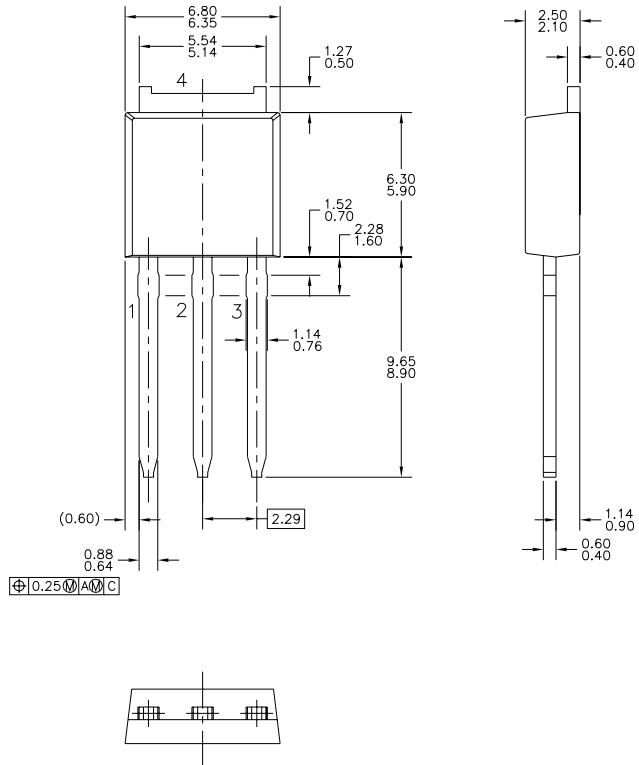


DETAIL A  
(ROTATED -90°)  
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:
- |    | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D  | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN  | 3.81 MIN  |
| D1 | 5.21 MIN  | 4.57 MIN  |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Mechanical Dimensions

I-PAK








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EnSigna <sup>™</sup>	OPTOLOGIC <sup>®</sup>	SuperSOT <sup>™</sup> -3	
FACT Quiet Series <sup>™</sup>	OPTOPLANAR <sup>®</sup>	SuperSOT <sup>™</sup> -6	
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