



FQD5P20 / FQU5P20

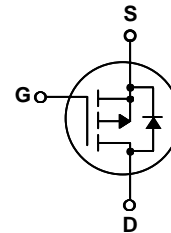
200V P-Channel MOSFET

General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

Features

- -3.7A, -200V, $R_{DS(on)} = 1.4\Omega @ V_{GS} = -10V$
- Low gate charge (typical 10 nC)
- Low Crss (typical 12 pF)
- Fast switching
- 100% avalanche tested
- RoHS Compliant



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

| Symbol | Parameter | FQD5P20 / FQU5P20 | Units |
|-----------------------------------|---|-------------------|-------|
| V _{DSS} | Drain-Source Voltage | -200 | V |
| I _D | Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C) | -3.7 | A |
| | | -2.34 | A |
| I _{DM} | Drain Current - Pulsed (Note 1) | -14.8 | A |
| V _{GSS} | Gate-Source Voltage | ± 30 | V |
| E _{AS} | Single Pulsed Avalanche Energy (Note 2) | 330 | mJ |
| I _{AR} | Avalanche Current (Note 1) | -3.7 | A |
| E _{AR} | Repetitive Avalanche Energy (Note 1) | 4.5 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | -5.5 | V/ns |
| P _D | Power Dissipation (T _A = 25°C) * | 2.5 | W |
| | Power Dissipation (T _C = 25°C) - Derate above 25°C | 45 | W |
| | | 0.36 | W/°C |
| T _J , T _{STG} | Operating and Storage Temperature Range | -55 to +150 | °C |
| T _L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | 300 | °C |

Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|------------------|---|-----|------|-------|
| R _{θJC} | Thermal Resistance, Junction-to-Case | -- | 2.78 | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient * | -- | 50 | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient | -- | 110 | °C/W |

* When mounted on the minimum pad size recommended (PCB Mount)

Elerical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------------------------------|---|--|------|-------|------|---------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$ | -200 | -- | -- | V |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | -- | -0.17 | -- | V/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$ | -- | -- | -1 | μA |
| | | $V_{DS} = -160\text{ V}, T_C = 125^\circ\text{C}$ | -- | -- | -10 | μA |
| I_{GSSF} | Gate-Body Leakage Current, Forward | $V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | -100 | nA |
| I_{GSSR} | Gate-Body Leakage Current, Reverse | $V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | 100 | nA |

On Characteristics

| | | | | | | |
|--------------|-----------------------------------|--|------|-----|------|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ | -3.0 | -- | -5.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = -10\text{ V}, I_D = -1.85\text{ A}$ | -- | 1.1 | 1.4 | Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = -40\text{ V}, I_D = -1.85\text{ A}$ (Note 4) | -- | 2.2 | -- | S |

Dynamic Characteristics

| | | | | | | |
|------------|------------------------------|---|----|-----|-----|----|
| C_{iss} | Input Capacitance | $V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | -- | 330 | 430 | pF |
| C_{oss} | Output Capacitance | | -- | 75 | 98 | pF |
| C_{riss} | Reverse Transfer Capacitance | | -- | 12 | 15 | pF |

Switching Characteristics

| | | | | | | |
|--------------|---------------------|--|----|-----|-----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = -100\text{ V}, I_D = -4.8\text{ A},$ $R_G = 25\ \Omega$ (Note 4, 5) | -- | 9 | 28 | ns |
| t_r | Turn-On Rise Time | | -- | 70 | 150 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 12 | 35 | ns |
| t_f | Turn-Off Fall Time | | -- | 25 | 60 | ns |
| Q_g | Total Gate Charge | $V_{DS} = -160\text{ V}, I_D = -4.8\text{ A},$ $V_{GS} = -10\text{ V}$ (Note 4, 5) | -- | 10 | 13 | nC |
| Q_{gs} | Gate-Source Charge | | -- | 2.8 | -- | nC |
| Q_{gd} | Gate-Drain Charge | | -- | 5.2 | -- | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|---|--|----|-------|------|---------------|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | -- | -- | -3.7 | A | |
| I_{SM} | Maximum Pulsed Drain-Source Diode Forward Current | -- | -- | -14.8 | A | |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = -3.7\text{ A}$ | -- | -- | -5.0 | V |
| t_{rr} | Reverse Recovery Time | $V_{GS} = 0\text{ V}, I_S = -4.8\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4) | -- | 175 | -- | ns |
| Q_{rr} | Reverse Recovery Charge | | -- | 1.07 | -- | μC |

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 36.2\text{ mH}, I_{AS} = -3.7\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq -4.8\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

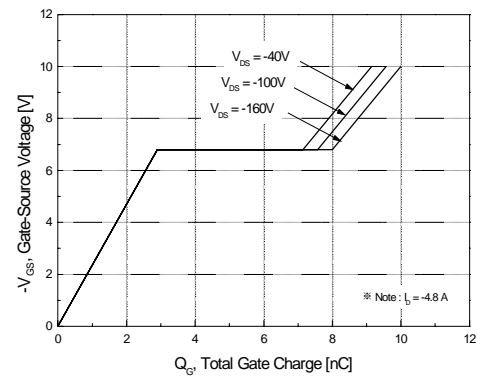
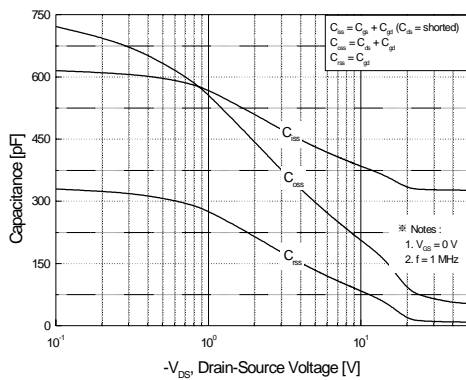
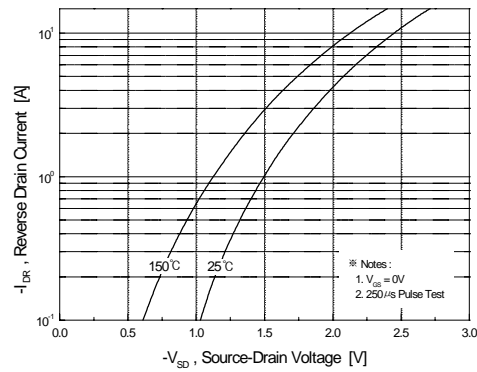
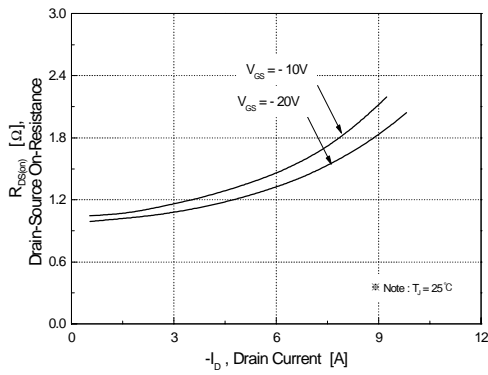
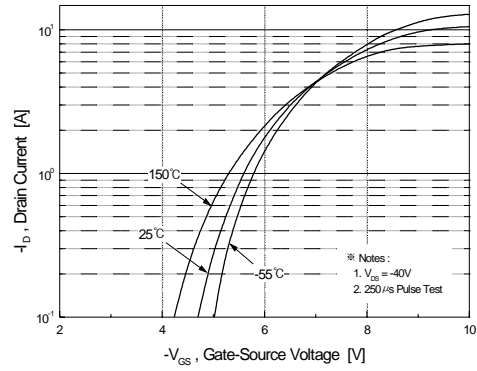
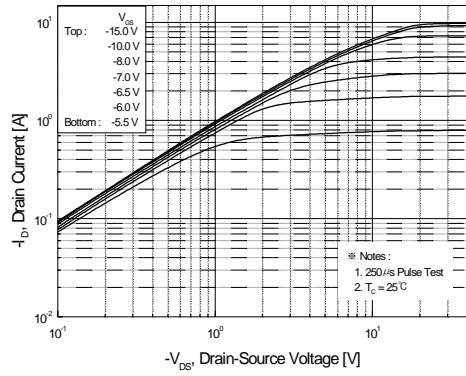


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

Typical Characteristics (Continued)

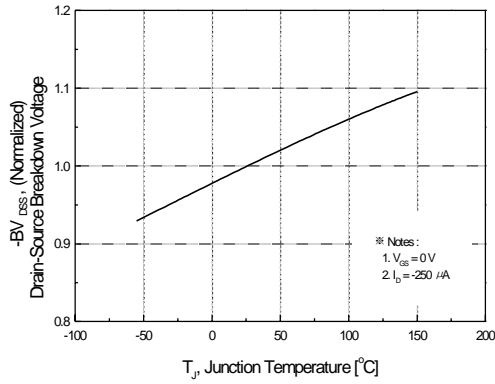


Figure 7. Breakdown Voltage Variation vs. Temperature

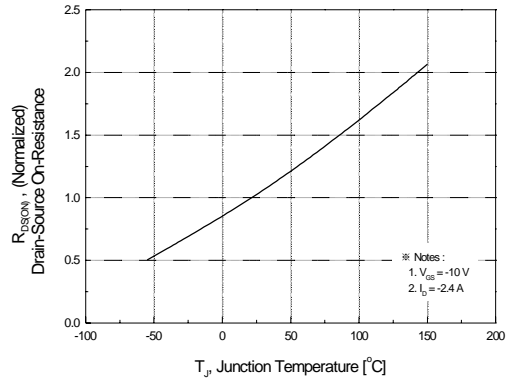


Figure 8. On-Resistance Variation vs. Temperature

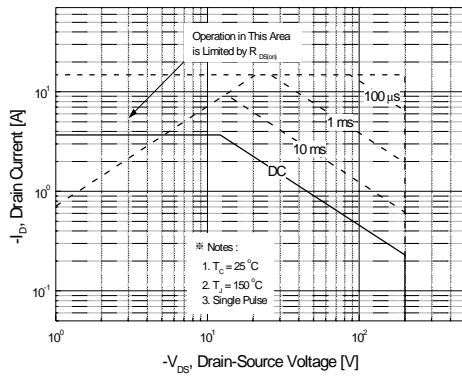


Figure 9. Maximum Safe Operating Area

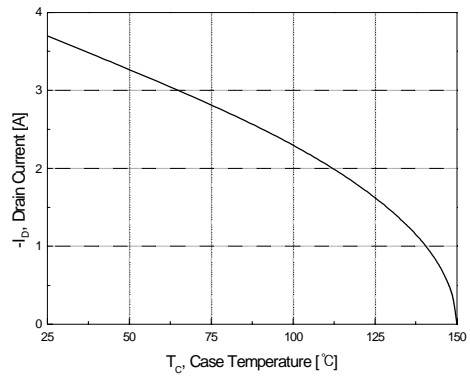


Figure 10. Maximum Drain Current vs. Case Temperature

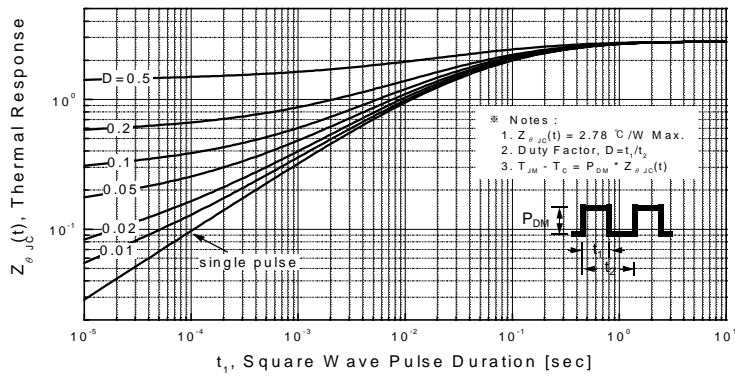
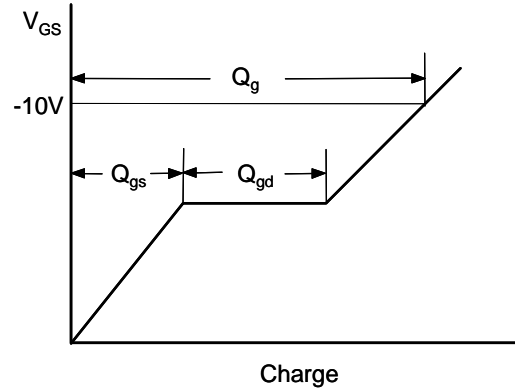
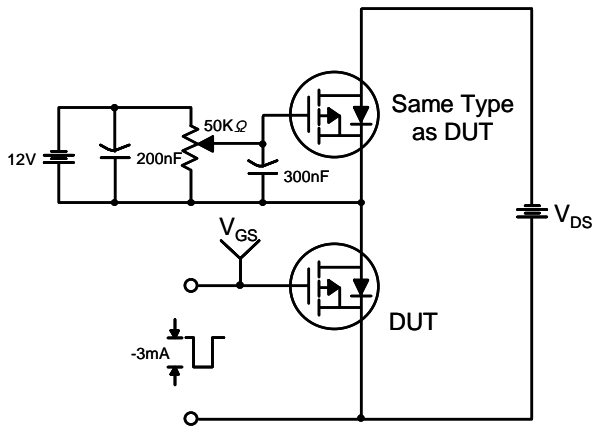
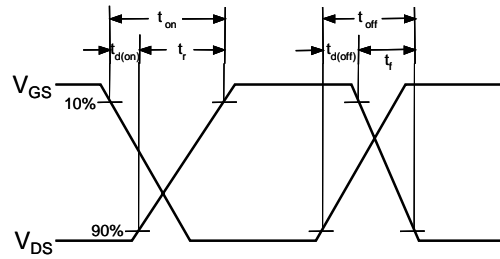
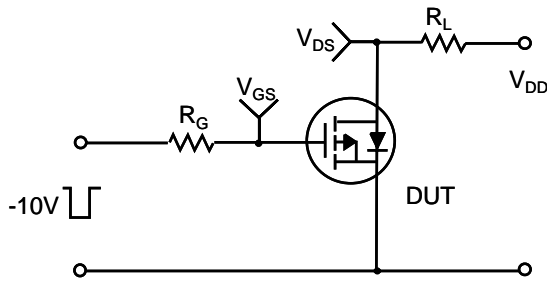


Figure 11. Transient Thermal Response Curve

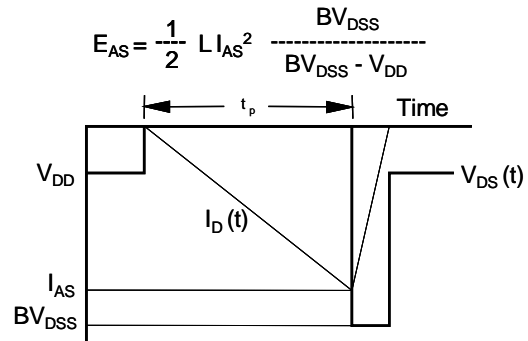
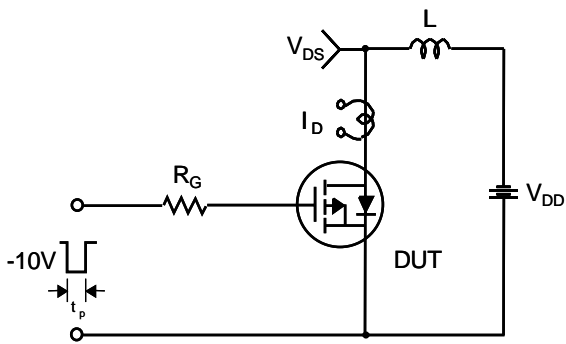
Gate Charge Test Circuit & Waveform



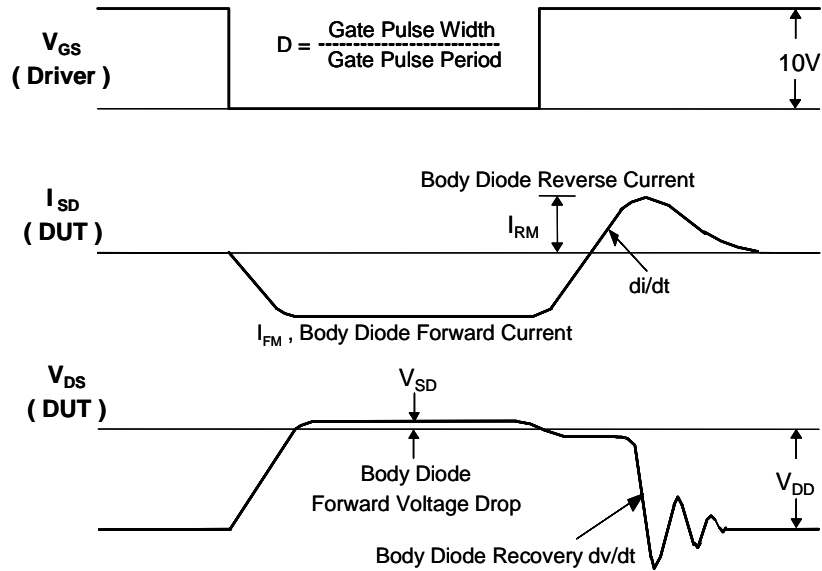
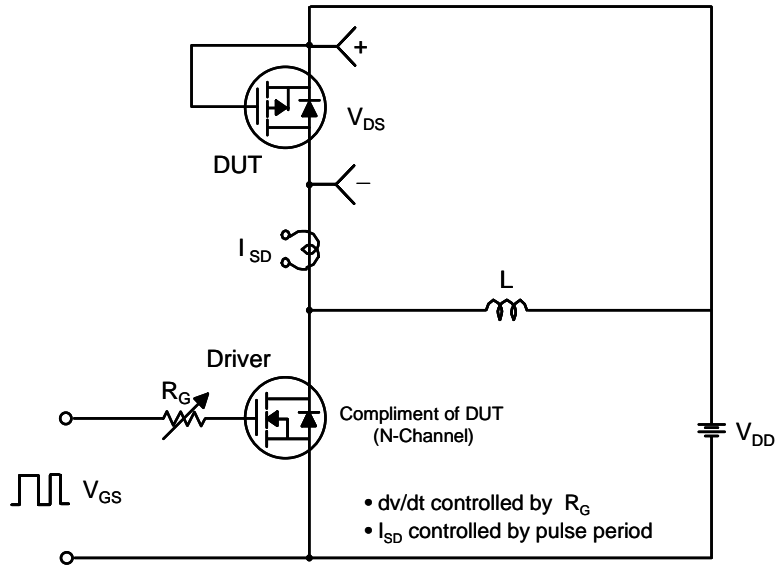
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

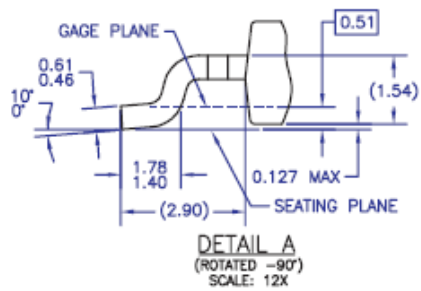
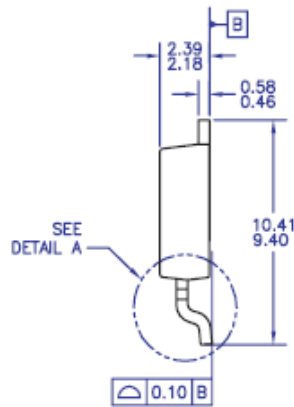
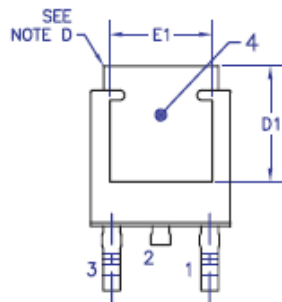
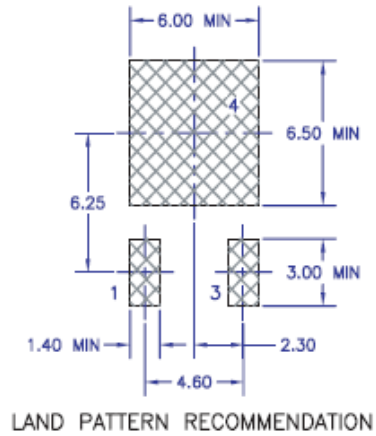
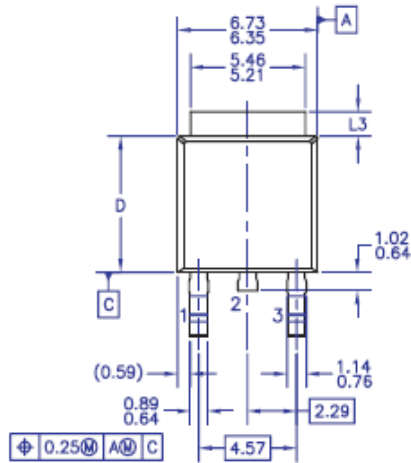


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

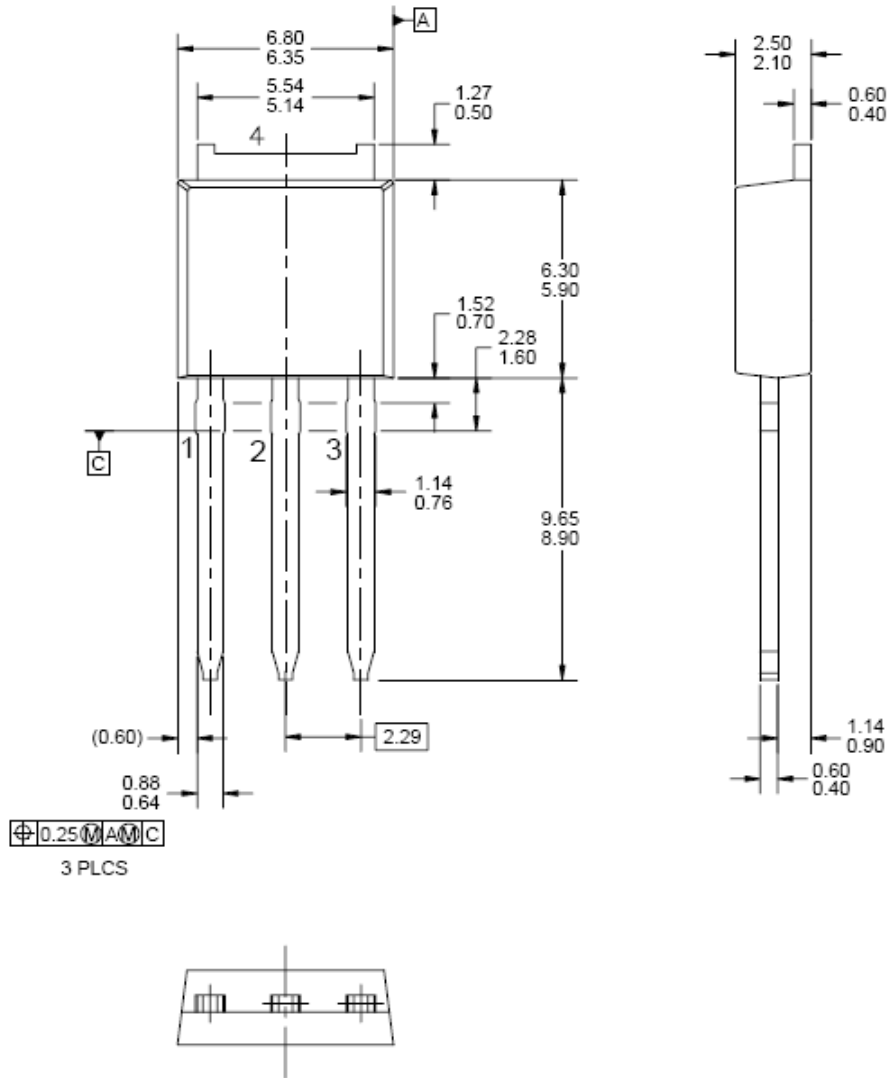
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Dimensions in Millimeters

Mechanical Dimensions

I - PAK



Dimensions in Millimeters





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