

FDD8N50NZ

N-Channel MOSFET

500V, 6.5A, 0.85Ω

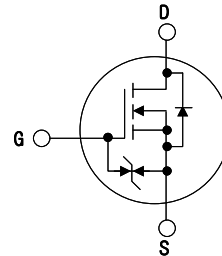
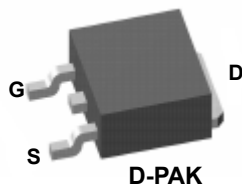
Features

- $R_{DS(on)} = 0.77\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 3.25A$
- Low Gate Charge (Typ. 14nC)
- Low C_{rss} (Typ. 5pF)
- Fast Switching
- 100% Avalanche Tested
- Improve dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Description

This N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advance technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	±25	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	6.5
		-Continuous ($T_C = 100^\circ\text{C}$)	3.9
I_{DM}	Drain Current	- Pulsed (Note 1)	26
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	287
I_{AR}	Avalanche Current	(Note 1)	6.5
E_{AR}	Repetitive Avalanche Energy	(Note 1)	9
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	90
		- Derate above 25°C	0.7
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8N50NZ	FDD8N50NZVT	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.5	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$	-	-	1 10	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 3.25\text{A}$	-	0.77	0.85	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 3.25\text{A}$ (Note 4)	-	6.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	565	735	pF
C_{oss}	Output Capacitance		-	80	105	pF
C_{rss}	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 6.5\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	14	18	nC
Q_{gs}	Gate to Source Gate Charge		-	4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	6	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 6.5\text{A}$ $R_G = 25\Omega, V_{GS} = 10\text{V}$ (Note 4, 5)	-	17	45	ns
t_r	Turn-On Rise Time		-	34	80	ns
$t_{d(off)}$	Turn-Off Delay Time		-	43	95	ns
t_f	Turn-Off Fall Time		-	27	60	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	8	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	30	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 6.5\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 6.5\text{A}$	-	228	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	1.43	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 13.6\text{mH}, I_{AS} = 6.5\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 6.5\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

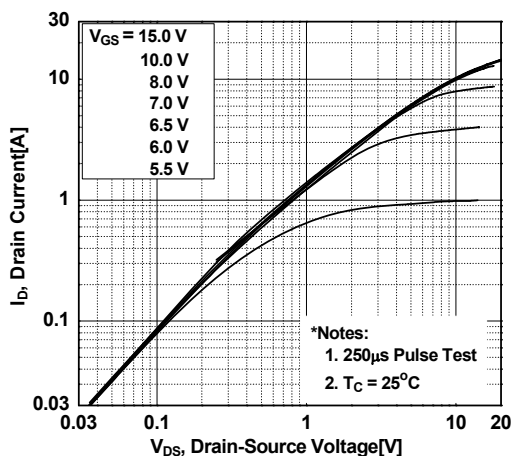


Figure 2. Transfer Characteristics

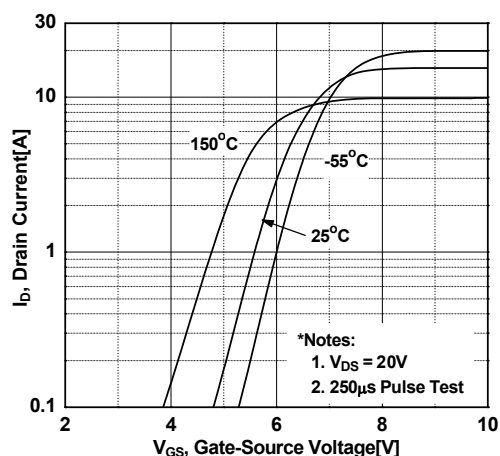


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

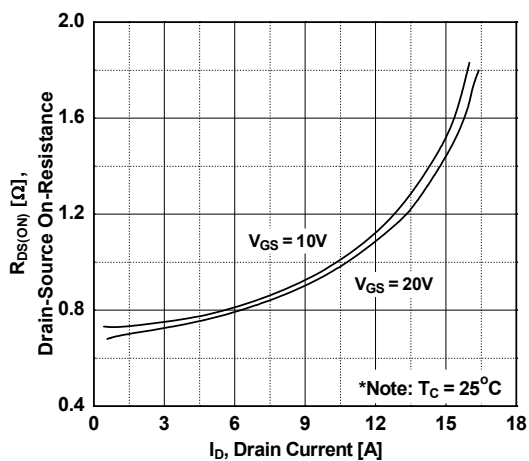


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

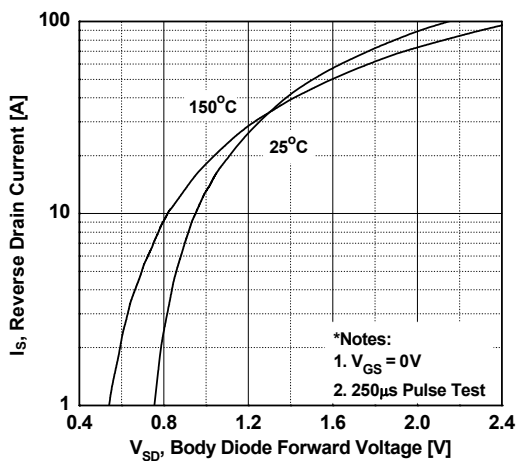


Figure 5. Capacitance Characteristics

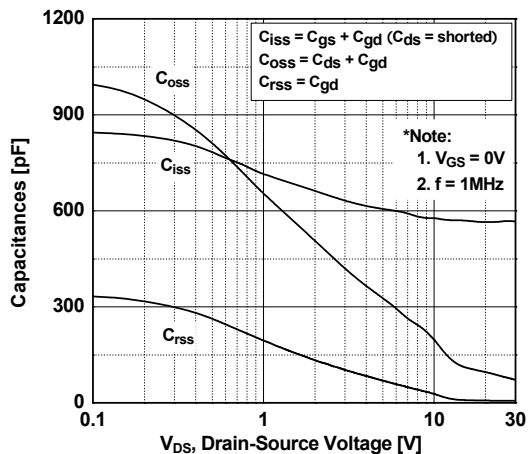
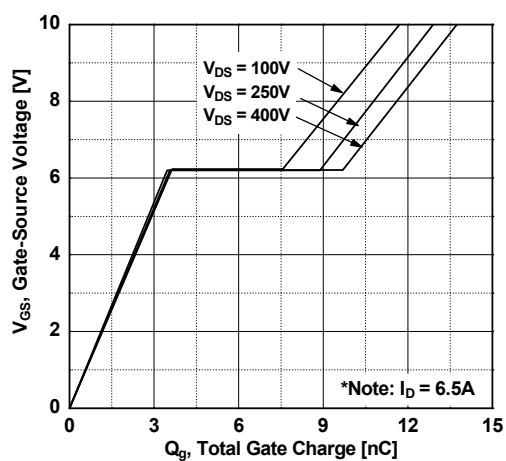


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

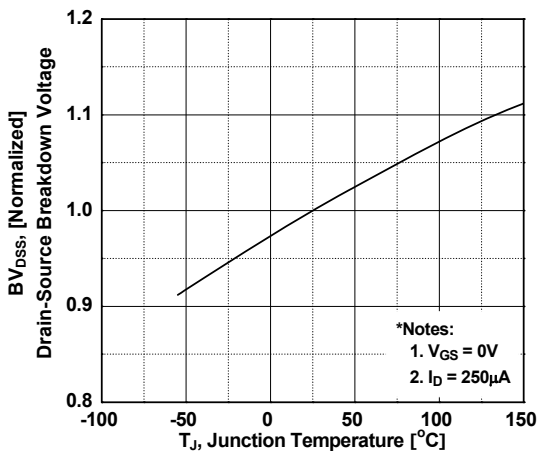


Figure 8. On-Resistance Variation vs. Temperature

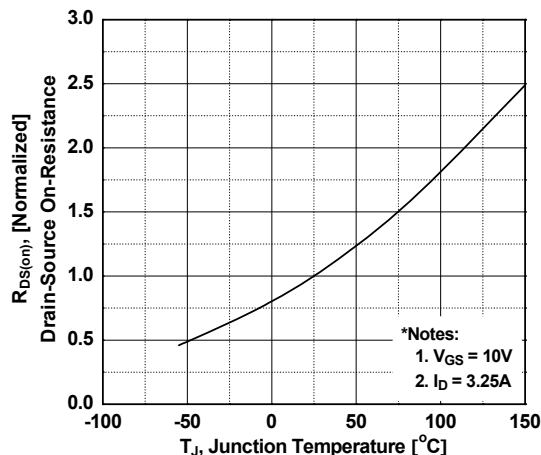


Figure 9. Maximum Safe Operating Area

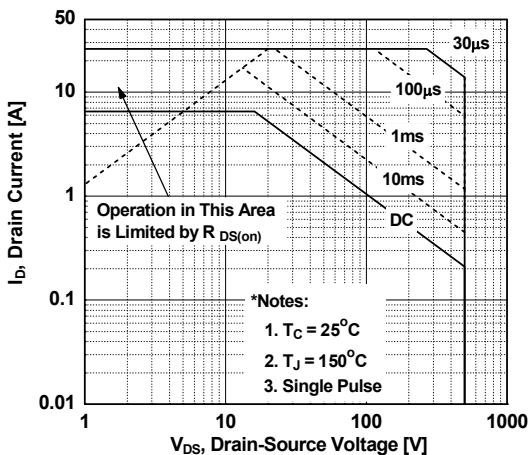


Figure 10. Maximum Drain Current vs. Case Temperature

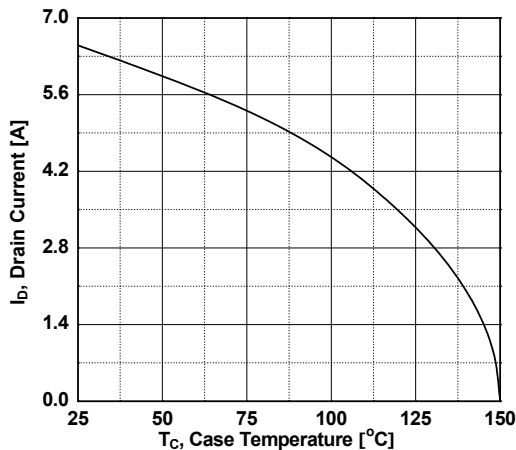
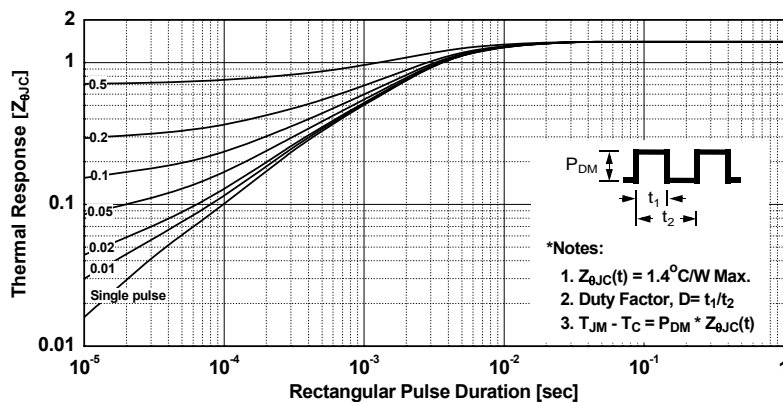
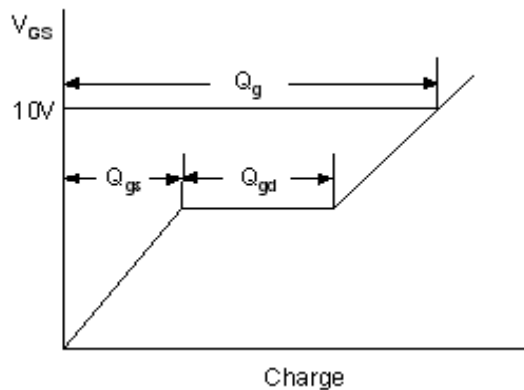
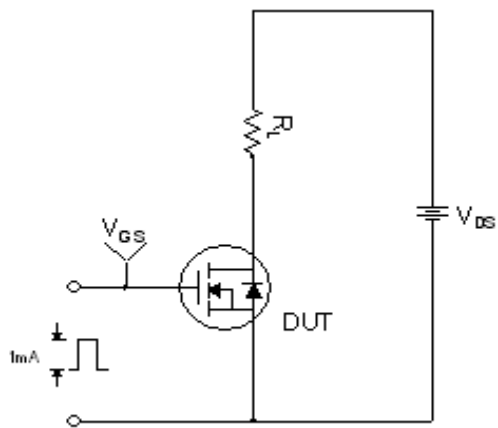


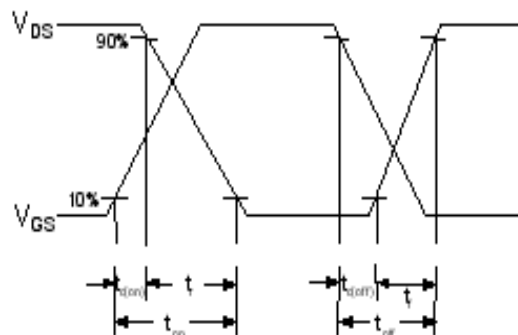
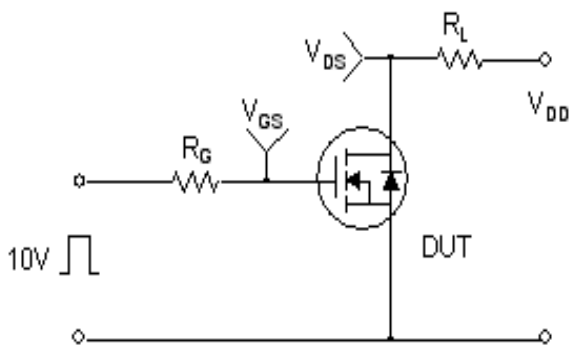
Figure 11. Transient Thermal Response Curve



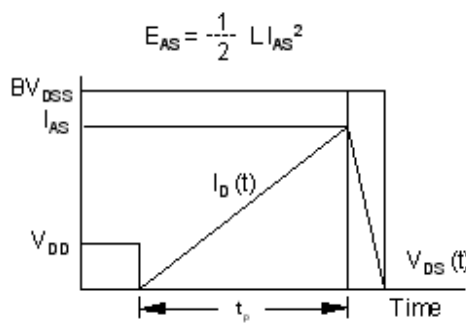
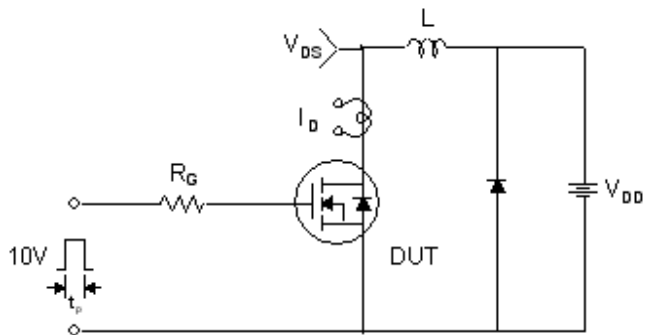
Gate Charge Test Circuit & Waveform



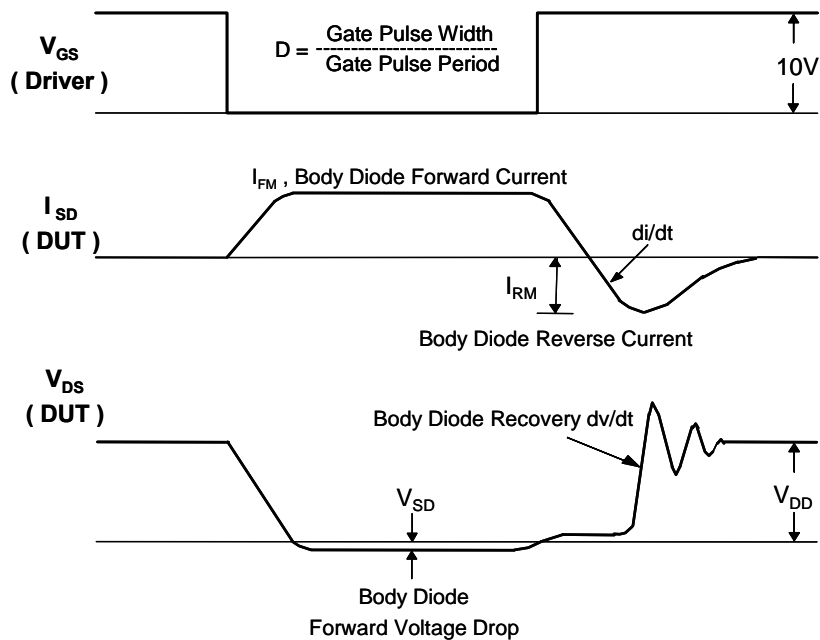
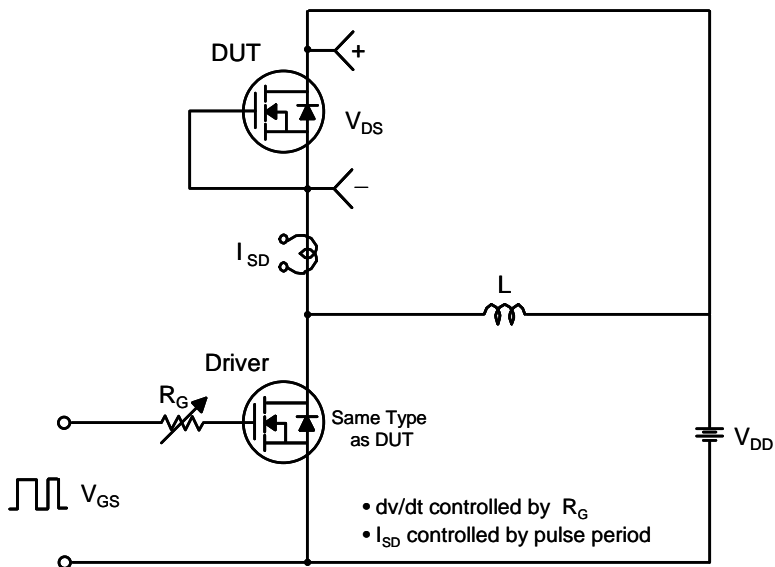
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

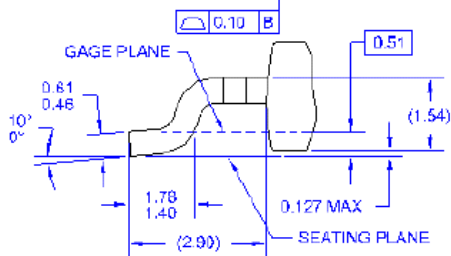
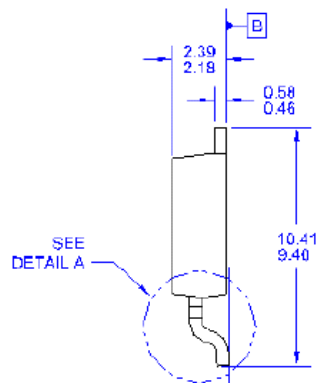
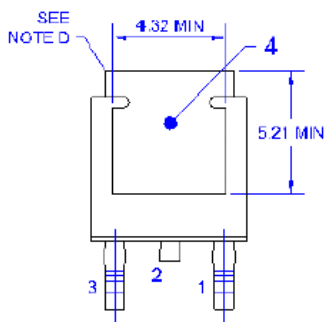
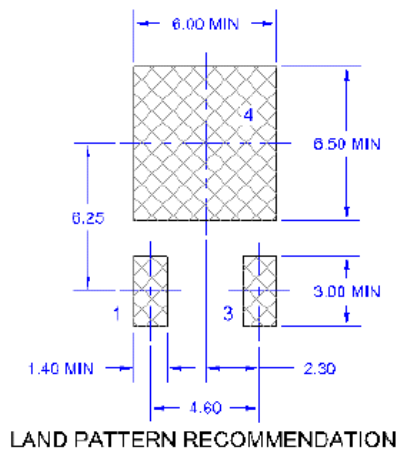
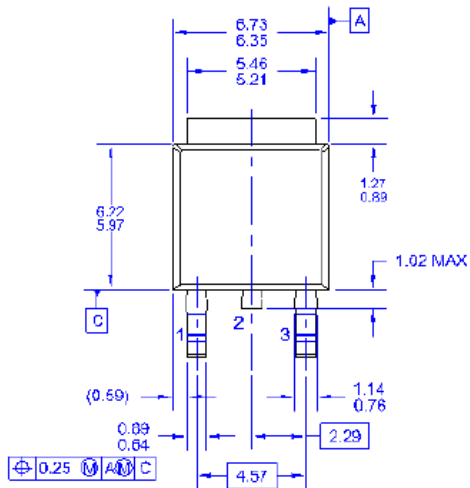


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED:
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND WIRE PROTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A, STD TO220P1003X238-3N.
 H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Dimensions in Millimeters



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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