FAIRCHILD SEMICONDUCTOR®

December 2010

UniFET™

# FDD10N20LZ

## N-Channel MOSFET
## 200V Logic, 7.6A, 0.36Ω

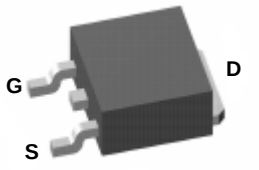
### Features

- $R_{DS(on)}$ = 0.30Ω ( Typ.) @ $V_{GS}$ = 10V, $I_D$ = 3.8A
- Low Gate Charge ( Typ.12nC)
- Low $C_{rss}$ ( Typ.11pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

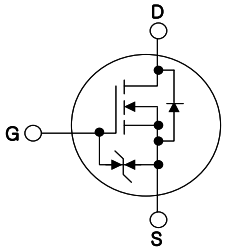
### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advance technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.




**D-PAK**
**FDD- Series**




## MOSFET Maximum Ratings $T_C$ = 25°C unless otherwise noted*

| Symbol | Parameter | | | FDD10N20LZ | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | | 200 | V |
| $V_{GSS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current | -Continuous ($T_C$ = 25°C) | | 7.6 | A |
| | | -Continuous ($T_C$ = 100°C) | | 4.5 | |
| $I_{DM}$ | Drain Current | - Pulsed | (Note 1) | 30 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | | (Note 2) | 121 | mJ |
| $I_{AR}$ | Avalanche Current | | (Note 1) | 7.6 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | | (Note 1) | 8.3 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | | (Note 3) | 10 | V/ns |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C) | | 56 | W |
| | | - Derate above 25°C | | 0.45 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | | -55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds | | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | - | 2.2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | - | 110 | |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDD10N20LZ | FDD10N20LZ | D-PAK | 380mm | 16mm | 2500 |

## Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

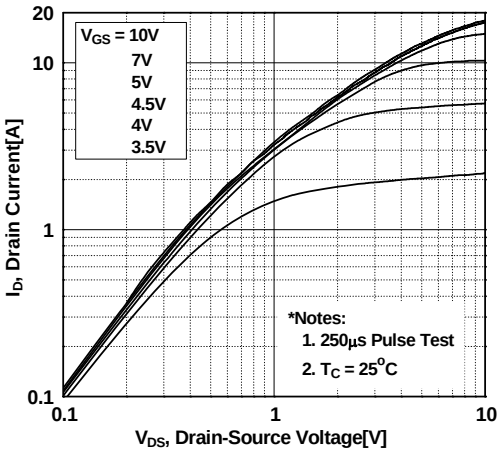
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250μA, $V_{GS}$ = 0V, $T_C = 25^oC$ | 200 | - | - | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, Referenced to $25^oC$ | - | 0.2 | - | $V/^oC$ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 200V, $V_{GS}$ = 0V | - | - | 1 | μA |
| | | $V_{DS}$ = 160V, $T_C = 125^oC$ | - | - | 10 | |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{GS}$ = ±16V, $V_{DS}$ = 0V | - | - | ±10 | μA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1.0 | - | 2.5 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10V, $I_D$ = 3.8A | - | 0.30 | 0.36 | Ω |
| | | $V_{GS}$ = 5V, $I_D$ = 3.8A | - | 0.32 | 0.38 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20V, $I_D$ = 3.8A (Note 4) | - | 8 | - | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, $V_{GS}$ = 0V f = 1MHz | - | 440 | 585 | pF |
| $C_{oss}$ | Output Capacitance | | - | 75 | 100 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 11 | 17 | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS}$ = 100V $I_D$ = 7.6A $V_{GS}$ = 10V (Note 4, 5) | - | 12 | 16 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 2 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | - | 3.5 | - | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 100V, $I_D$ = 7.6A $R_G$ = 25Ω (Note 4, 5) | - | 10 | 30 | ns |
| $t_r$ | Turn-On Rise Time | | - | 15 | 40 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 55 | 120 | ns |
| $t_f$ | Turn-Off Fall Time | | - | 25 | 60 | ns |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 7.6 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 30 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0V, $I_{SD}$ = 7.6A | - | - | 1.4 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0V, $I_{SD}$ = 7.6A $dI_F/dt$ = 100A/μs (Note 4) | - | 115 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 0.5 | - | μC |

**Notes:**

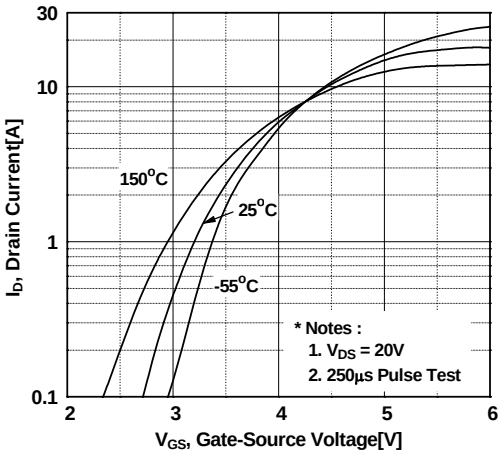
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 4.2mH, $I_{AS}$ = 7.6A, $V_{DD}$ = 50V, $R_G$ = 25Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 7.6A, di/dt ≤ 200A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

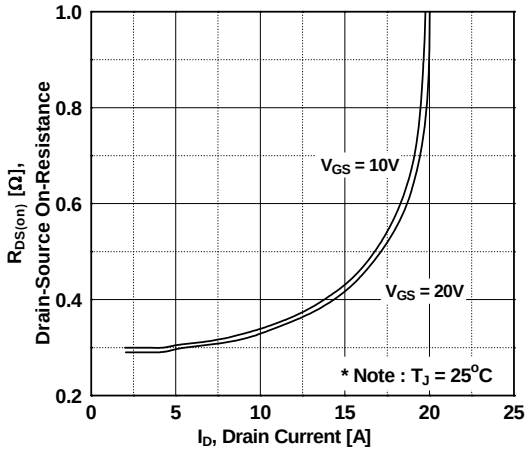
### Figure 1. On-Region Characteristics



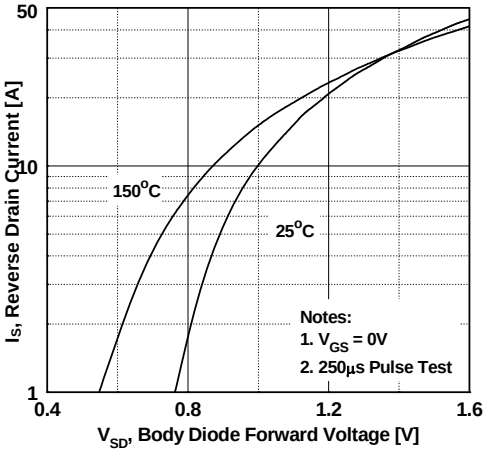

### Figure 2. Transfer Characteristics



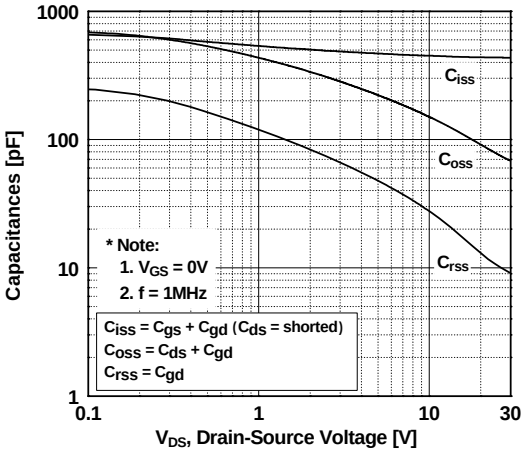

### Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage



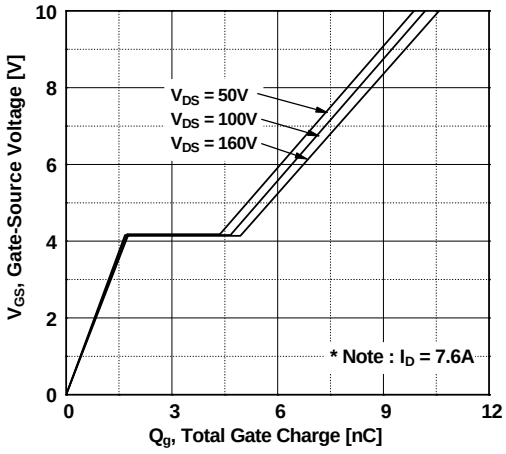

### Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature




### Figure 5. Capacitance Characteristics




### Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

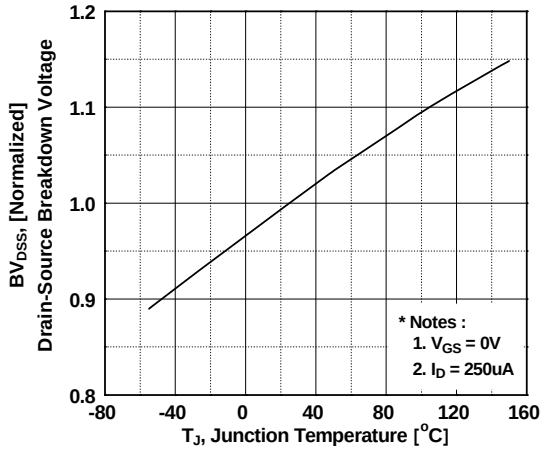



**Figure 8. On-Resistance Variation vs. Temperature**

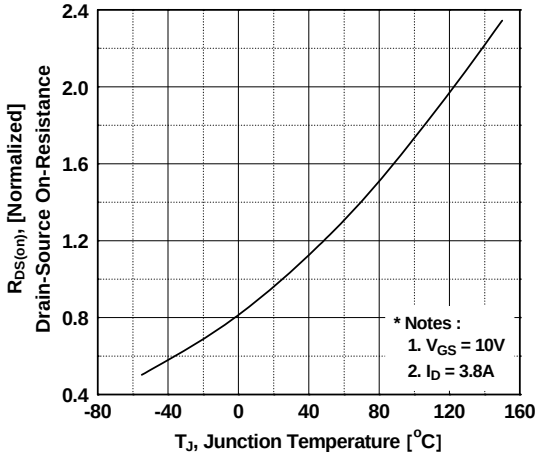



**Figure 9. Maximum Safe Operating Area - FDD10N20LZ**

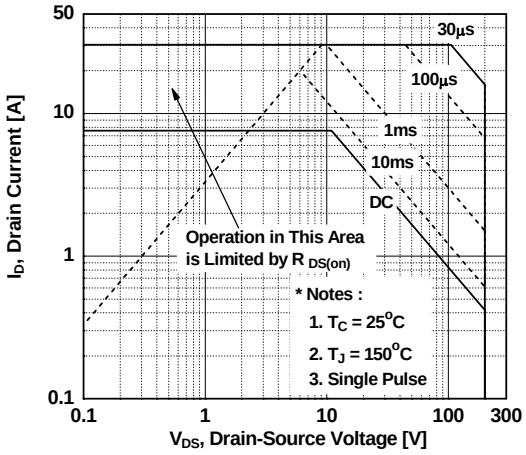



**Figure 10. Maximum Drain Current vs. Case Temperature**

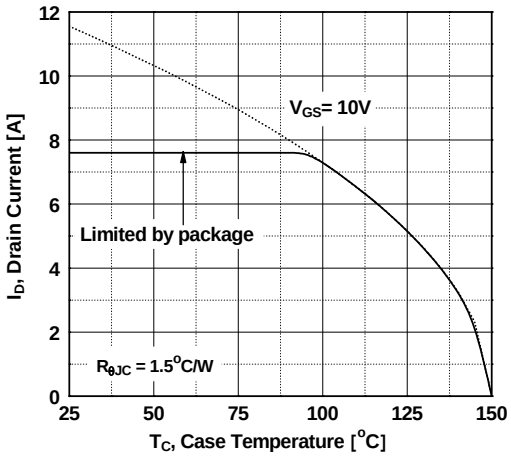
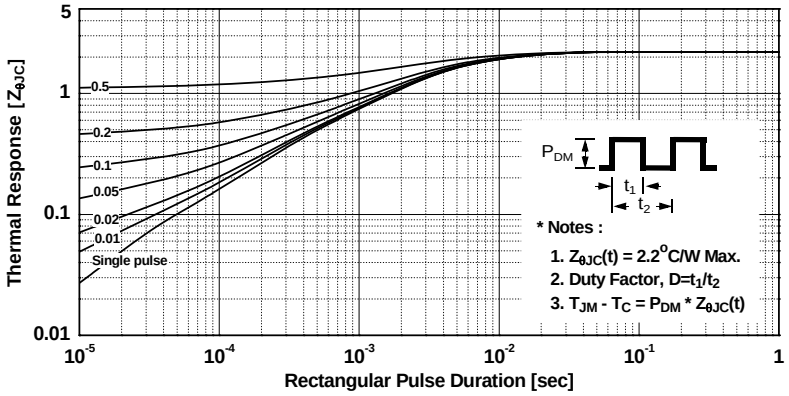
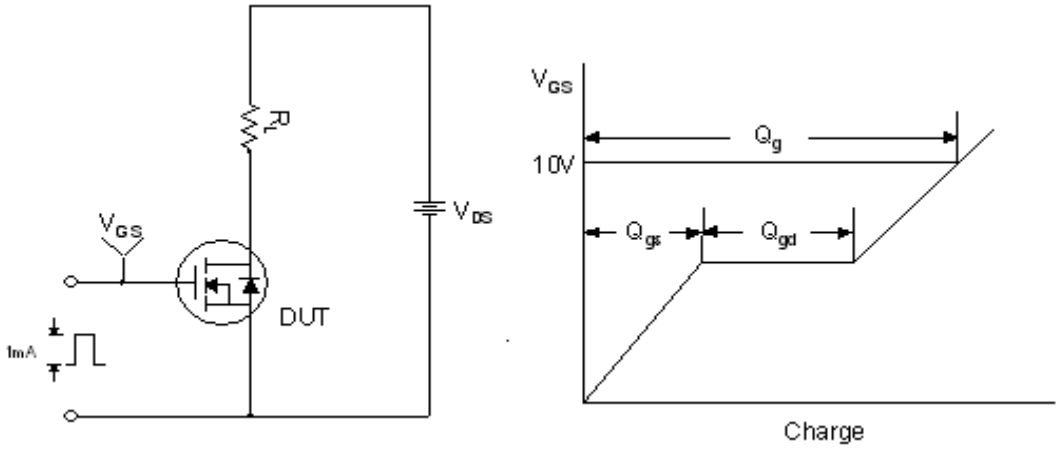


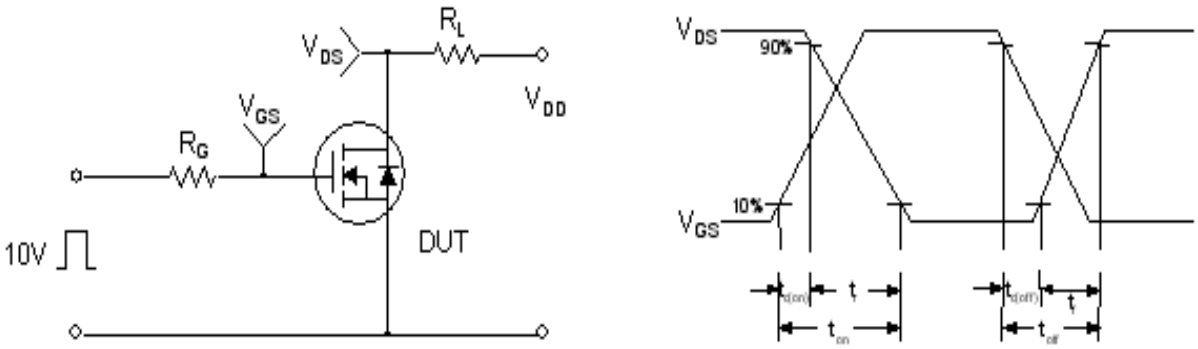

**Figure 11. Transient Thermal Response Curve - FDD10N20LZ**



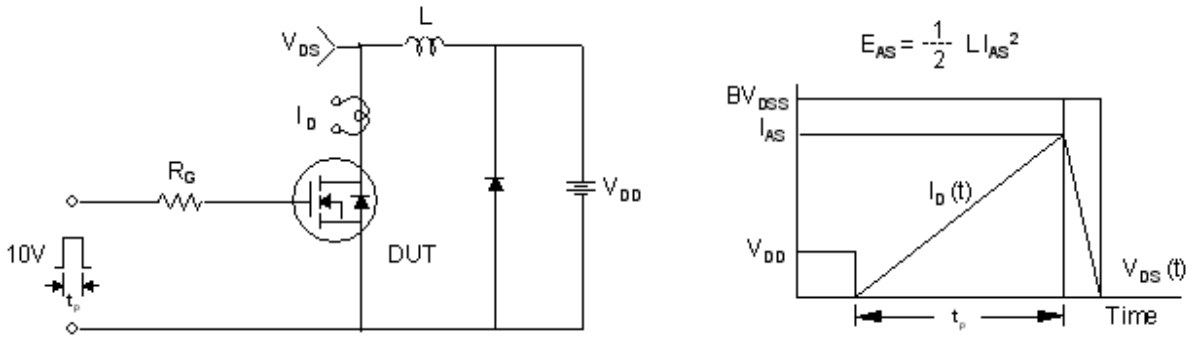
**Gate Charge Test Circuit & Waveform**



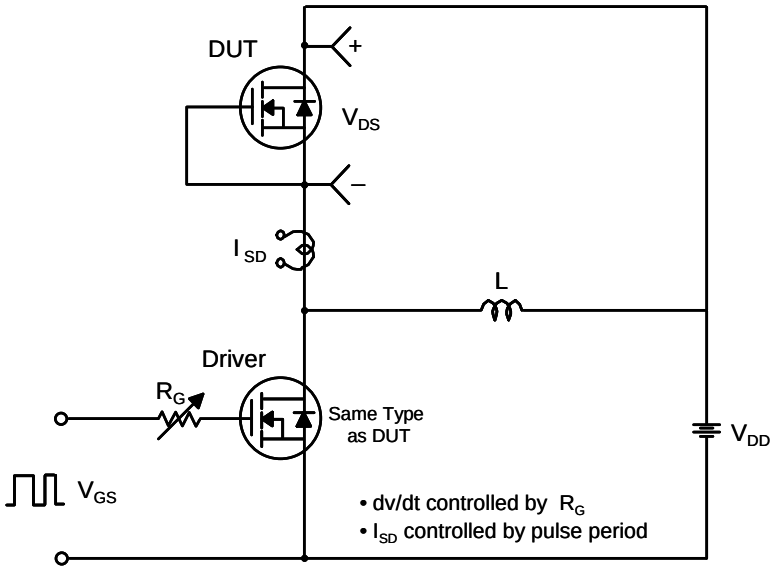

**Resistive Switching Test Circuit & Waveforms**

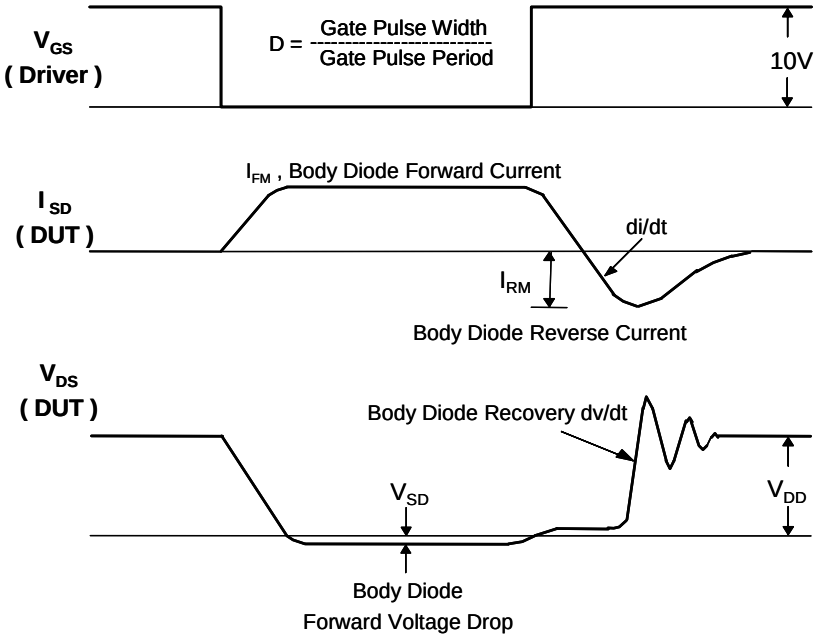



**Unclamped Inductive Switching Test Circuit & Waveforms**



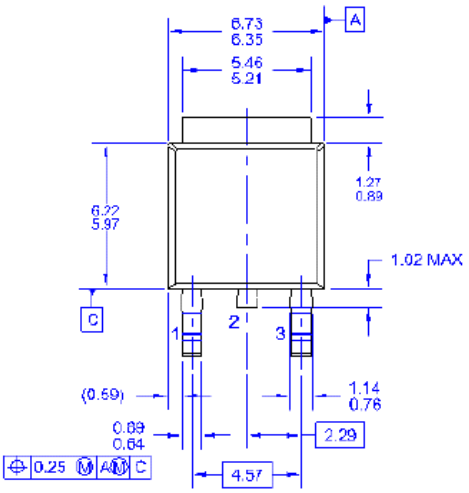
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**

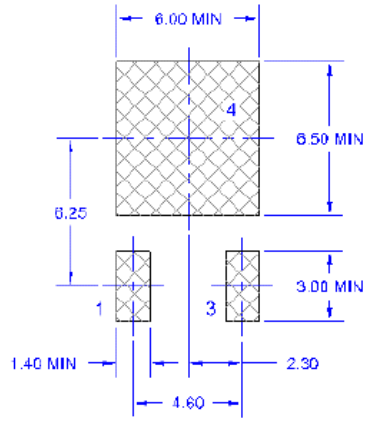


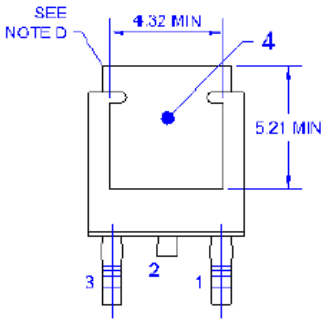
## Mechanical Dimensions

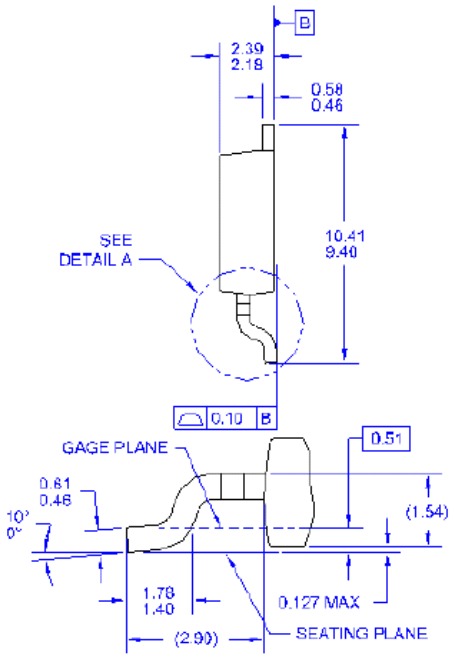
# D-PAK




LAND PATTERN RECOMMENDATION




NOTES: UNLESS OTHERWISE SPECIFIED
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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X235-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REVB

Dimensions in Millimeters

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|---|---|---|
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