

# FDP075N15A\_F102 / FDB075N15A

## N-Channel PowerTrench® MOSFET

150V, 130A, 7.5mΩ

### Features

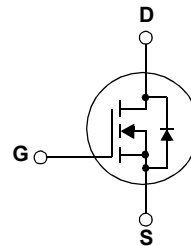
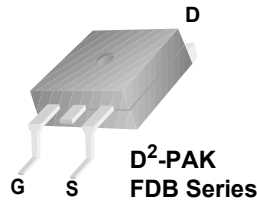
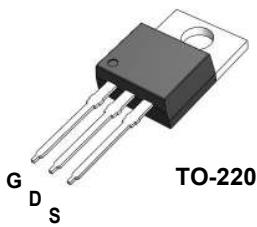
- $R_{DS(on)} = 6.25m\Omega$  (Typ.) @  $V_{GS} = 10V, I_D = 100A$
- Fast Switching
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC to DC Converters
- Synchronous Rectification for Telecommunication PSU
- Battery Charger
- AC motor drives and Uninterruptible Power Supplies
- Off-line UPS



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted\*

Symbol	Parameter	FDP075N15A_F102 FDB075N15A	Units
$V_{DSS}$	Drain to Source Voltage	150	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ C$ )	130
		-Continuous ( $T_C = 100^\circ C$ )	92
$I_{DM}$	Drain Current	- Pulsed (Note 1)	522
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	588
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	6.0
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ )	333
		- Derate above $25^\circ C$	2.22
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

\*Package limitation current is 120A.

### Thermal Characteristics

Symbol	Parameter	FDP075N15A_F102 FDB075N15A	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.45	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

## Package Marking and Ordering Information

Device Marking	Device	Package	Description	Quantity
FDP075N15A	FDP075N15A_F102	TO-220	F102: Trimmed Leads	50

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB075N15A	FDB075N15A	D2-PAK	330mm	24mm	800

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	150	-	-	V
$\Delta BV_{DSS}$ $\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.1	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}$ , $V_{GS} = 0\text{V}$ $V_{DS} = 120\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	$\pm 100$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 100\text{A}$	-	6.25	7.5	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}$ , $I_D = 100\text{A}$ (Note 4)	-	164	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	5525	7350	pF
$C_{oss}$	Output Capacitance		-	516	685	pF
$C_{rss}$	Reverse Transfer Capacitance		-	21	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 75\text{V}$ , $V_{GS} = 0\text{V}$	-	909	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 75\text{V}$ , $I_D = 100\text{A}$ $V_{GS} = 10\text{V}$	-	77	100	nC
$Q_{gs}$	Gate to Source Gate Charge		-	26	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	11	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	16	-	nC
ESR	Equivalent Series Resistance(G-S)		Drain Open, $f = 1\text{MHz}$	-	2.29	-

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{V}$ , $I_D = 100\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GEN} = 4.7\Omega$	-	28	66	ns
$t_r$	Turn-On Rise Time		-	37	84	ns
$t_{d(off)}$	Turn-Off Delay Time		-	62	134	ns
$t_f$	Turn-Off Fall Time		-	21	52	ns

### Drain-Source Diode Characteristics

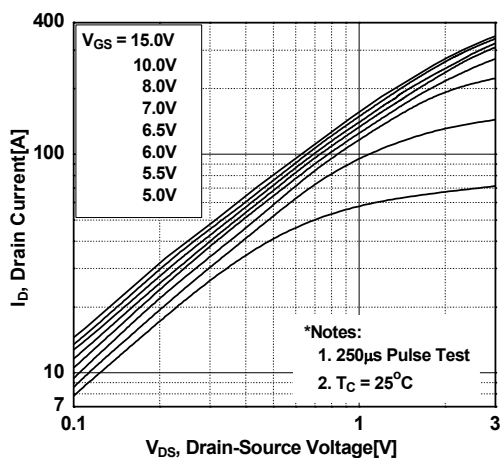
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	130	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	520	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_{SD} = 100\text{A}$	-	-	1.25	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}$ , $V_{DD} = 75\text{V}$ , $I_{SD} = 100\text{A}$	-	97	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	264	-	nC

#### Notes:

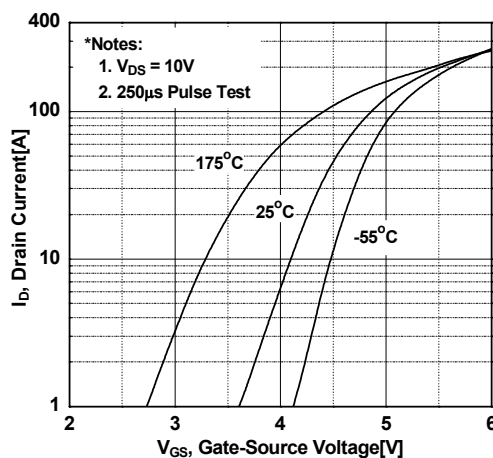
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 19.8\text{ A}$
3.  $I_{SD} \leq 100\text{ A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Dual Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

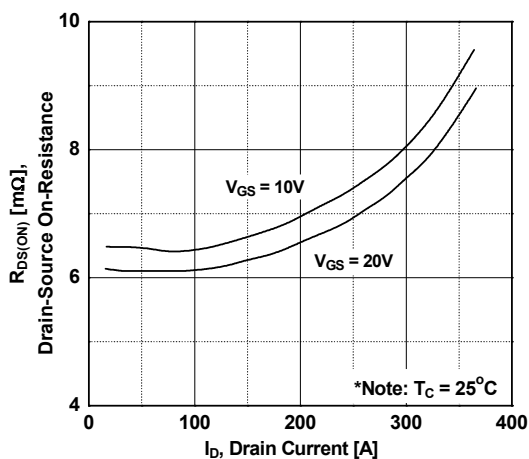
**Figure 1. On-Region Characteristics**



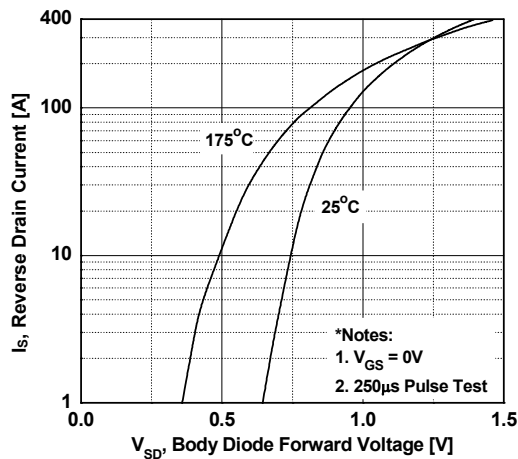
**Figure 2. Transfer Characteristics**



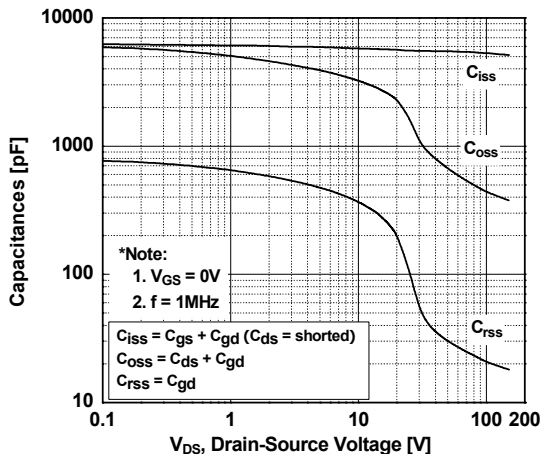
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



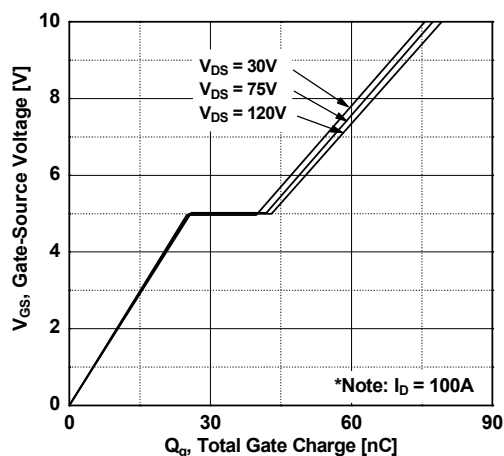
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

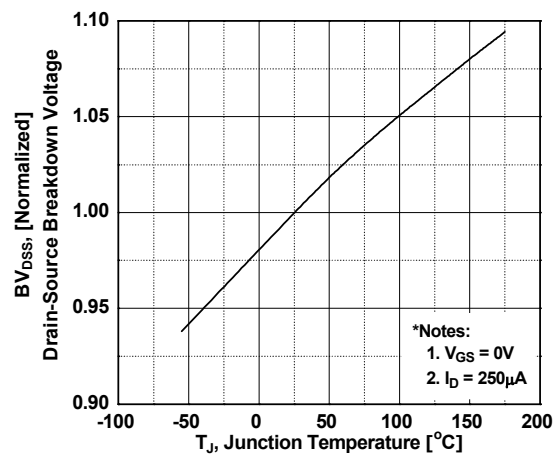


**Figure 6. Gate Charge Characteristics**

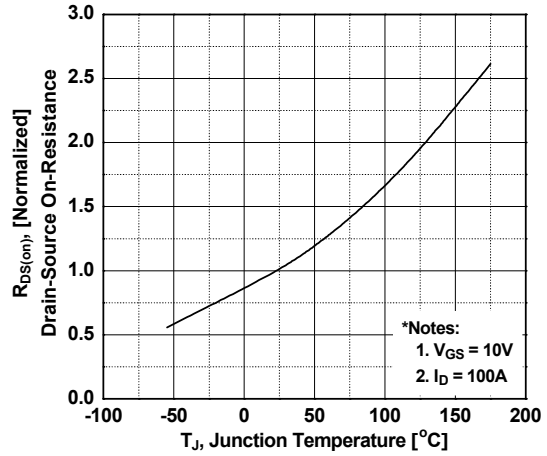


**Typical Performance Characteristics** (Continued)

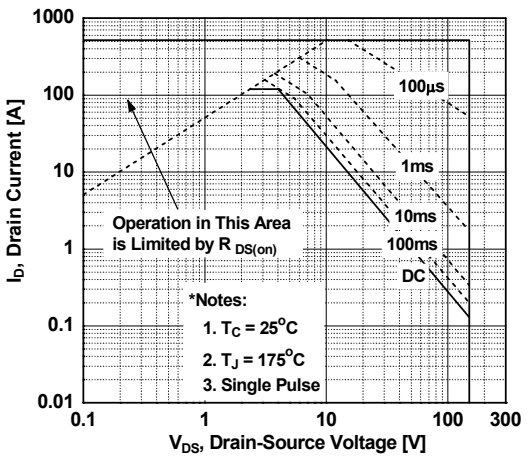
**Figure 7. Breakdown Voltage Variation vs. Temperature**



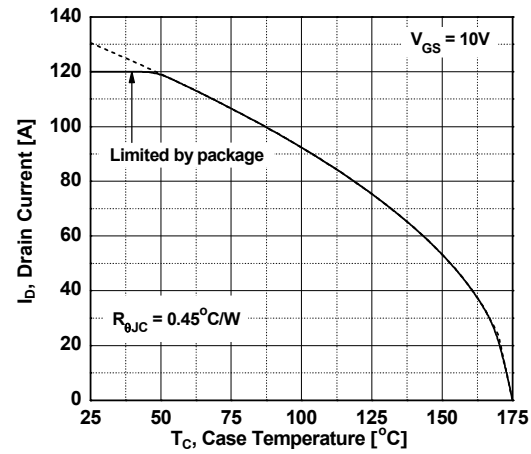
**Figure 8. On-Resistance Variation vs. Temperature**



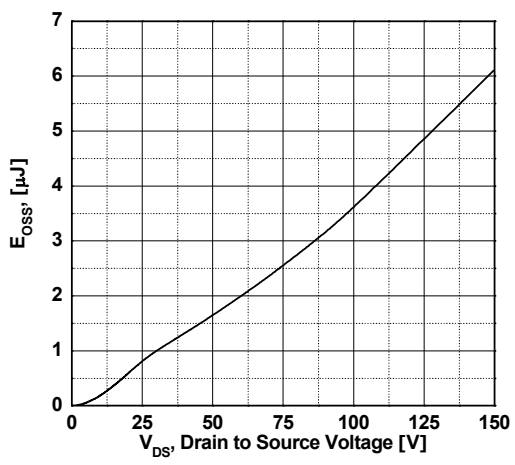
**Figure 9. Maximum Safe Operating Area vs. Case Temperature**



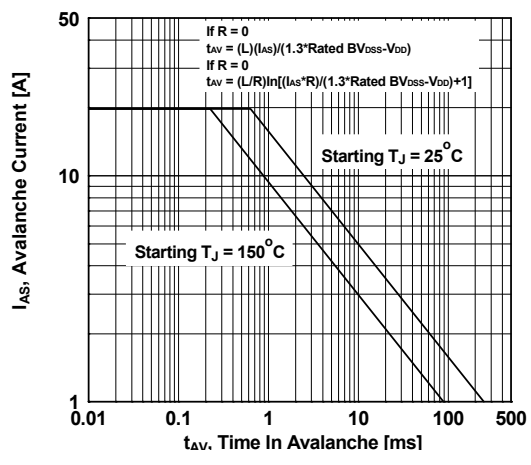
**Figure 10. Maximum Drain Current**



**Figure 11. E\_oss vs. Drain to Source Voltage**

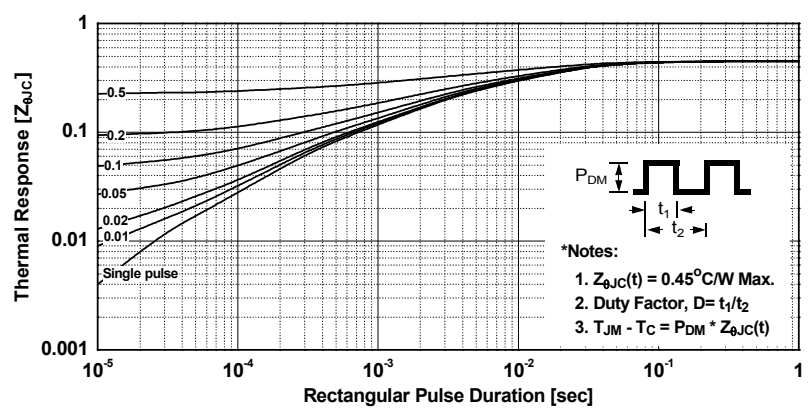


**Figure 12. Unclamped Inductive Switching Capability**

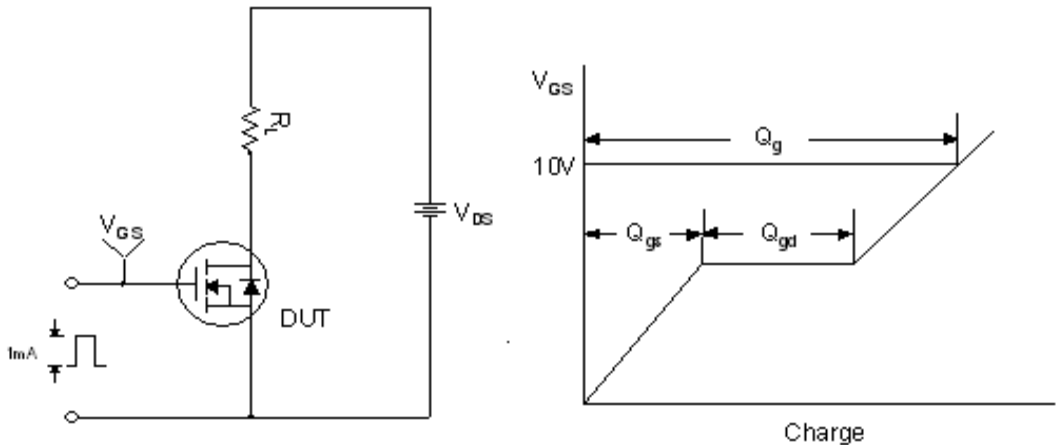


Typical Performance Characteristics (Continued)

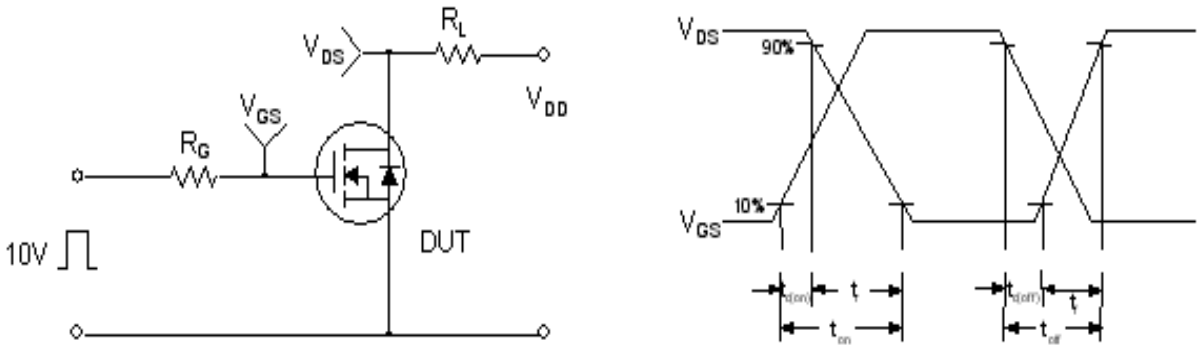
Figure 13. Transient Thermal Response Curve



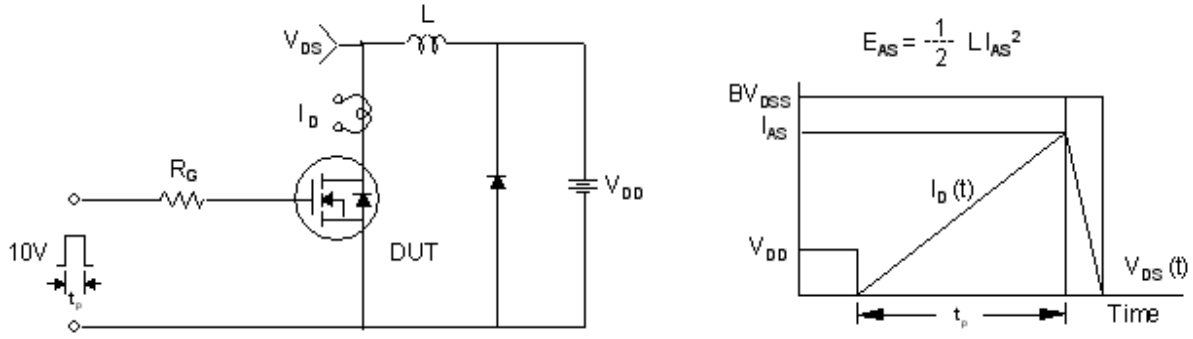
**Gate Charge Test Circuit & Waveform**



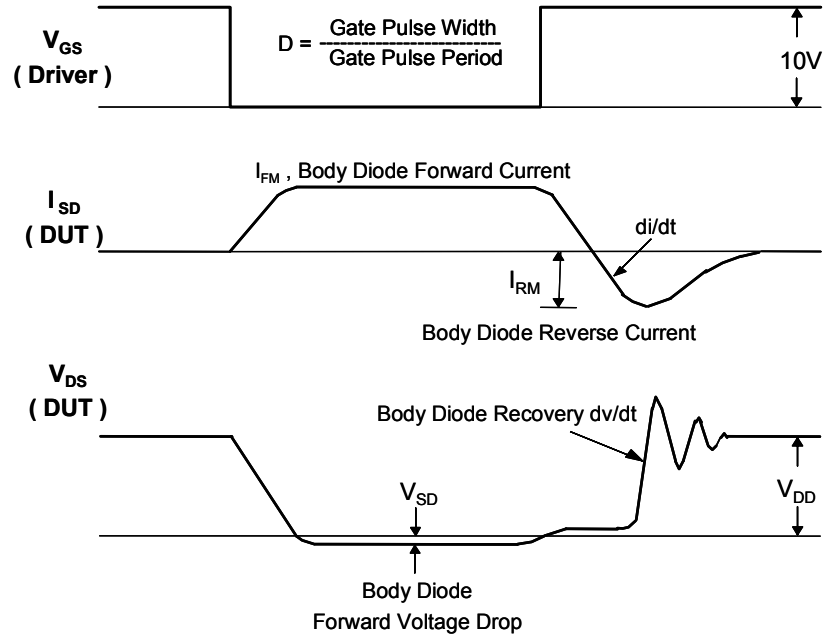
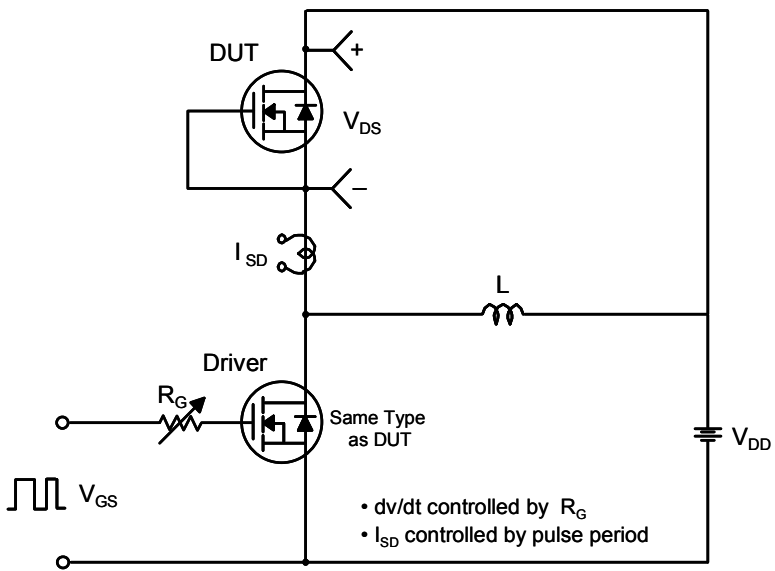
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

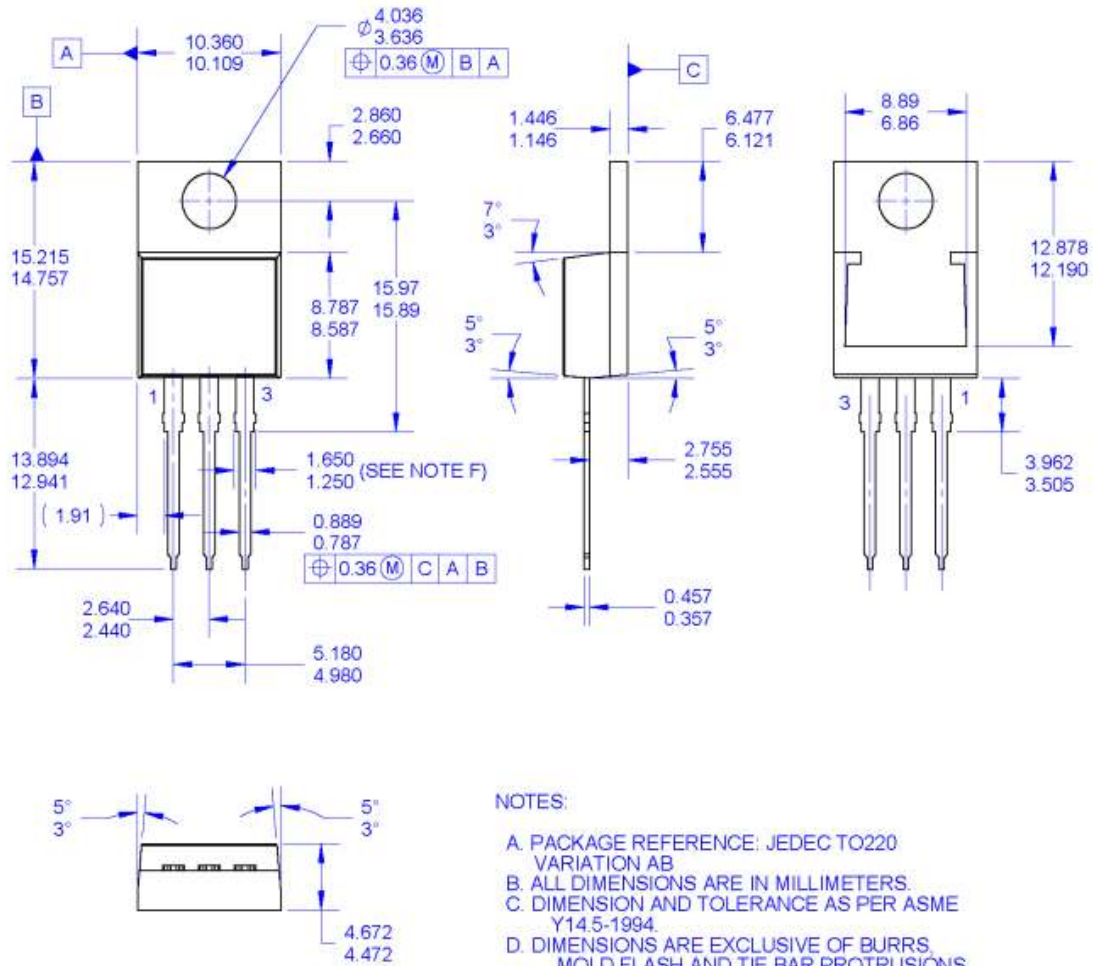


Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

### TO-220 (F102: Trimmed Leads)



#### NOTES:

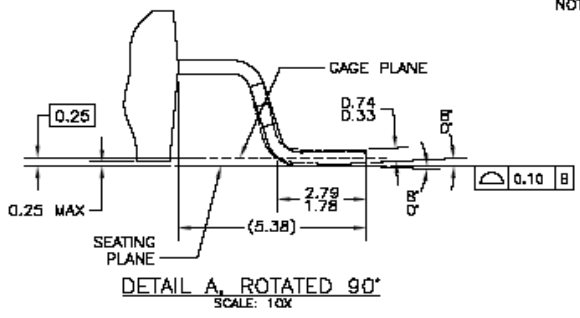
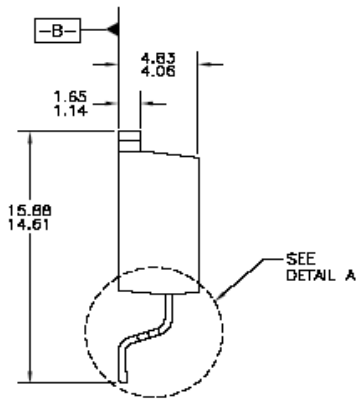
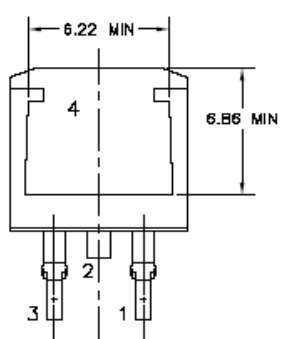
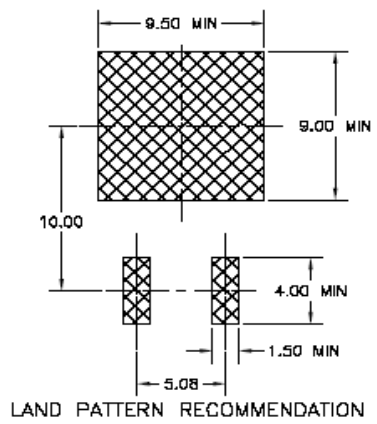
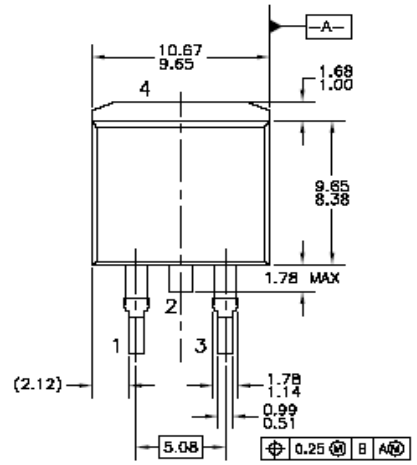
- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. THIS PACKAGE IS FSZZ INTERNAL PRODUCTION AND INTENDED FOR DELTA CUSTOMER ONLY.
- F. MAX WIDTH FOR F102 DEVICE = 1.35mm.
- G. DRAWING FILE NAME: TO220T03REV2

Dimensions in Millimeters



# Mechanical Dimensions

## D<sup>2</sup>PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
  - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
  - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

T02B3AD2REV0

Dimensions in Millimeters



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