FAIRCHILD
SEMICONDUCTOR®

March 2012

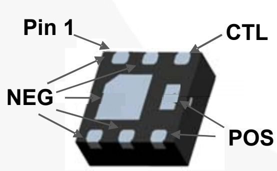
FR011L5J (11mΩ, -30V) Low-Side Reverse Bias Protector

Features

- Up to -30V Reverse-Bias Protection
- Nano Seconds of Reverse-Bias Blocking Response Time
- +29V 24-Hour "Withstand" Rating
- 11mΩ Typical Series Resistance at 5V
- MicroFET™ 2x2mm Package Size
- RoHs Compliant
- USB Tested and Compatible

Applications

- USB 1.0, 2.0 and 3.0 Devices
- USB Charging
- Mobile Devices
- Mobile Medical
- POS Systems
- Toys
- Any DC Barrel Jack Powered Device
- Any DC Devices subject to Negative Hot Plug or Inductive Transients
- Automotive Peripherals



MicroFET2x2 mm

Description

Reverse bias is an increasingly common fault event that may be generated by user error, improperly installed batteries, automotive environments, erroneous connections to third-party chargers, negative "hot plug" transients, inductive transients, and readily available negatively biased rouge USB chargers.

Fairchild circuit protection is proud to offer a new type of reverse bias protection devices. The FR devices are low resistance, series switches that, in the event of a reverse bias condition, shut off power and block the negative voltage to help protect downstream circuits.

The FR devices are optimized for the application to offer best in class reverse bias protection and voltage capabilities while minimizing size, series voltage drop, and normal operating power consumption.

In the event of a reverse bias application, FR011L5J devices effectively provide a full voltage block and can easily protect -0.3V rated silicon.

From a power perspective, in normal bias, an 11mΩ FR device in a 1.5A application will generate only 17mV of voltage drop or 25mW of power loss. In reverse bias, FR devices dissipate less then 20μW in a 16V reverse bias event. This type of performance is not possible with a diode solution.

Benefits extend beyond the device. Due to low power dissipation, not only is the device small, but heat sinking requirements and cost can be minimized as well.

Ordering Information

Part Number	Top Mark	Package	Packing Method
FR011L5J	11L	6-Lead, Molded Leadless Package (MLP), Dual, Non-JEDEC, 2mm Square, Single-Tied DAP	3000 on Tape & Reel; 7-inch Reel, 12mm Tape

Diagrams

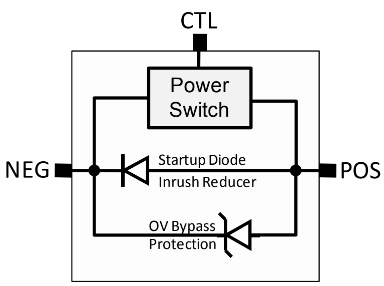


Figure 1. Block Diagram

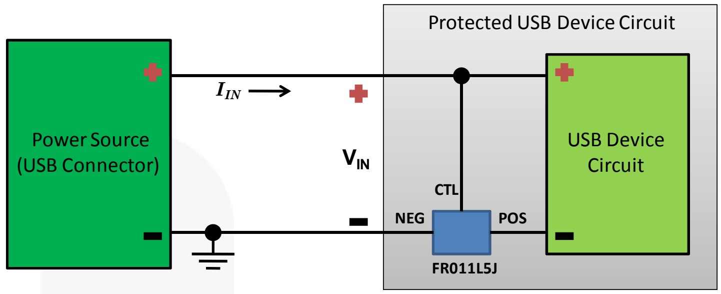


Figure 2. Typical Schematic

Pin Configuration

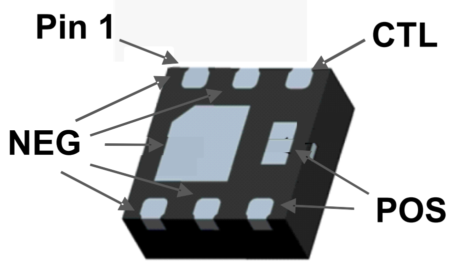


Figure 3. Pin Assignments

Pin Definitions

Name	Pin	Description
POS	4	The ground of the load circuit being protected. Current flows into this pin during normal operation.
CTL	3	The control pin of the device. A positive voltage to the NEG pin turns the switch on and a negative voltage turns the switch to a high-impedance state.
NEG	1, 2, 5, 6	The ground of the input power source. Current flows out of this pin during normal operation.

Absolute Maximum Ratings

Values are at T_A=25°C unless otherwise noted.

Symbol	Parameter		Values	Unit
$V+_{MAX\_OP}$	Steady-State Normal Operating Voltage between CTL and NEG Pins (V_{IN} = $V+_{MAX\_OP}$, I_{IN} = 1.5A, Switch On)		+20	V
$V+_{24}$	24-Hour Normal Operating Voltage Withstand Capability between CTL and NEG Pins (V_{IN} = $V+_{24}$, I_{IN} = 1.5A, Switch On)		+29	
$V-_{MAX\_OP}$	Steady-State Reverse Bias Standoff Voltage between CTL and NEG Pins (V_{IN} = $V-_{MAX\_OP}$)		-30	
T_J	Operating Junction Temperature		150	°C
P_D	Power Dissipation	T_A = 25°C[(2)] *(see Figure 4)*	2.4	W
		T_A = 25°C[(2)] *(see Figure 5)*	0.9	
I_{DIODE_CONT}	Steady-State Diode Continuous Forward Current from POS to NEG		2	A
I_{DIODE_PULSE}	Pulsed Diode Forward Current from POS to NEG (300µs Pulse)		210	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	600	V
		Charged Device Model, JESD22-C101	2000	

Notes:

1. The V_{+24} rating is NOT a survival guarantee. It is a statistically calculated survivability reference point taken on qualification devices, where the predicted failure rate is less than 0.01% at the specified voltage for 24 hours. It is intended to indicate the device's ability to withstand transient events that exceed the recommended operating voltage rating. Specification is based on qualification devices tested using accelerated destructive testing at higher voltages, as well as production pulse testing at the V_{+24} level. Production device field life results may vary. Results are also subject to variation based on implementation, environmental considerations, and circuit dynamics. Systems should never be designed with the intent to normally operate at V_{+24} levels. *Contact Fairchild Semiconductor for additional information.*
2. The device power dissipation and thermal resistance (R_θ) are characterized with device mounted on the following FR4 printed circuit boards, as shown in Figure 4 and Figure 5

Figure 4. 1 Square Inch of 2-ounce copper

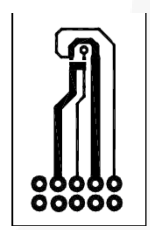


Figure 5. Minimum Pads of 2-ounce Copper

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient[(2)] *(see Figure 4)*	61	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient[(2)] *(see Figure 5)*	153	

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Positive Bias Characteristics						
R_{ON}	Device Resistance, Switch On	V_{IN} = +4V, I_{IN} = 1.5A		13	20	mΩ
		V_{IN} = +5V, I_{IN} = 1.5A		11	15	
		V_{IN} = +5V, I_{IN} = 1.5A, T_J = 125°C		15		
		V_{IN} = +12V, I_{IN} = 1.5A		9	13	
V_{ON}	Input Voltage, V_{IN}, at which Voltage at POS, V_{POS}, Reaches a Certain Level at Given Current	I_{IN} = 100mA, V_{POS} = 45mV, V_{NEG} = 0V	1.4	2.4	3.5	V
$\Delta V_{ON} / \Delta T_J$	Temperature Coefficient of V_{ON}			-3.9		mV/°C
I_{DIODE_CONT}	Continuous Diode Forward Current	V_{CTL} = V_{POS}			2	A
V_F	Diode Forward Voltage	V_{CTL} = V_{POS}, I_{DIODE} = 0.1A, Pulse width < 300µs	0.56	0.60	0.73	V
I_{BIAS}	Bias Current Flowing out of NEG Pin during Normal Bias Operation	V_{CTL} = 5V, V_{NEG} = 0V, No Load		15		nA
Negative Bias Characteristics						
$V-_{MAX\_OP}$	Reverse Bias Breakdown Voltage	I_{IN} = -250µA, V_{CTL} = V_{POS} = 0V			-30	V
$\Delta V-_{MAX\_OP} / \Delta T_J$	Reverse Bias Breakdown Voltage Temperature Coefficient			16		mV/°C
I-	Leakage Current from NEG to POS in Reverse-Bias Condition	V_{NEG} = 20V, V_{CTL} = V_{POS} = 0V		1		µA
t_{RN}	Time to Respond to Negative Bias Condition	V_{NEG} = 5V, V_{CTL} = 0V, C_{LOAD} = 10µF, Reverse Bias Startup Inrush Current = 0.2A			50	ns
Dynamic Characteristics						
C_I	Input Capacitance between CTL and NEG	V_{IN} = -5V, V_{CTL} = V_{POS} = 0V, f = 1MHz		1011		pF
C_S	Switch Capacitance between POS and NEG			81		
C_O	Output Capacitance between CTL and POS			1456		
R_C	Control Internal Resistance			1.7		Ω

Typical Characteristics

T_J = 25°C unless otherwise specified.

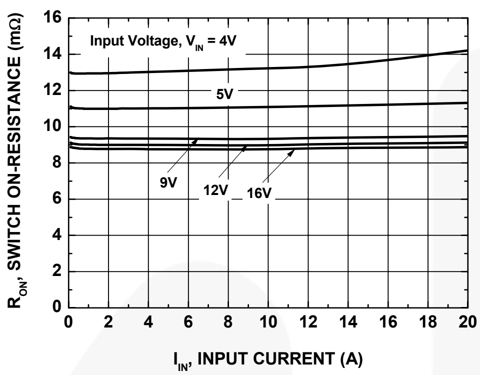


Figure 6. Switch On Resistance vs. Switch Current

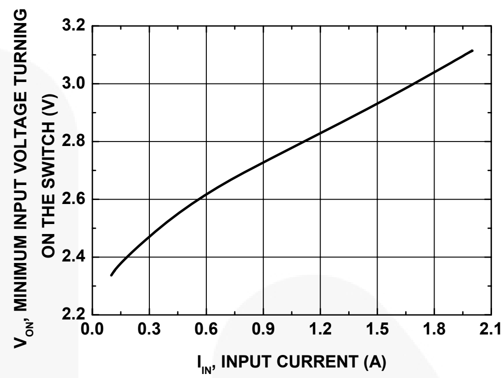


Figure 7. Minimum Input Voltage to Turn On Switch vs. Current at 45mV Switch Voltage Drop

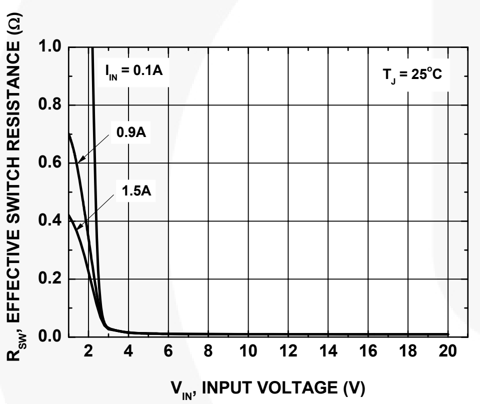


Figure 8. Effective Switch Resistance R_{SW} vs. Input Voltage V_{IN}

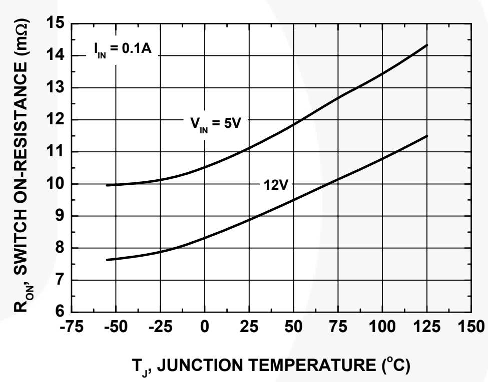


Figure 9. Switch On Resistance vs. Junction Temperature at 0.1A

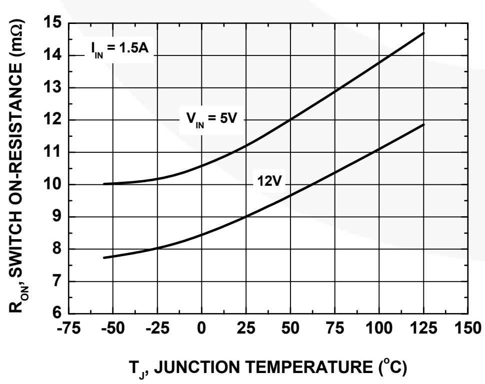


Figure 10. Switch On Resistance vs. Junction Temperature at 1.5A

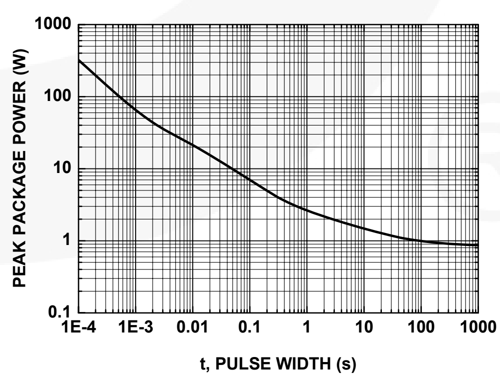


Figure 11. Single-Pulse Maximum Power vs. Time

Typical Characteristics

T_J = 25°C unless otherwise specified.

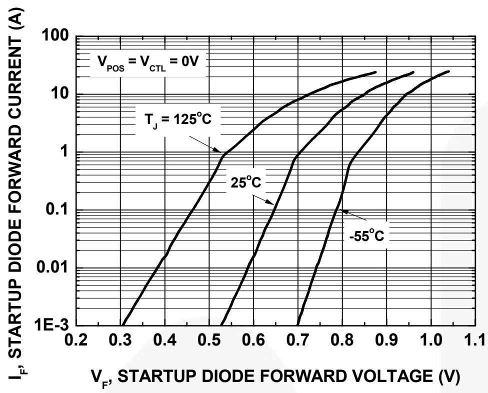


Figure 12. Startup Diode Current vs. Forward Voltage

Application Test Configurations

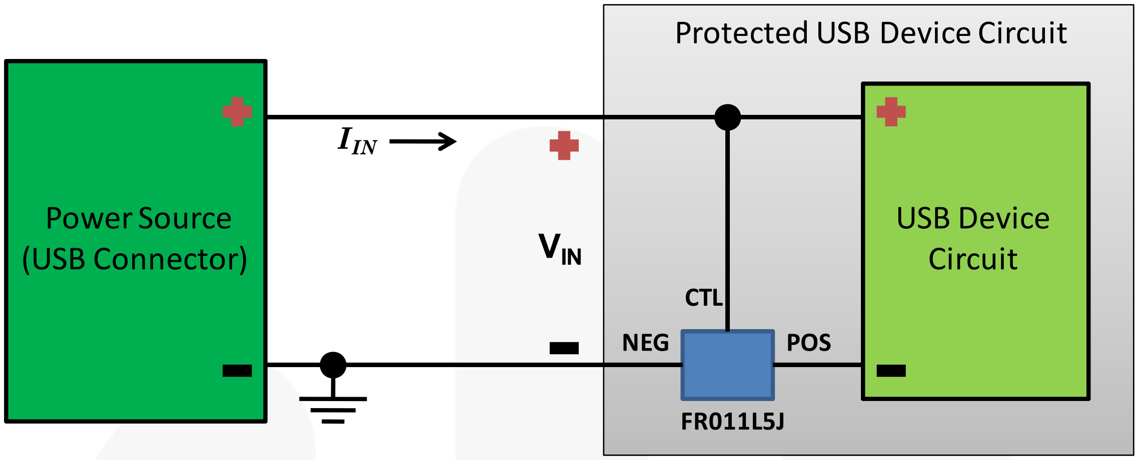


Figure 13. Typical Application Circuit for USB Applications

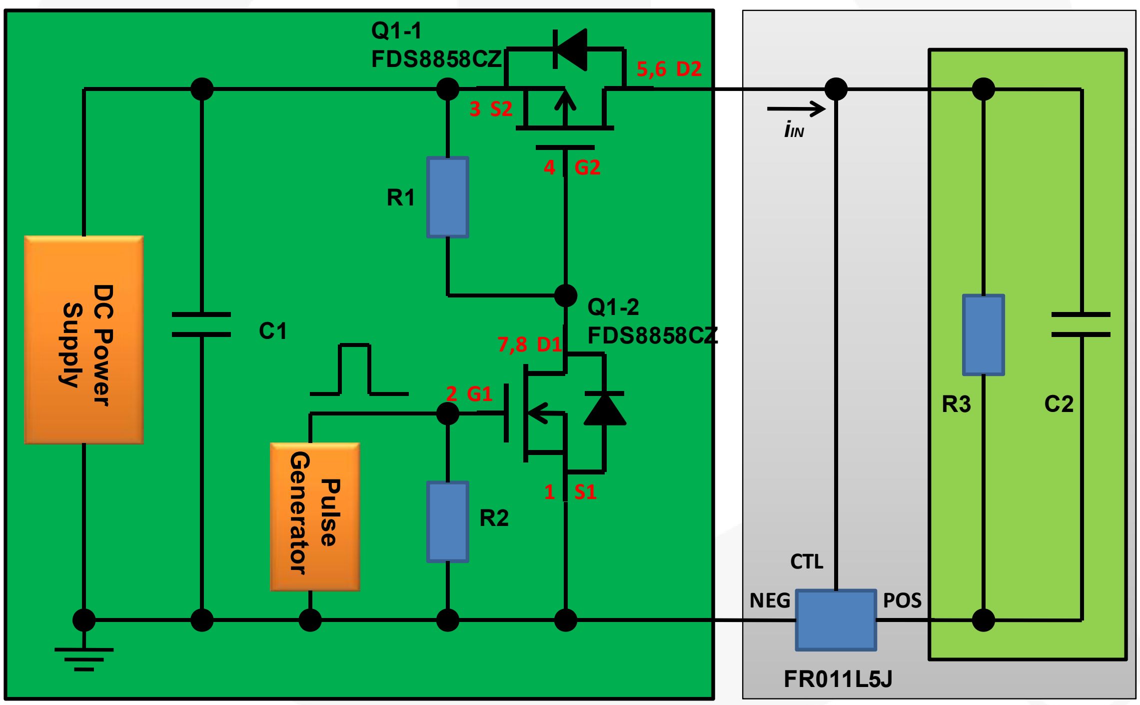


Figure 14. Startup Test Circuit – Normal Bias with FR011L5J

Application Test Configurations (Continued)

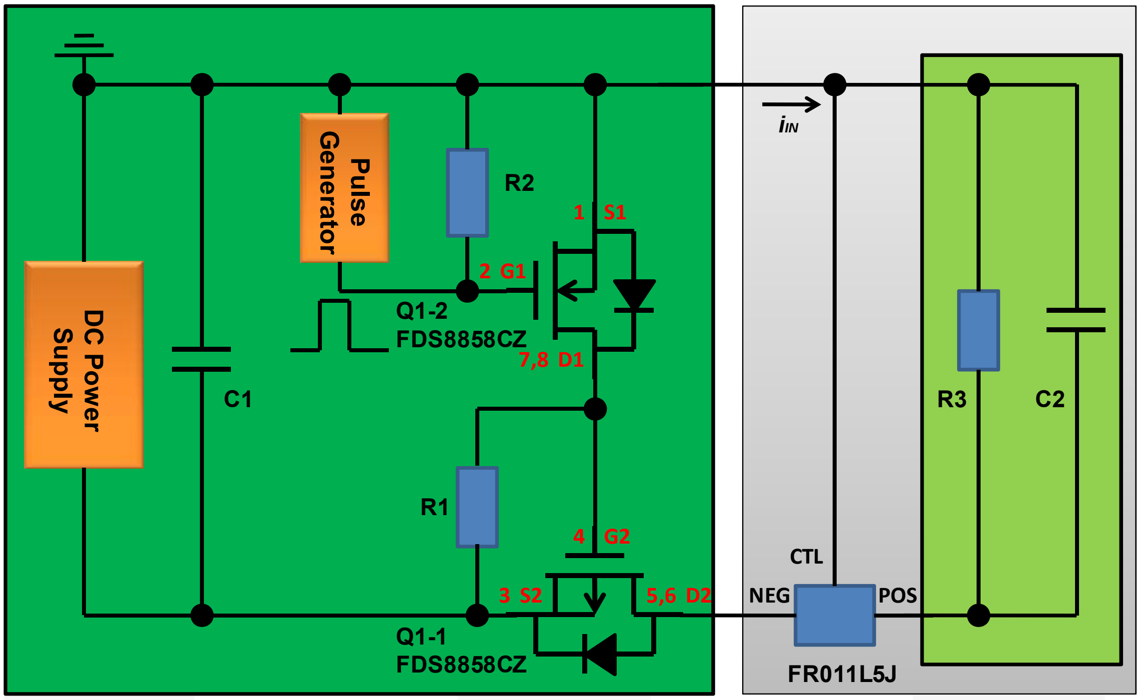


Figure 15. Startup Test Circuit – Reverse Bias with FR011L5J

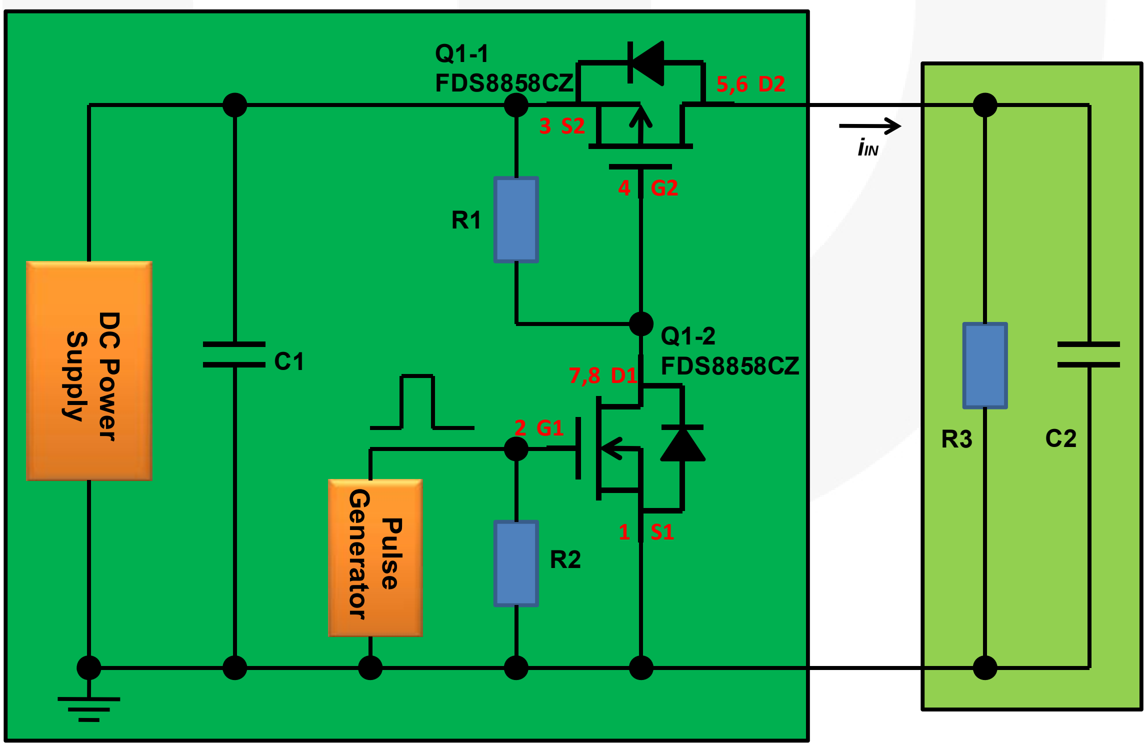


Figure 16. Startup Test Circuit – without FR011L5J

Typical Application Waveforms

Typical USB3.0 conditions.

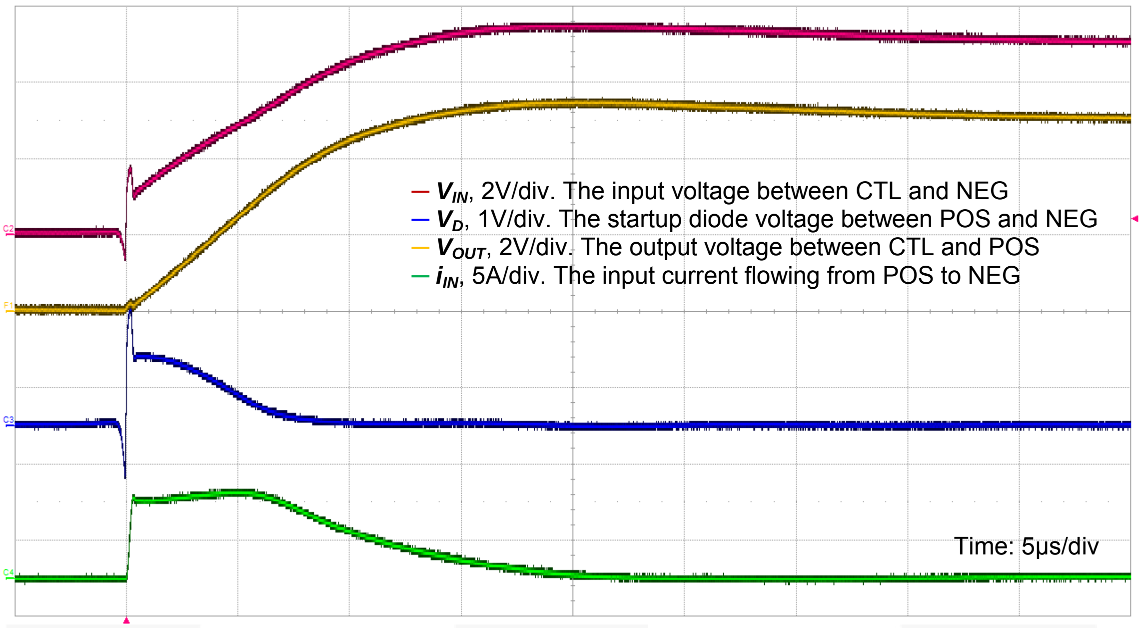


Figure 17. Normal Bias Startup Waveform, DC Power Source=5V, C_1=100µF, C_2=10µF, R_1=R_2=10kΩ, R_3=27Ω

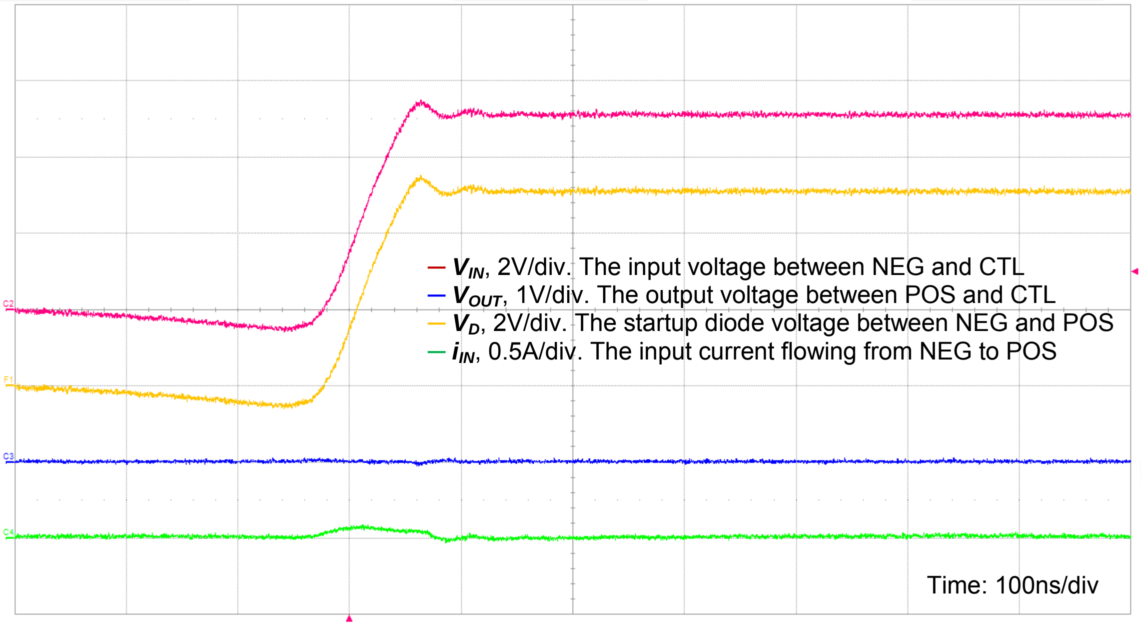


Figure 18. Reverse Bias Startup Waveform, DC Power Source=5V, C_1=100µF, C_2=10µF, R_1=R_2=10kΩ, R_3=27Ω

Typical Application Waveforms (Continued)

Typical USB3.0 conditions.

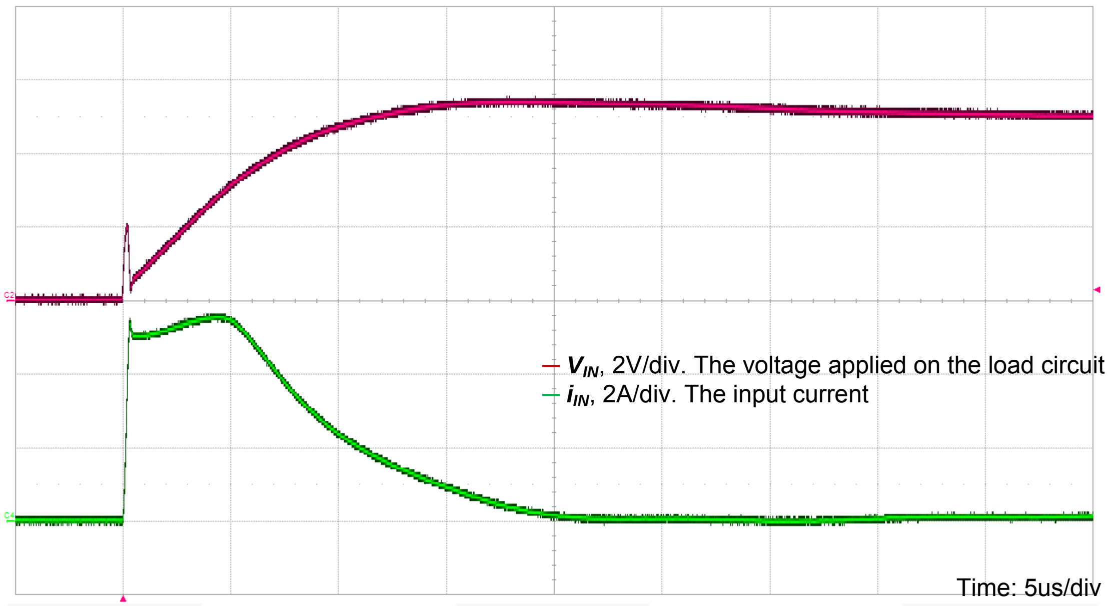


Figure 19. Startup Waveform without FR011L5J, DC Power Source=5V, C_1=100µF, C_2=10uF, R_1=R_2=10kΩ, R_3=27Ω

Application Information

Figure 17 shows the voltage and current waveforms when a virtual USB3.0 device is connected to a 5V source. A USB application allows a maximum source output capacitance of C_1 = 120µF and a maximum device-side input capacitance of C_2 = 10µF plus a maximum load (minimum resistance) of R_3 = 27Ω. C_1 = 100µF, C_2 = 10µF and R_3 = 27Ω were used for testing.

When the DC power source is connected to the circuit *(refer to Figure 13)*, the built-in startup diode initially conducts the current such that the USB device powers up. Due to the initial diode voltage drop, the FR011L5J effectively reduces the peak inrush current of a hot plug event. Under these test conditions, the input inrush current reaches about 6.3A peak. While the current flows, the input voltage increases. The speed of this input voltage increase depends on the time constant formed by the load resistance R_3 and load capacitance C_2. The larger the time constant, the slower the input voltage increase. As the input voltage approaches a level equal to the protector's turn-on voltage, V_{ON}, the protector turns on and operates in Low-Resistance Mode as defined by V_{IN} and operating current I_{IN}.

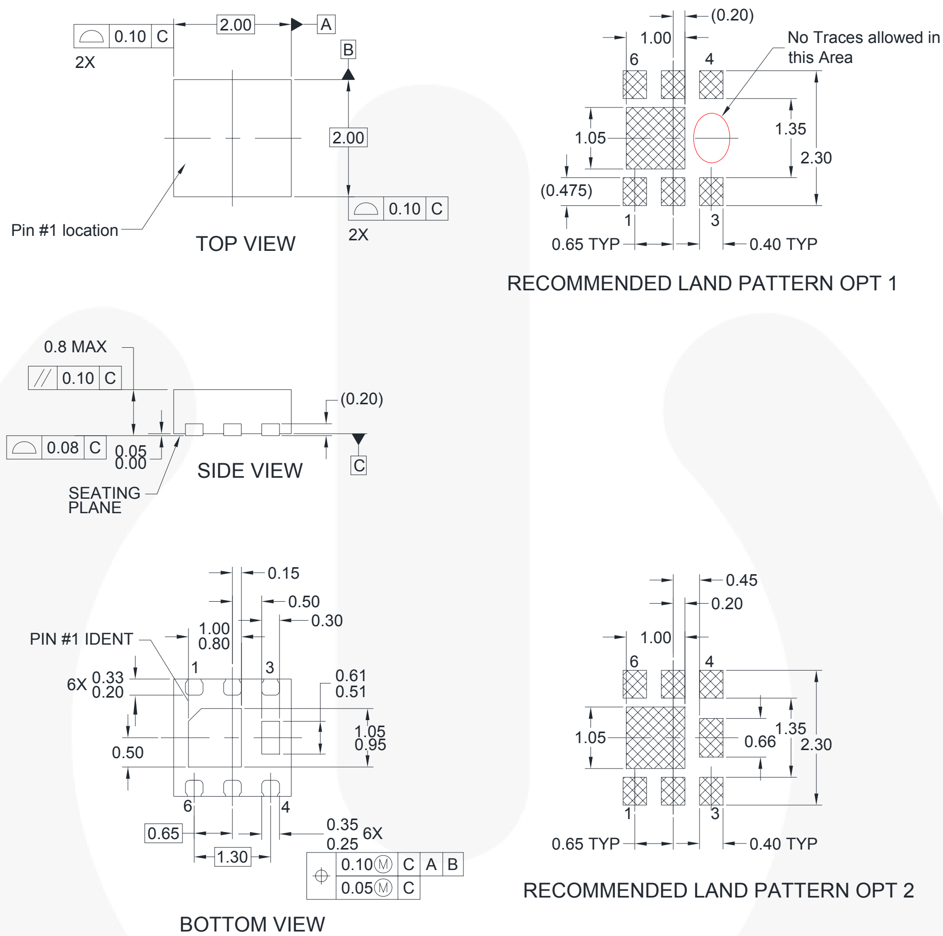
In the event of a negative transient, or when the DC power source is reversely connected to the circuit, the device blocks the flow of current and holds off the voltage, thereby protecting the USB device. Figure 18 shows the voltage and current waveforms when a virtual USB3.0 device is reversely biased; the output voltage is near 0 and response time is less than 50ns.

Figure 19 shows the voltage and current waveforms when no reverse bias protection is implemented. In Figure 17, while the reverse bias protector is present, the input voltage, V_{IN}, and the output voltage, V_O, are separated and look different. When this reverse bias protector is removed, V_{IN} and V_O merge, as shown in Figure 19 as V_{IN}. This V_{IN} is also the voltage applied to the load circuit. It can be seen that, with reverse bias protection, the voltage applied to the load and the current flowing into the load look very much the same as without reverse bias protection.

Benefits of Reverse Bias Protection

The most important benefit is to prevent accidently reverse-biased voltage from damaging the USB load. Another benefit is that, the peak startup inrush current can be reduced. How fast the input voltage rises, the input/output capacitance, the input voltage, and how heavy the load is determine how much the inrush current can be reduced. In a 5V USB application, for example, the inrush current can be 5% - 20% less with different input voltage rising rate and other factors. This can offer a system designer the option of increasing C_2 while keeping "effective" USB device capacitance down.

Physical Dimensions



NOTES:

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MO-229 DATED AUG/2003
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994
D. DRAWING FILENAME: MKT-MLP06Lrev3.

Figure 20. 6-Lead, Molded Leadless Package (MLP), Dual, Non-JEDEC, 2mm Square, Single-Tied DAP

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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