

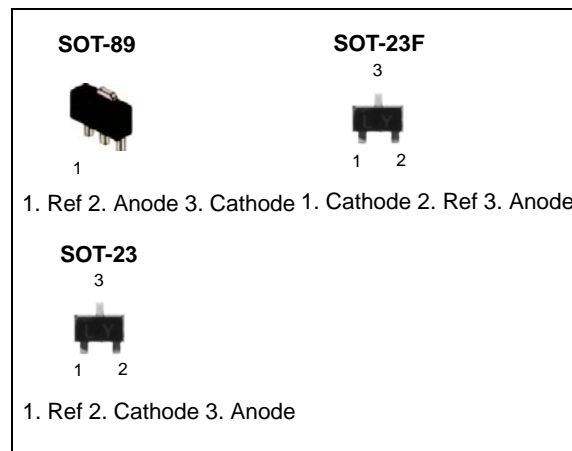
LM431SA/LM431SB/LM431SC Programmable Shunt Regulator

Features

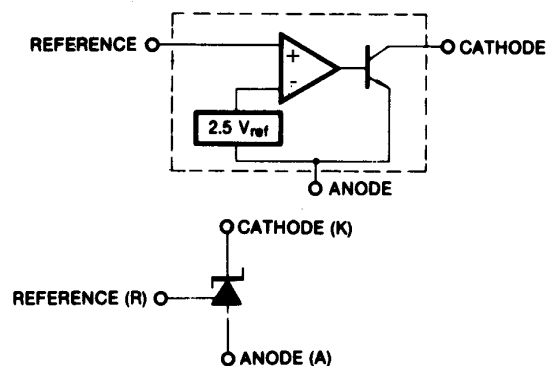
- Programmable Output Voltage to 36 Volts
- Low Dynamic Output Impedance 0.2Ω Typical
- Sink Current Capability of 1.0 to 100mA
- Equivalent Full-Range Temperature Coefficient of 50ppm/°C Typical
- Temperature Compensated for Operation Over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- Fast Turn-on Response

Description

The LM431SA/LM431SB/LM431SC are three terminal output adjustable regulators with thermal stability over operating temperature range. The output voltage can be set any value between V_{REF} (approximately 2.5 volts) and 36 volts with two external resistors. These devices have a typical dynamic output impedance of 0.2Ω. Active output circuit provides a sharp turn-on characteristic, making these devices excellent replacement for Zener Diodes in many applications.



Internal Block Diagram



Absolute Maximum Ratings

(Operating temperature range applies unless otherwise specified.)

Parameter	Symbol	Value	Unit
Cathode Voltage	V_{KA}	37	V
Cathode current Range (Continuous)	I_{KA}	-100 ~ +150	mA
Reference Input Current Range	I_{REF}	-0.05 ~ +10	mA
Thermal Resistance Junction-Air (Note1,2)	$R_{\theta JA}$	220	°C/W
ML Suffix Package (SOT-89)		350	
MF Suffix Package (SOT-23F)		400	
Power Dissipation (Note3,4)	P_D	560	mW
ML Suffix Package (SOT-89)		350	
MF Suffix Package (SOT-23F)		310	
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_{OPR}	-25 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note:

- Thermal resistance test board
Size: 76.2mm * 114.3mm * 1.6mm (1S0P)
JEDEC Standard: JESD51-3, JESD51-7
- Assume no ambient airflow.
- $T_{JMAX} = 150^{\circ}\text{C}$, Ratings apply to ambient temperature at 25°C
- Power dissipation calculation: $P_D = (T_J - T_A)/R_{\theta JA}$

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Cathode Voltage	V_{KA}	V_{REF}	-	36	V
Cathode Current	I_{KA}	1.0	-	100	mA

Electrical Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Conditions	LM431SA			LM431SB			LM431SC			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Reference Input Voltage	V_{REF}	$V_{KA}=V_{REF}$, $I_{KA}=10\text{mA}$	2.450	2.500	2.550	2.470	2.495	2.520	2.482	2.495	2.508	V	
Deviation of Reference Input Voltage Over-Temperature	$\Delta V_{REF}/\Delta T$	$V_{KA}=V_{REF}$, $I_{KA}=10\text{mA}$ $T_{MIN} \leq T_A \leq T_{MAX}$	SOT-89 SOT-23F	-	4.5	17	-	4.5	17	-	4.5	17	mV
			SOT-23	-	6.6	24	-	6.6	24	-	6.6	24	mV
Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	$I_{KA} = 10\text{mA}$	$\Delta V_{KA}=10\text{V}$ $-V_{REF}$	-	-1.0	-2.7	-	-1.0	-2.7	-	-1.0	-2.7	mV/V
			$\Delta V_{KA}=36\text{V}$ -10V	-	-0.5	-2.0	-	-0.5	-2.0	-	-0.5	-2.0	
Reference Input Current	I_{REF}	$I_{KA}=10\text{mA}$, $R_1=10\text{K}\Omega$, $R_2=\infty$	-	1.5	4	-	1.5	4	-	1.5	4	μA	
Deviation of Reference Input Current Over Full Temperature Range	$\Delta I_{REF}/\Delta T$	$I_{KA}=10\text{mA}$, $R_1=10\text{K}\Omega$, $R_2=\infty$, $T_A = \text{Full Range}$	SOT-89 SOT-23F	-	0.4	1.2	-	0.4	1.2	-	0.4	1.2	μA
			SOT-23	-	0.8	2.0	-	0.8	2.0	-	0.8	2.0	μA
Minimum Cathode Current for Regulation	$I_{KA(MIN)}$	$V_{KA}=V_{REF}$	-	0.45	1.0	-	0.45	1.0	-	0.45	1.0	mA	
Off -Stage Cathode Current	$I_{KA(OFF)}$	$V_{KA}=36\text{V}$, $V_{REF}=0$	-	0.05	1.0	-	0.05	1.0	-	0.05	1.0	μA	
Dynamic Impedance	Z_{KA}	$V_{KA}=V_{REF}$, $I_{KA}=1$ to 100mA , $f \geq 1.0\text{kHz}$	-	0.15	0.5	-	0.15	0.5	-	0.15	0.5	Ω	

Note1

$T_{MIN} = -25^\circ\text{C}$, $T_{MAX} = +85^\circ\text{C}$

Test Circuits

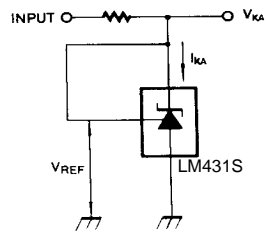


Figure 1. Test Circuit for $V_{KA} = V_{REF}$

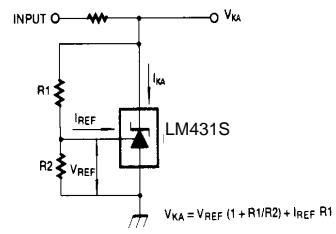


Figure 2. Test Circuit for $V_{KA} \geq V_{REF}$

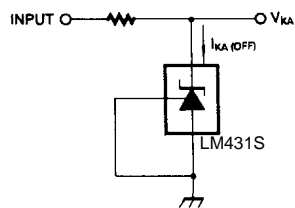


Figure 3. Test Circuit for $I_{KA(OFF)}$

Typical Performance Characteristics

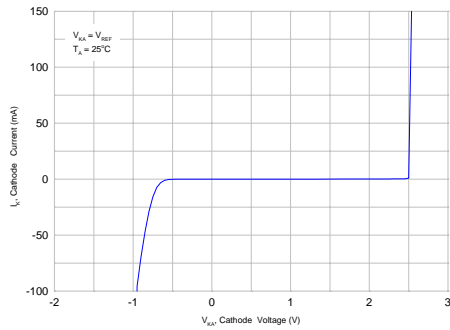


Figure 4. Cathode Current vs. Cathode Voltage

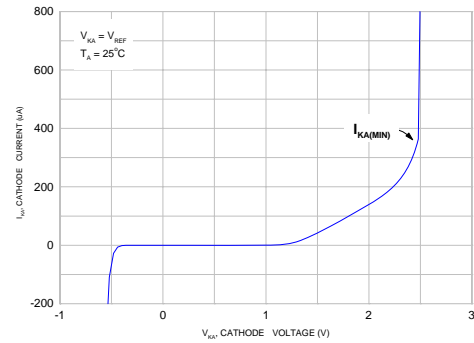


Figure 5. Cathode Current vs. Cathode Voltage

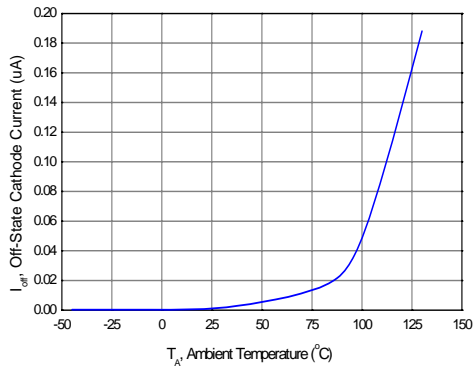


Figure 6. OFF-State Cathode Current vs. Ambient Temperature

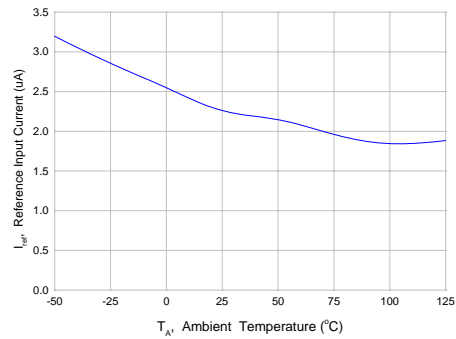


Figure 7. Reference Input Current vs. Ambient Temperature

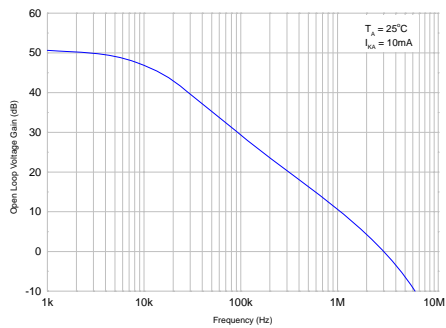


Figure 8. Small Signal Voltage Amplification vs. Frequency

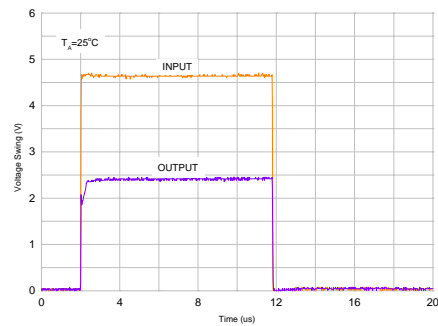


Figure 9. Pulse Response

Typical Performance Characteristics (Continued)

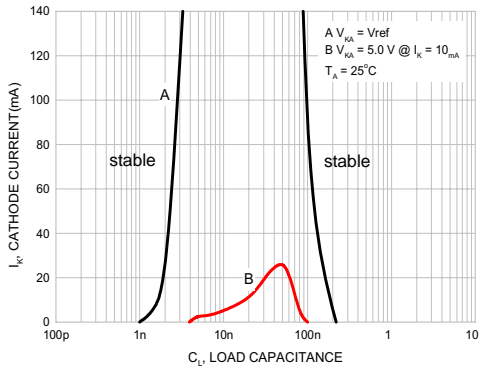


Figure 10. Stability Boundary Conditions

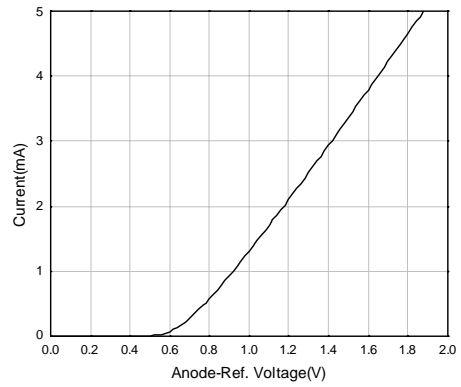


Figure 11. Anode-Reference Diode Curve

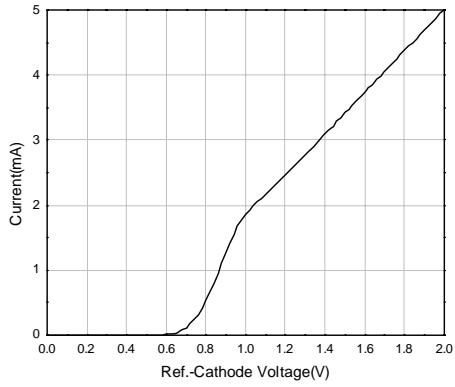


Figure 12. Reference-Cathode Diode Curve

Typical Application

$$V_O = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

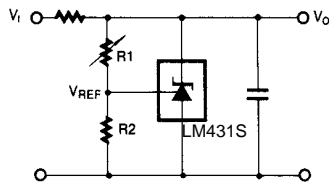


Figure 13. Shunt Regulator

$$V_O = V_{ref} \left(1 + \frac{R_1}{R_2}\right)$$

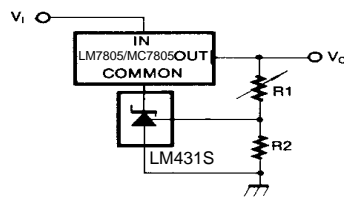


Figure 14. Output Control for Three-Terminal Fixed Regulator

$$V_O = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

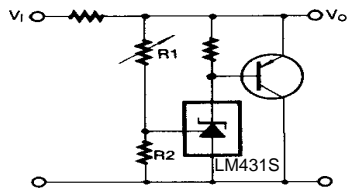


Figure 15. High Current Shunt Regulator

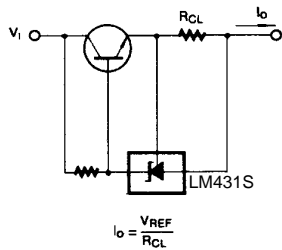


Figure 16. Current Limit or Current Source

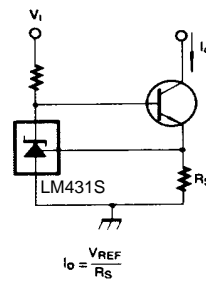


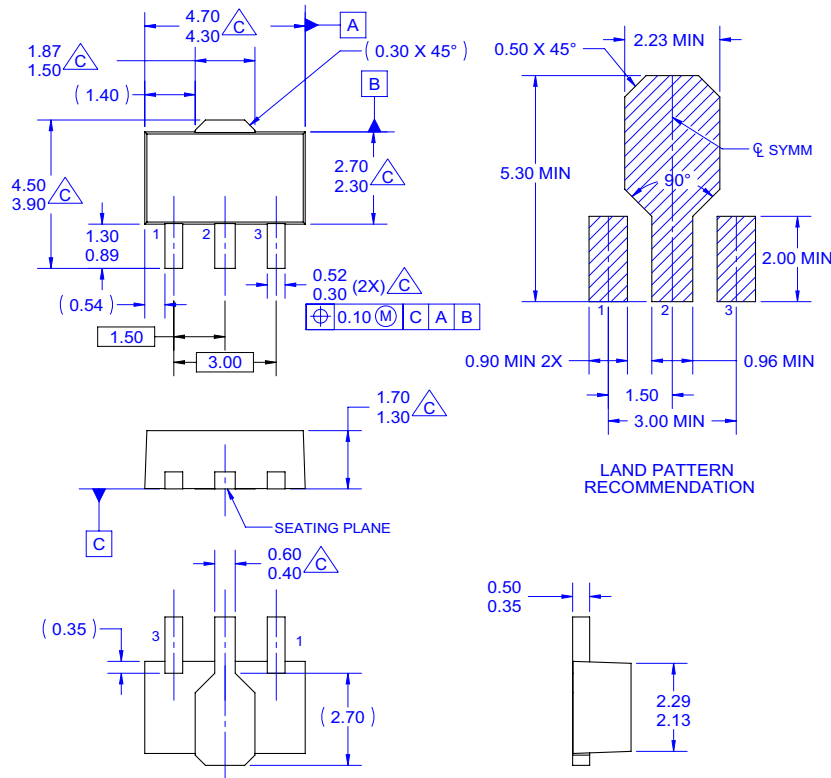
Figure 17. Constant-Current Sink

Mechanical Dimensions

Package

Dimensions in millimeters

SOT-89



NOTES: UNLESS OTHERWISE SPECIFIED.

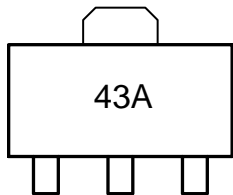
A. REFERENCE TO JEDEC TO-243 VARIATION AA.
B. ALL DIMENSIONS ARE IN MILLIMETERS.

$\triangle C$ DOES NOT COMPLY JEDEC STANDARD VALUE.

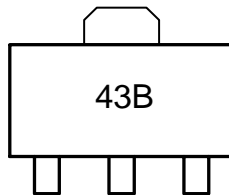
D. DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR PROTRUSION.
E. DIMENSION AND TOLERANCE AS PER ASME
Y14.5-1994.

F. DRAWING FILE NAME: MA03CREV2

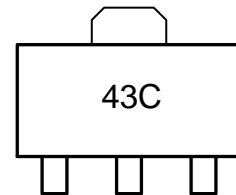
Marking



2% tolerance



1% tolerance



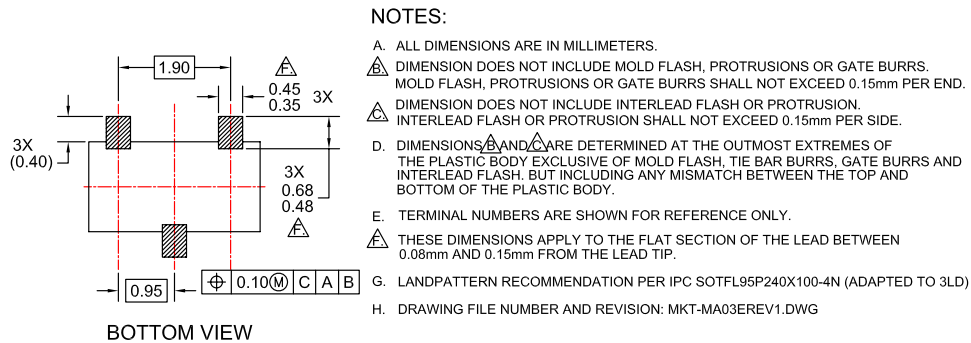
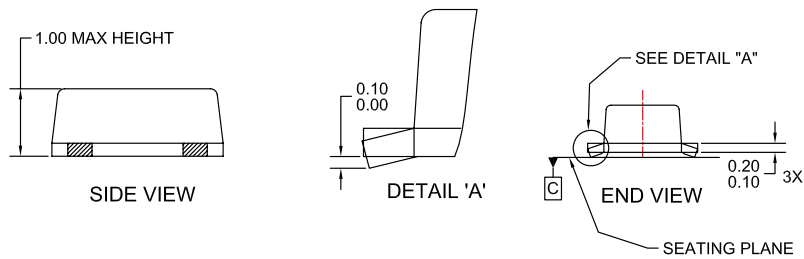
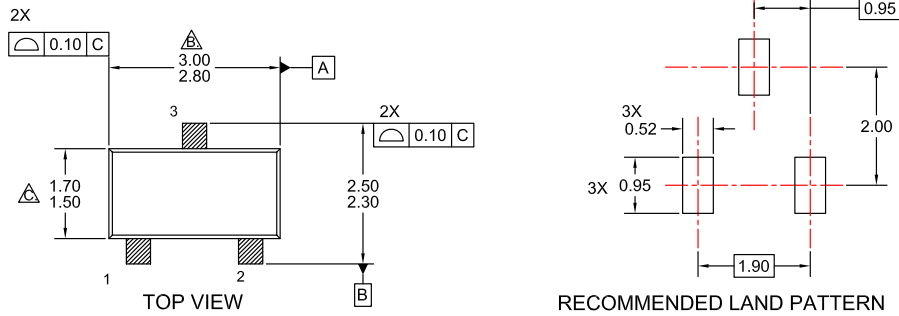
0.5% tolerance

Mechanical Dimensions (Continued)

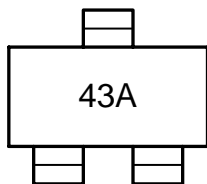
Package

Dimensions in millimeters

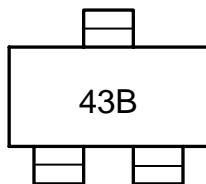
SOT-23F



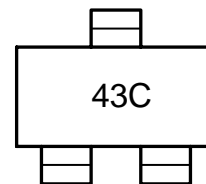
Marking



2% tolerance



1% tolerance



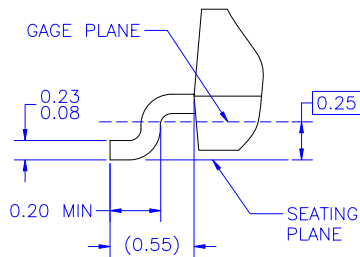
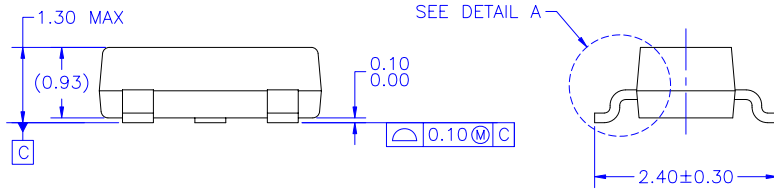
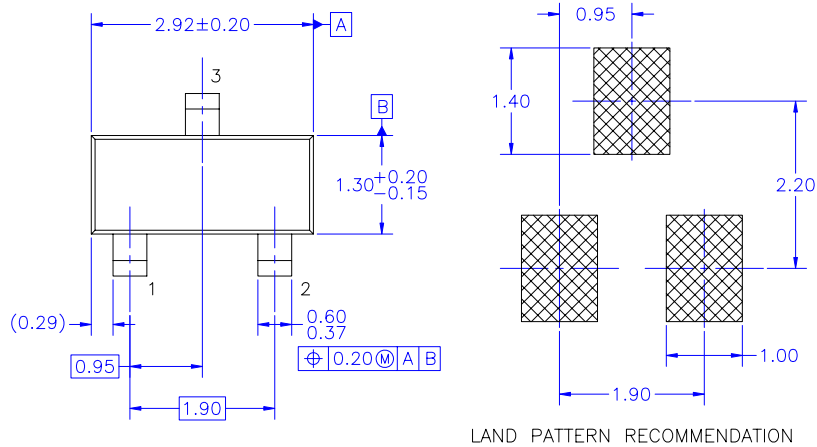
0.5% tolerance

Mechanical Dimensions (Continued)

Package

Dimensions in millimeters

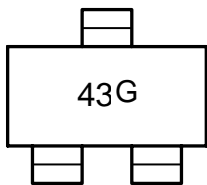
SOT-23



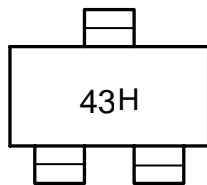
NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
- E) DRAWING FILE NAME: MA03DREV9

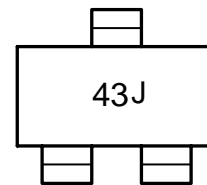
Marking



2% tolerance



1% tolerance



0.5% tolerance

Ordering Information



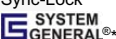
Product Number	Output Voltage Tolerance	Operating Temperature	Package	Packing Method
LM431SCCMLX	0.5%	-25 ~ +85°C	SOT-89	Tape and Reel
LM431SCCMFX			SOT-23F	
LM431SCCM32X			SOT-23	
LM431SBCMLX	1%		SOT-89	
LM431SBCMFX			SOT-23F	
LM431SBCM32X			SOT-23	
LM431SACMLX	2%		SOT-89	
LM431SACMFX			SOT-23F	
LM431SACM32X			SOT-23	

Note : X suffix means " Tape and Reel " packing.



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| FastvCore™ | OptoHiT™ |  SYSTEM GENERAL®* | XS™ |
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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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