

December 2011

# FAN5903 Buck Converter with Bypass Mode for 3G/3.5G/4G PAs

#### **Features**

- 2.7V to 5.5V Input Voltage Range
- V<sub>OUT</sub> Range from 0.4V to 3.50V (or V<sub>IN</sub>)
- Small Form Factor Inductor
  - o 2012 470nH or 540nH for Minimal PCB Area
  - o 2020 1.0µH for Higher Efficiency
- Bypass Dropout at 500mA, 60mV Typical
- 100% Duty Cycle for Low Dropout Operation
- Input Under-Voltage Lockout / Thermal Shutdown
- 1.34mm x 1.29mm, 9-Bump, 0.4mm-Pitch WLCSP
- 3MHz / 6MHz Selectable Switching Frequency to Facilitate System Optimization
- High-Efficiency PFM Operation at Low Power
- Sleep Mode for Very Low IQ Operation
- Up to 96% Efficient Synchronous Operation at High-Power Conditions
- 10µs Output Voltage Step Response for Early Power Loop Settling

## **Applications**

- Dynamic Supply Bias for 3G/3.5G and 4G PAs
- Power Supply for WCDMA/LTE PAs

#### Resources

For more information or a full copy of this datasheet, please contact a Fairchild representative.

#### **Description**

FAN5903 is a high-efficiency, low-noise, synchronous, step-down, DC-DC converter designed for powering 3G/3.5G/4G RF Power Amplifiers (PAs) in handsets and other mobile applications.

The output voltage may be dynamically varied from 0.40V to 3.50V, proportional to an analog input  $V_{\rm CON}$ , ranging from 0.16V to 1.40V provided by an external DAC. This allows the PA to be supplied with the voltage that enables maximum power-added efficiency.

An integrated bypass FET automatically switches on when battery voltage drops close to the desired output voltage ( $V_{OUT}$ = $V_{BAT}$ -200mV). The DC-DC switches back to Synchronous Mode when the voltage dropout exceeds 375mV. The integrated bypass FET is also enabled when  $V_{CON}$  is nominally greater than to 1.5V.

The FAN5903 offers fast transition times, enabling changes to the output voltage in less than 10µs for power transitions. Moreover, a Current-Mode control loop with fast transient response ensures excellent line and load regulation.

Light-load efficiency is optimized by operating in PFM Mode for load currents typically less than 100mA.

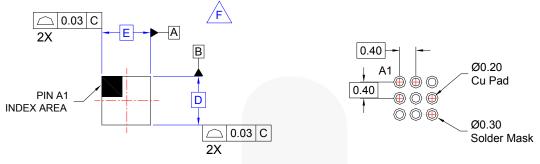
The switching frequency may be set to 3MHz or 6MHz, enabling further optimization of system performance. The FAN5903 typically uses a single, small-form-factor inductor of 540nH. Efficiency may be further optimized using a 1.0µH inductor when running at 3MHz.

When output regulation is not required, the FAN5903 may be placed in Sleep Mode by setting  $V_{\text{CON}}$  nominally to 100mV. This ensures a very low  $I_{\text{Q}}$  (<70µA) while enabling a fast return to output regulation. The FAN5903 enables significant current reduction and increased talk time and is available in a 1.34mm x 1.29mm, 9-bump, 0.40mm-pitch, WLCSP package.

## **Ordering Information**

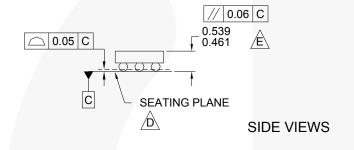
Part Number	Operating Temperature Range	Package	Packing Method
FAN5903UCX	-40 to +85°C	1.34mm x 1.29mm, 9-bump, 0.4mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)	Tape and Reel

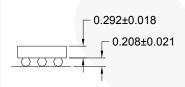
## **Physical Dimensions**

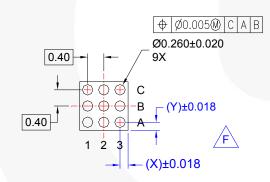


#### **TOP VIEW**

## LAND PATTERN RECOMMENDATION (NSMD PAD TYPE)







**BOTTOM VIEW** 

#### NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
  - G. DRAWING FILNAME: MKT-UC009AErev1

Product	D	E	X	Y	Unit
FAN5903UCX	1.292 ± 0.030	1.342 ± 0.030	0.271	0.246	mm

Figure 42. 1.34 x 1.29mm, 9-Bump, 0.4mm-Pitch WLCSP

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