

### March 2010

# FAN6210 Primary-Side Synchronous Rectifier (SR) Trigger Controller for Dual Forward Converter

### Features

- Primary-Side Trigger Controller for Dual Forward Converters with Synchronous Rectifier (SR)
- Specialized SR Controller for Dual Forward Converter
- Programmable Turn-on Delay Time for the Powering SR (RDLY Pin)
- Winding Voltage Detection for Precision Control at Light-Load Condition (DET Pin)
- Green-Mode Operation to Improve Light-Load Efficiency
- Differential Mode Control Signal with Better Noise Immunity
- V<sub>DD</sub> Over-Voltage Protection (OVP)

## Applications

- Personal Computer (PC) Power Supply
- Entry-Level Server Power Supply

## Description

FAN6210 is a primary-side SR trigger Integrated Circuit (IC) specially designed for the synchronous rectifier (SR) in dual forward converters employing FAN6206. FAN6210 provides drive signal for the primary-side power switches by using an output signal from PWM controller. FAN6210 can be combined with any PWM controller that can drive a dual-forward converter. To obtain optimal timing for the SR drive signals, transformer winding voltage is also monitored. To improve light-load efficiency, green mode operation is employed, which disables the SR turn-on trigger signal, minimizing gate drive power consumption at light load.

FAN6210 is available in 8-pin SOP package.

### **Ordering Information**





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## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage		30	V
V <sub>SIN</sub>	Logic Input Voltage		30	V
V <sub>SOUT</sub>	Low Side Output Voltage		18	V
V <sub>H</sub>	XP, XN		30	V
VL	DET, RDLY		7	V
PD	Power Dissipation $T_A < 50^{\circ}C$		400	mW
heta ja	Thermal Dissipation (Junction-to-Air)		150	°C/W
TJ	Operating Junction Temperature	-40	+125	°C
T <sub>STG</sub>	Storage Temperature Range	-55	+150	°C
TL	Lead Temperature (Soldering) 10 Seconds		260	°C
ESD	Human Body Model, JEDEC:JESD22-A114		4.0	KV
	Charged Device Model, JEDEC:JESD22-C101		1.5	KV

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

2. All voltage values, except differential voltages, are given with respect to GND pin.

## **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T <sub>A</sub>	Operating Ambient Temperature	-40	+105	°C

## **Electrical Characteristics**

 $V_{DD}$ =20V,  $T_A$ =25°C, unless otherwise specified.

Symbol	Parameter Conditions			Тур.	Max.	Units
VDD Section		1	1	1	1	I
V <sub>DD</sub>	DC Supply Voltage		7		24	V
V <sub>DD-ON</sub>	Turn-On Threshold Voltage			10	11	V
V <sub>TH-OFF</sub>	Turn-Off Threshold Voltage		7	8	9	V
V <sub>DD-OVP</sub>	V <sub>DD</sub> Over-Voltage Protection (OVP)		23.0	25.5	28.0	V
V <sub>DD-OVP-HYS</sub>	Hysteresis voltage for V <sub>DD</sub> OVP		0.3	0.8	1.3	V
t <sub>OVP</sub>	V <sub>DD</sub> OVP Debounce Time			250		μs
SIN Section						
V <sub>SIN</sub>	Logic Input Voltage		10.5		24.5	V
t <sub>DLY_OUTH</sub>	Delay Time Between SIN-HIGH and SOUT-HIGH		240	300	350	ns
t <sub>DLY_OUTL</sub>	Delay Time Between SIN-LOW and SOUT-LOW		75	100	150	ns
t <sub>on_max</sub>	SOUT Maximum On Time and Stop XP Pulse		8.5	10.0	12.0	μs
<b>DET Section</b>						
V <sub>DET H</sub>	Detect Input Voltage to Send XP After SOUT Fall	ing	2.5	3.0	3.5	V
V <sub>DET_L</sub>	Voltage to Drive XP Signal After SOUT Falling		1.5	2.0	2.5	V
t <sub>PD DET</sub>	Delay Time to Send XP		30	50	100	ns
XP XN Section	on					
t <sub>PLS_XN</sub>	High-Level Pulsewidth of XN Signal		250	300	350	ns
t <sub>PLS_XP</sub>	High-Level Pulsewidth of XP Signal		600	700	800	ns
t <sub>PD_XN</sub>	Delay Time to Trigger XN by SIN Rising or Falling Edge			50	75	ns
D <sub>PLS_OFF</sub>	SIN Duty Ratio Shorter than DPLS_OFF Stop XP Pu	lse		10		%
V <sub>XN</sub>	XN Signal Output Voltage Level				8.0	V
Vxp	XP Signal Output Voltage Level		5.5		8.0	V
t <sub>R_XP</sub>	XP Rising Time	$V_{DD}$ = 15V; $C_{L}$ = 100pF; SOUT= 1V to 6V			30	ns
t <sub>F_XP</sub>	XP Falling Time $V_{DD} = 15V;$ $C_L = 100pF;$ SOUT= 7V to 2V				30	ns
<b>RDLY Sectio</b>	n					
V <sub>RDLY</sub>	RDLY Voltage	$R_{RDLY}=24k\Omega$	1.08	1.20	1.32	V
t <sub>DLY_XP</sub>	Delay Time to Trigger XP by SOUT Rising Edge	R <sub>RDLY</sub> =24kΩ	280	340	400	ns
Vz	Output Voltage Maximum (Clamp)	V <sub>DD</sub> =25V			18.5	V
V <sub>OL</sub>	Output Voltage LOW	V <sub>DD</sub> =15V; I <sub>O</sub> = 50mA			1.5	V
V <sub>OH</sub>	Output Voltage HIGH	V <sub>DD</sub> =15V; I <sub>O</sub> = 50mA	10			V
t <sub>R</sub>	SOUT Rising Time	$V_{DD}$ = 15V; $C_L$ = 5nF; SOUT= 2V to 9V	30	70	120	ns
t <sub>F</sub>	SOUT Falling Time	$V_{DD} = 15V; C_L = 5nF;$ SOUT= 9V to 2V	30	50	100	ns

## **Typical Performance Characteristics**

These characteristic graphs are normalized at  $T_A = 25^{\circ}C$ .



Figure 5. Turn-On Threshold Voltage



Figure 7. Delay Time Between SIN-HIGH and SOUT-HIGH



Figure 9. High-Level Pulsewidth of XN Signal



Falling Edge



Figure 6. Turn-Off Threshold Voltage



Figure 8. Delay Time Between SIN-LOW and SOUT-LOW



Figure 10. High-Level Pulsewidth of XP Signal



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### **Function Description**

Figure 13 and Figure 14 show the simplified circuit diagram of dual-forward converter and its key waveforms. Switches Q1 and Q2 are turned on and off together. Once Q<sub>1</sub> and Q<sub>2</sub> are turned on, input voltage is applied across the transformer primary side and power is delivered to the secondary side through the transformer, powering diode D1. During this time, the magnetizing current linearly increases. When Q1 and Q2 are turned off, the magnetizing current of the transformer forces the reset diodes ( $D_{R1}$  and  $D_{R2}$ ) and negative input voltage is applied across the transformer primary side. During this time, magnetizing current linearly decreases to zero and the secondary-side inductor current freewheels through diode D2. When synchronous rectifiers SR1 and SR2 are used instead of diodes D<sub>1</sub> and D<sub>2</sub>, it is important to have proper timing between drive signals for SR<sub>1</sub> and SR<sub>2</sub>.





Figure 15 shows the typical application circuit of FAN6210. SIN is the gate drive output of the PWM controller. SOUT is obtained from SIN by adding a delay, which is used to drive two switches  $Q_1$  and  $Q_2$ .

The value of the DET resistor is recommended as  $10k\Omega$  and  $D_B$  is used to block high voltage on winding. The breakdown voltage of Zener diode  $D_Z$  is typically 5~6V to protect the DET pin from over voltage.



Figure 15. Typical Application Circuit

Figure 16 shows the timing diagrams for heavy-load and light-load conditions.

The switching operation of the secondary SR MOSFETs is determined by the SN and SP signals. FAN6206 turns on SR MOSFETs at the rising edge of the XP signal, while it turns off SR MOSFETs at the rising edge of XN. Within one switching cycle, XP and XN are obtained two times, respectively.

The XN signal has a 300ns pulse-width and is triggered by the rising edge and falling edge of the SIN signal after a short time delay  $(t_{PD_XN})$ .

XP signal has a 700ns pulse-width and is triggered by the rising edge of the SOUT signal after an adjustable time delay ( $t_{DLY_XP}$ ) and by the falling edge of the DET signal. The relation between the delay resistor ( $R_{DELAY}$ ) and the delay time is shown in Figure 17. The triggering of the XP signal by DET is prohibited while the XN signal is HIGH. Therefore, the XP signal is not triggered at the falling edge of the DET signal and is delayed until the XN signal drops to zero at heavy-load condition. At light-load condition, the DET falling edge comes after the XN signal drops to zero and the XP signal is triggered at the falling edge of the DET signal after a short time delay ( $t_{PD DET}$ ).









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