Sup*IR*Buck™

USER GUIDE FOR iP1837 EVALUATION BOARD

DESCRIPTION

The iP1837 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 7.7mm X 7.7 mm LGA package.

Key features offered by the iP1837 include programmable soft-start ramp, precision 0.6V reference voltage, Power Good, thermal protection, overvoltage protection, programmable switching frequency, Enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the iP1837 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for iP1837 is available in the iP1837 data sheet.

BOARD FEATURES

- V_{in} = +12V (+ 13.2V Max)
- Vcc=+3.3V (3.46V Max)
- V_{out} = +1.8V @ 0- 35A
- F_s=600kHz
- L= 0.215uH
- C_{in}= 7x22uF (ceramic 1206) + 1X330uF (electrolytic)
- C_{out}=15x22uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 35A load should be connected to VOUT+ and VOUT-. The inputs and outputs of the board are listed in Table I.

iP1837 has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 3.13V-3.46V supply and it would be connected to Vcc+ and Vcc-.

External Enable signal can be applied to the board via exposed Enable pad and *R18 should be removed for this purpose, For proper operation of iP1837, the voltage at Enable should always be kept below Vcc.*

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Vcc input
Vcc-	Ground for Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out} (+1.8V)
Enable	Enable
P_Good	Power Good Signal

LAYOUT

The PCB is a 6-layer board. All of layers are 2 Oz. copper. The iP1837 and most of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors and feedback components are located close to iP1837. The feedback resistors are connected to the output of the remote sense amplifier of the iP1837 and are located close to the iP1837. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path. Separate power ground and analog ground are used and may be connected together using a 0 ohm resistor at one of two possible locations

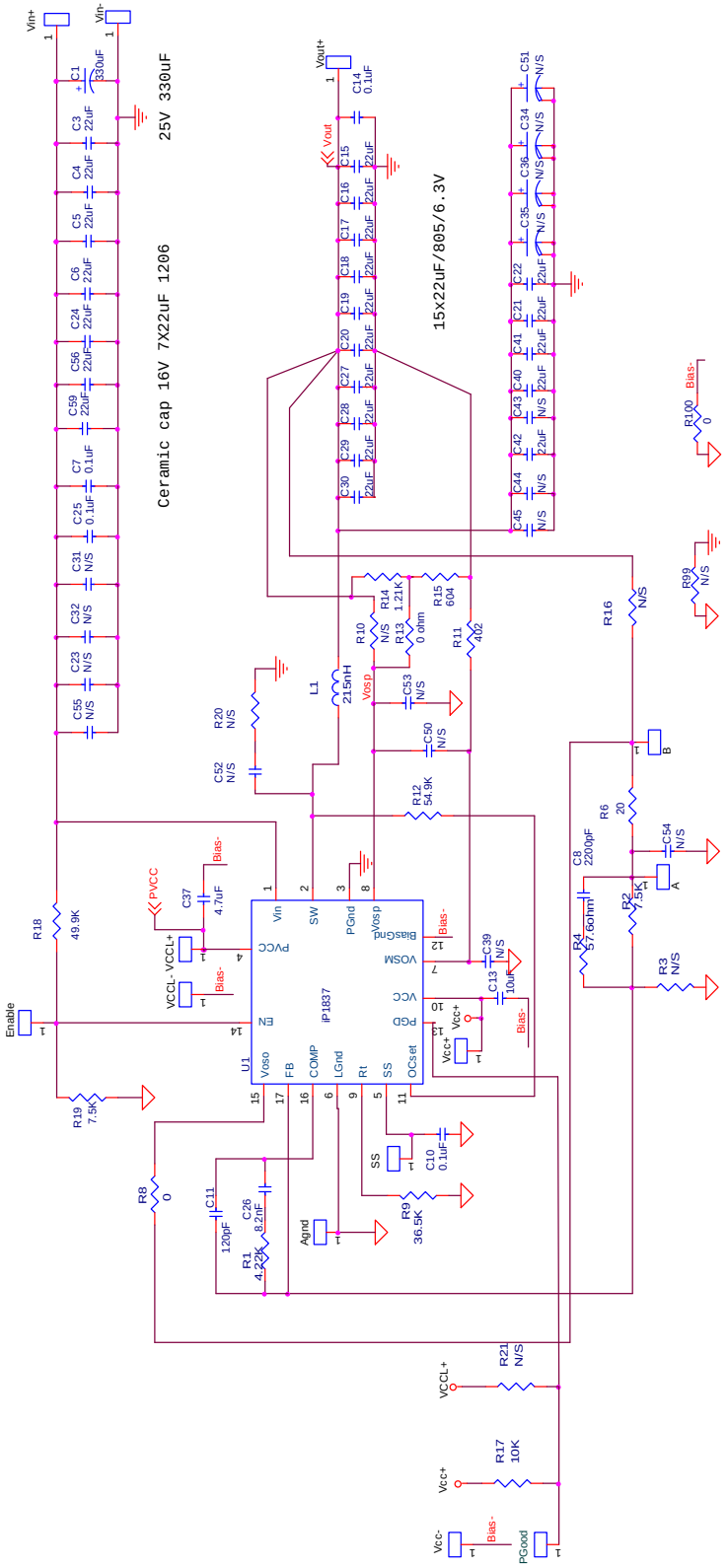


Fig. 1: Schematic of the iP1837 evaluation board

Bill of Materials

Item	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	7	C3 C4 C5 C6 C24 C56 C59	22uF	22uF,1206,16V, X5R, 20%	TDK	C3216X5R1C226M
2	1	C1	330uF	SMD Elecrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
3	4	C7 C14 C25 C10	0.1uF	0603, 25V, X7R, 10%	Panasonic	ECJ-1VB1E104K
4	1	C8	2200pF	2200pF,0603,50V,X7R	Panasonic	ECJ-1VB1H222K
5	1	C11	120pF	50V, 0603, NP0, 5%	Murata	GRM1885C1H121JA01D
6	15	C15 C16 C17 C18 C19 C20 C21 C22 C27 C28 C29 C30 C40 C41 C42	22uF	0805, 6.3V, X5R, 20%	Panasonic	ECJ-2FB0J226M
7	1	C37	4.7uF	0805, 10V, X5R	TDK	C2012X5R1A475K
8	1	C26	8200pF	0603, 50V, X7R, 10%	Panasonic	ECJ-1VB1H822K
9	1	L1	0.215uH	0.215uH, DCR=0.29mohm	Cyntec	PCDC1008-R215EMO
10	1	R1	4.22K	0603,1/10W,1%	Rohm	MCR03EZPFX4221
11	1	R2	7.5k	0603,1/10W,1%	Rohm	MCR03EZPFX7501
12	1	R4	57.6	0603,1/10W,1%	Vishay/Dale	CRCW060357R6FKEA
13	1	R6	20	20,0603,1/10 W,1%	Vishay/Dale	CRCW060320R0FKEA
14	1	R9	36.5K	0603,1/10W,1%	Rohm	MCR03EZPFX3652
15	3	R8 R100 R13	0	0,0603,1/10 W,5%	Vishay/Dale	CRCW06030000Z0EA
16	1	C13	10uF	0603, X5R, 6.3V	TDK	C1608X5R0J106M
17	1	R12	54.9K	0603,1/10 W,1%	Rohm	MCR03EZPFX5492
18	1	R14	1.21K	0603,1/10 W,1%	Rohm	MCR03EZPFX1211
19	1	R15	604	0603,1/10 W,1%	Rohm	MCR03EZPFX6040
20	1	R11	402	0603,1/10 W,1%	Rohm	MCR03EZPFX4020
21	1	R18	49.9K	49.9K,0603,1/10 W,1%	Rohm	MCR03EZPFX4992
22	1	R19	7.5K	7.5K,0603,1/10W,1%	Rohm	MCR03EZPFX7501
23	1	R17	10K	0603,1/10 W,1%	Rohm	MCR03EZPFX1002
24	1	U1	iP1837	iP1837 7.7mmX7.7mm	International Rectifier	iP1837PbF

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A-35A, Room Temperature, no airflow

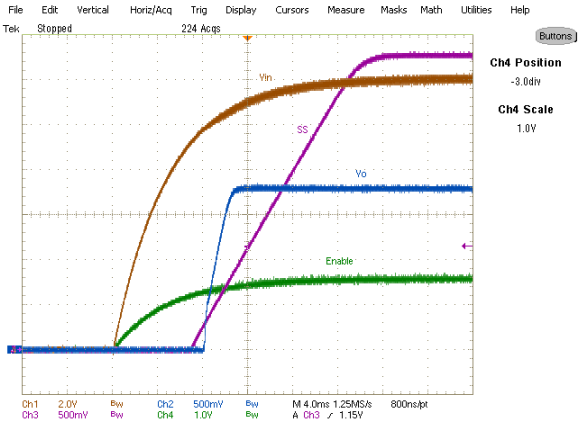


Fig. 2: Start up at 35A Load
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:Enable

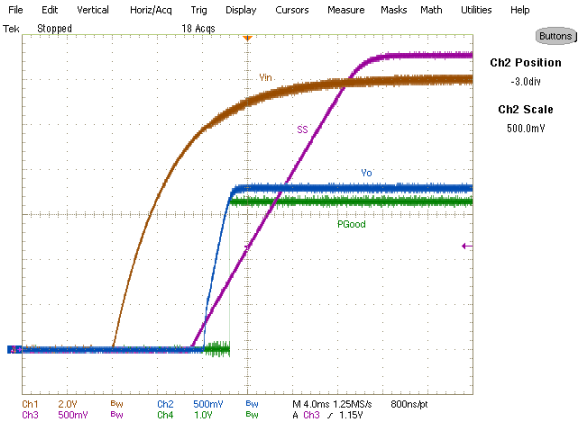


Fig. 3: Start up at 35A Load,
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:V_{PGood}

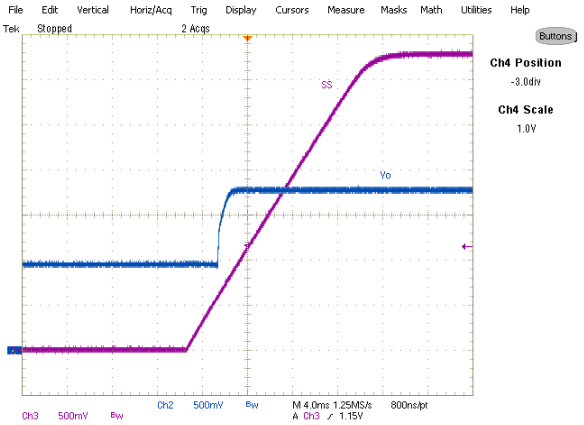


Fig. 4: Start up with 1V Pre Bias , 0A Load, Ch_2:V_o, Ch_3:V_{SS}

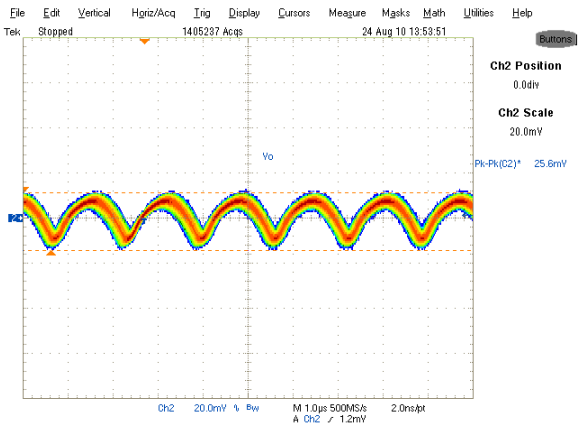


Fig. 5: Output Voltage Ripple, 35A load
Ch_2: V_{out}

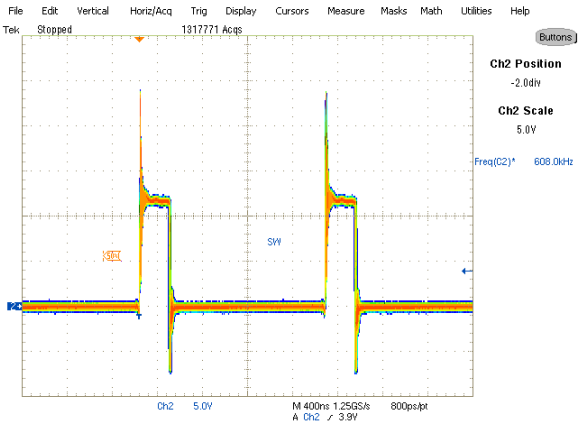


Fig. 6: Inductor node at 35A load
Ch_2:LX

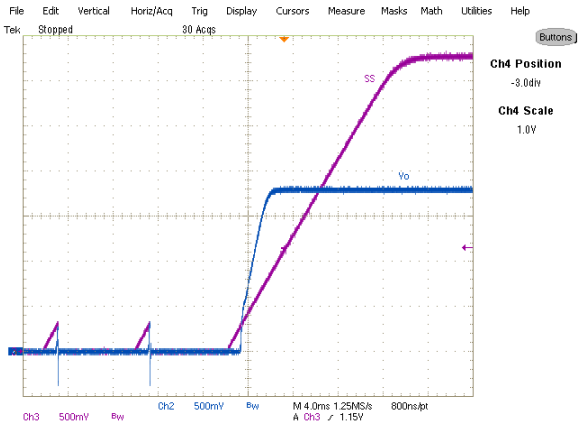


Fig. 7: Short (Hiccup) Recovery
Ch_2:V_{out} , Ch_3:V_{ss}

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=3.5A-14A, Room Temperature, no air flow

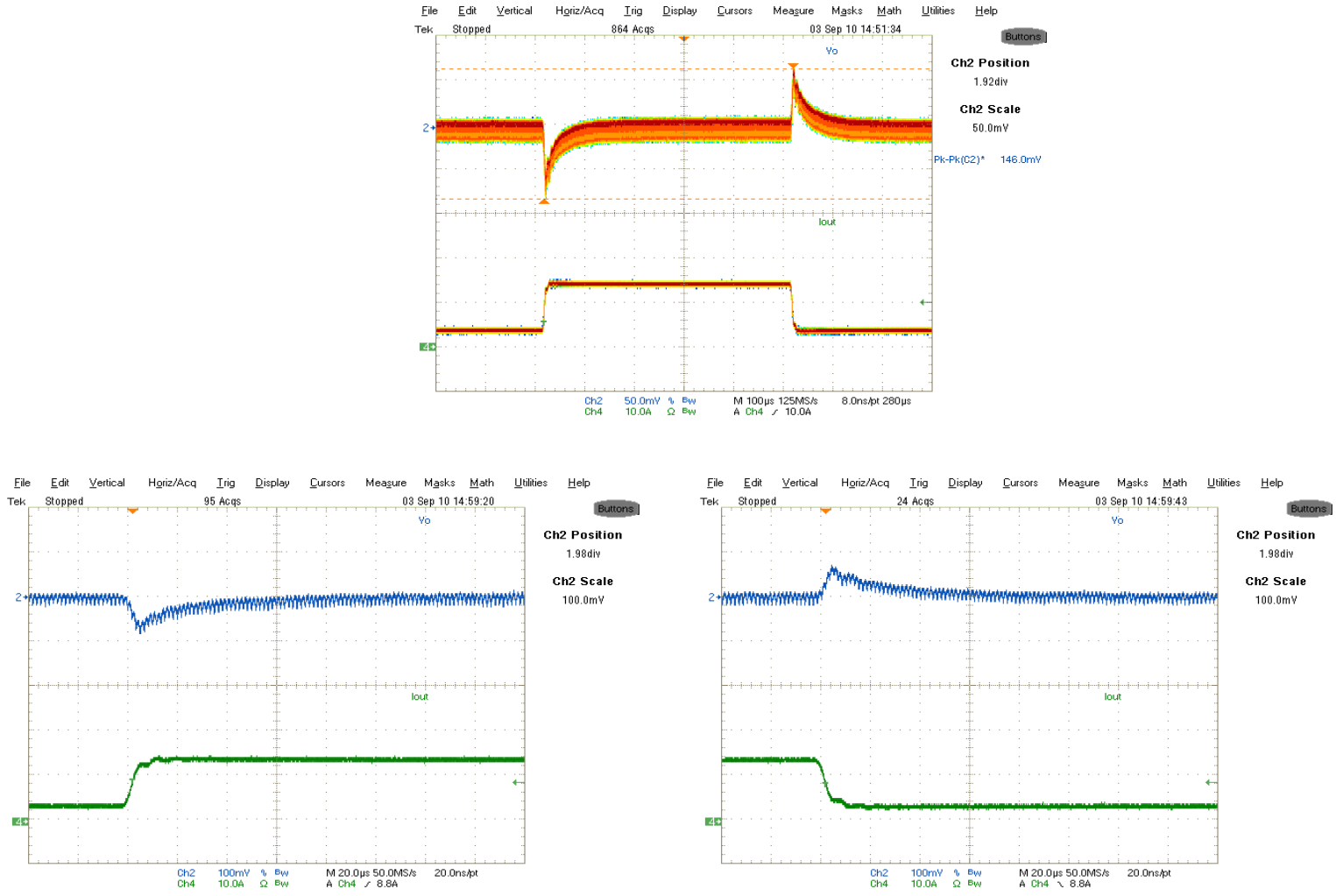


Fig. 8: Transient Response, 3.5A to 14A step (2.5A/us)
Ch_2:V_{out}

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=24.5A-35A, Room Temperature, no air flow

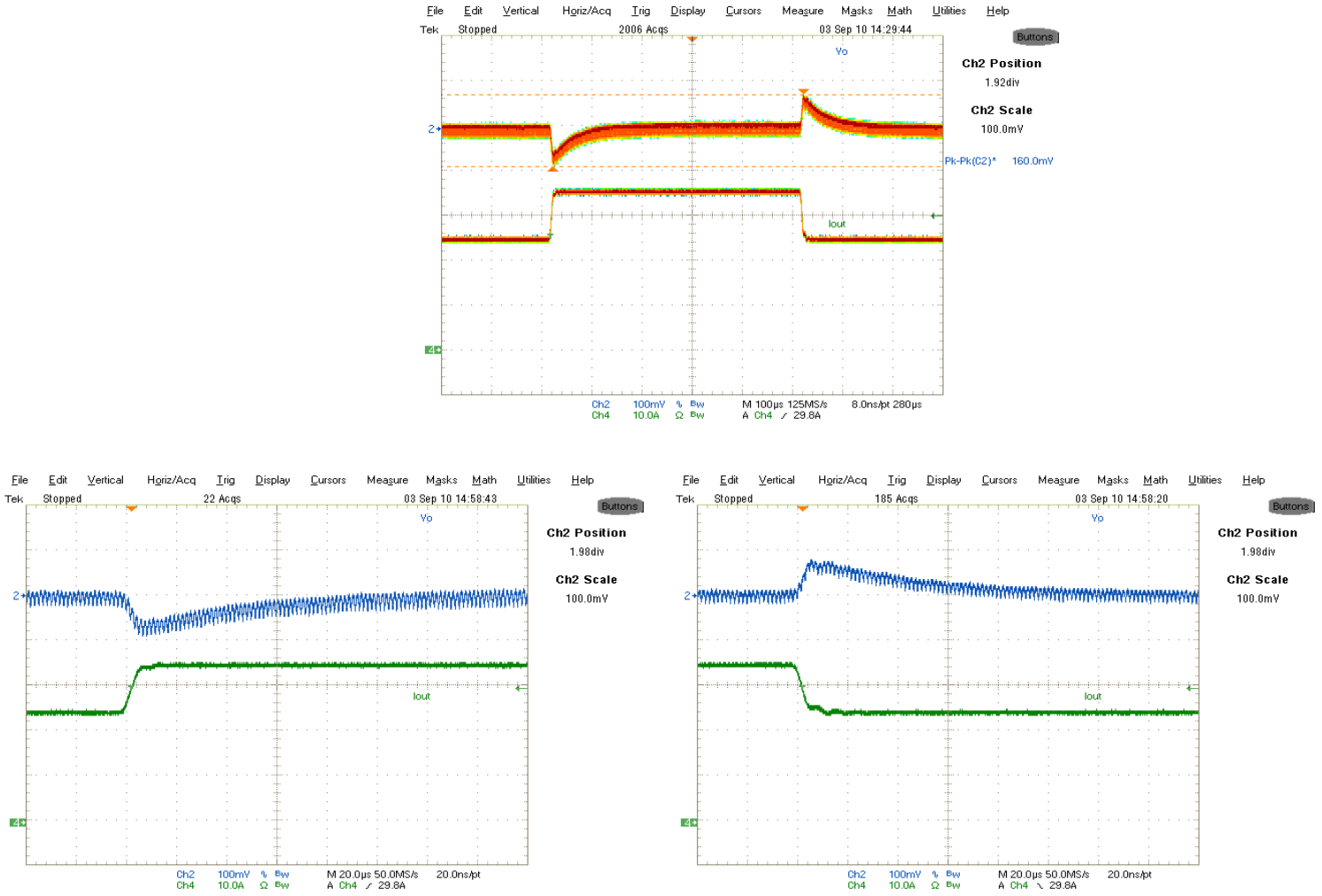


Fig. 9: Transient Response, 24.5A to 35A step (2.5A/us)

Ch_2:V_{out}

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A-35A, Room Temperature

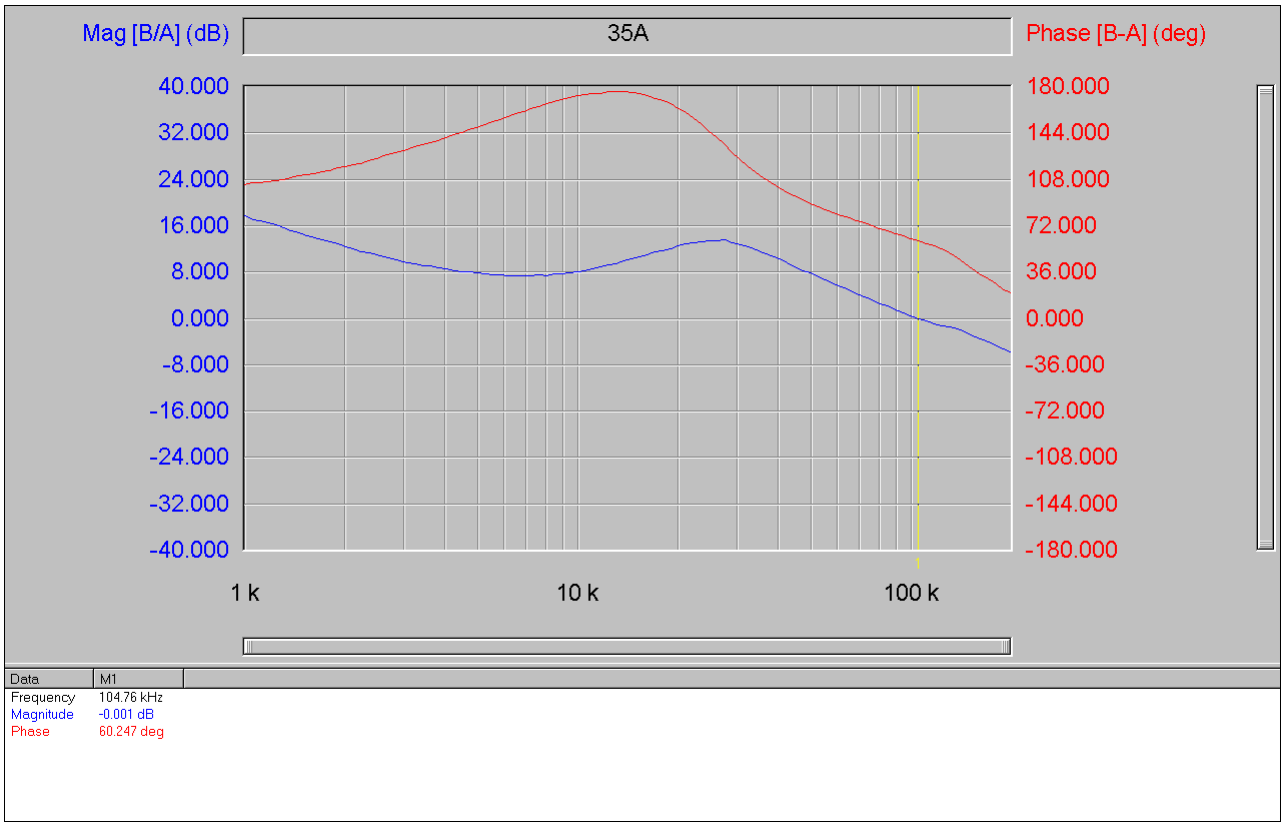


Fig. 10: Bode Plot at 35A load shows a bandwidth of 102.04kHz and phase margin of 56.20 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A-35A, Room Temperature, no air flow

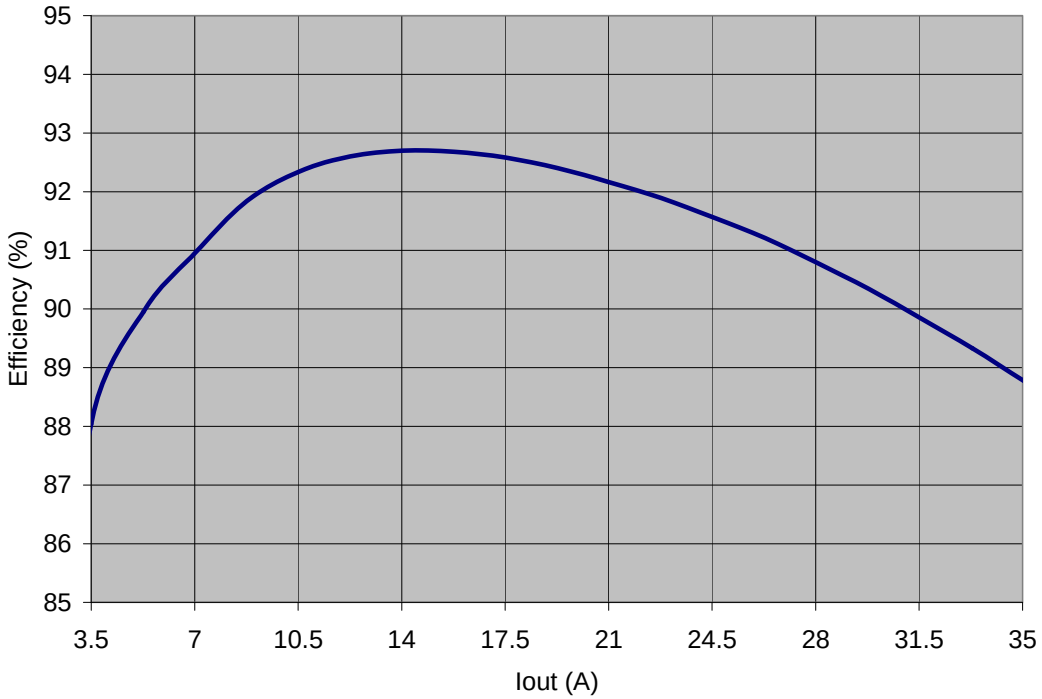


Fig.11: Efficiency versus load current

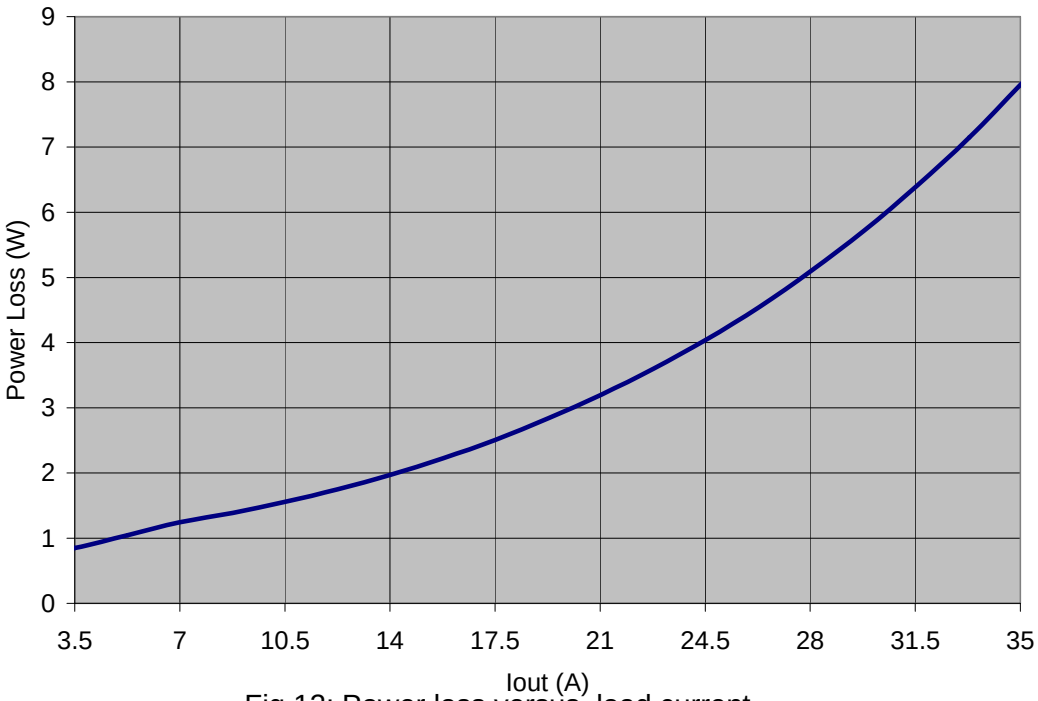


Fig.12: Power loss versus load current

THERMAL IMAGES
Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A-35A, Room Temperature, 200 LFM

Fig. 13: Thermal Image of the board at 35A load
Test point 1 is iP1837
Test point 2 is inductor

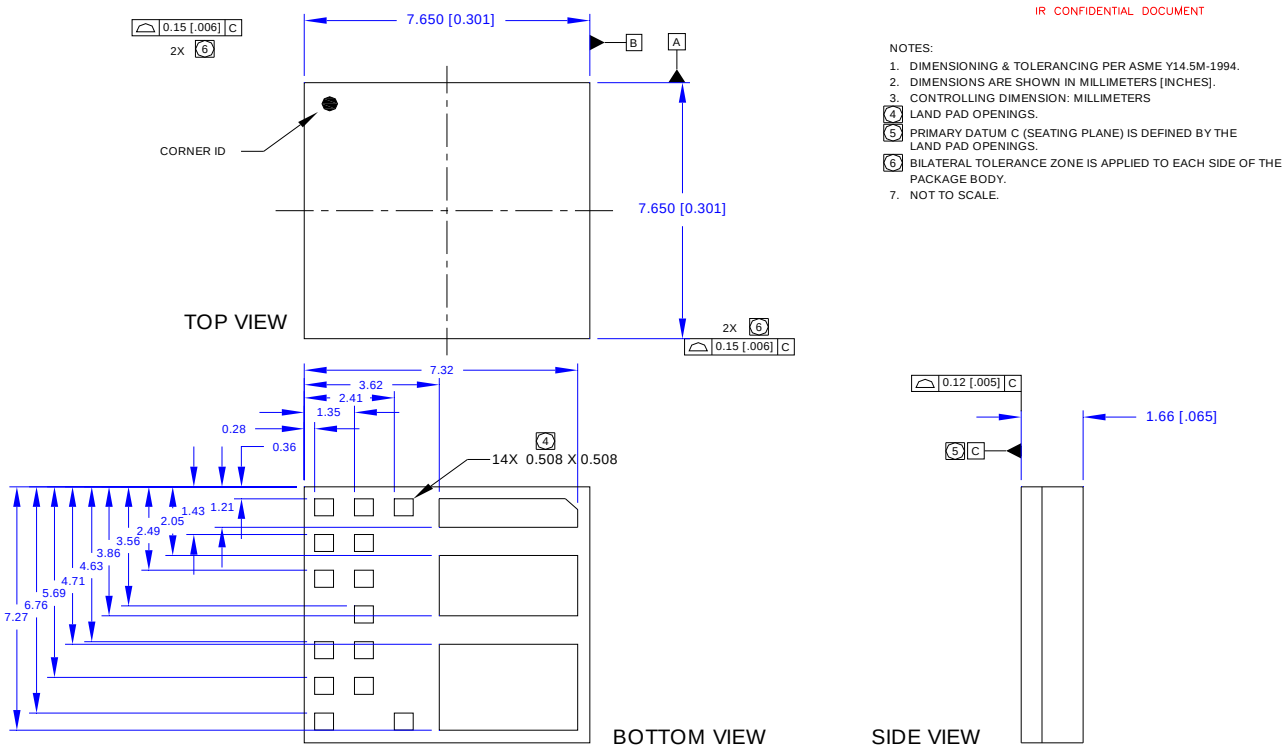


Fig. 14. Mechanical Outline Drawing

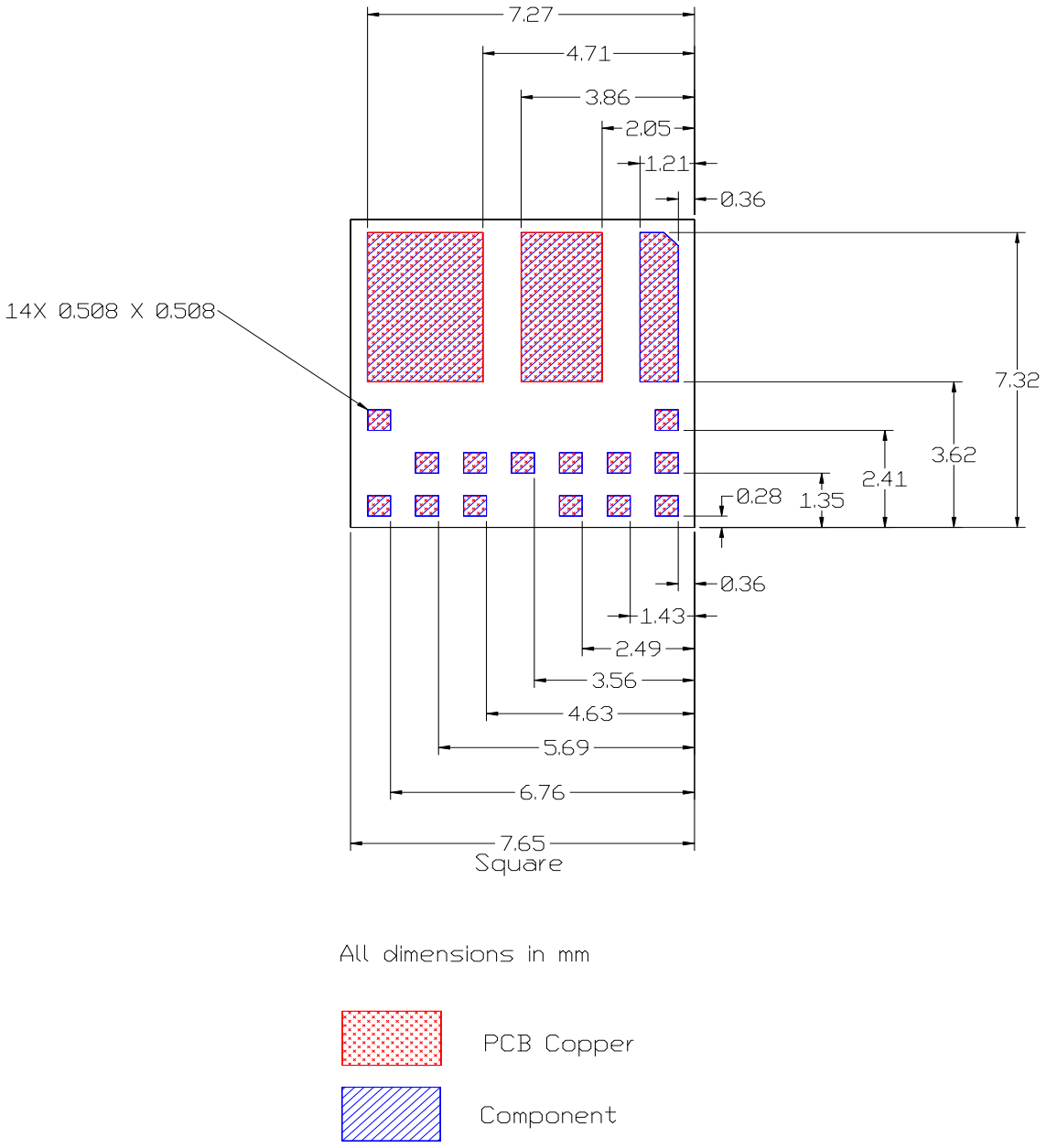


Fig. 15. PCB Metal and Components Placement

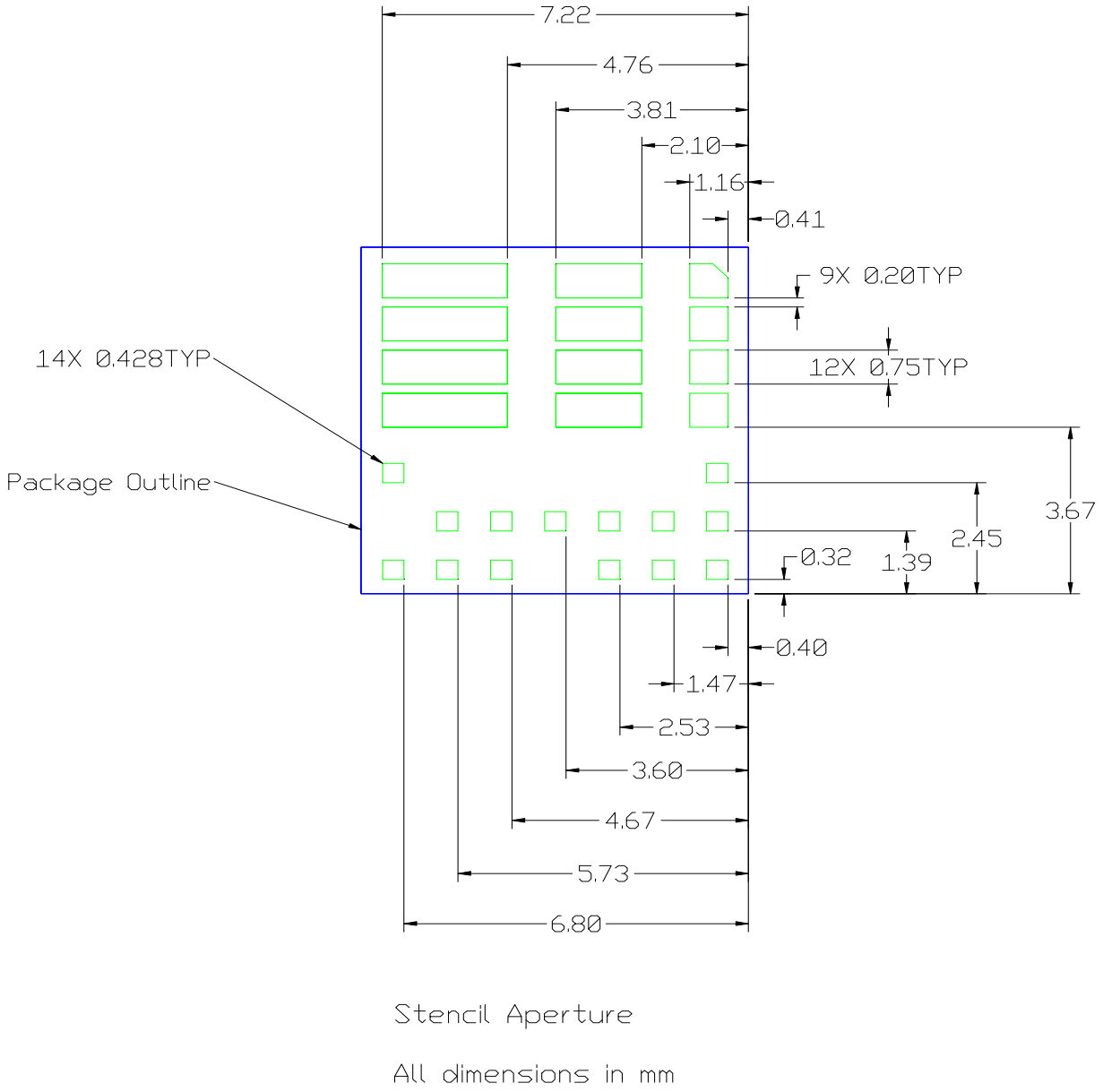


Fig. 16. Stencil Design

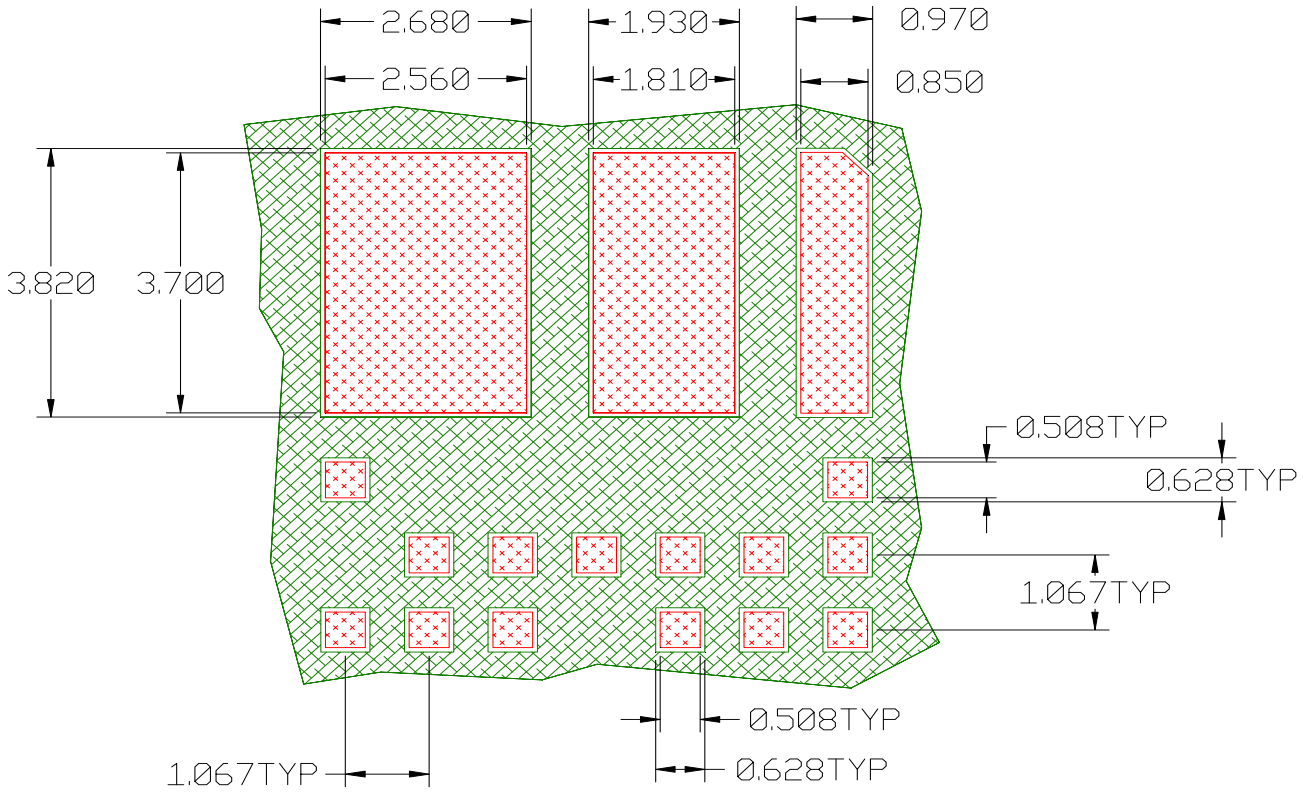
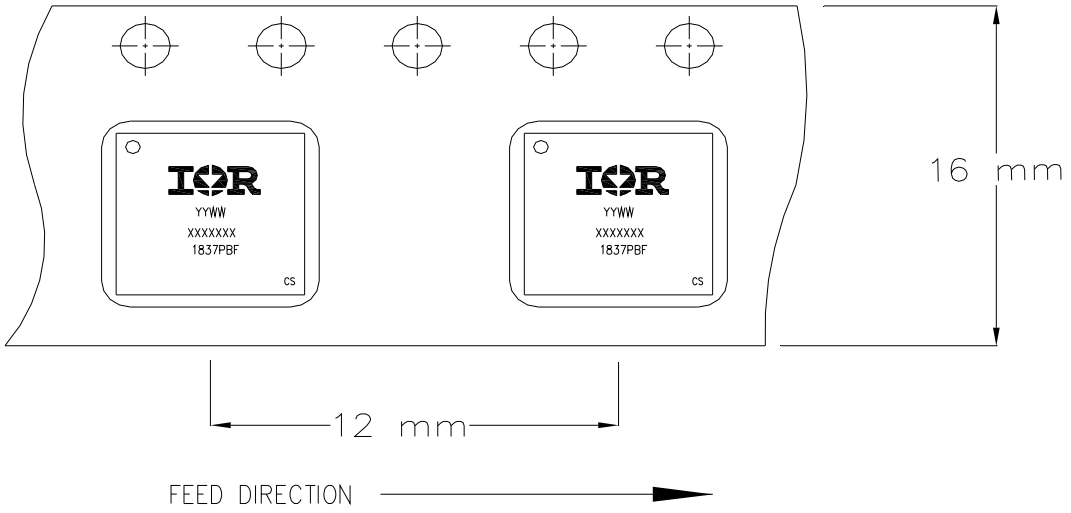
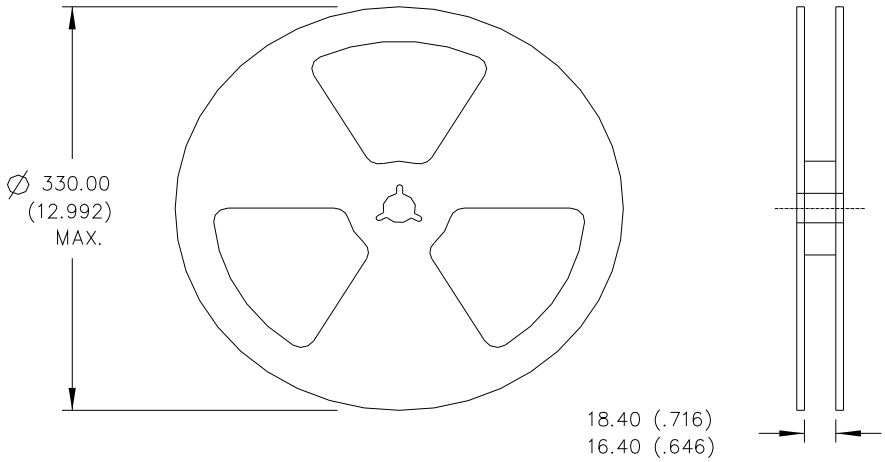


Fig. 17. Solder Resist





NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Fig. 18. Tape and Reel Information

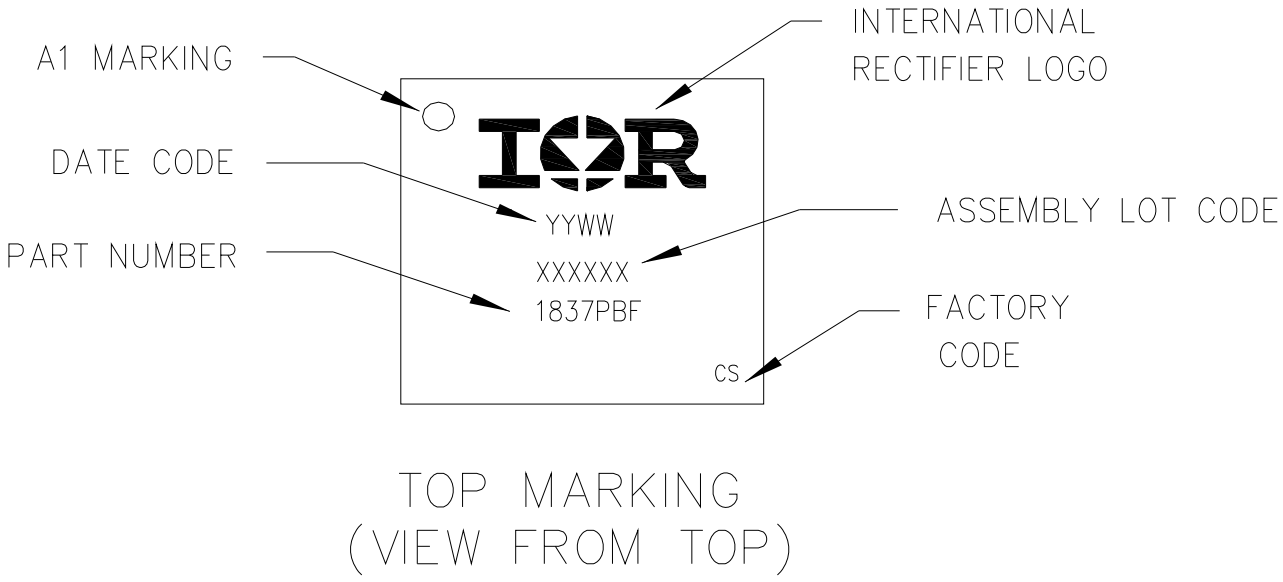


Fig. 19. Part Marking

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