FEATURES

- Intel VR11.x compliant Digital PWM Controller
- Programmable 1-phase to 8-phase operation
- Customized Digital Over-Clocking features an easy-to-use SMBus Gamer command and a Gamer VID control up to 2.3V, Gamer Vmax, VID Override or Track, Digital Load-Line Adjust, Gamer OC/OVP, Gamer OFF pin and Gamer OTP
- IR Efficiency Shaping features a Variable Gate Drive and Dynamic Phase Control
- 1-phase to 4-phase PSI for Light Loads
- Adaptive Transient Algorithm minimizes capacitors
- Designed for use with coupled inductors
- Enables Thermal Phase Balancing
- SMBus Fault Indicators: OVP, UVP, OCP, OTP
- SMBus interface for configuring and monitoring; SMBus commands include monitoring input current and power
- Compatible with IR ATL Drivers and tri-state Drivers
- 9 bytes of NVM storage available for customer use
- +3.3V supply voltage; 0ºC to 85ºC Ambient operation
- RoHS Compliant, MSL level 1 package

APPLICATIONS

- Intel® VR11.x CPU VRD and VRM; DDR Memory
- High Performance Desktops and Servers
- Over-clocking and High-Efficiency Application

DESCRIPTION

The CHL8318-20 is an 8-phase digital synchronous buck controller for core regulation of high-performance Intel® VR11.1 and VR11.0 platforms. The CHL8318-20 is fully compliant with VR11.1 including Power Status Indicator (PSI) and for improved light load efficiency and accurate current output (IMON).

The IR CHL8318-20 includes a customized set of digital over-clocking features which require no external components. Gaming applications can use the SMBus interface to place the VRD into “Gamer Mode” to extend VID up to 2.3V with 6.25 mV resolution.

The CHL8318-20 deploys a number of efficiency shaping features such as variable MOSFET gate drive versus load, programmable PSI modes for optimum light-load along with programmable phase shedding to autonomously add/drop phases versus load.

CHL8318-20 supports three NTC temperature sensors to report temperature and trigger VR HOT and OTP faults. Digital thermal balancing allows proportional current imbalance between phases.

The CHL8318-20 provides extensive OVP, UVP, OCP and OTP fault protection. Device and fault configuration parameters are easily defined using the IR Power Designer GUI and stored in on-chip non-volatile memory (NVM).

The 3-pin SMBus interface can be used to monitor a variety of operating parameters on up to seven CHL8318-20 based VRs. The controller includes a unique sensorless and lossless input current monitoring capability.

BASIC APPLICATION

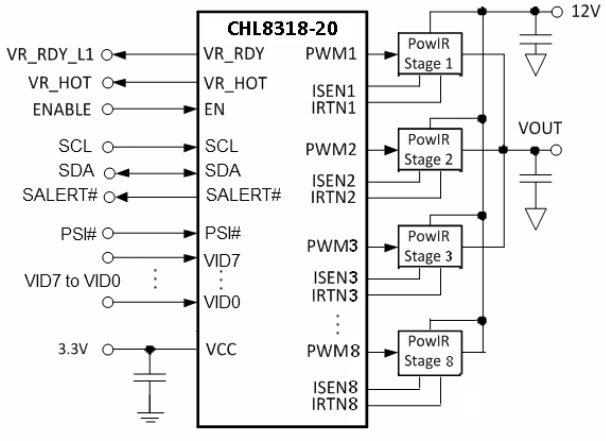


Figure 1: CHL8318-20 Basic Application Circuit

PIN DIAGRAM

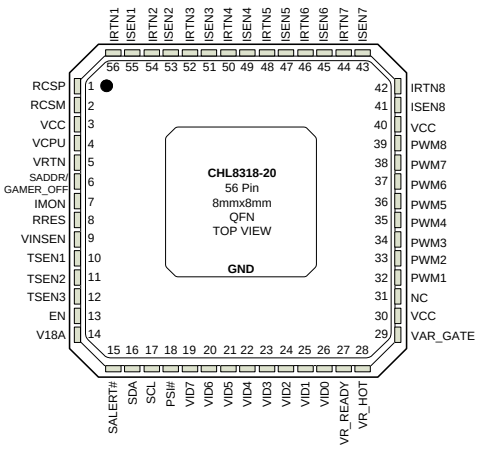
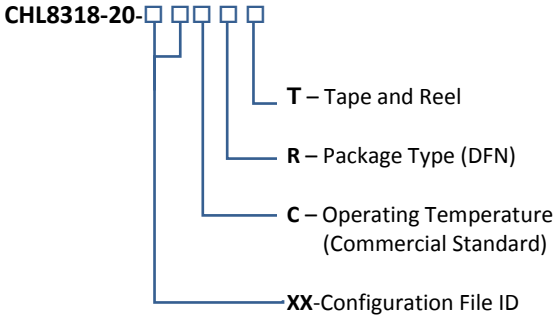


Figure 2: CHL8318-20 Package Top View

ORDERING INFORMATION



Package	Tape & Reel Qty	Part Number
QFN	3000	CHL8318-20-00CRT[1]
QFN	3000	CHL8318-20-xxCRT[2]

Notes:

1. For unprogrammed/default parts, use configuration file 00. Unprogrammed parts will not start up until programmed in order to ensure a safe power up.
2. "xx" indicates customer specific configuration file.

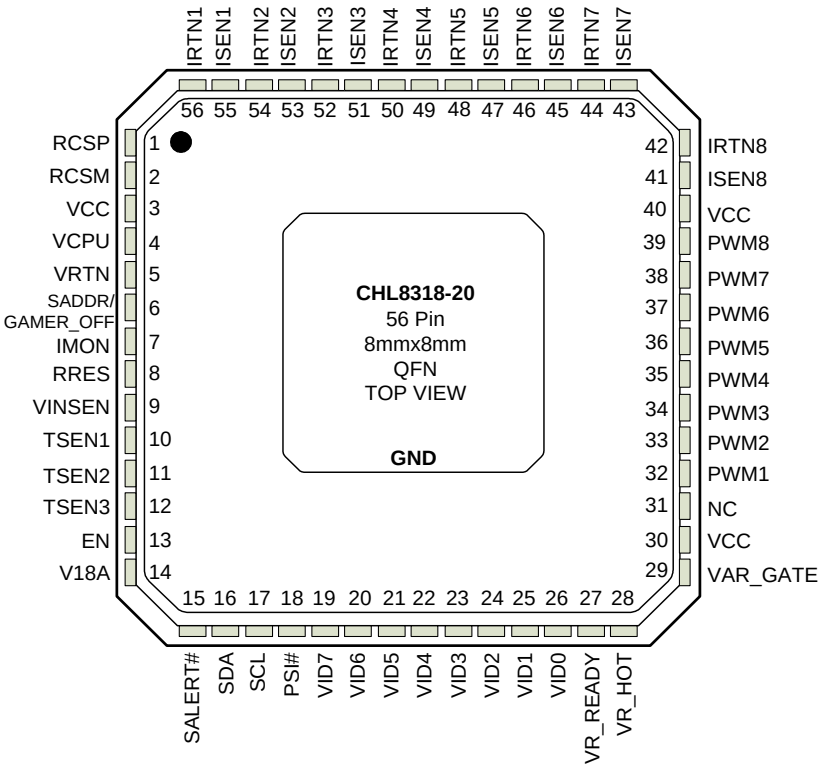


Figure 3: CHL8318-20 Top View Enlarged