

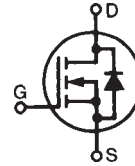
# Trench Gate Power MOSFET

## IXTQ88N28T

$V_{DSS} = 280V$   
 $I_{D25} = 88A$   
 $R_{DS(on)} \leq 44m\Omega$

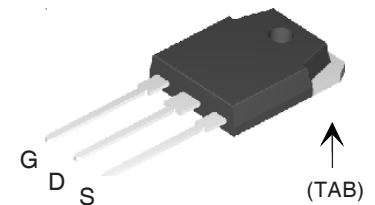
N-Channel Enhancement Mode

For Plasma Display Applications



Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ C$ to $150^\circ C$	280	V
$V_{DGR}$	$T_J = 25^\circ C$ to $150^\circ C$ ; $R_{GS} = 1 M\Omega$	280	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ C$	88	A
$I_{DRMS}$	External lead current limit	75	A
$I_{DM}$	$T_C = 25^\circ C$ , pulse width limited by $T_{JM}$	250	A
$P_D$	$T_C = 25^\circ C$	625	W
$T_J$		-55 ... +150	$^\circ C$
$T_{JM}$		150	$^\circ C$
$T_{stg}$		-55 ... +150	$^\circ C$
$T_L$	Maximum lead temperature for soldering	300	$^\circ C$
$T_{SOLD}$	1.6mm (0.062 in.) from case for 10s	260	$^\circ C$
$M_d$	Mounting torque	1.13/10	Nm/lb.in.
<b>Weight</b>		5.5	g

TO-3P (IXTQ)



G = Gate      D = Drain  
 S = Source    TAB = Drain

### Features

- Trench gate construction for low  $R_{DS(on)}$
- International standard package
- Low package inductance
  - easy to drive and to protect

### Advantages

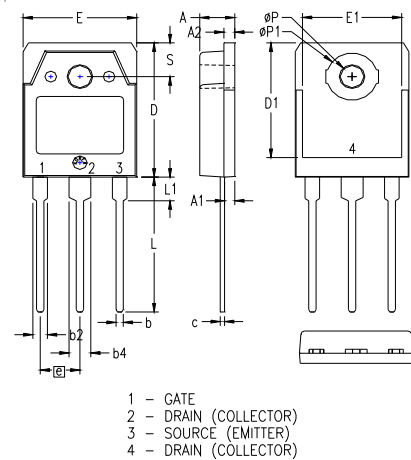
- Easy to mount
- Space savings

Symbol	Test Conditions ( $T_J = 25^\circ C$ , unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$V_{DSS}$	$V_{GS} = 0 V, I_D = 1mA$	280		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1mA$	3.0		5.0 V
$I_{GSS}$	$V_{GS} = \pm 20 V, V_{DS} = 0V$			$\pm 200$ nA
$I_{DSS}$	$V_{DS} = V_{DSS}$ $V_{GS} = 0 V$ $T_J = 125^\circ C$			1 $\mu A$ 200 $\mu A$
$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 0.5 \cdot I_{D25}$ , Note 1	38	44	$m\Omega$

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 10\text{ V}$ , $I_D = 0.5 I_{D25}$ , Note 1	40	66	S
$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$		5750	pF
$C_{oss}$			600	pF
$C_{rss}$			52	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 15\text{ V}$ , $V_{DS} = 220\text{ V}$ , $I_D = 44\text{ A}$ $R_G = 5\Omega$ (External)		38	ns
$t_r$			60	ns
$t_{d(off)}$			96	ns
$t_f$			57	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 0.5 \cdot I_{D25}$		138	nC
$Q_{gs}$			48	nC
$Q_{gd}$			40	nC
$R_{thJC}$				$0.20^\circ\text{C/W}$
$R_{thCK}$		0.25		$^\circ\text{C/W}$

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		Min.	typ.	Max.
$I_S$	$V_{GS} = 0\text{ V}$			88 A
$I_{SM}$	Repetitive, pulse width limited by $T_{JM}$			250 A
$V_{SD}$	$I_F = I_S$ , $V_{GS} = 0\text{ V}$ , Note 1			1.5 V
$t_{rr}$	$I_F = 25\text{ A}$ $-di/dt = 100\text{ A}/\mu\text{s}$		200	ns
$Q_{RM}$		$V_R = 100\text{ V}$		2.0

Notes: 1. Pulse test,  $t \leq 300\mu\text{s}$ ; duty cycle,  $d \leq 2\%$ .

**TO-3P (IXTQ) Outline**


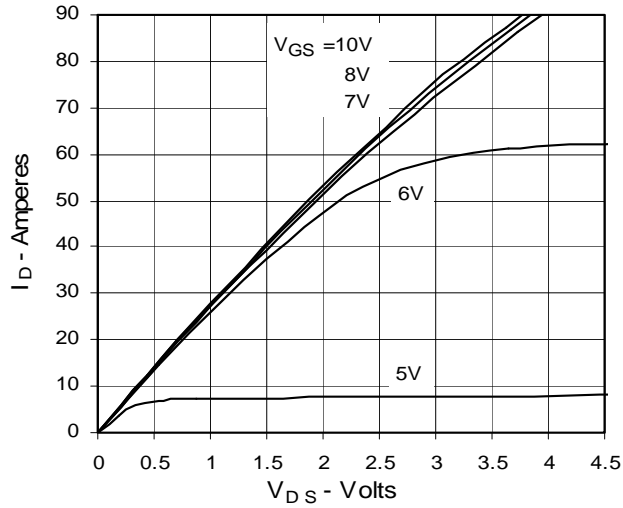
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.791	19.80	20.10
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
phi P1	.126	.134	3.20	3.40
S	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

All metal area are tin plated.

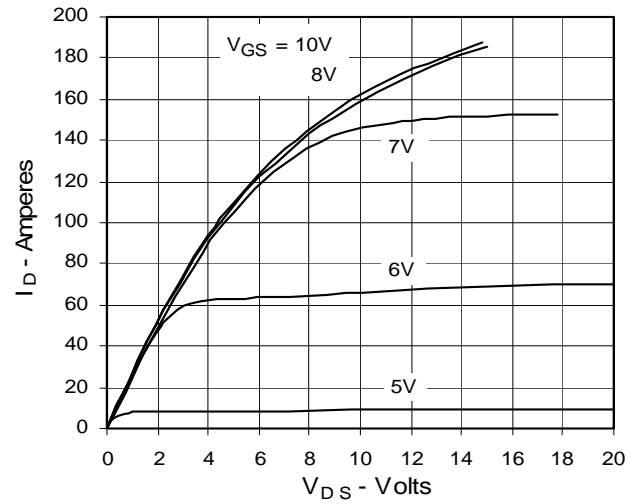
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123B1	6,534,343	6,710,405B2	6,759,692	7,063,975B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728B1	6,583,505	6,710,463	6,771,478B2	7,071,537	

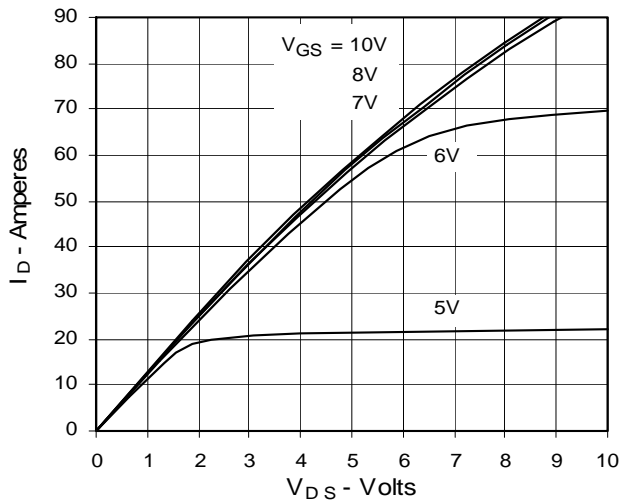
**Fig. 1. Output Characteristics**  
@ 25°C



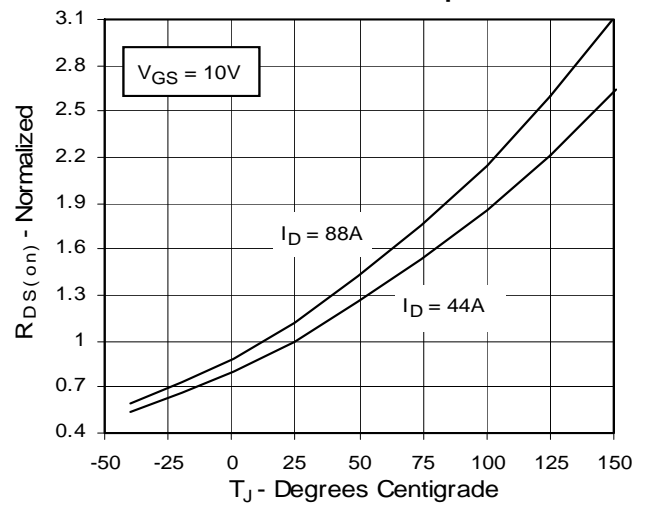
**Fig. 2. Extended Output Characteristics**  
@ 25°C



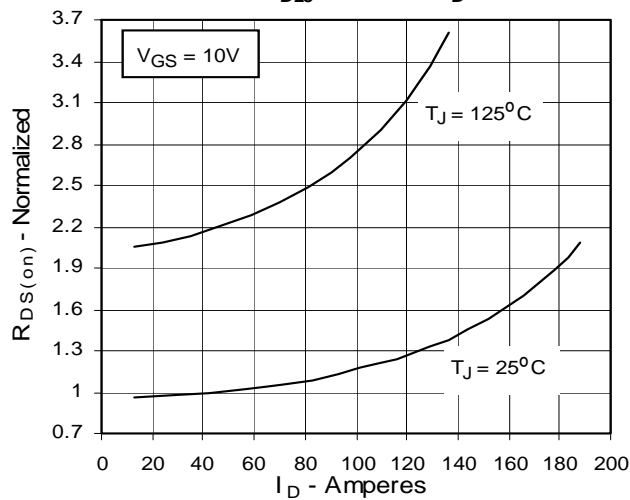
**Fig. 3. Output Characteristics**  
@ 125°C



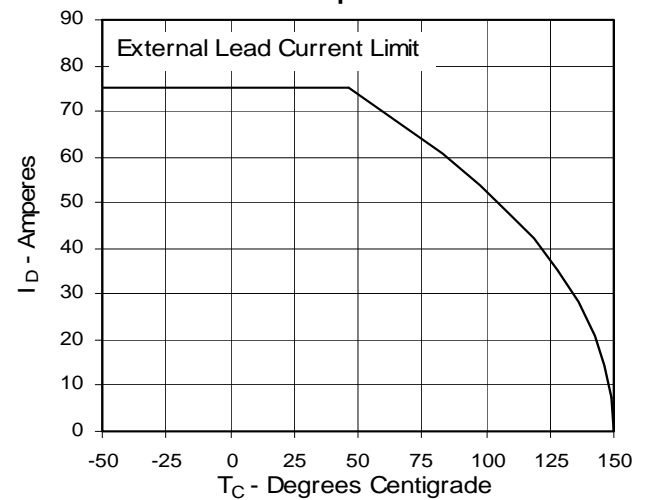
**Fig. 4.  $R_{DS(on)}$  Normalized to 0.5  $I_{D25}$  Value vs. Junction Temperature**



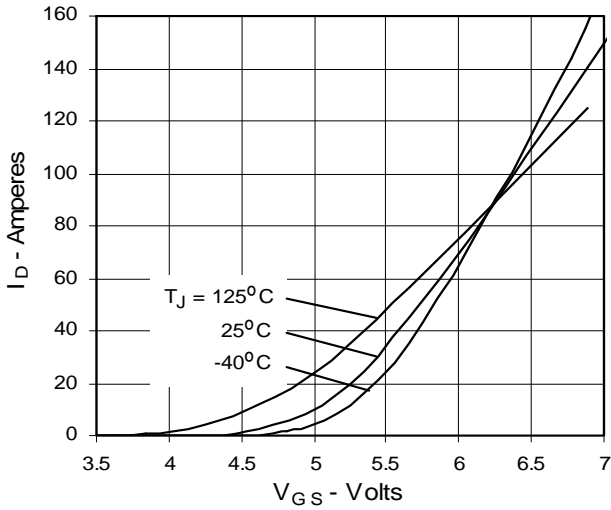
**Fig. 5.  $R_{DS(on)}$  Normalized to 0.5  $I_{D25}$  Value vs.  $I_D$**



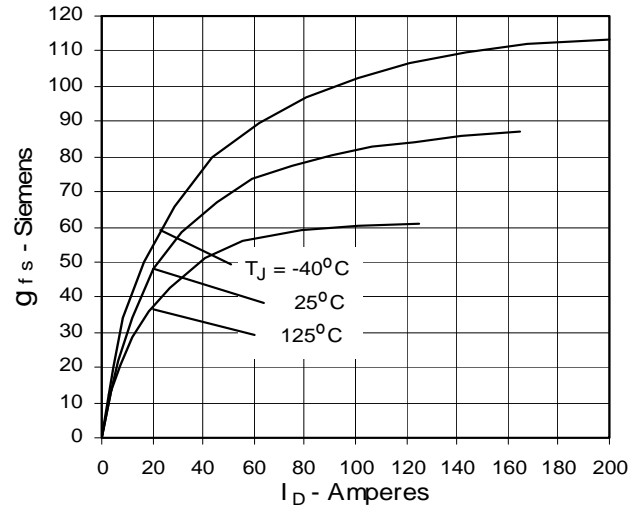
**Fig. 6. Drain Current vs. Case Temperature**



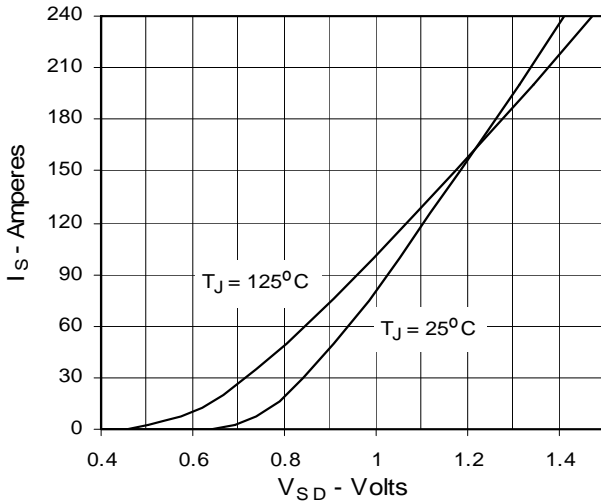
**Fig. 7. Input Admittance**



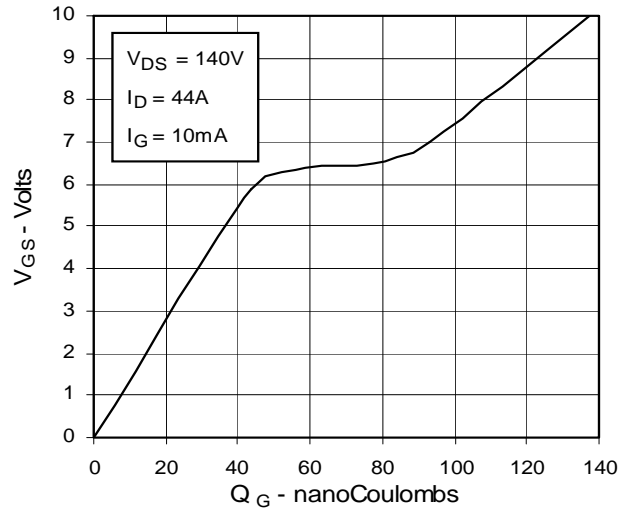
**Fig. 8. Transconductance**



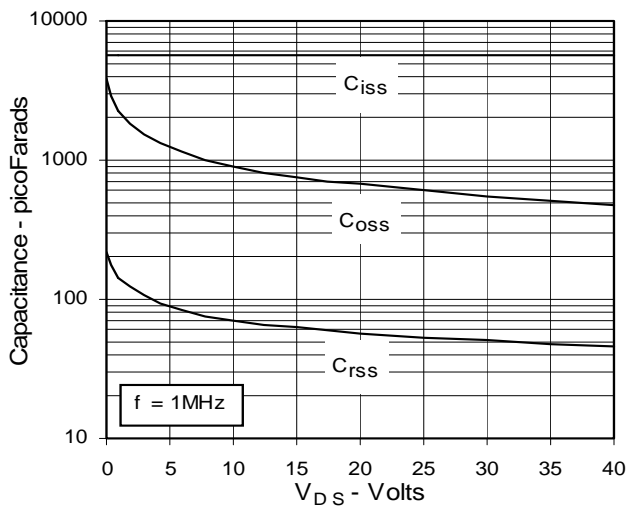
**Fig. 9. Source Current vs. Source-To-Drain Voltage**



**Fig. 10. Gate Charge**



**Fig. 11. Capacitance**



**Fig. 12. Forward-Bias Safe Operating Area**

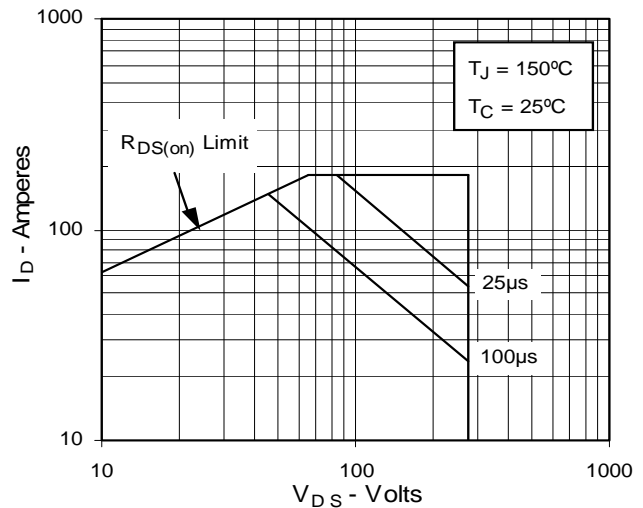


Fig. 13. Maximum Transient Thermal Impedance

