IXYS

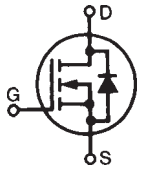
Preliminary Technical Information

Trench™ Power MOSFET

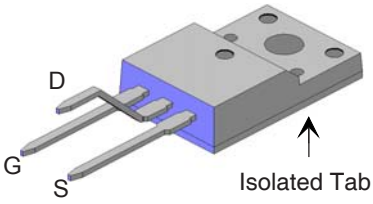
IXTP60N28TM-A

V_{DSS} = 280V
I_{D25} = 18A
$R_{DS(on)}$ ≤ 58mΩ

N-Channel Enhancement Mode
Avalanche Rated



OVERMOLDED TO-220 W/ FORMED LEAD (IXTP...M-A)



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	280	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	280	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	T_C = 25°C	18	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	140	A
dV/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	15	V/ns
P_D	T_C = 25°C	50	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from case for 10s	300	°C
T_{SOLD}	Plastic body for 10 seconds	260	°C
M_d	Mounting torque	1.13 / 10	Nm/lb.in.
Weight		2.5	g

Features

- Plastic overmolded tab for electrical isolation
- Low $R_{DS(ON)}$
  - for minimum on-state conduction losses
- Fast switching

Applications

- PDP Screen Drivers, ER circuit

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 1mA	280			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	3.0		5.0	V
I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V			± 100	nA
I_{DSS}	$V_{DS} = V_{DSS}$			5	μA
	V_{GS} = 0V, T_J = 125°C			250	μA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 30A, Note 1			58	mΩ

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10V, I_D = 30A, Note 1	40	70		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		5070		pF
C_{oss}			455		pF
C_{rss}			54		pF
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 30A		84		nC
Q_{gs}			24		nC
Q_{gd}			23		nC
$t_{d(on)}$	**Resistive Switching Times T_J = 25°C**		15		ns
t_r	V_{GS} = 15V, V_{DS} = 0.5 • V_{DSS}, I_D = 30A		24		ns
$t_{d(off)}$	R_G = 15Ω (External)		56		ns
t_f			23		ns
$t_{d(on)}$	**Resistive Switching Times T_J = 125°C**		14		ns
t_r	V_{GS} = 15V, V_{DS} = 0.5 • V_{DSS}, I_D = 30A		22		ns
$t_{d(off)}$	R_G = 15Ω (External)		60		ns
t_f			17		ns
R_{thJC}				2.5	°C/W

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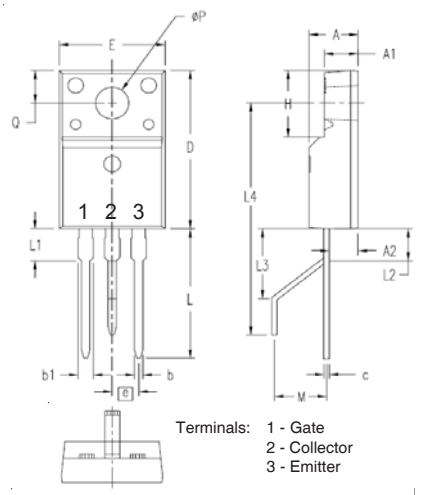

Terminals: 1 - Gate
2 - Collector
3 - Emitter

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.016	.024	0.40	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.500	.523	12.70	13.30
L1	.119	.135	3.03	3.43
L2	.098	.138	2.50	3.50
L3	.256	.295	6.50	7.50
L4	.906	.945	23.00	24.00
M	.177	.216	4.50	5.50
ØP	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			60	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			180	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.3	V
t_{rr}	I_F = 30A, -di/dt = 150A/µs, V_R= 100V, V_{GS} = 0V		170		ns

Notes: 1. Pulse test, t ≤ 300µs; duty cycle, d ≤ 2%.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ 25ºC

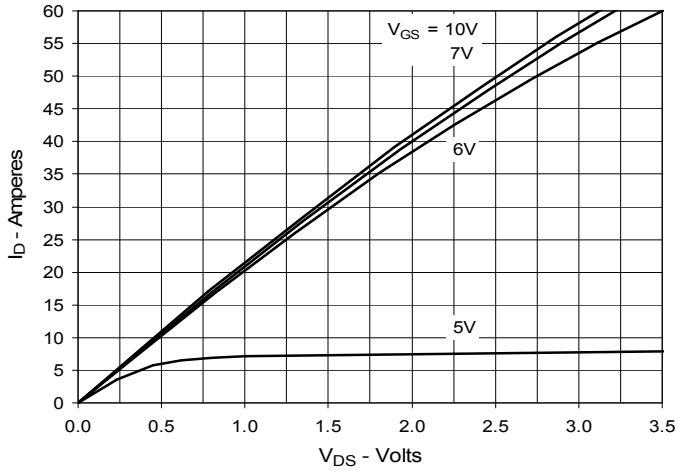

Fig. 2. Extended Output Characteristics @ 25ºC

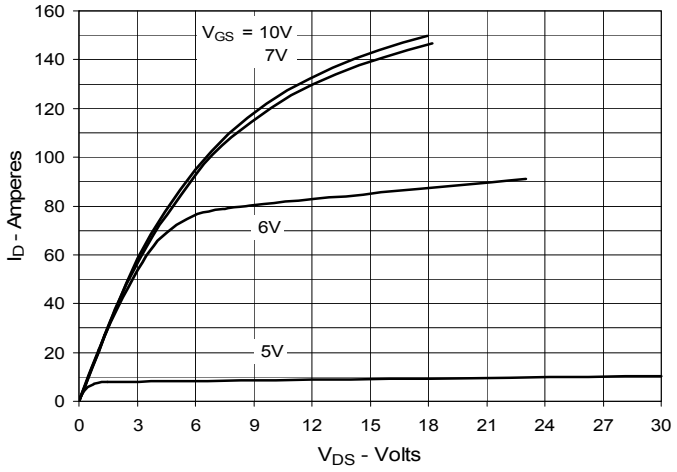

Fig. 3. Output Characteristics @ 125ºC

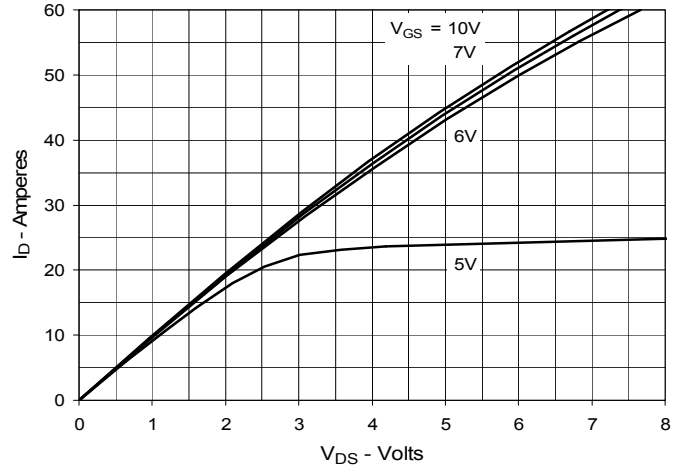

Fig. 4. $R_{DS(on)}$ Normalized to I_D = 30A Value vs. Junction Temperature

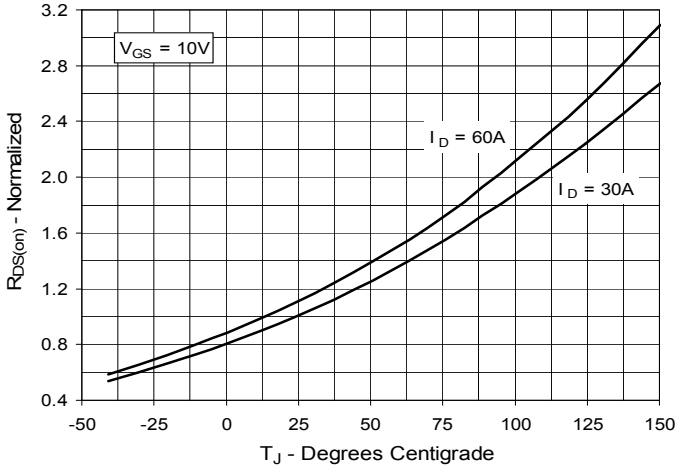

Fig. 5. $R_{DS(on)}$ Normalized to I_D = 30A Value vs. Drain Current

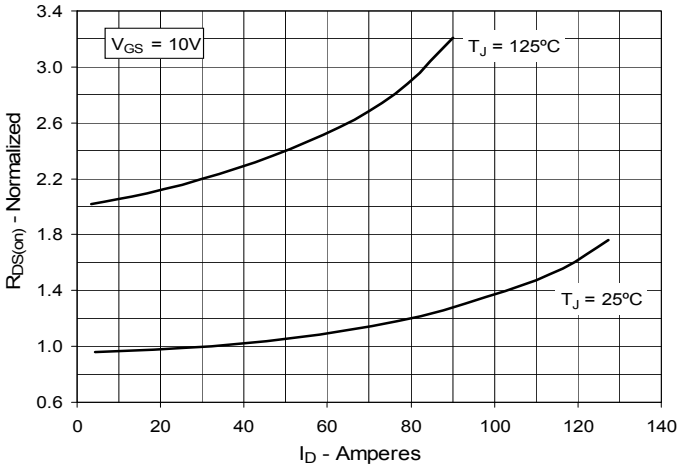

Fig. 6. Maximum Drain Current vs. Case Temperature

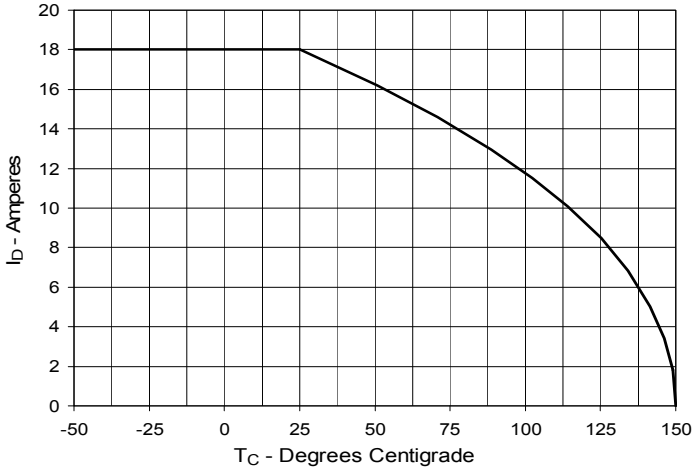

Fig. 7. Input Admittance

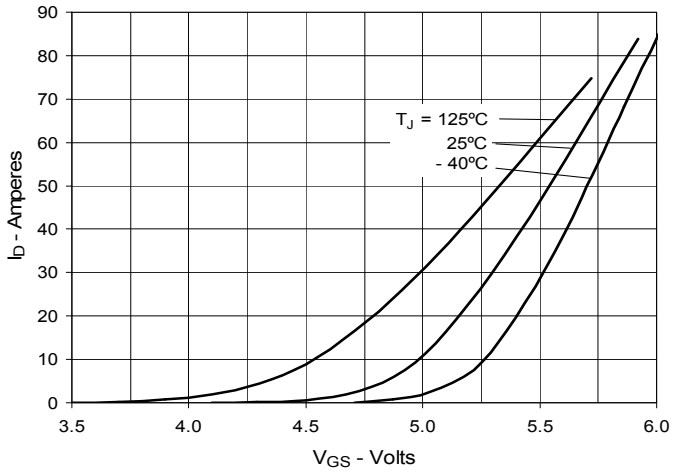

Fig. 8. Transconductance

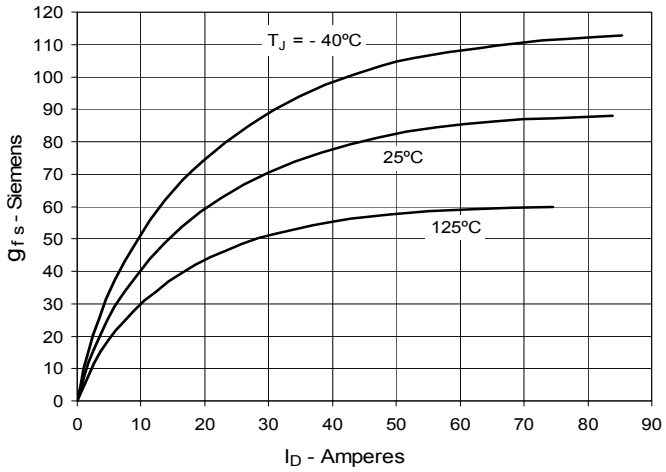

Fig. 9. Forward Voltage Drop of Intrinsic Diode

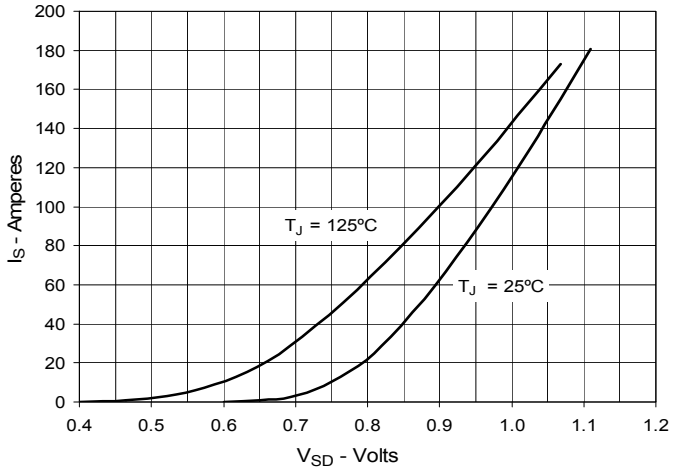

Fig. 10. Gate Charge

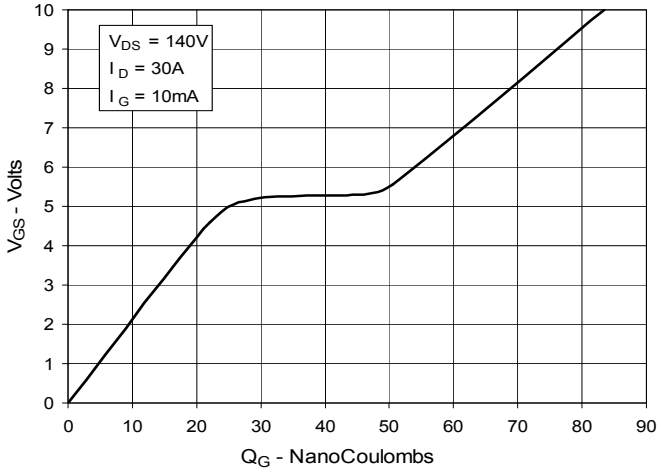

Fig. 11. Capacitance

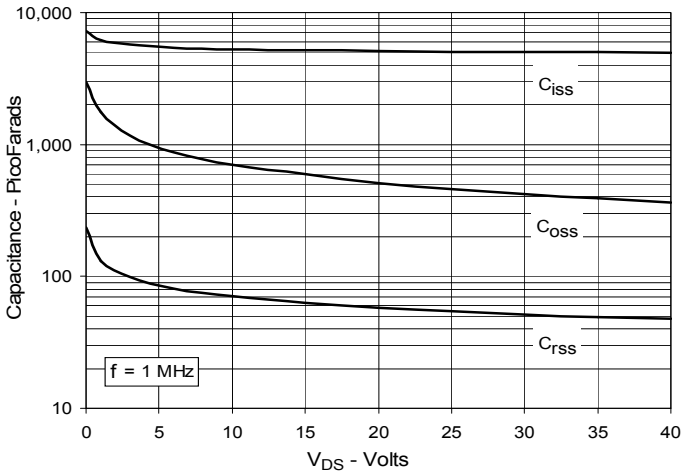

Fig. 12. Forward-Bias Safe Operating Area

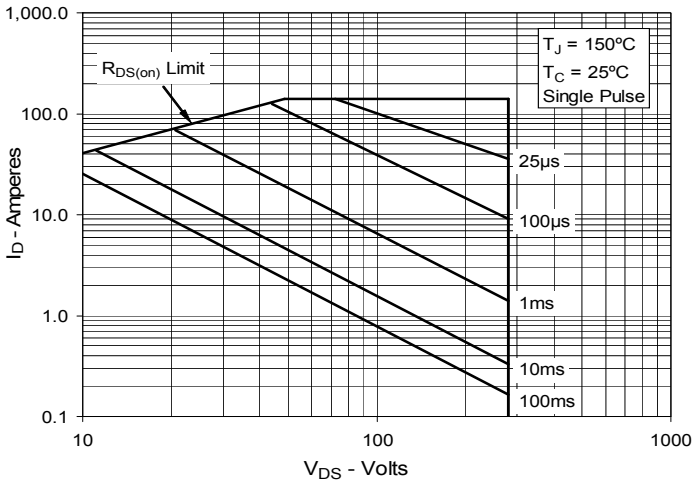

Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

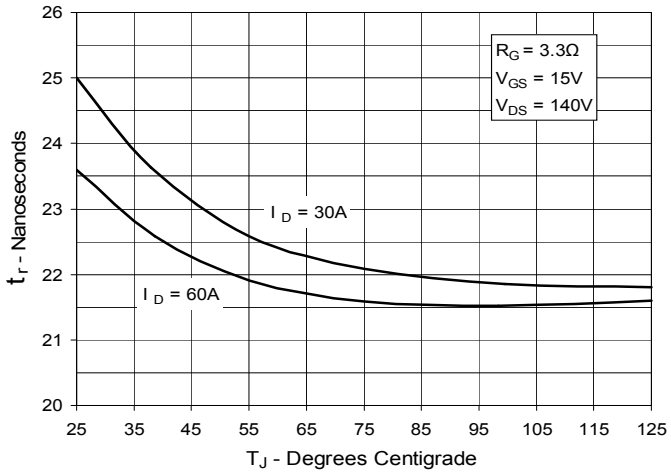

Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

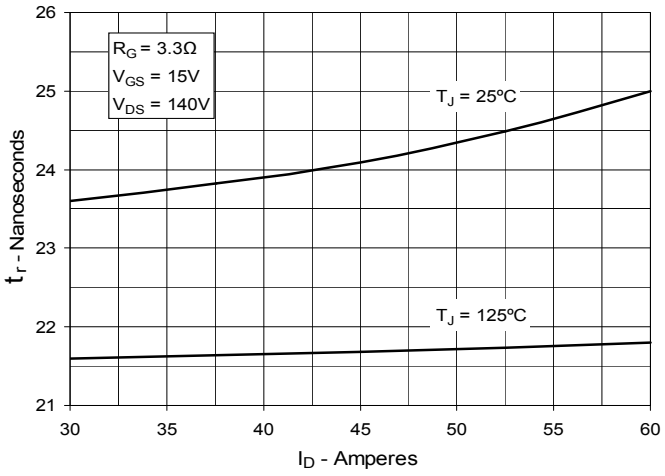

Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

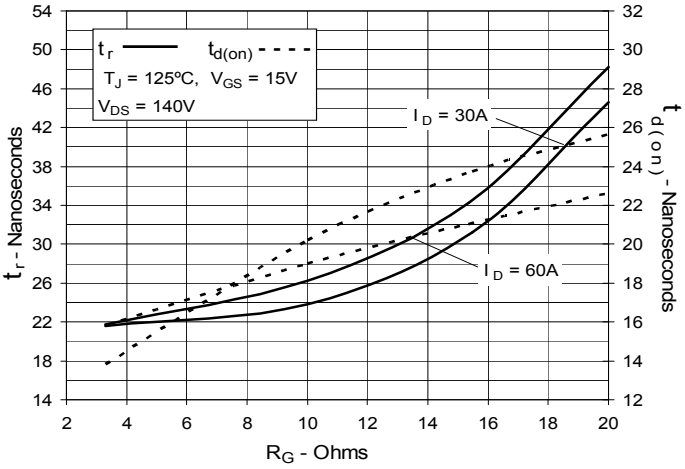

Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

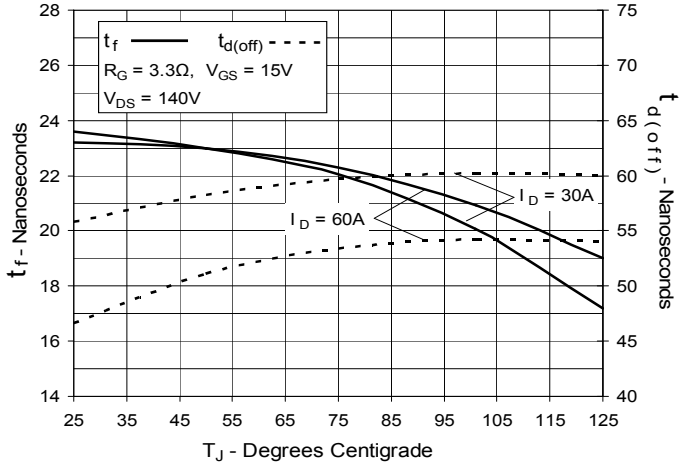

Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

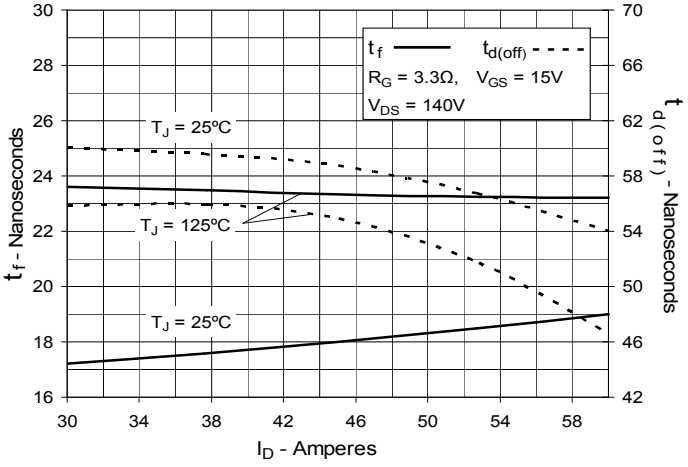

Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

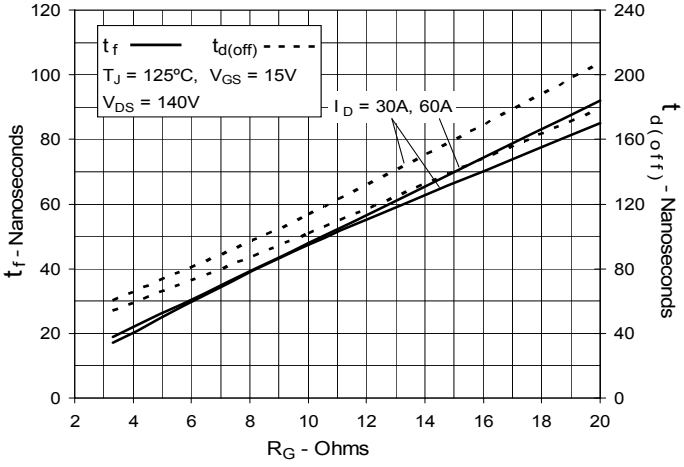

Fig. 19. Maximum Transient Thermal Impedance