

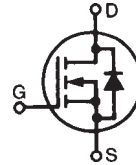
TrenchT2™
Power MOSFET
IXTA80N12T2
IXTP80N12T2

$$V_{DSS} = 120V$$

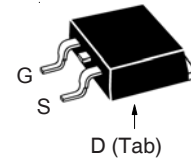
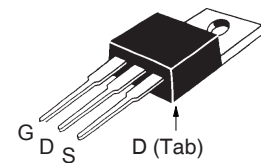
$$I_{D25} = 80A$$

$$R_{DS(on)} \leq 17m\Omega$$

N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Rectifier



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $175^\circ C$	120	V
V_{DGR}	$T_J = 25^\circ C$ to $175^\circ C$, $R_{GS} = 1M\Omega$	120	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ C$	80	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	200	A
I_A	$T_C = 25^\circ C$	40	A
E_{AS}	$T_C = 25^\circ C$	400	mJ
P_D	$T_C = 25^\circ C$	325	W
T_J		-55 ... +175	$^\circ C$
T_{JM}		175	$^\circ C$
T_{stg}		-55 ... +175	$^\circ C$
T_L	1.6mm (0.062in.) from Case for 10s	300	$^\circ C$
T_{sold}	Plastic Body for 10 Seconds	260	$^\circ C$
M_d	Mounting Torque (TO-220)	1.13 / 10	Nm/lb.in.
Weight	TO-263	2.5	g
	TO-220	3.0	g

TO-263 AA (IXTA)

TO-220AB (IXTP)


G = Gate D = Drain
 S = Source Tab = Drain

Features

- International Standard Packages
- 175°C Operating Temperature
- Avalanche Rated
- Low $R_{DS(on)}$
- Fast Intrinsic Rectifier
- High Current Handling Capability

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Synchronous Rectification
- DC/DC Converters and Off-Line UPS
- Primary- Side Switch
- High Current Switching Applications

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	120		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.0		4.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 150^\circ C$			5 μA
				175 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Notes 1, 2			17 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	36	60	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		4740	pF
C_{oss}			415	pF
C_{rss}			66	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 10\Omega$ (External)		21	ns
t_r			14	ns
$t_{d(off)}$			39	ns
t_f			28	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		80	nC
Q_{gs}			23	nC
Q_{gd}			20	nC
R_{thJC}				0.46 $^\circ\text{C/W}$
R_{thCH}	TO-220		0.50	$^\circ\text{C/W}$

Source-Drain Diode

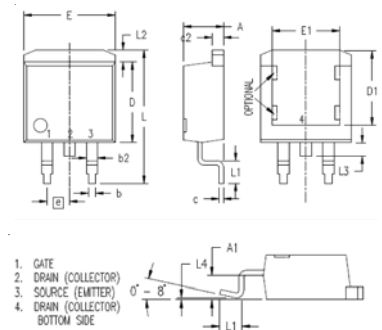
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			80 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			320 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.3 V
t_{rr}	$I_F = 0.5 \cdot I_{D25}$, $V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 60\text{V}$		90	ns
I_{RM}			4	A
Q_{RM}			180	nC

- Notes: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. On through-hole packages, $R_{DS(on)}$ Kelvin test contact location must be 5mm or less from the package body.

ADVANCE TECHNICAL INFORMATION

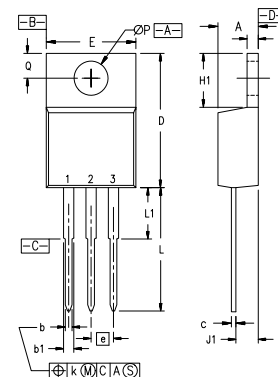
The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

TO-263 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

TO-220 Outline



- Pins: 1 - Gate 2 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

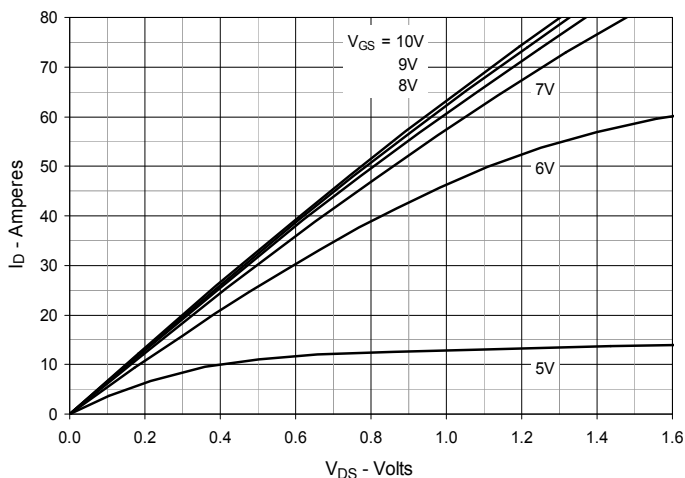


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

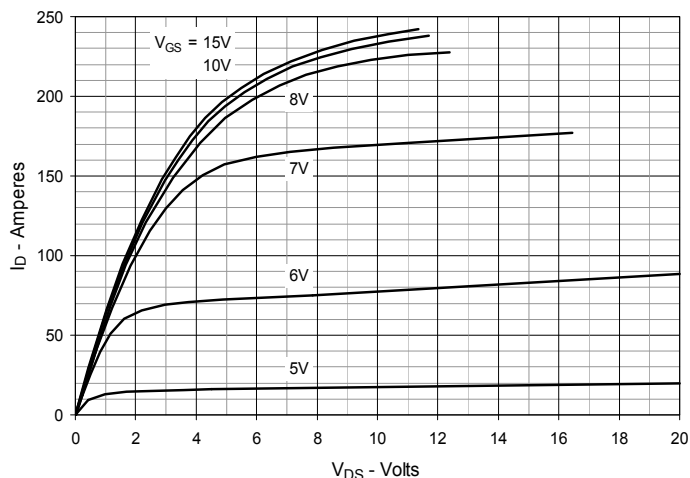


Fig. 3. Output Characteristics @ $T_J = 150^\circ\text{C}$

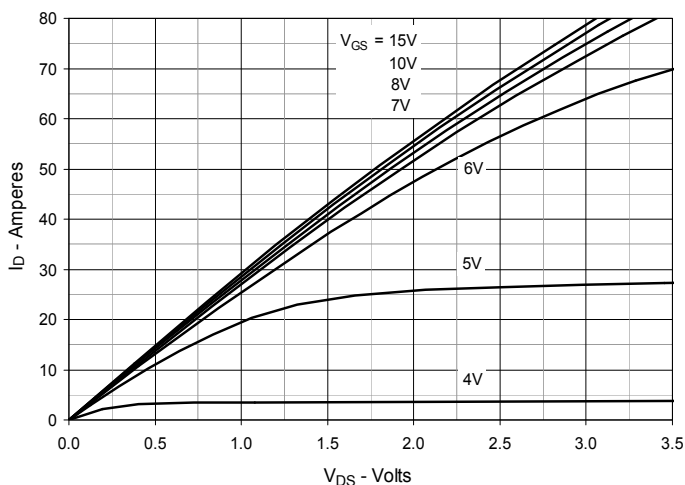


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 40\text{A}$ Value vs. Junction Temperature

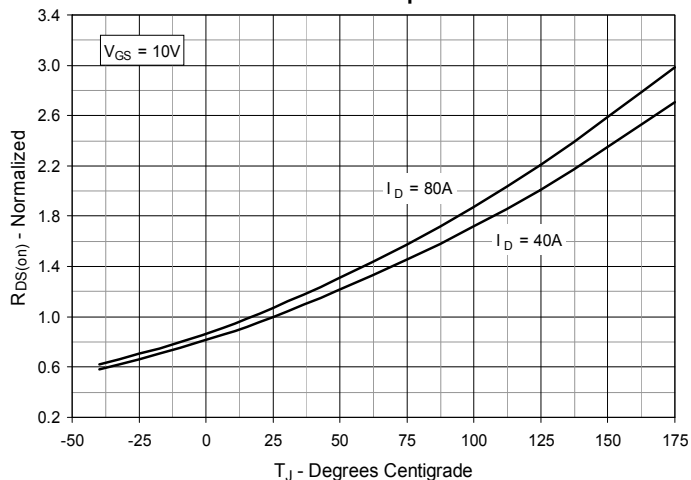


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 40\text{A}$ Value vs. Drain Current

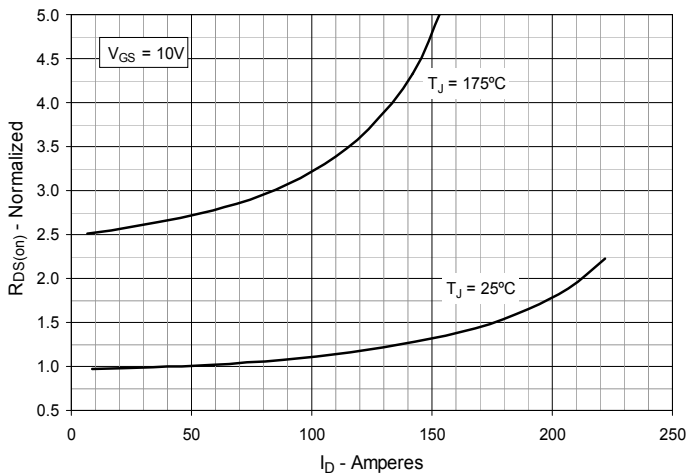


Fig. 6. Drain Current vs. Case Temperature

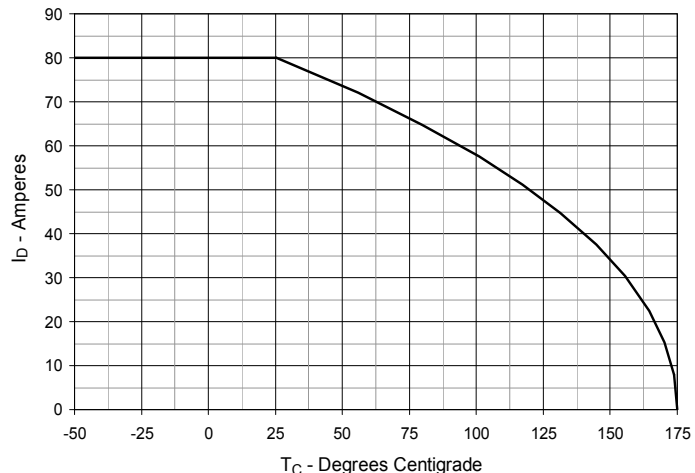


Fig. 7. Input Admittance

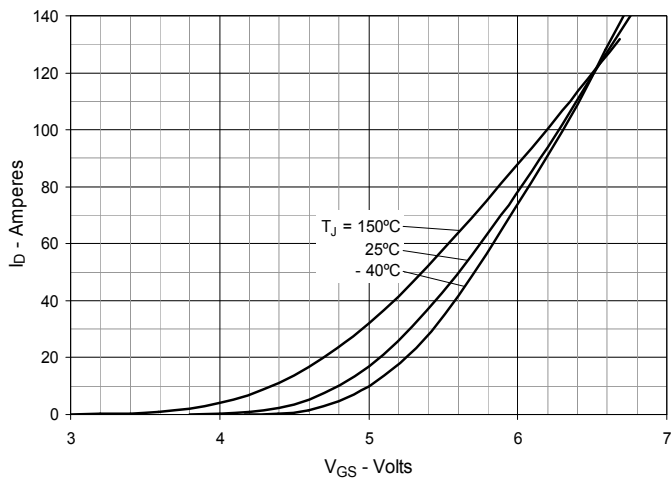


Fig. 8. Transconductance

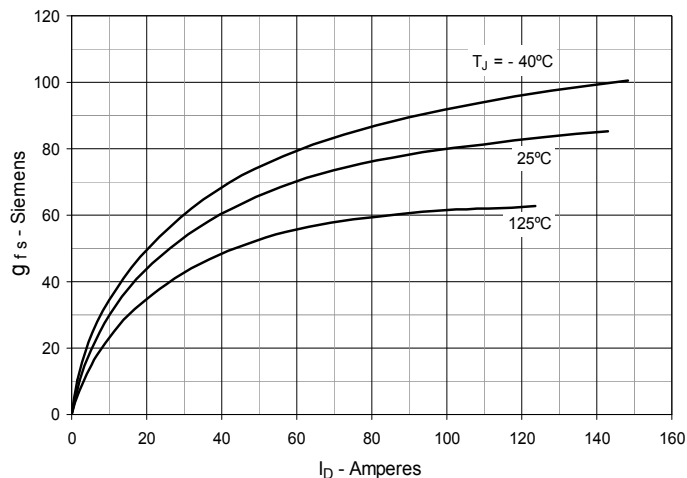


Fig. 9. Forward Voltage Drop of Intrinsic Diode

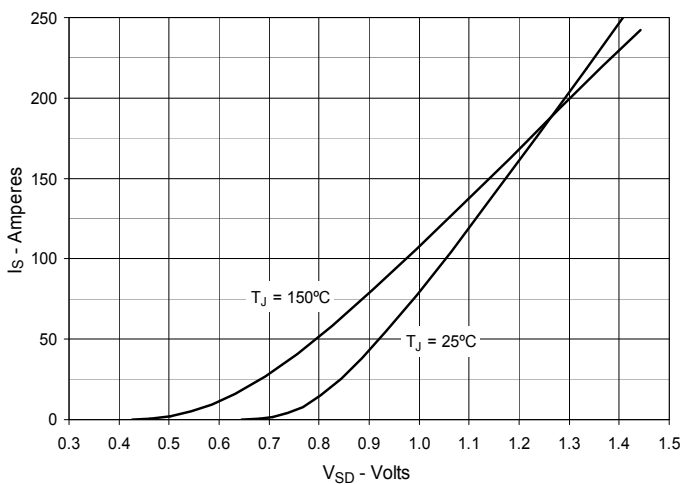


Fig. 10. Gate Charge

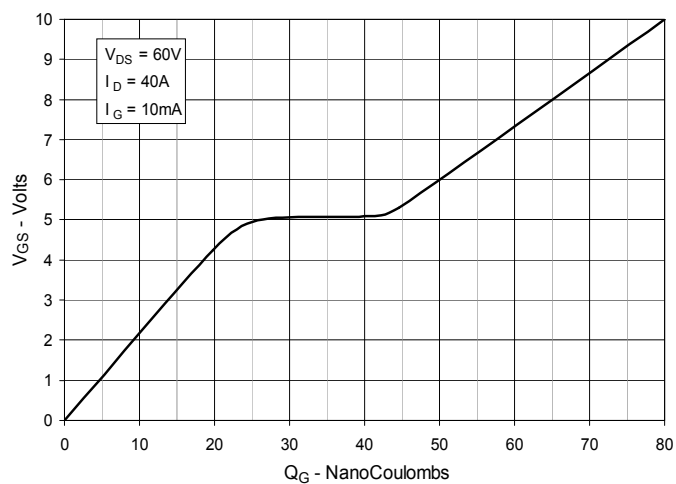


Fig. 11. Capacitance

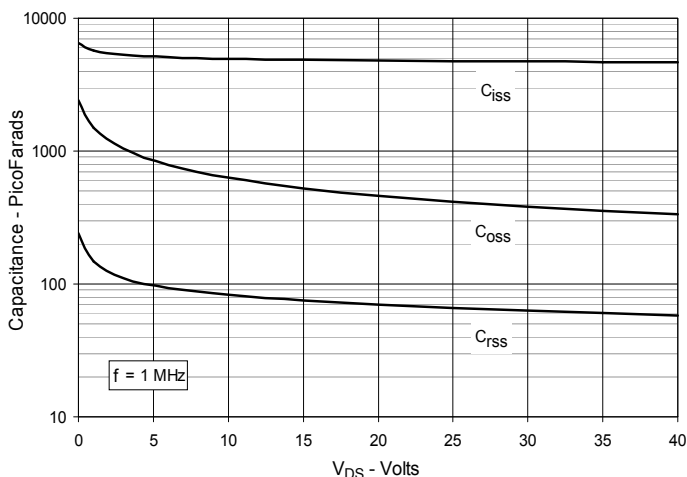
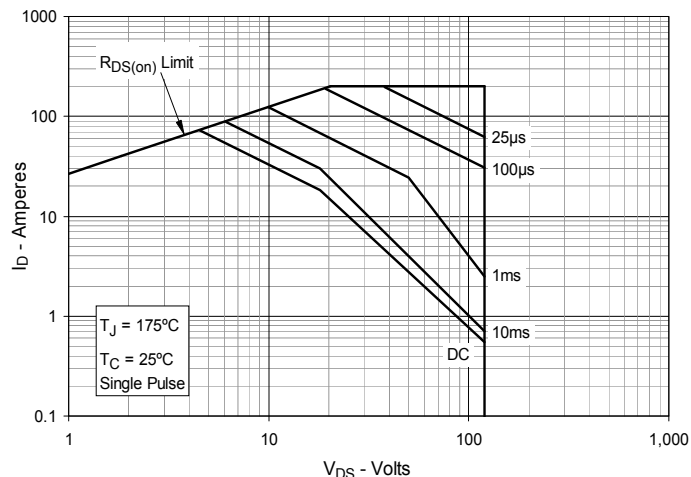


Fig. 12. Forward-Bias Safe Operating Area



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

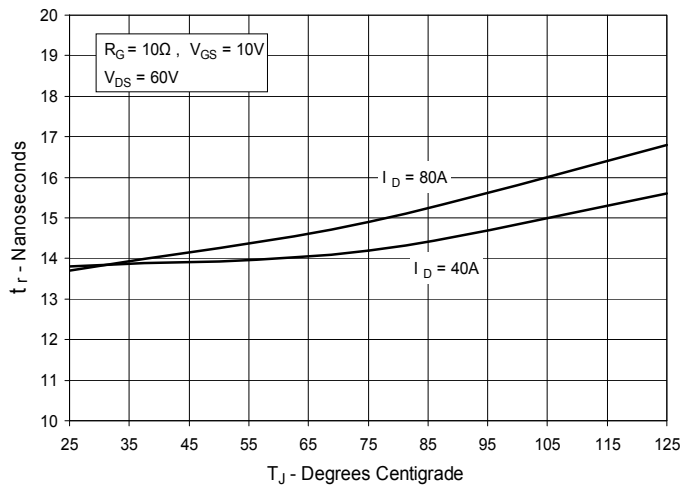


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

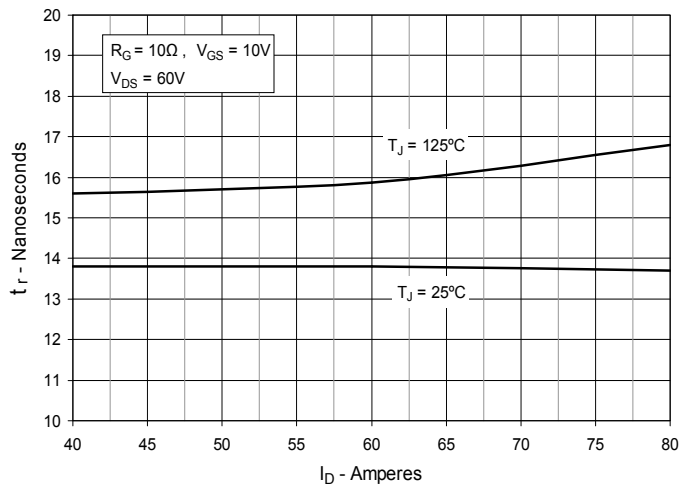


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

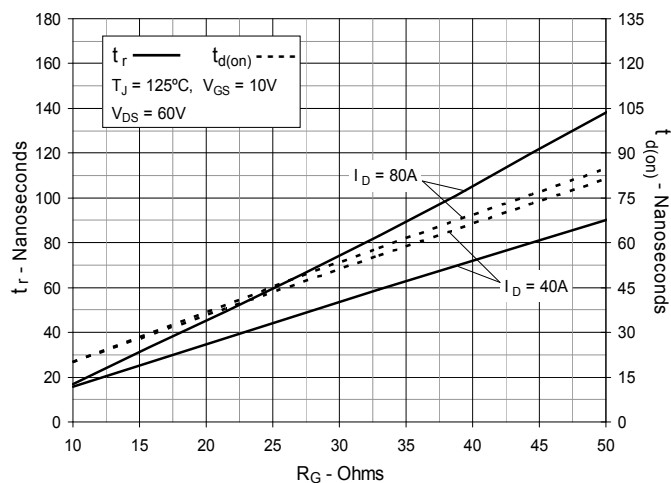


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

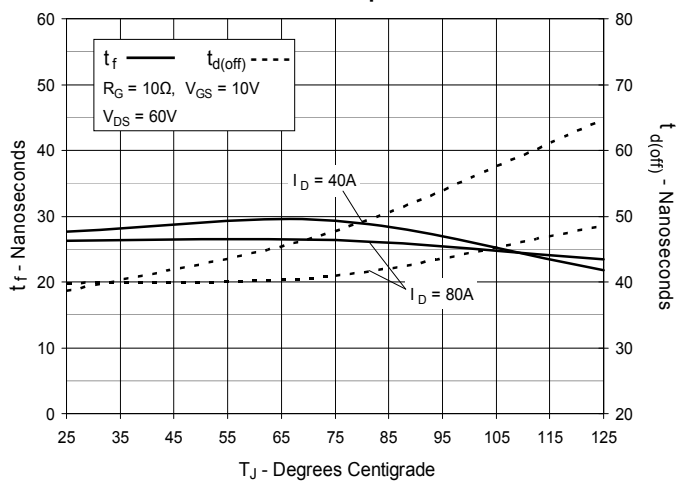


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

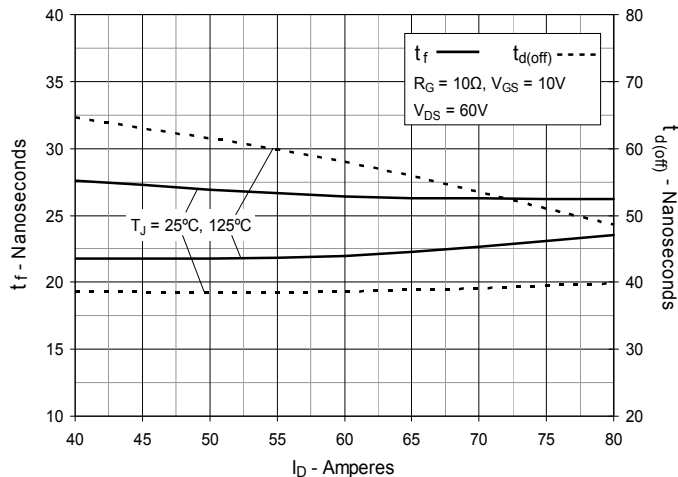


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

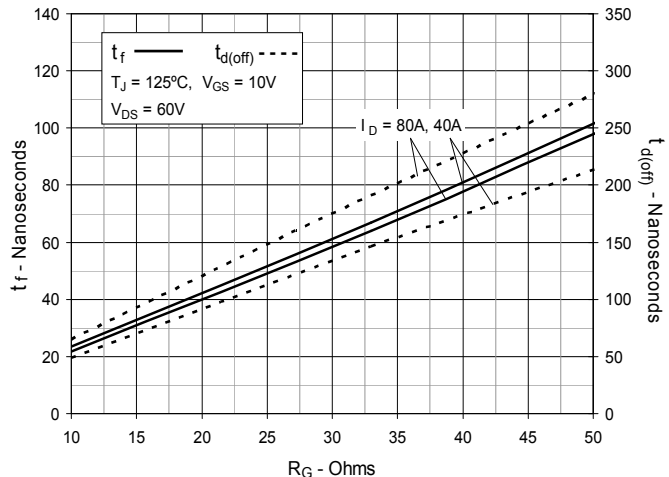


Fig. 19. Maximum Transient Thermal Impedance

