

TrenchT2™ GigaMOS™
HiperFET™
Power MOSFET

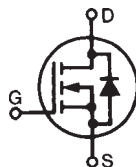
MMIX1F520N075T2

$$V_{DSS} = 75V$$

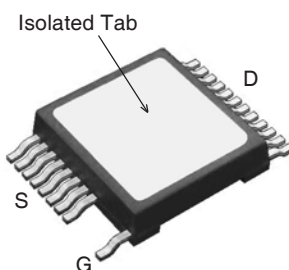
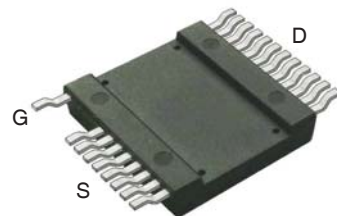
$$I_{D25} = 500A$$

$$R_{DS(on)} \leq 1.6m\Omega$$

(Electrically Isolated Tab)



N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Diode



G = Gate D = Drain
 S = Source

| Symbol | Test Conditions | Maximum Ratings | |
|---------------|---|------------------|------------|
| V_{DSS} | $T_J = 25^\circ C$ to $175^\circ C$ | 75 | V |
| V_{DGR} | $T_J = 25^\circ C$ to $175^\circ C$, $R_{GS} = 1M\Omega$ | 75 | V |
| V_{GSS} | Continuous | ± 20 | V |
| V_{GSM} | Transient | ± 30 | V |
| I_{D25} | $T_C = 25^\circ C$ | 500 | A |
| I_{DM} | $T_C = 25^\circ C$, Pulse Width Limited by T_{JM} | 1700 | A |
| I_A | $T_C = 25^\circ C$ | 200 | A |
| E_{AS} | $T_C = 25^\circ C$ | 3 | J |
| P_D | $T_C = 25^\circ C$ | 830 | W |
| T_J | | -55 ... +175 | $^\circ C$ |
| T_{JM} | | 175 | $^\circ C$ |
| T_{stg} | | -55 ... +175 | $^\circ C$ |
| T_L | 1.6mm (0.062 in.) from Case for 10s | 300 | $^\circ C$ |
| T_{SOLD} | Plastic Body for 10s | 260 | $^\circ C$ |
| V_{ISOL} | 50/60 Hz, 1 Minute | 2500 | V~ |
| F_C | Mounting Force | 50..200 / 11..45 | N/lb. |
| Weight | | 8 | g |

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Substrate
 - Excellent Thermal Transfer
 - Increased Temperature and Power Cycling Capability
 - High Isolation Voltage (2500V~)
- 175 $^\circ C$ Operating Temperature
- Very High Current Handling Capability
- Fast Intrinsic Diode
- Avalanche Rated
- Very Low $R_{DS(on)}$

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC-DC Converters and Off-Line UPS
- Primary-Side Switch
- High Speed Power Switching Applications

| Symbol | Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified) | Characteristic Values | | |
|--------------|---|-----------------------|------|----------------------|
| | | Min. | Typ. | Max. |
| BV_{DSS} | $V_{GS} = 0V$, $I_D = 3mA$ | 75 | | V |
| $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 8mA$ | 2.5 | | V |
| I_{GSS} | $V_{GS} = \pm 20V$, $V_{DS} = 0V$ | | | ± 200 nA |
| I_{DSS} | $V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 150^\circ C$ | | | 25 μA 2.0 mA |
| $R_{DS(on)}$ | $V_{GS} = 10V$, $I_D = 100A$, Note 1 | | | 1.6 m Ω |

| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified) | Characteristic Values | | |
|--------------|--|-----------------------|------|-------------------------|
| | | Min. | Typ. | Max. |
| g_{fs} | $V_{DS} = 10\text{V}$, $I_D = 60\text{A}$, Note 1 | 95 | 155 | S |
| C_{iss} | $V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$ | | 41 | nF |
| C_{oss} | | | 4150 | pF |
| C_{rss} | | | 530 | pF |
| R_{GI} | Gate Input Resistance | | 1.36 | Ω |
| $t_{d(on)}$ | Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 200\text{A}$ $R_G = 1\Omega$ (External) | | 48 | ns |
| t_r | | | 36 | ns |
| $t_{d(off)}$ | | | 80 | ns |
| t_f | | | 35 | ns |
| $Q_{g(on)}$ | $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 260\text{A}$ | | 545 | nC |
| Q_{gs} | | | 177 | nC |
| Q_{gd} | | | 135 | nC |
| R_{thJC} | | | | 0.18 $^\circ\text{C/W}$ |
| R_{thCS} | | 0.05 | | $^\circ\text{C/W}$ |

Source-Drain Diode

| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified) | Characteristic Values | | |
|----------|--|-----------------------|------|--------|
| | | Min. | Typ. | Max. |
| I_S | $V_{GS} = 0\text{V}$ | | | 520 A |
| I_{SM} | Repetitive, Pulse Width Limited by T_{JM} | | | 1600 A |
| V_{SD} | $I_F = 100\text{A}$, $V_{GS} = 0\text{V}$, Note 1 | | | 1.25 V |
| t_{rr} | $I_F = 150\text{A}$, $V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 37.5\text{V}$ | | | 150 ns |
| I_{RM} | | | 7 | A |
| Q_{RM} | | | 357 | nC |

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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| | | | | | | | | | | |
|--|-----------|-----------|-----------|-----------|--------------|--------------|--------------|--------------|--------------|-------------|
| IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: | 4,835,592 | 4,931,844 | 5,049,961 | 5,237,481 | 6,162,665 | 6,404,065 B1 | 6,683,344 | 6,727,585 | 7,005,734 B2 | 7,157,338B2 |
| | 4,850,072 | 5,017,508 | 5,063,307 | 5,381,025 | 6,259,123 B1 | 6,534,343 | 6,710,405 B2 | 6,759,692 | 7,063,975 B2 | |
| | 4,881,106 | 5,034,796 | 5,187,117 | 5,486,715 | 6,306,728 B1 | 6,583,505 | 6,710,463 | 6,771,478 B2 | 7,071,537 | |

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

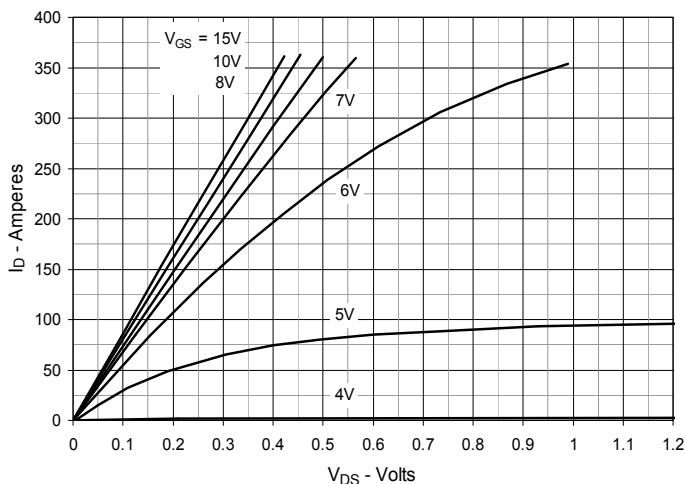


Fig. 2. Output Characteristics @ $T_J = 150^\circ\text{C}$

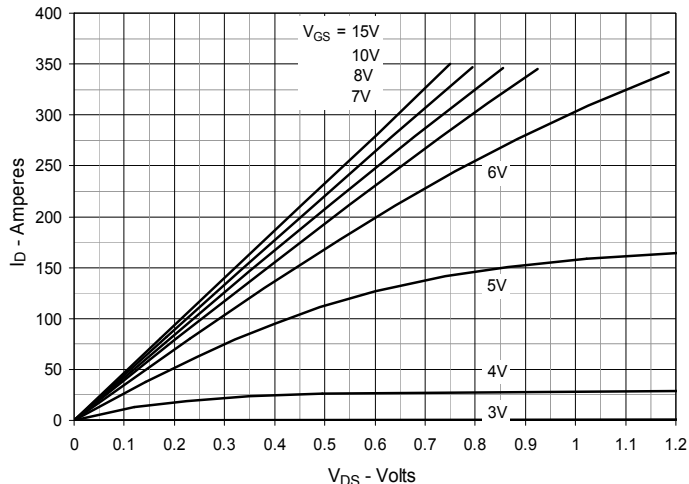


Fig. 3. Normalized $R_{DS(on)}$ vs. Junction Temperature

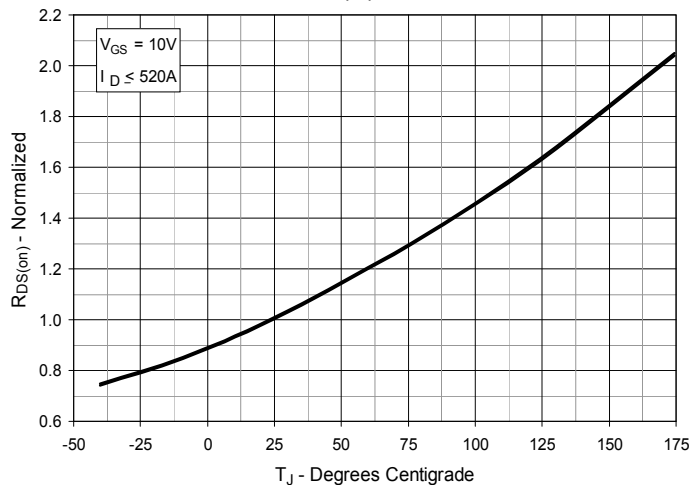


Fig. 4. Normalized $R_{DS(on)}$ vs. Drain Current

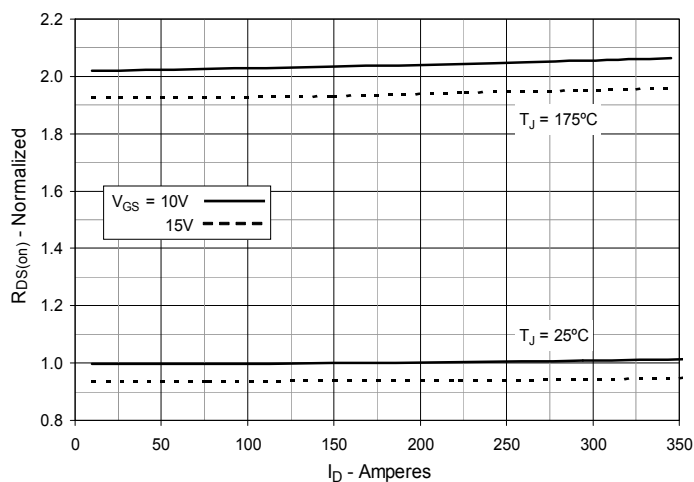


Fig. 5. Drain Current vs. Case Temperature

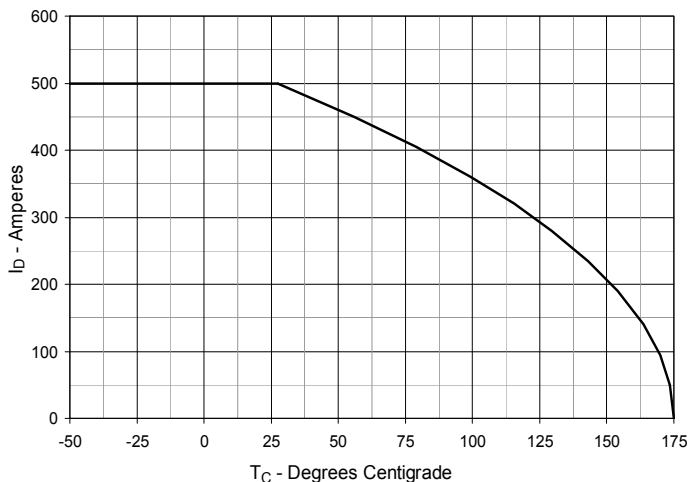


Fig. 6. Input Admittance

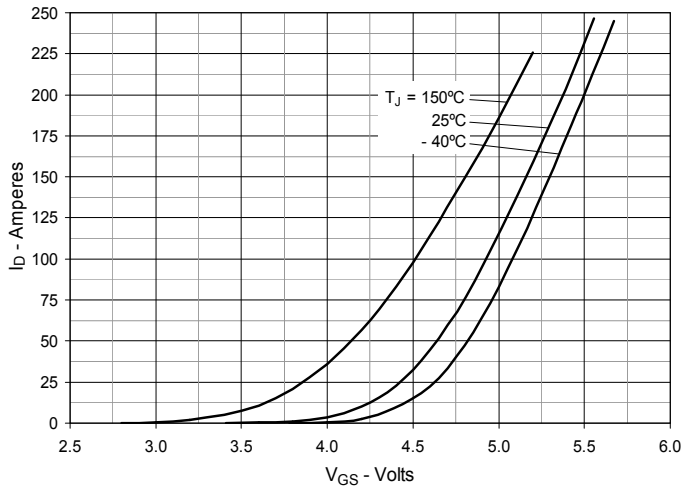


Fig. 7. Transconductance

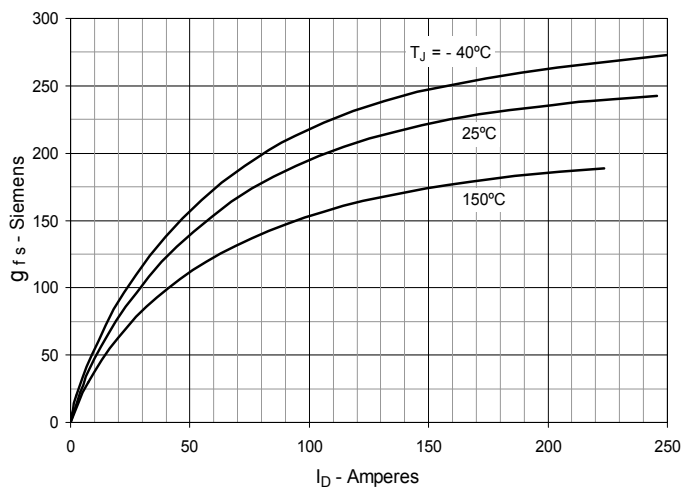


Fig. 8. Forward Voltage Drop of Intrinsic Diode

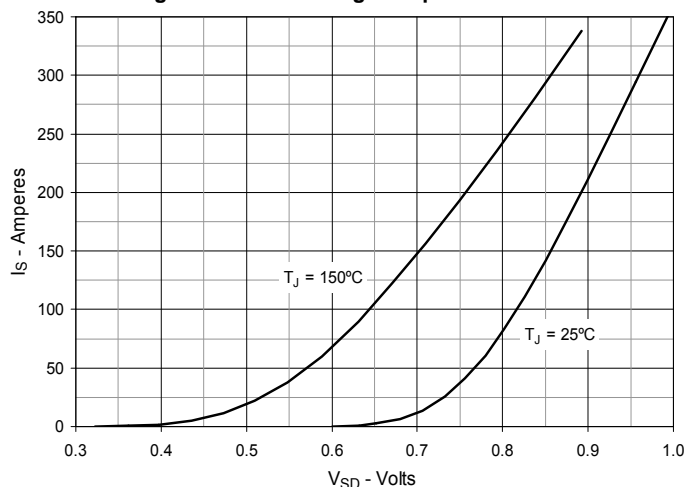


Fig. 9. Gate Charge

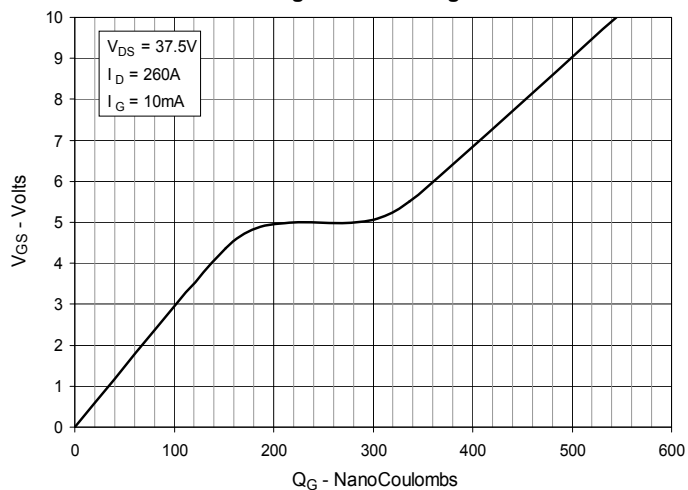


Fig. 10. Capacitance

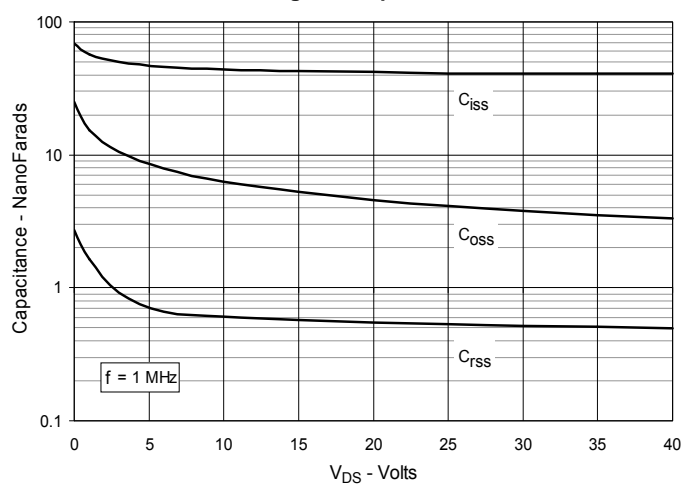


Fig. 11. Forward-Bias Safe Operating Area

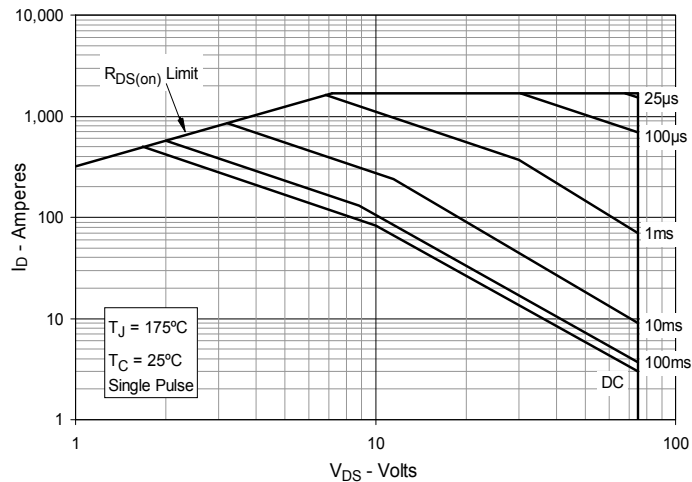


Fig. 12. Maximum Transient Thermal Impedance

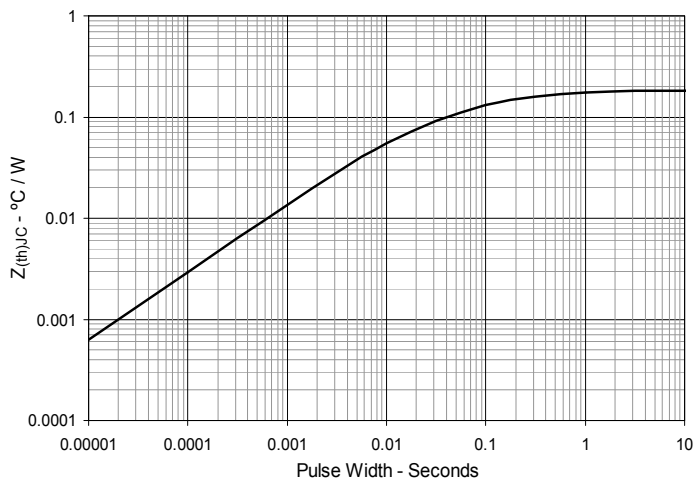


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

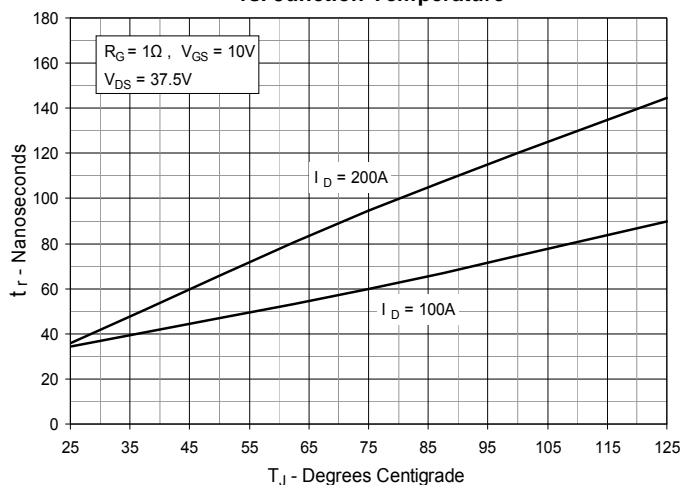


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

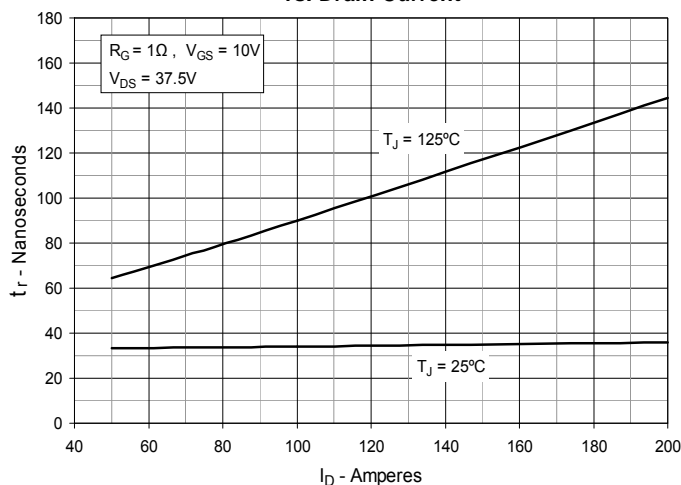


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

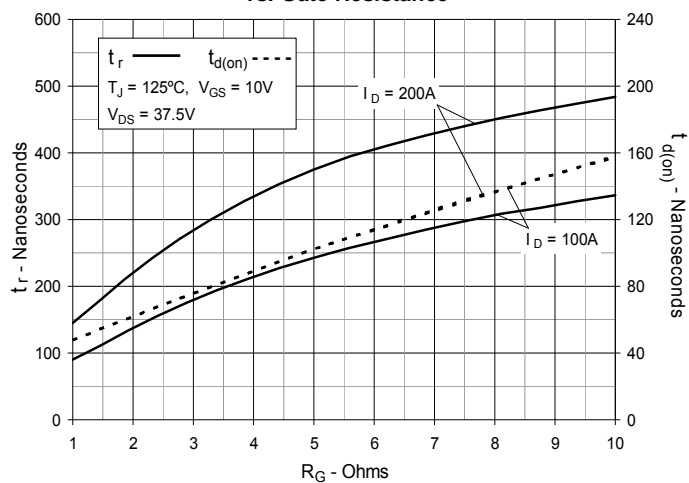


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

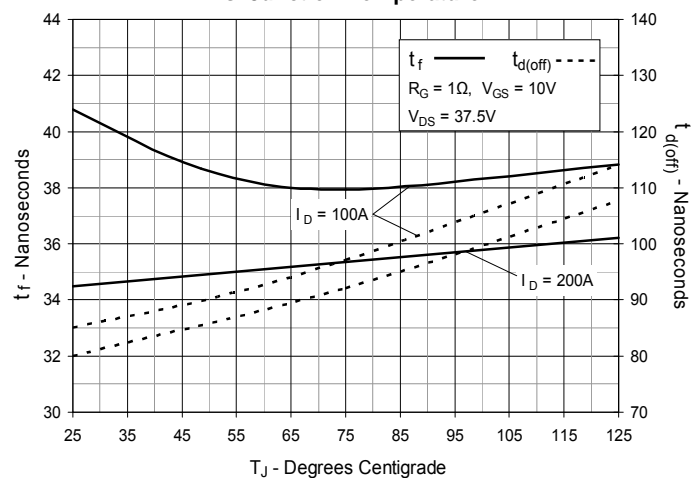


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

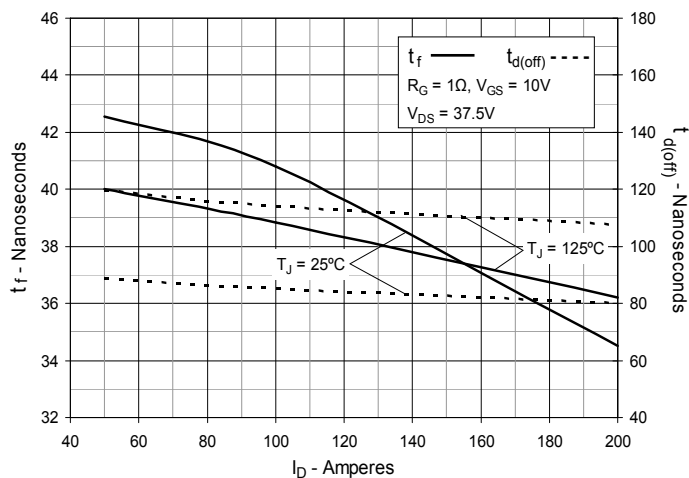
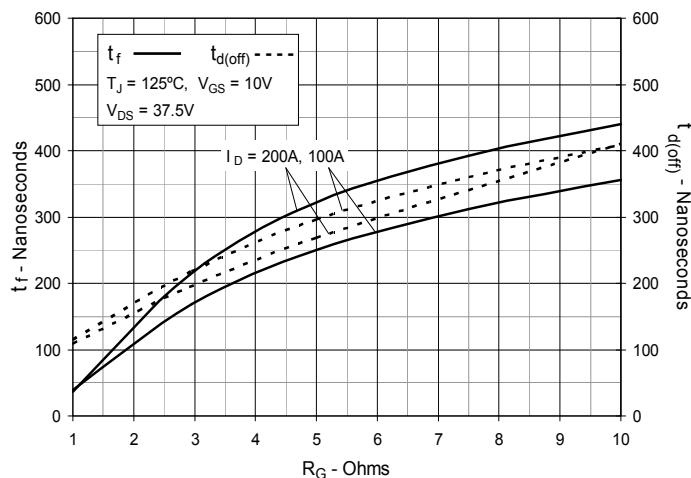
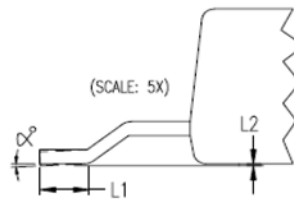
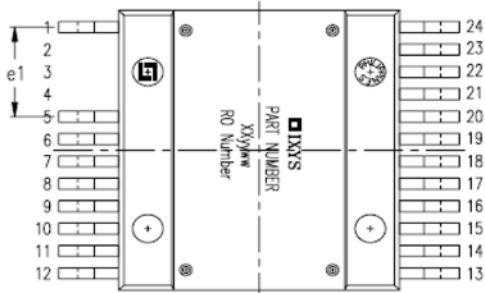
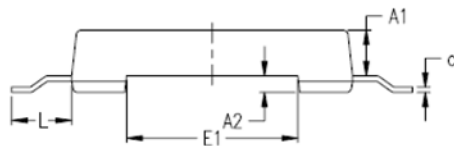
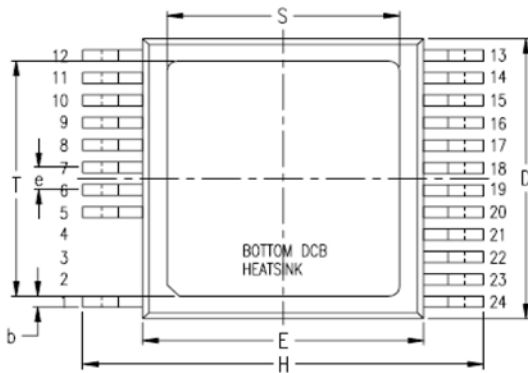


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance



Package Outline


| SYM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .209 | .224 | 5.30 | 5.70 |
| A1 | .154 | .161 | 3.90 | 4.10 |
| A2 | .055 | .063 | 1.40 | 1.60 |
| b | .035 | .045 | 0.90 | 1.15 |
| c | .018 | .026 | 0.45 | 0.65 |
| D | .976 | .994 | 24.80 | 25.25 |
| E | .898 | .915 | 22.80 | 23.25 |
| E1 | .543 | .559 | 13.80 | 14.20 |
| e | .079 BSC | | 2.00 BSC | |
| e1 | .315 BSC | | 8.00 BSC | |
| H | 1.272 | 1.311 | 32.30 | 33.30 |
| L | .181 | .209 | 4.60 | 5.30 |
| L1 | .051 | .067 | 1.30 | 1.70 |
| L2 | .000 | .006 | 0.00 | 0.15 |
| S | .736 | .760 | 18.70 | 19.30 |
| T | .815 | .839 | 20.70 | 21.30 |
| α | 0 | 4° | 0 | 4° |

PIN: 1 = Gate
5-12 = Source
13-24 = Drain