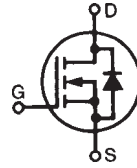


TrenchT2™ Power MOSFETs

N-Channel Enhancement Mode
Avalanche Rated

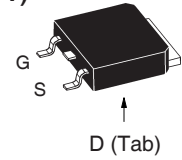
IXTY90N055T2
IXTA90N055T2
IXTP90N055T2

V_{DSS} = 55V
I_{D25} = 90A
R_{DS(on)} ≤ 8.4mΩ

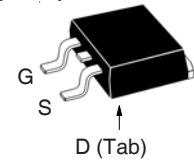


Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 175°C	55	V
V _{DGR}	T _J = 25°C to 175°C, R _{GS} = 1MΩ	55	V
V _{GSM}	Transient	± 20	V
I _{D25}	T _C = 25°C	90	A
I _{LRMS}	Lead Current Limit, RMS	75	A
I _{DM}	T _C = 25°C, Pulse Width Limited by T _{JM}	230	A
I _A	T _C = 25°C	50	A
E _{AS}	T _C = 25°C	300	mJ
P _D	T _C = 25°C	150	W
T _J		-55 ... +175	°C
T _{JM}		175	°C
T _{stg}		-55 ... +175	°C
T _L	1.6mm (0.062in.) from Case for 10s Plastic Body for 10 seconds	300 260	°C °C
M _d	Mounting Torque (TO-220)	1.13 / 10	Nm/lb.in.
Weight	TO-252	0.35	g
	TO-263	2.50	g
	TO-220	3.00	g

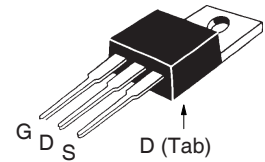
TO-252 (IXTY)



TO-263 AA (IXTA)



TO-220AB (IXTP)



G = Gate D = Drain
S = Source Tab = Drain

Features

- International Standard Package
- 175°C Operating Temperature
- Avalanche Rated
- High Current Handling Capability
- Fast Intrinsic Rectifier
- Low R_{DS(on)} and Q_G
- ROHS Compliant
- High Performance Trench

Advantages

- High Power Density
- Easy to Mount
- Space Savings
- Synchronous

Applications

- Automotive Engine Control
- Synchronous Buck Converter (for Notebook Systempower & General Purpose Point & Load.)
- DC/DC Converters
- High Current Switching Applications
- Power Train Management
- Distributed Power Architecture

Symbol	Test Conditions (T _J = 25°C Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV _{DSS}	V _{GS} = 0V, I _D = 250μA	55		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0 V
I _{GSS}	V _{GS} = ± 20V, V _{DS} = 0V			±200 nA
I _{DSS}	V _{DS} = V _{DSS} , V _{GS} = 0V T _J = 150°C			2 μA
				200 μA
R _{DS(on)}	V _{GS} = 10V, I _D = 25A, Notes 1, 2	7.0	8.4	mΩ

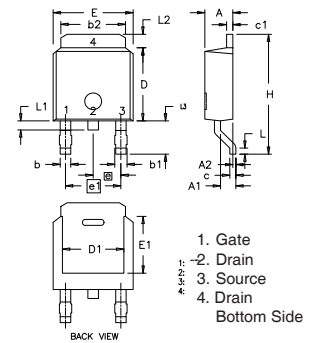
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	25	43	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		2770	pF
C_{oss}			420	pF
C_{rss}			102	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 30\text{V}$, $I_D = 25\text{A}$ $R_G = 5\Omega$ (External)		19	ns
t_r			21	ns
$t_{d(off)}$			39	ns
t_f			19	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 25\text{A}$		42	nC
Q_{gs}			14	nC
Q_{gd}			8.5	nC
R_{thJC}			1.00	$^\circ\text{C/W}$
R_{thCH}	TO-220	0.50		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			90 A
I_{SM}	Repetitive, Pulse width limited by T_{JM}			360 A
V_{SD}	$I_F = 25\text{A}$, $V_{GS} = 0\text{V}$, Note 1	0.85	1.0	V
t_{rr}	$I_F = 45\text{A}$, $V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 27\text{V}$		37	ns
I_{RM}			2.2	A
Q_{RM}			40	nC

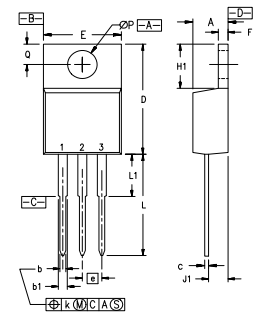
- Notes: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. On through-hole packages, $R_{DS(on)}$ Kelvin test contact location must be 5mm or less from the package body.

TO-252 AA Outline



Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

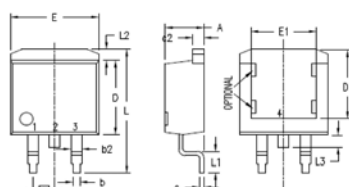
TO-220 Outline



- Pins: 1 - Gate
2 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

TO-263 Outline



- 1 = Gate
2 = Drain
3 = Source
4 = Drain
Bottom Side

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

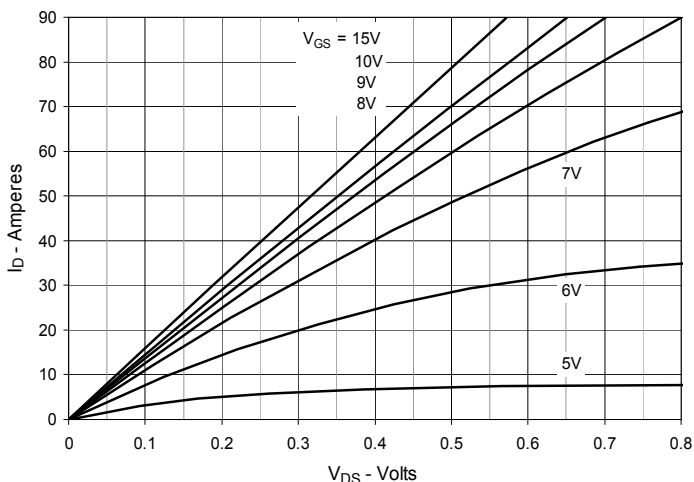


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

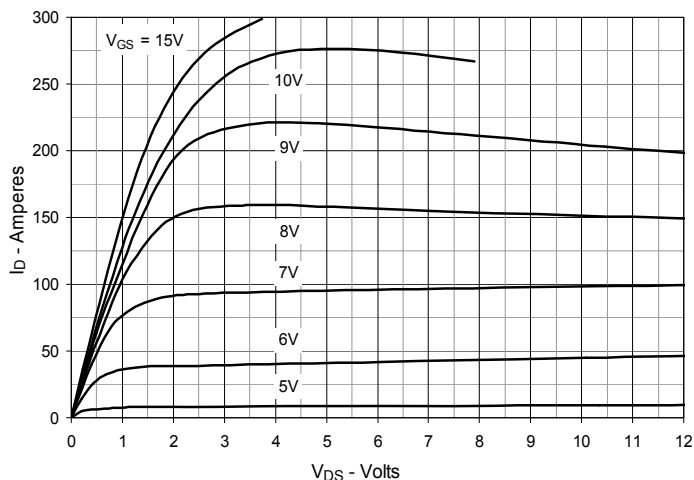


Fig. 3. Output Characteristics @ $T_J = 150^\circ\text{C}$

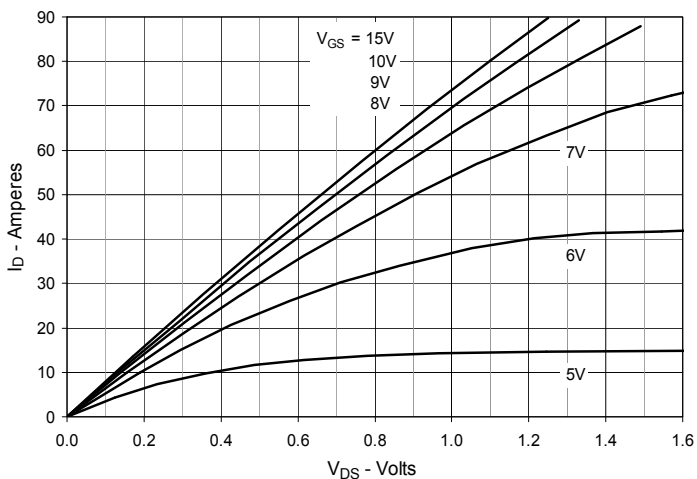


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 45\text{A}$ Value vs. Junction Temperature

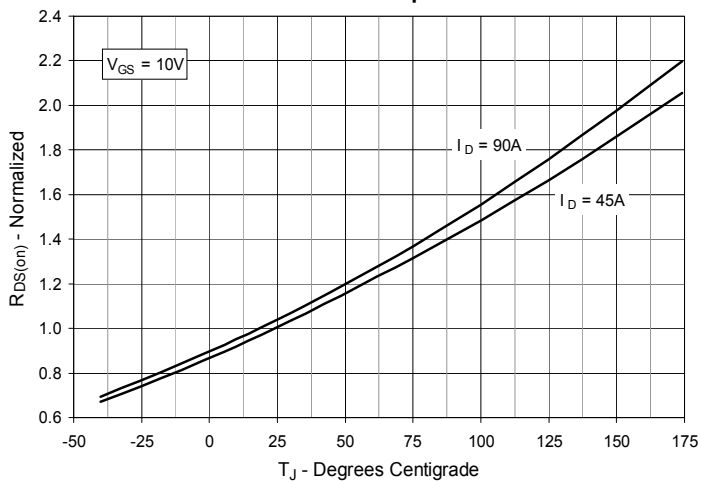


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 45\text{A}$ Value vs. Drain Current

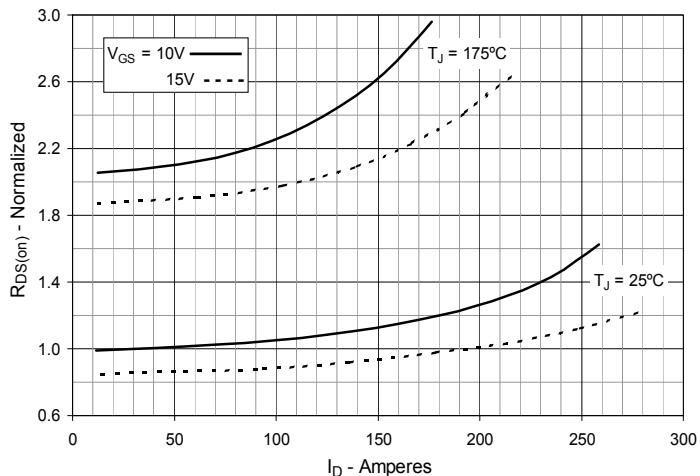


Fig. 6. Drain Current vs. Case Temperature

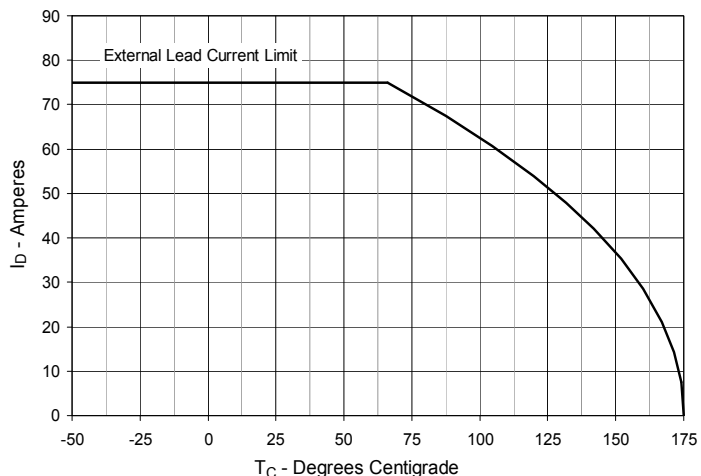


Fig. 7. Input Admittance

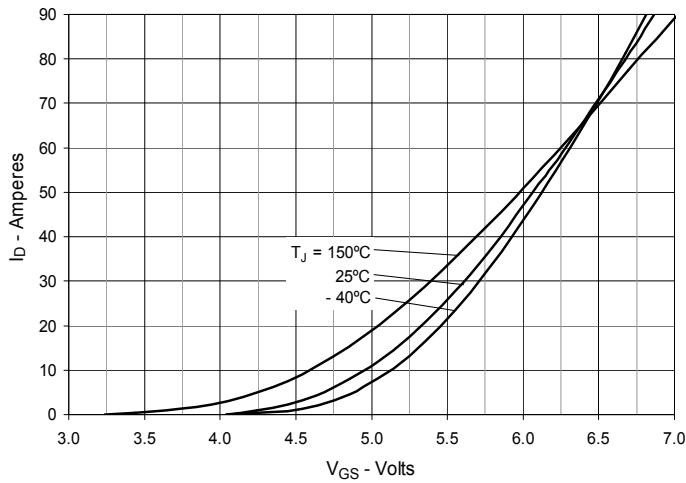


Fig. 8. Transconductance

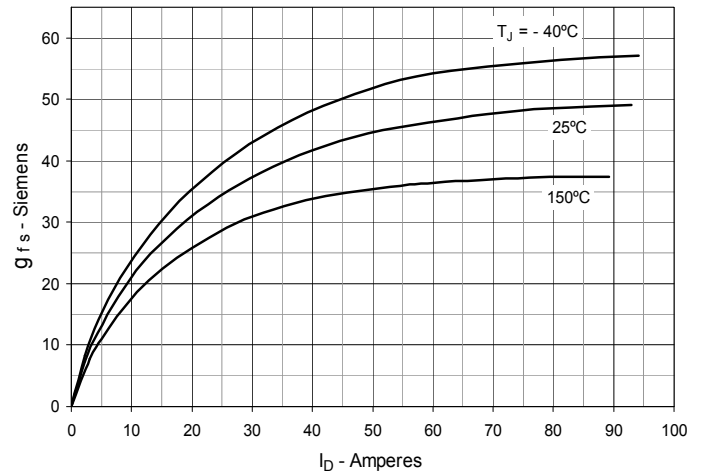


Fig. 9. Forward Voltage Drop of Intrinsic Diode

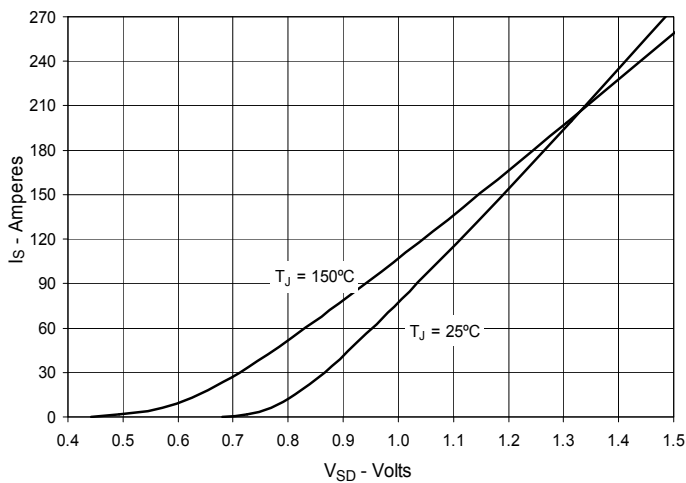


Fig. 10. Gate Charge

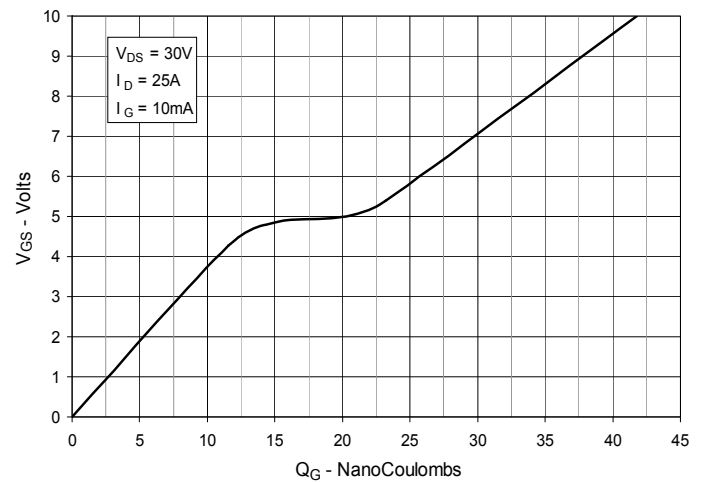


Fig. 11. Capacitance

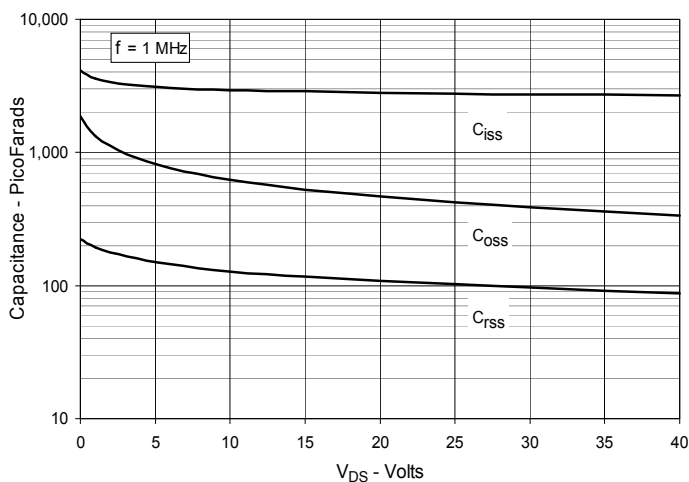
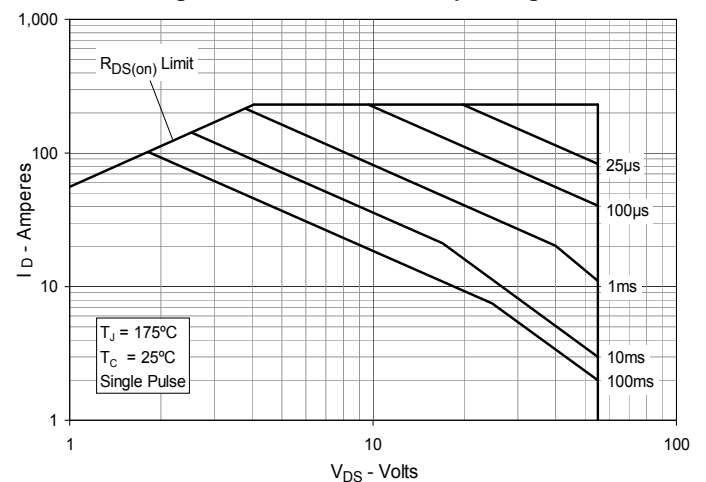


Fig. 12. Forward-Bias Safe Operating Area



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

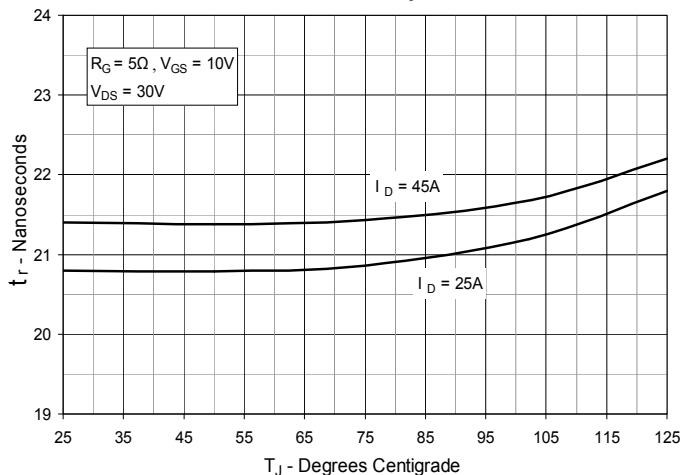


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

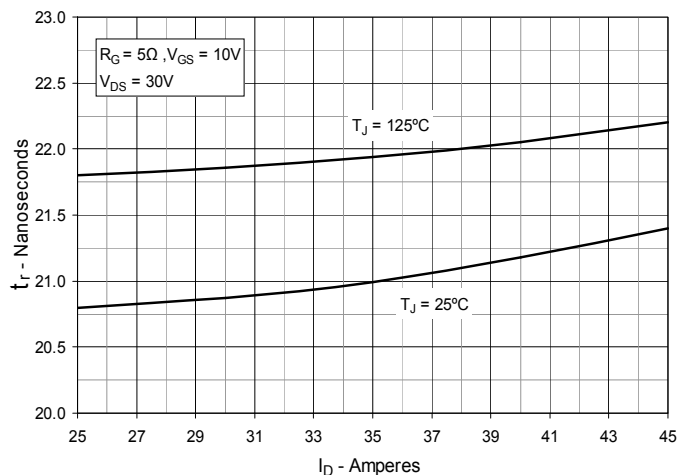


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

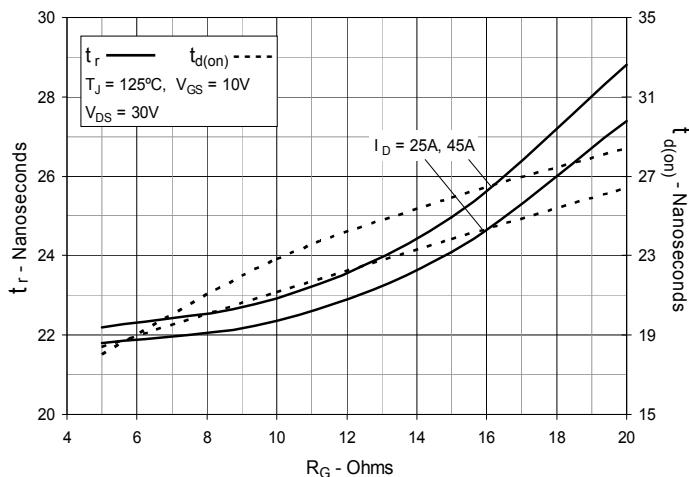


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

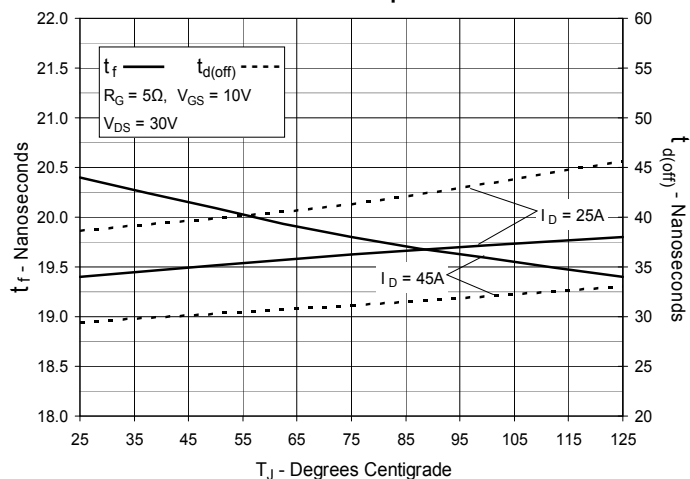


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

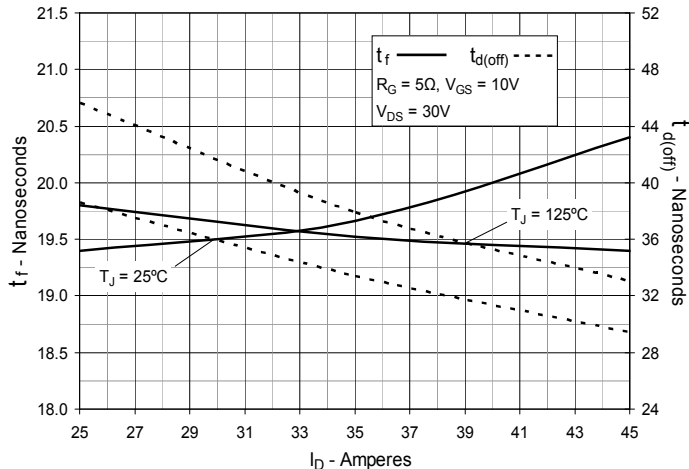


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

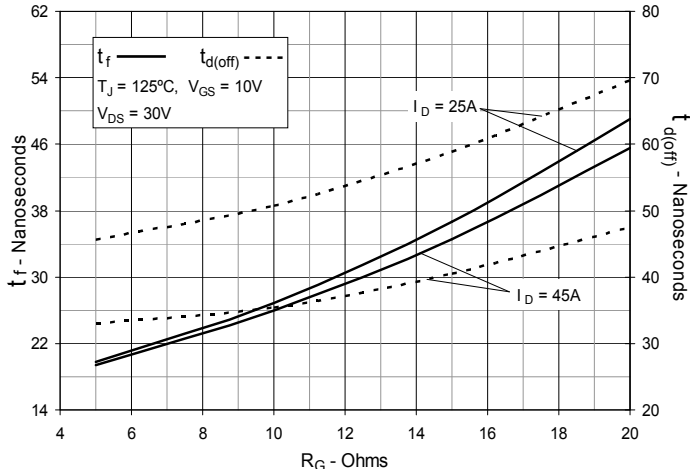


Fig. 19. Maximum Transient Thermal Impedance

