CPC3720
N-Channel Depletion-Mode FET

PRELIMINARY

BV_{DSX}/ BV_{DGX}	$R_{DS(on)}$ (max)	I_{DSS} (min)	Package
$350V_P$	22Ω	130mA	SOT-89

Features

- Offers Low $R_{DS(on)}$ at Cold Temperatures
- $R_{DS(on)}$ 22Ω max. at 25°C
- High Input Impedance
- High Breakdown Voltage: $350V_P$
- Low $V_{GS(off)}$ Voltage: -1.6 to -3.9V
- Small Package Size SOT-89

Applications

- Ignition Modules
- Normally-On Switches
- Solid State Relays
- Converters
- Telecommunications
- Power Supply

Description

The CPC3720 is an N-channel, depletion mode, field effect transistor (FET) that utilizes Clare's proprietary third-generation vertical DMOS process. The third-generation process realizes world class, high voltage MOSFET performance in an economical silicon gate process. Our vertical DMOS process yields a robust device, with high input impedance, for use in high power applications. The CPC3720 is a highly reliable FET device that has been used extensively in Clare's solid state relays for industrial and telecommunications applications.

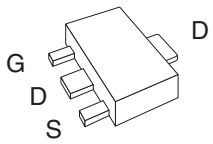
This device excels in power applications requiring low drain-source resistance, particularly in cold environments such as automotive ignition modules. The CPC3720 offers a low, 22Ω maximum, on-state resistance at 25°C.

The CPC3720 has a minimum breakdown voltage of $350V_P$, and is available in an SOT-89 package. As with all MOS devices, the FET structure prevents thermal runaway and thermal-induced secondary breakdown.

Ordering Information

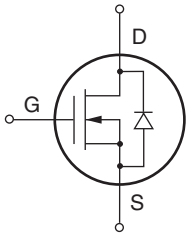
Part #	Description
CPC3720CTR	SOT-89 (1000/Reel)

Package Pinout



(SOT-89)

Circuit Symbol



Absolute Maximum Ratings @ 25°C

Parameter	Ratings	Units
Drain-to-Source Voltage	350	V_P
Gate-to-Source Voltage	±20	V_P
Total Package Dissipation	1.6 [1]	W
Operational Temperature	-55 to +125	°C
Storage Temperature	-55 to +125	°C

[1] Mounted on FR4 board 1"x1"x0.062"

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Electrical Characteristics @ 25°C (Unless Otherwise Noted)

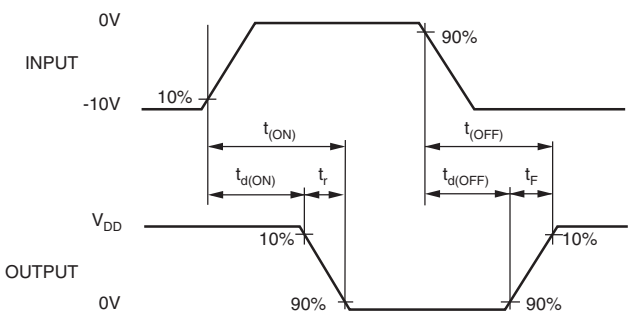
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	BV_{DSX}	V_{GS}= -5V, I_D=100µA	350	-	-	V_P
Gate-to-Source Off Voltage	$V_{GS(off)}$	V_{DS}= 10V, I_D=1mA	-1.6	-2.4	-3.9	V
Change in $V_{GS(off)}$ with Temperatures	$d_{VGS(off)}/dT$	V_{DS}= 10V, I_D=1mA	-	-	3.3	mV/°C
Gate Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	100	nA
Drain-to-Source Leakage Current	$I_{D(off)}$	V_{GS}= -5V, V_{DS}=Max Rating	-	-	1	µA
		V_{GS}= -5V, V_{DS}=280V, T_A=125°C	-	-	1	mA
Saturated Drain-to-Source Current	I_{DSS}	V_{GS}= 0V, V_{DS}=15V	130	-	-	mA
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$	V_{GS}= 0V, I_D=130mA	-	-	22	Ω
Change in $R_{DS(on)}$ with Temperatures	$dR_{DS(on)}/dT$	V_{GS}= 0V, I_D=130mA	-	-	0.9	%/°C
Forward Transconductance	G_{FS}	I_D= 100mA, V_{DS} = 10V	225	-	-	m℧
Input Capacitance	C_{ISS}	V_{GS}= -5V V_{DS}= 25V f= 1MHz	-	70	350	pF
Common Source Output Capacitance	C_{OSS}			20	60	
Reverse Transfer Capacitance	C_{RSS}			10	60	
Turn-ON Delay Time	$t_{d(on)}$	V_{DD}= 25V I_D= 150mA V_{GS}= 0V to -10V R_{GEN}= 50Ω	-	20	-	ns
Rise Time	t_r			10		
Turn-OFF Delay Time	$t_{d(off)}$			20		
Fall time	t_f			50		
Source-Drain Diode Voltage Drop	V_{SD}	V_{GS}= -5V, I_{SD}= 150mA	-	0.6	1.8	V

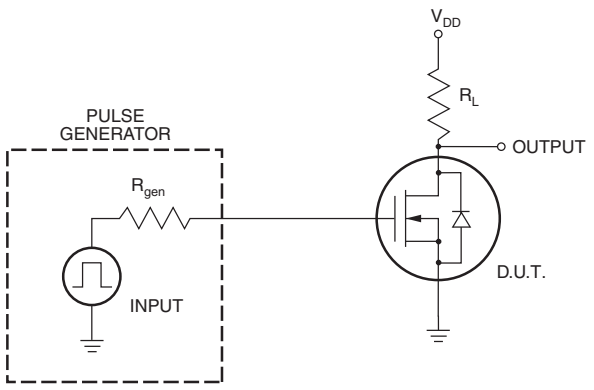
Thermal Characteristics

Package	I_D (continuous)	I_D (pulsed)	Power Dissipation @T_A=25°C	θ_{ic} °C/W	I_{DR}	I_{DRM}
SOT-89	130mA	600mA	1.6W[1]	15	130mA	600mA

[1] Mounted on FR4 board 1"x1"x0.062"

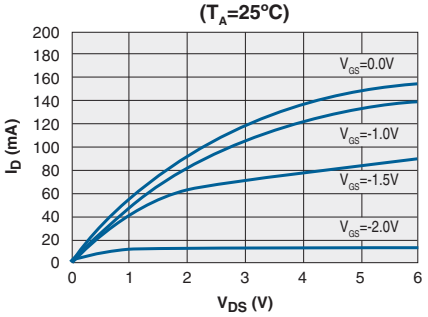
Switching Waveform & Test Circuit



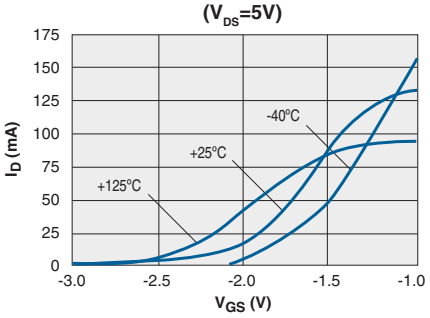


PERFORMANCE DATA*

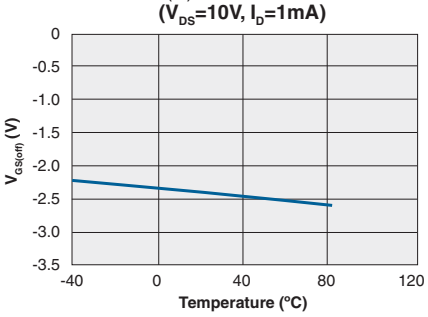
Output Characteristics
(T_A=25°C)



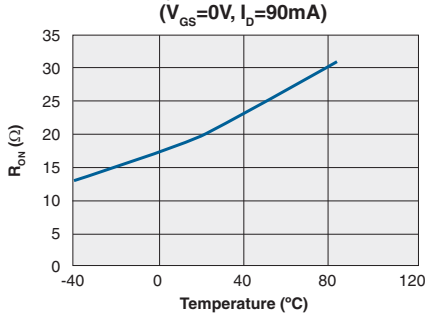
Transfer Characteristics
(V_{DS}=5V)



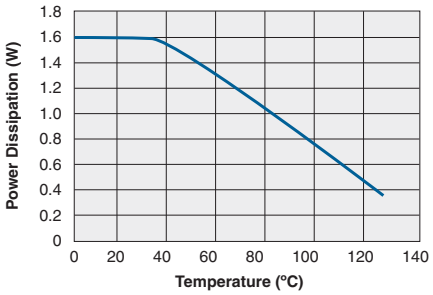
$V_{GS(off)}$ vs. Temperature
(V_{DS}=10V, I_D=1mA)



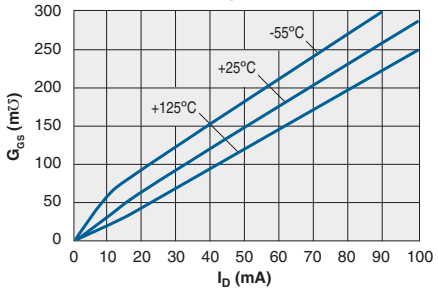
R_{ON} vs. Temperature
(V_{GS}=0V, I_D=90mA)



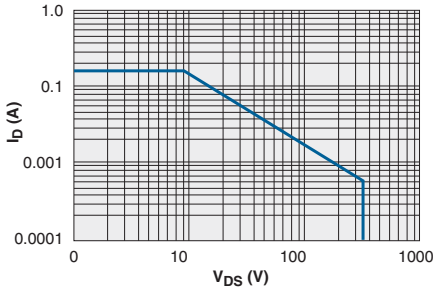
Power Dissipation vs.
Ambient Temperature



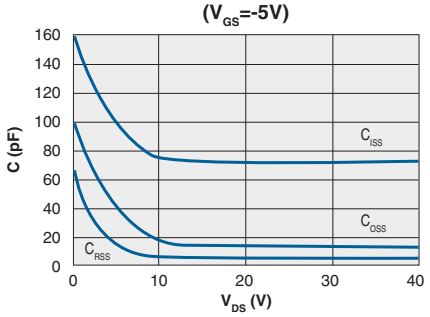
Transconductance vs. Drain Current
(V_{DS}=10V)



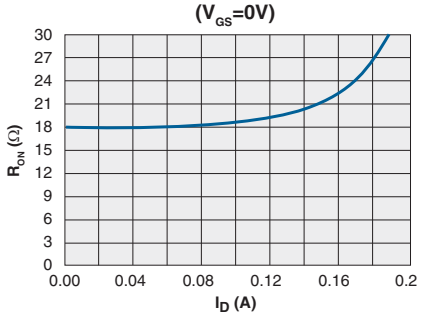
Maximum Rated Safe Operating Area
at 25°C



Capacitance vs. Drain Source Voltage
(V_{GS}=-5V)



On-Resistance vs. Drain Current
(V_{GS}=0V)



*The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

Manufacturing Information

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Clare classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC3720C	MSL 1

ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

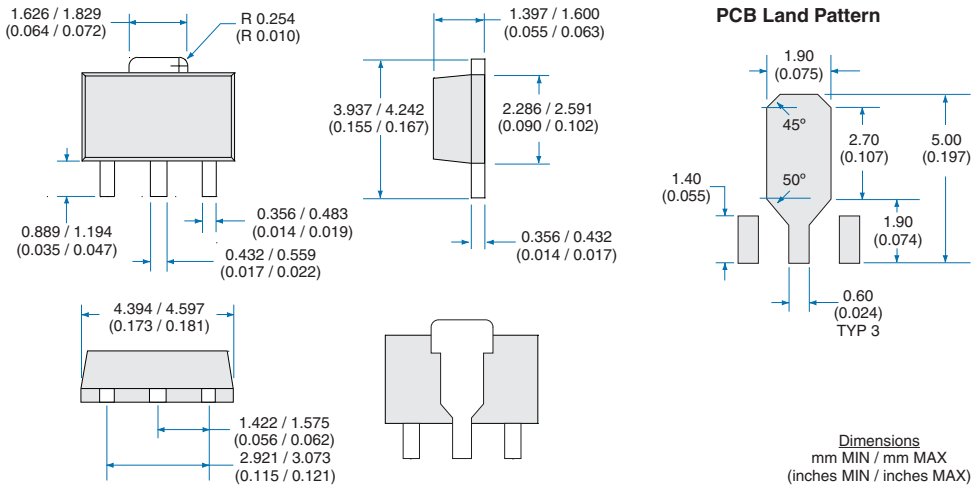
Device	Maximum Temperature x Time
CPC3720C	260°C for 30 seconds

Board Wash

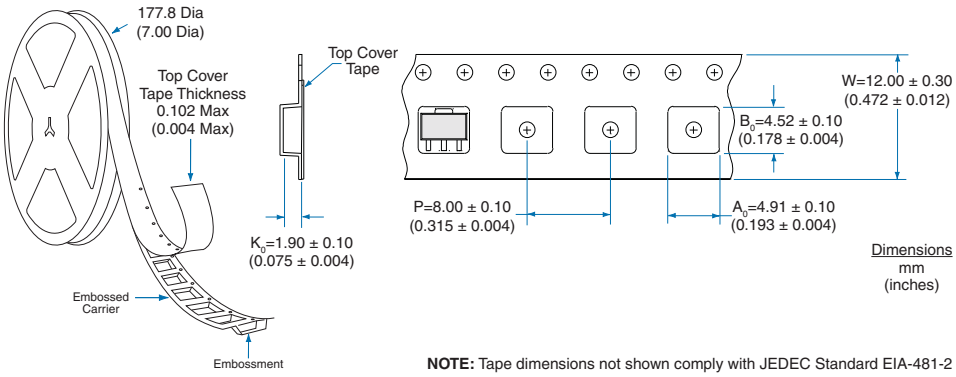
Clare recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable. Since Clare employs the use of silicone coating as an optical waveguide in many of its optically isolated products, the use of a short drying bake may be necessary if a wash is used after solder reflow processes. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

MECHANICAL DIMENSIONS

CPC3720C



CPC3720C Tape & Reel



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

For additional information please visit our website at: www.clare.com

Specification: DS-CPC3720-R00B

5/24/2011