

$BV_{DSX}/$ BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)	Package
250V	4Ω	360mA	SOT-89

Features

- Depletion mode device offers low $R_{DS(ON)}$ at cold temperatures
- Low on resistance 4 ohms max. at 25°C
- High input impedance
- High breakdown voltage 250V
- Low $V_{GS(off)}$ voltage -1.6 to -3.9V
- Small package size SOT89

Applications

- Ignition Modules
- Normally-on Switches
- Solid State Relays
- Converters
- Telecommunications
- Power Supply

Description

The CPC3703 is an N-channel, depletion mode, field effect transistor (FET) that utilizes Clare's proprietary third-generation vertical DMOS process. The third-generation process realizes world class, high voltage MOSFET performance in an economical silicon gate process. Our vertical DMOS process yields a robust device, with high input impedance, for use in high-power applications. The CPC3703 is a highly reliable FET device that has been used extensively in Clare's Solid State Relays for industrial and telecommunications applications.

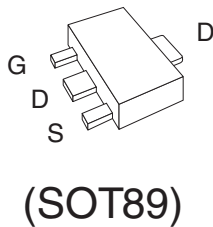
This device excels in power applications that require low drain-source resistance, particularly in cold environments such as automotive ignition modules. The CPC3703 offers a low, 4Ω maximum, on-state resistance at 25°C.

The CPC3703 has a minimum breakdown voltage of 250V, and is available in an SOT89 package. As with all MOS devices, the FET structure prevents thermal runaway and thermal-induced secondary breakdown.

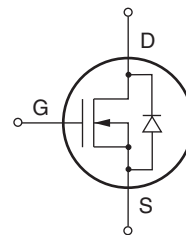
Ordering Information

Part #	Description
CPC3703C	SOT89 (100/Tube)
CPC3703CTR	SOT89 (2000/Reel)

Package Pinout



Circuit Symbol



Absolute Maximum Ratings

Parameter	Ratings	Units
Drain-to-Source Voltage	250	V
Gate-to-Source Voltage	±20	V
Total Package Dissipation ¹	1.6	W
Operational Temperature	-55 to +125	°C
Storage Temperature	-55 to +125	°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

¹ Mounted on 1"x1" FR4 board.

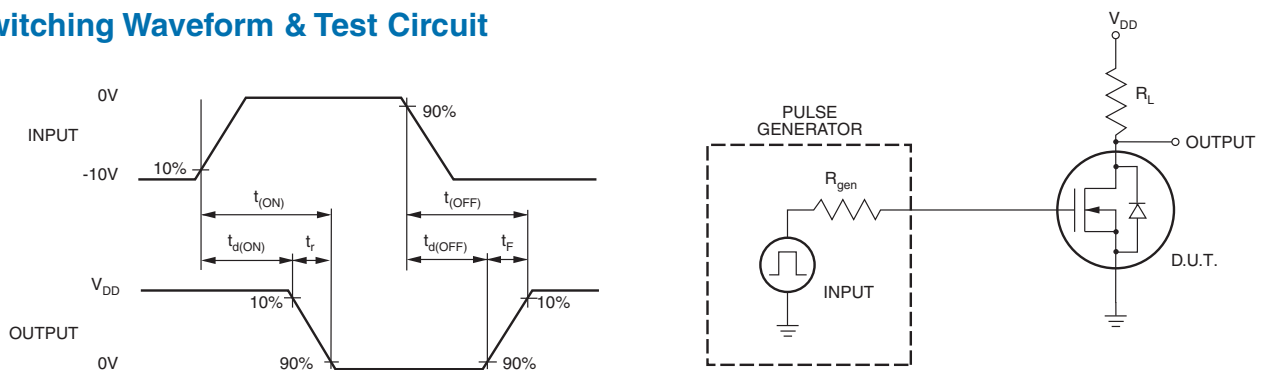
Thermal Characteristics

Package	I _D (continuous)	I _D (pulsed)	Power Dissipation @T _A =25°C	θ _{jc} °C/W	I _{DR}	I _{DRM}
SOT-89	360mA	600mA	1.6W	15	360mA	600mA

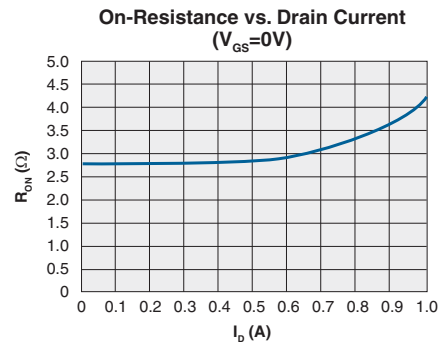
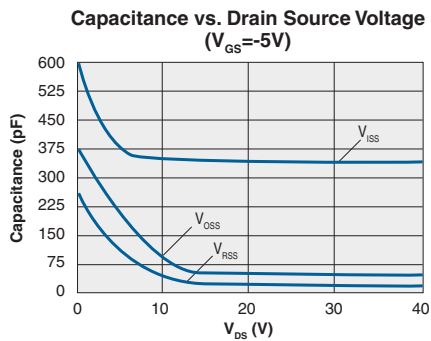
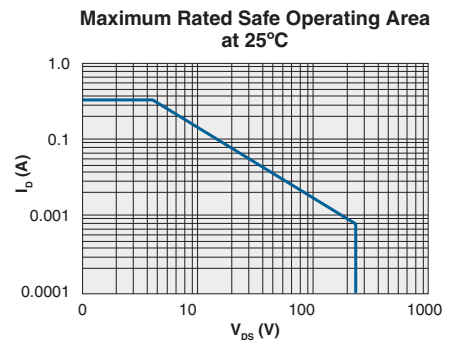
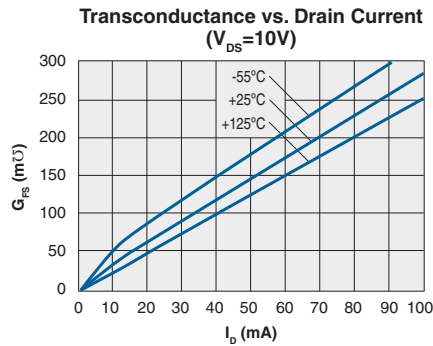
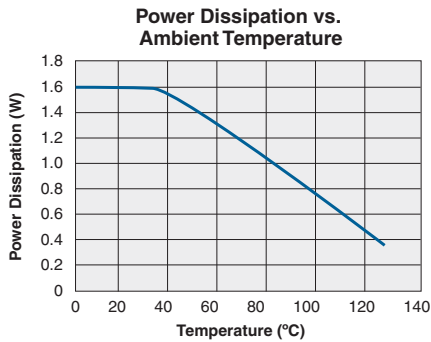
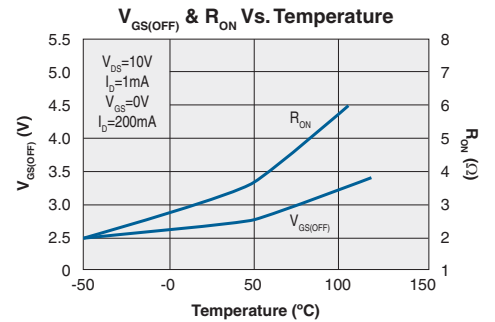
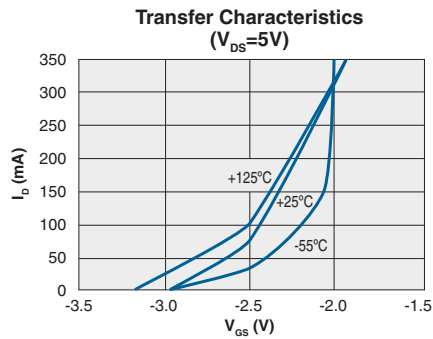
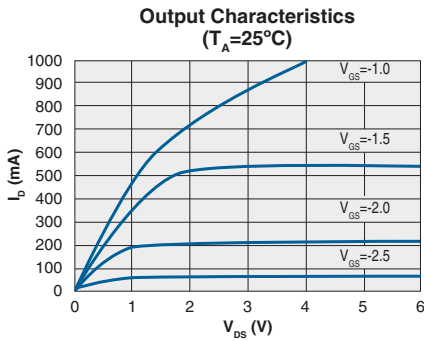
Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	BV _{DSX}	V _{GS} = -5V, I _D =100µA	250	-	-	V
Gate-to-Source Off Voltage	V _{GS(off)}	V _{DS} = 15V, I _D =1mA	-1.6	-	-3.9	V
Change in V _{GS(off)} with Temperature	dV _{GS(off)} /dT	V _{DS} = 15V, I _D =1mA	-	-	4.5	mV/°C
Gate Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	100	nA
Drain-to-Source Leakage Current	I _{D(off)}	V _{GS} = -5V, V _{DS} =Max Rating	-	-	1	µA
		V _{GS} = -5V, V _{DS} =200V, T _A =125°C	-	-	1	mA
Saturated Drain-to-Source Current	I _{DSS}	V _{GS} = 0V, V _{DS} =15V	300	-	-	mA
Static Drain-to-Source On-State Resistance	R _{DS(on)}	V _{GS} = 0V, I _D =200mA	-	-	4	Ω
Change in R _{DS(on)} with Temperature	dR _{DS(on)} /dT		-	-	1.1	%/°C
Forward Transconductance	G _{FS}	I _D = 100mA, V _{DS} = 10V	225	-	-	mS
Input Capacitance	C _{ISS}	V _{GS} = -5V	-	327	350	pF
Common Source Output Capacitance	C _{OSS}	V _{DS} = 25V	-	51	65	
Reverse Transfer Capacitance	C _{RSS}	f= 1MHz	-	27	35	
Turn-ON Delay Time	t _{d(on)}	V _{DD} = 25V I _D = 150mA V _{GS} = 0V to -10V R _{GEN} = 50Ω	-	23	35	ns
Rise Time	t _r		-	8	20	
Turn-OFF Delay Time	t _{d(off)}		-	17	25	
Fall Time	t _f		-	70	80	
Source-Drain Diode Voltage Drop	V _{SD}	V _{GS} = -5V, I _{SD} =150mA	-	0.6	1.8	V

Switching Waveform & Test Circuit



PERFORMANCE DATA*



*The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

Manufacturing Information

Soldering

For proper assembly, the component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

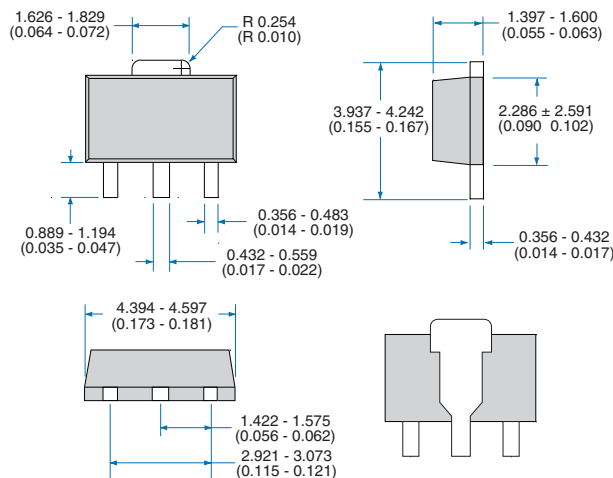
Washing

Clare does not recommend ultrasonic cleaning or the use of chlorinated solvents.

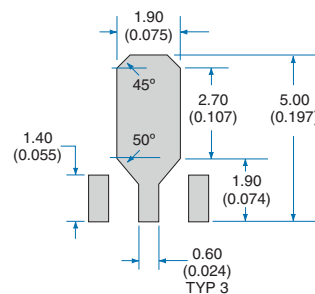


MECHANICAL DIMENSIONS

SOT89 Package

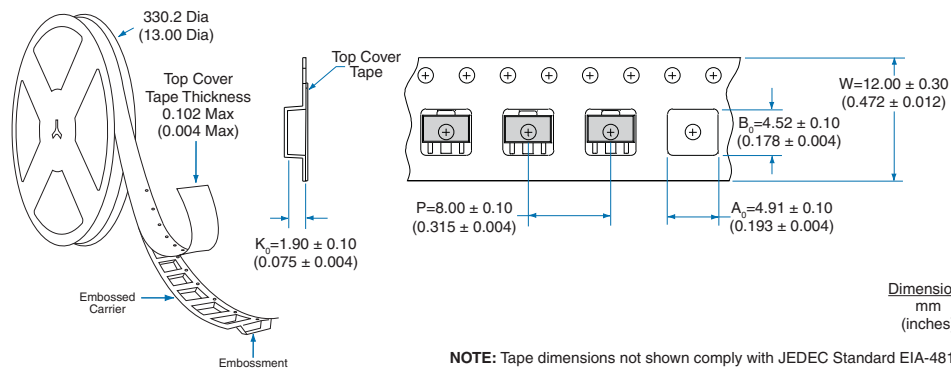


Recommended PCB Land Pattern



Dimensions
mm
(inches)

Tape and Reel Packaging for SOT89 Package



Dimensions
mm
(inches)

NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

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