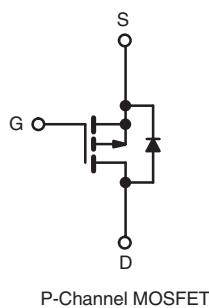
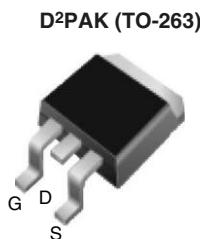


## Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	- 100
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = - 10 V      0.30
Q <sub>g</sub> (Max.) (nC)	38
Q <sub>gs</sub> (nC)	6.8
Q <sub>gd</sub> (nC)	21
Configuration	Single



### FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- 175 °C Operating Temperature
- Fast Switching
- Lead (Pb)-free Available


**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free	IRF9530SPbF	IRF9530STRLPbFa	IRF9530STRRPbFa
	SiHF9530S-E3	SiHF9530STL-E3a	SiHF9530STR-E3a
SnPb	IRF9530S	IRF9530STRLa	IRF9530STRRa
	SiHF9530S	SiHF9530STLa	SiHF9530STRa

#### Note

a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS T<sub>C</sub> = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	- 100	
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current	I <sub>D</sub>	- 12	
		- 8.2	A
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	- 48	
Linear Derating Factor		0.59	
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.025	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	400	mJ
Avalanche Current <sup>a</sup>	I <sub>AR</sub>	- 12	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	8.8	mJ
Maximum Power Dissipation	P <sub>D</sub>	88	
Maximum Power Dissipation (PCB Mount) <sup>e</sup>		3.7	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	- 5.5	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = - 25 V, starting T<sub>J</sub> = 25 °C, L = 4.2 mH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = - 12 A (see fig. 12).
- I<sub>SD</sub> ≤ - 12 A, dI/dt ≤ 140 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 175 °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

**Note**

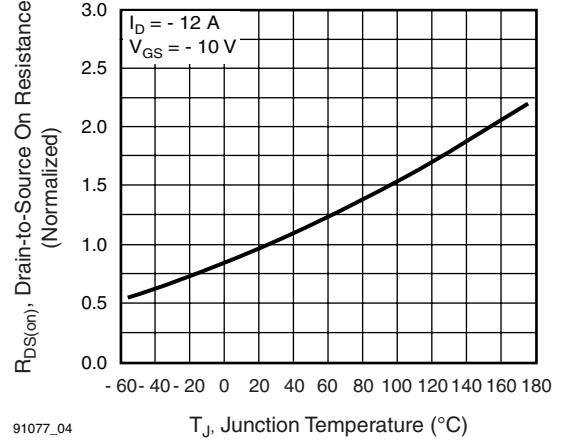
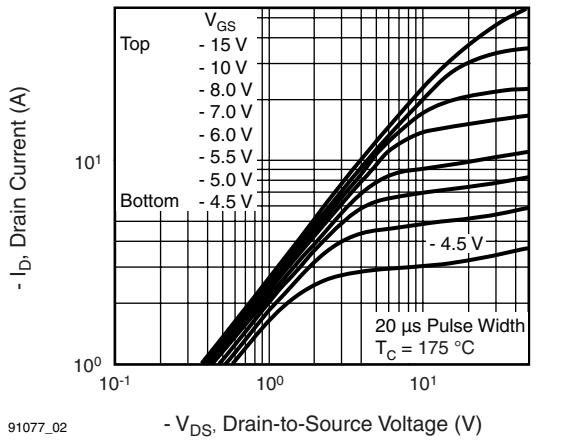
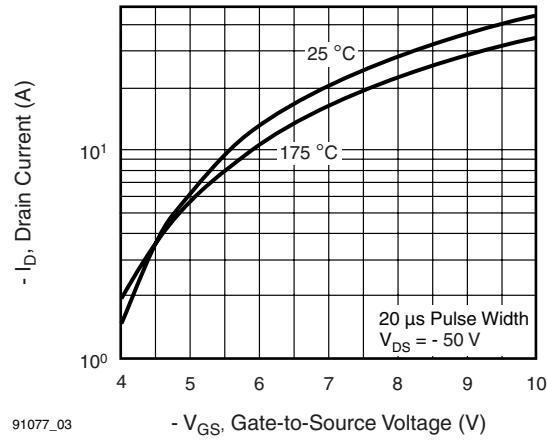
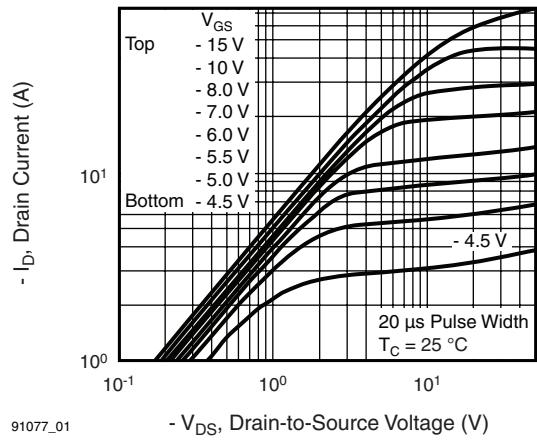
- a. When mounted on 1" square PCB (FR-4 or G-10 material).

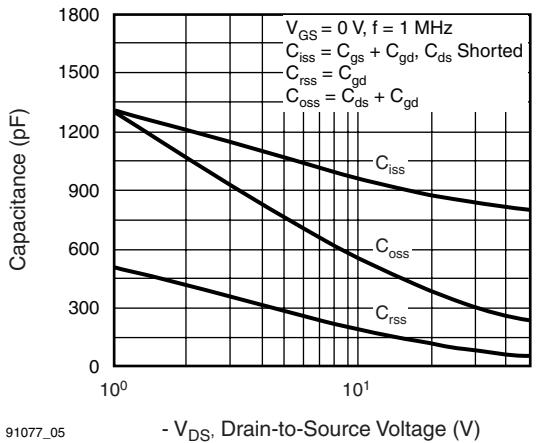
**SPECIFICATIONS  $T_J = 25 \text{ }^{\circ}\text{C}$ , unless otherwise noted**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = - 250 \mu\text{A}$		- 100	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$ , $I_D = - 1 \text{ mA}$		-	- 0.10	-	$\text{V}/\text{ }^{\circ}\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = - 250 \mu\text{A}$		- 2.0	-	- 4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = - 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	- 100	$\mu\text{A}$	
		$V_{DS} = - 80 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 150 \text{ }^{\circ}\text{C}$		-	-	- 500		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = - 10 \text{ V}$	$I_D = - 7.2 \text{ A}^b$	-	-	0.30	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = - 50 \text{ V}$ , $I_D = - 7.2 \text{ A}^b$		3.7	-	-	S	
<b>Dynamic</b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = - 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	860	-	pF	
Output Capacitance	$C_{oss}$			-	340	-		
Reverse Transfer Capacitance	$C_{rss}$			-	93	-		
Total Gate Charge	$Q_g$	$V_{GS} = - 10 \text{ V}$	$I_D = - 12 \text{ A}$ , $V_{DS} = - 80 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	38	nC	
Gate-Source Charge	$Q_{gs}$			-	-	6.8		
Gate-Drain Charge	$Q_{gd}$			-	-	21		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = - 50 \text{ V}$ , $I_D = - 12 \text{ A}$ , $R_G = 12 \Omega$ , $R_D = 3.9 \Omega$ , see fig. 10 <sup>b</sup>		-	12	-	ns	
Rise Time	$t_r$			-	52	-		
Turn-Off Delay Time	$t_{d(off)}$			-	31	-		
Fall Time	$t_f$			-	39	-		
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	$L_S$			-	7.5	-		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 12	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	- 48		
Body Diode Voltage	$V_{SD}$	$T_J = 25 \text{ }^{\circ}\text{C}$ , $I_S = - 12 \text{ A}$ , $V_{GS} = 0 \text{ V}^b$		-	-	- 6.3	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25 \text{ }^{\circ}\text{C}$ , $I_F = - 12 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	120	240	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.46	0.92	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )						

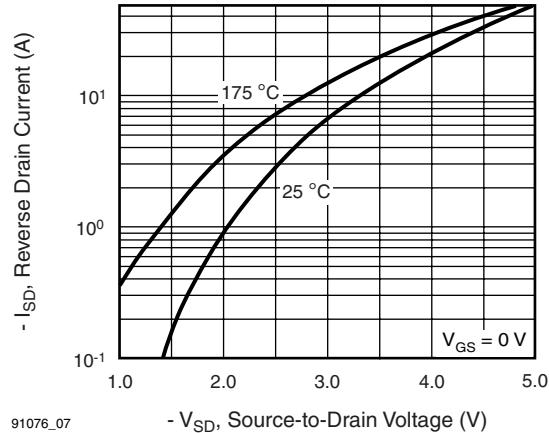
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2 \%$ .

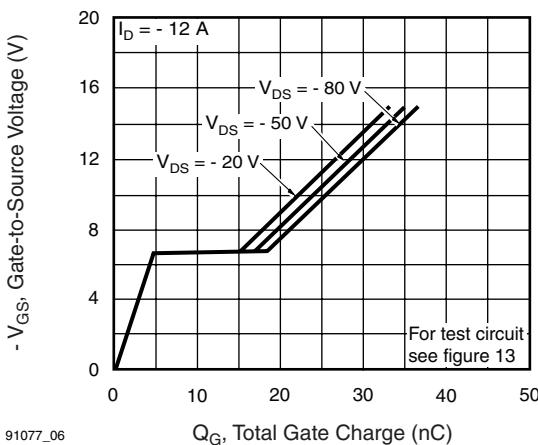
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted




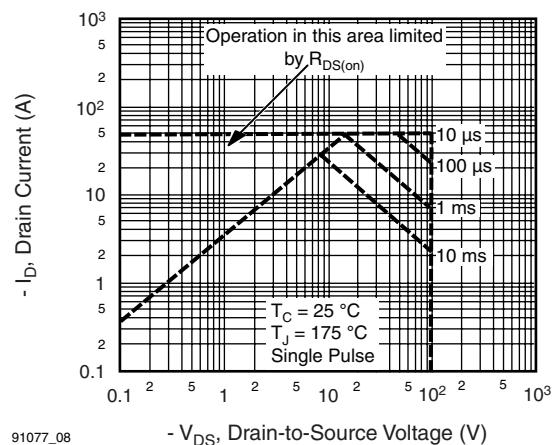
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



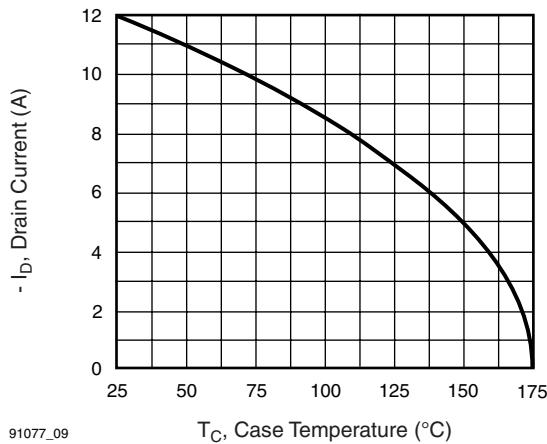
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



**Fig. 8 - Maximum Safe Operating Area**



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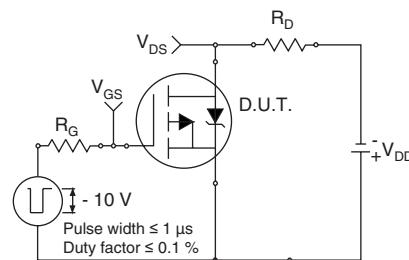


Fig. 10a - Switching Time Test Circuit

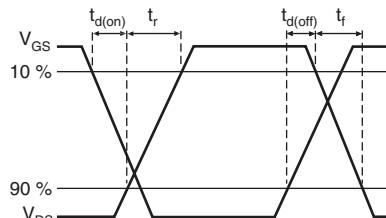
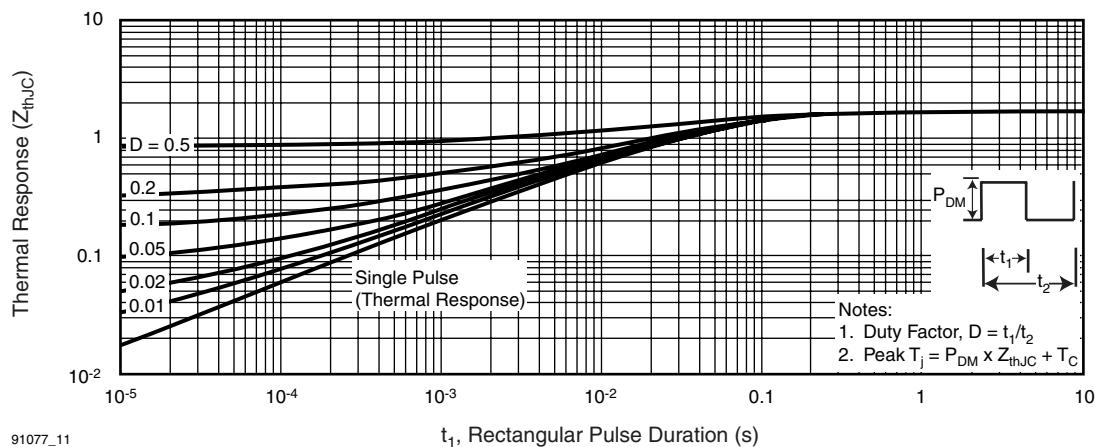


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

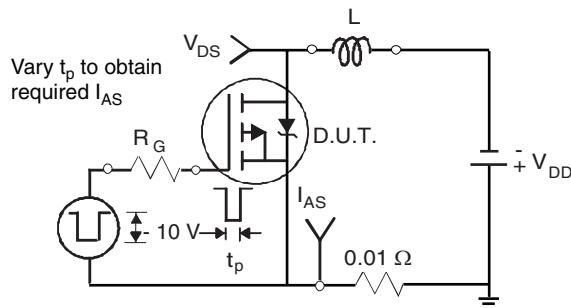


Fig. 12a - Unclamped Inductive Test Circuit

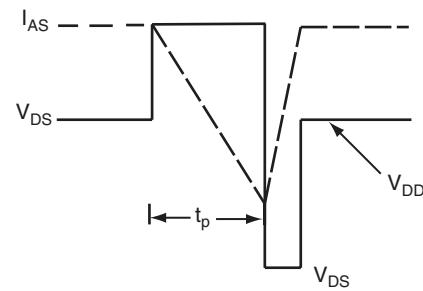


Fig. 12b - Unclamped Inductive Waveforms

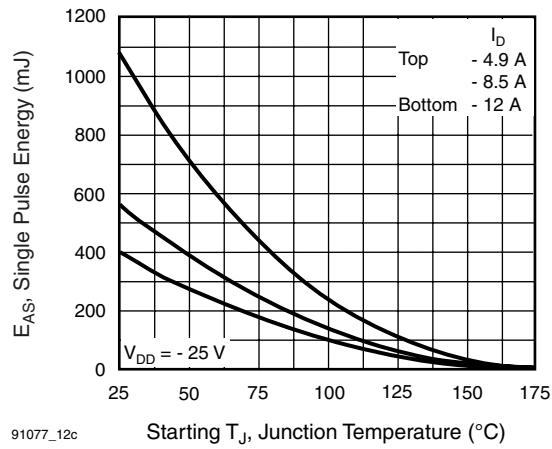


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

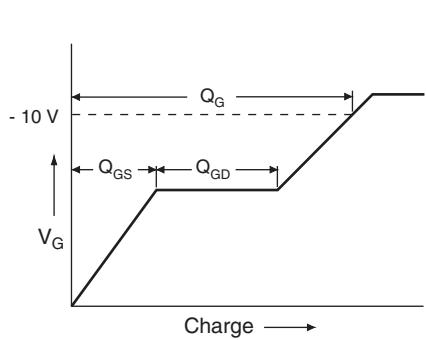


Fig. 13a - Basic Gate Charge Waveform

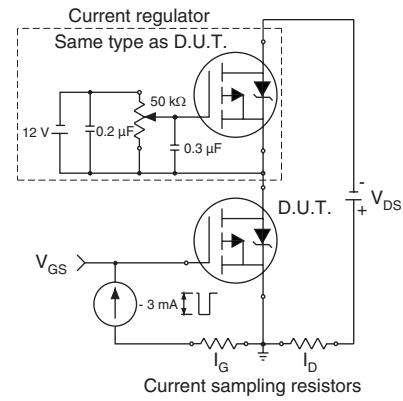
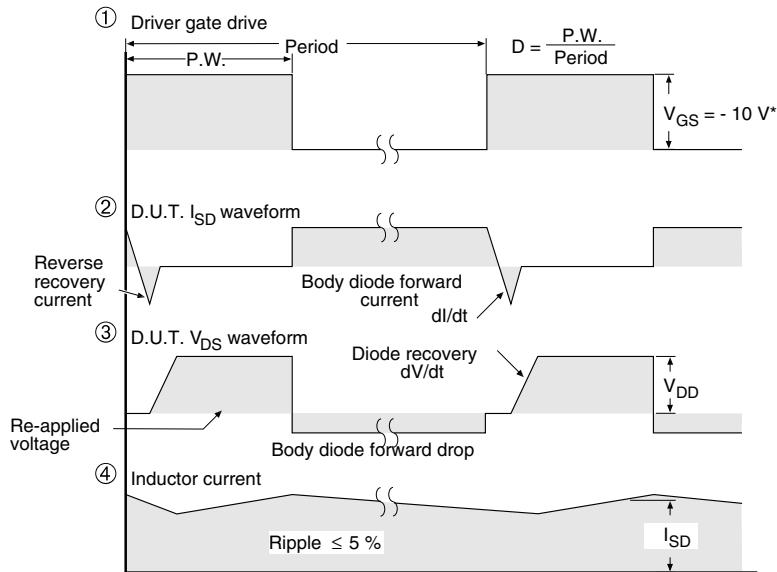
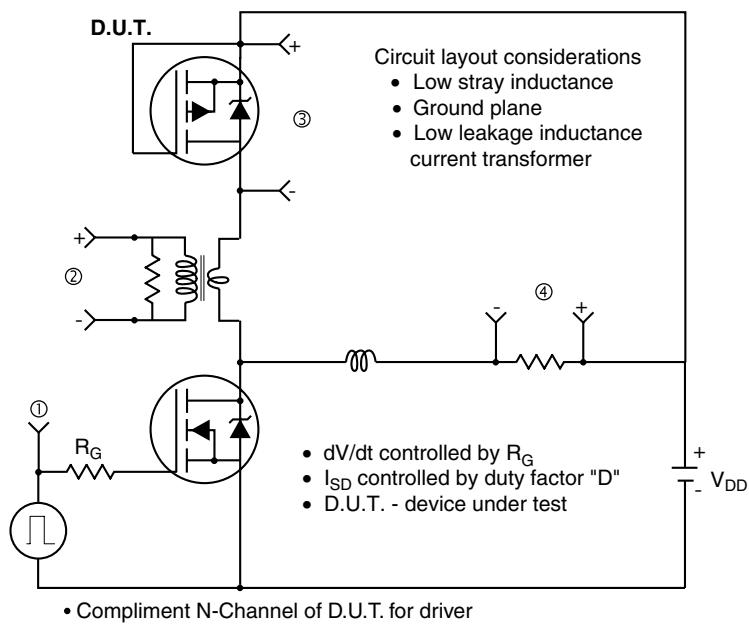


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = -5 \text{ V}$  for logic level and  $-3 \text{ V}$  drive devices

**Fig. 14 - For P-Channel**

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