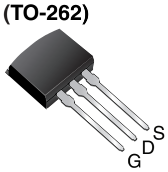
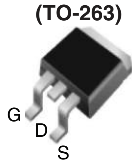
Power MOSFET

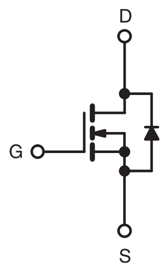
PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Max.) (Ω)	V_{GS} = 10 V	1.40
Q_g (Max.) (nC)	24	
Q_{gs} (nC)	6.3	
Q_{gd} (nC)	11	
Configuration	Single	

I²PAK (TO-262)



D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} specified
- Lead (Pb)-free Available

Available
RoHS*
COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half Bridge and Full Bridge

ORDERING INFORMATION			
Package	D²PAK (TO-263)	D²PAK (TO-263)	I²PAK (TO-262)
Lead (Pb)-free	IRF830ASPbF	IRF830ASTRLPbF[a]	IRF830ALPbF
	SiHF830AS-E3	SiHF830ASTL-E3[a]	SiHF830AL-E3
SnPb	IRF830AS	IRF830ASTRL[a]	IRF830AL
	SiHF830AS	SiHF830ASTL[a]	SiHF830AL

Note
a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	5.0	A
		T_C = 100 °C		3.2	
Pulsed Drain Current[a, e]			I_{DM}	20	
Linear Derating Factor				0.59	W/°C
Single Pulse Avalanche Energy[b, e]			E_{AS}	230	mJ
Avalanche Current[a]			I_{AR}	5.0	A
Repetiitive Avalanche Energy[a]			E_{AR}	7.4	mJ
Maximum Power Dissipation	T_A = 25 °C		P_D	3.1	W
	T_C = 25 °C			74	
Peak Diode Recovery dV/dt[c, e]			dV/dt	5.3	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

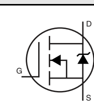
Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 18 mH, R_G = 25 Ω, I_{AS} = 5.0 A (see fig. 12).
c. $I_{SD} \le 5.0$ A, dI/dt ≤ 370 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
d. 1.6 mm from case.
e. Uses SiHF830A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB Mounted, steady-state)[a]	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA[d]	-	0.60	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 3.0 A[b]	-	-	1.4	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3.0 A[d]	2.8	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5[d]	-	620	-	pF
Output Capacitance	C_{oss}		-	93	-	
Reverse Transfer Capacitance	C_{rss}		-	4.3	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V; V_{DS} = 1.0 V, f = 1.0 MHz	-	886	-	
		V_{GS} = 0 V; V_{DS} = 400 V, f = 1.0 MHz	-	27	-	
Effective Output Capacitance	C_{oss} eff.	V_{GS} = 0 V; V_{DS} = 0 V to 400 V[c, d]	-	39	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 5.0 A, V_{DS} = 400 V, see fig. 6 and 13[b, d]	-	-	24	nC
Gate-Source Charge	Q_{gs}		-	-	6.3	
Gate-Drain Charge	Q_{gd}		-	-	11	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 5.0 A, R_G = 14 Ω, R_D = 49 Ω, see fig. 10[b, d]	-	10	-	ns
Rise Time	t_r		-	21	-	
Turn-Off Delay Time	$t_{d(off)}$		-	21	-	
Fall Time	t_f		-	15	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.0	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	20	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 5.0 A, V_{GS} = 0 V[b]	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 5.0 A, dI/dt = 100 A/µs[b, d]	-	430	650	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.0	3.0	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}.

d. Uses SiHF830A data and test conditions.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

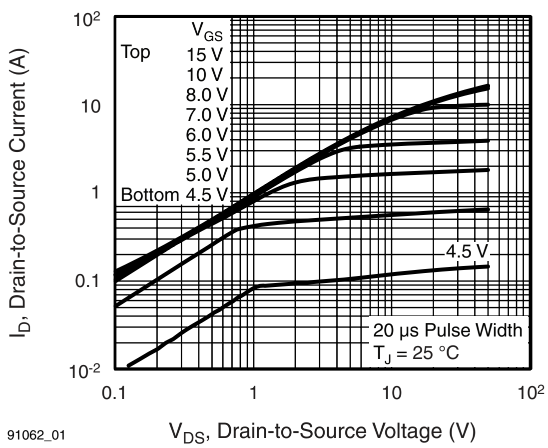


Fig. 1 - Typical Output Characteristics

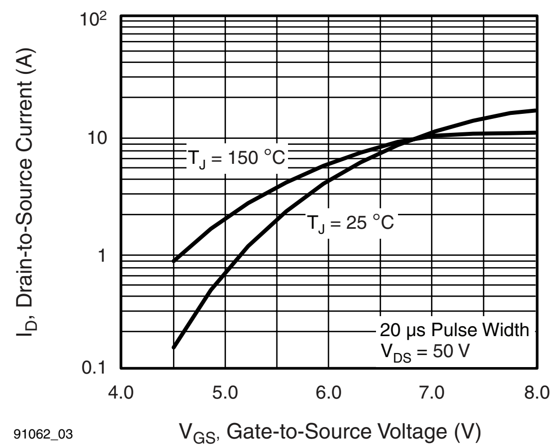


Fig. 3 - Typical Transfer Characteristics

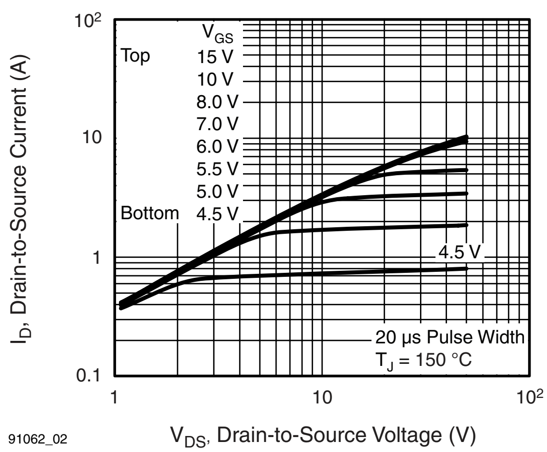


Fig. 2 - Typical Output Characteristics

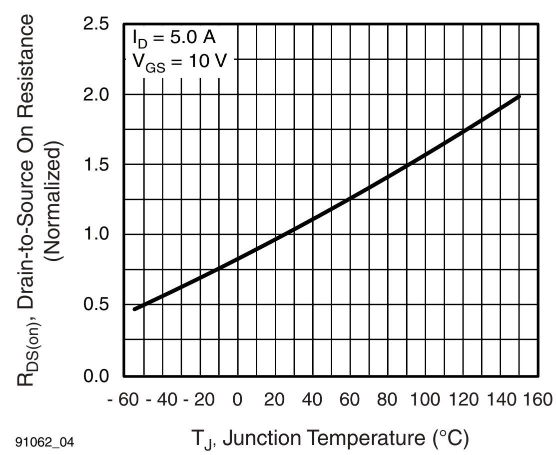


Fig. 4 - Normalized On-Resistance vs. Temperature

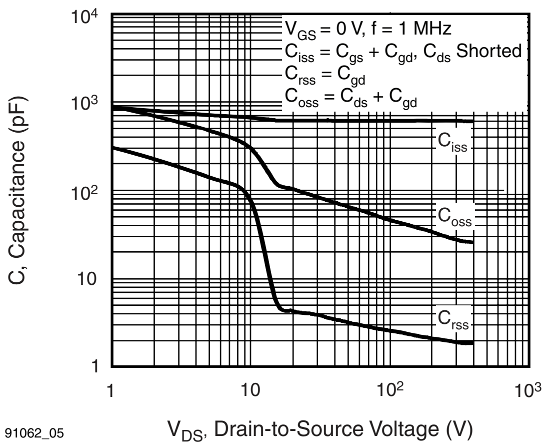


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

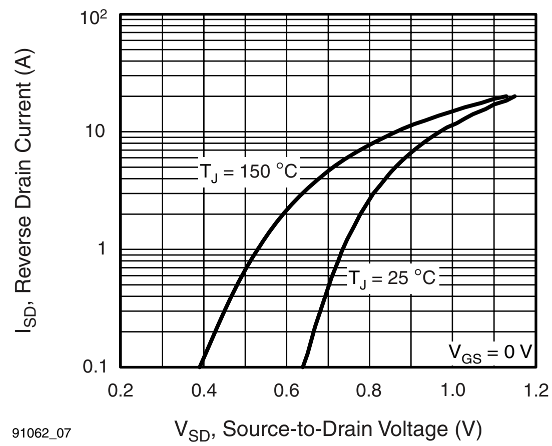


Fig. 7 - Typical Source-Drain Diode Forward Voltage

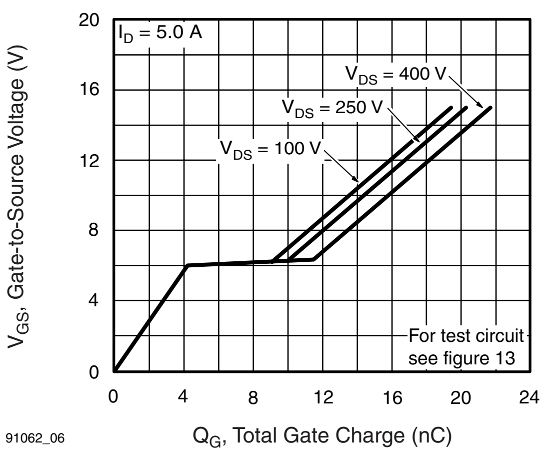


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

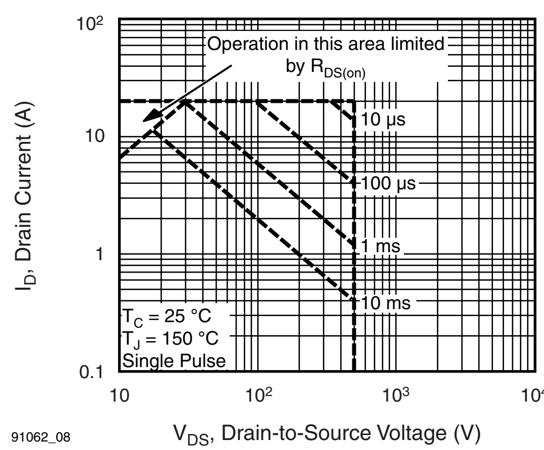


Fig. 8 - Maximum Safe Operating Area

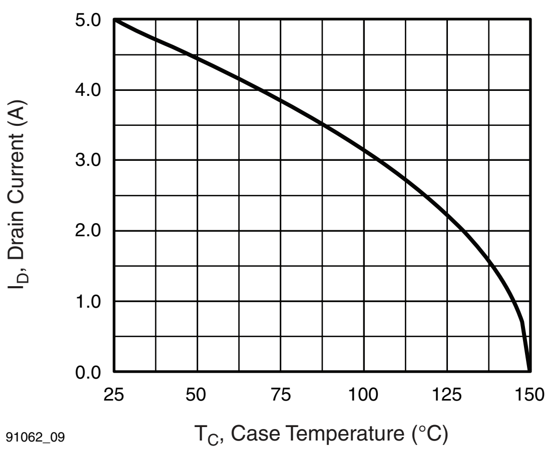


Fig. 9 - Maximum Drain Current vs. Case Temperature

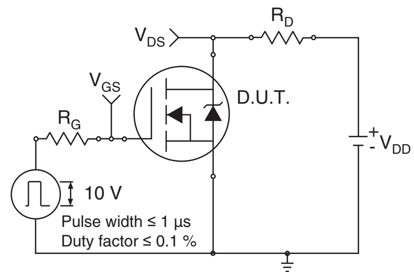


Fig. 10a - Switching Time Test Circuit

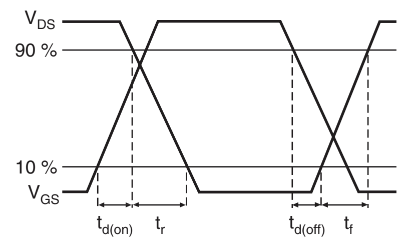


Fig. 10b - Switching Time Waveforms

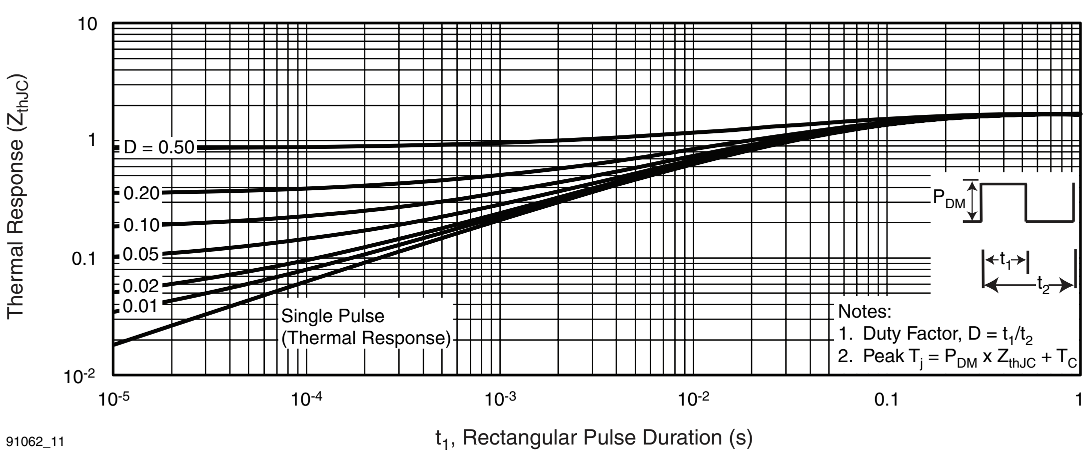


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

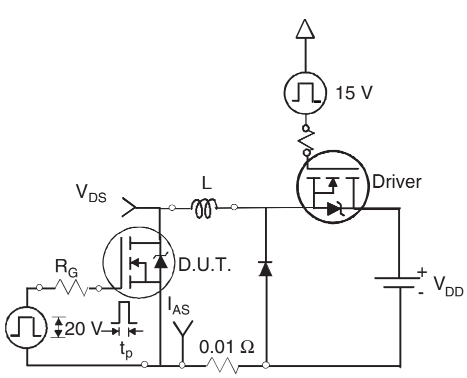


Fig. 12a - Unclamped Inductive Test Circuit

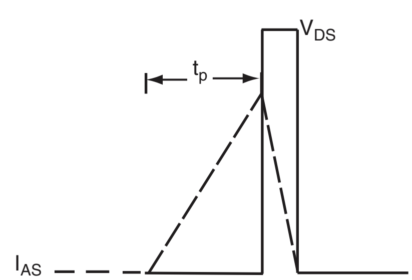


Fig. 12b - Unclamped Inductive Waveforms

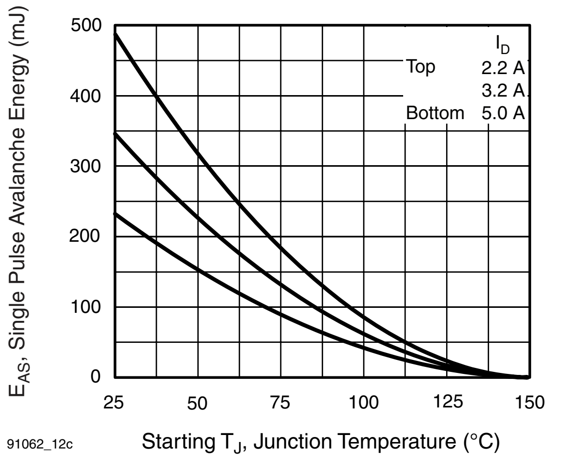


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

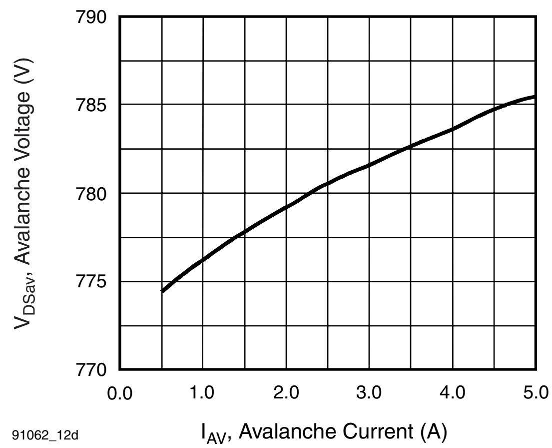


Fig. 12d - Basic Gate Charge Waveform

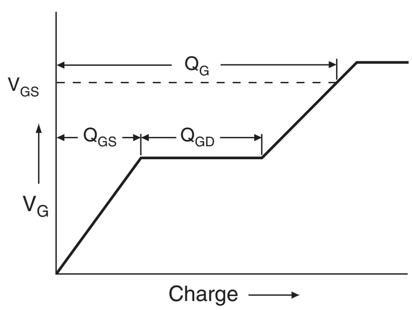


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

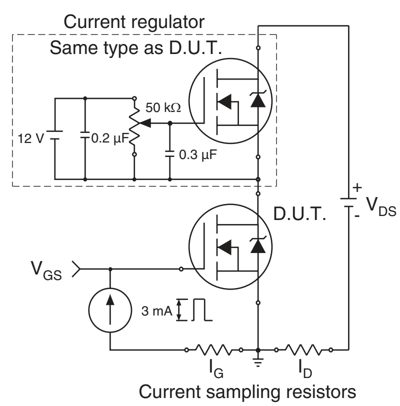


Fig. 13b - Gate Charge Test Circuit

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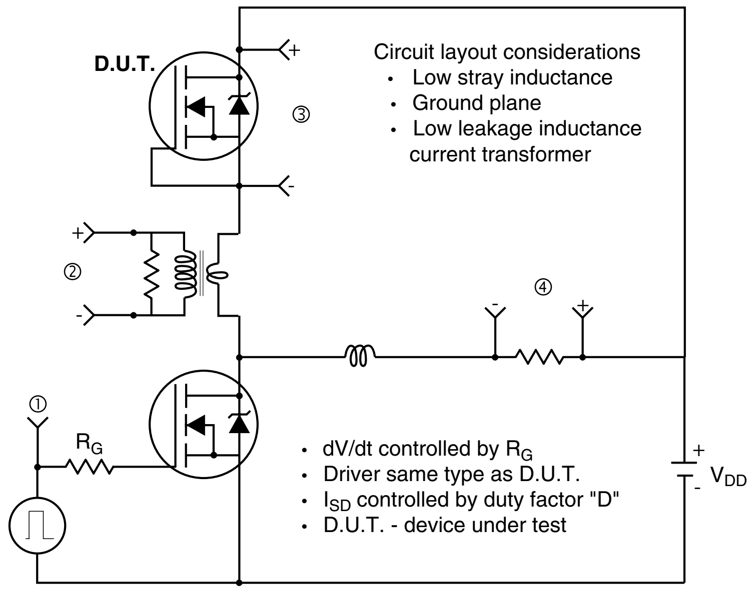
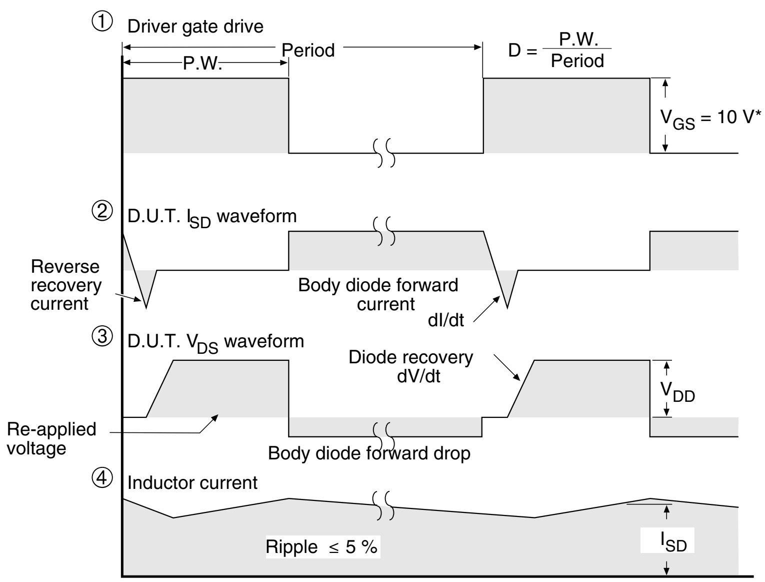
Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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