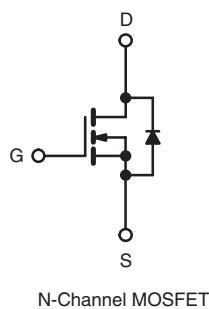
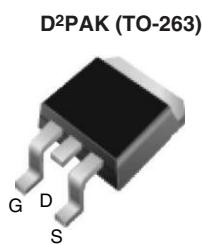


Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	500
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.85
Q _g (Max.) (nC)	63
Q _{gs} (nC)	9.3
Q _{gd} (nC)	32
Configuration	Single


RoHS*
COMPLIANT

FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirement
- Lead (Pb)-free Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION			
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free	IRF840SPbF SiHF840S-E3	IRF840STRLPbFa SiHF840STL-E3 ^a	IRF840STRRPbFa SiHF840STR-E3 ^a
SnPb	IRF840S SiHF840S	IRF840STR ^a L SiHF840STL ^a	IRF840STR ^a SiHF840STR ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	500	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	I _D	8.0 5.1	A
Pulsed Drain Current ^a	I _{DM}	32	
Linear Derating Factor		1.0	W/°C
Linear Derating Factor (PCB Mount) ^e		0.025	
Single Pulse Avalanche Energy ^b	E _{AS}	510	mJ
Avalanche Current ^a	I _{AR}	8.0	A
Repetitive Avalanche Energy ^a	E _{AR}	13	mJ
Maximum Power Dissipation	P _D	125	W
Maximum Power Dissipation (PCB Mount) ^e		3.1	
Peak Diode Recovery dV/dt ^c	dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 14 mH, R_G = 25 Ω, I_{AS} = 8.0 A (see fig. 12).
- c. I_{SD} ≤ 8.0 A, dI/dt ≤ 100 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

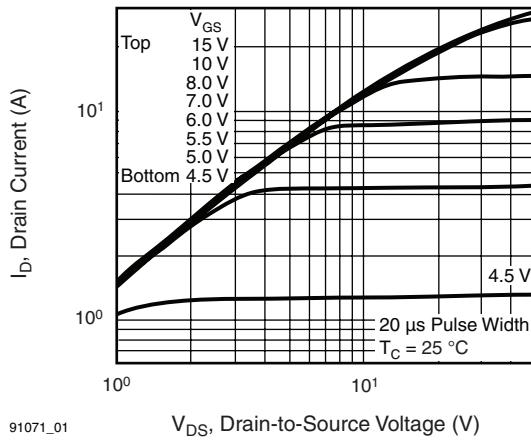
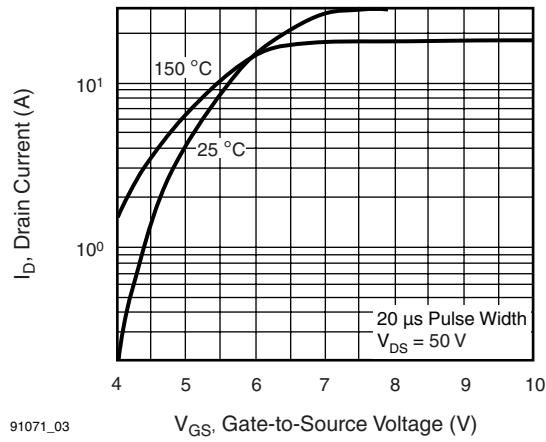
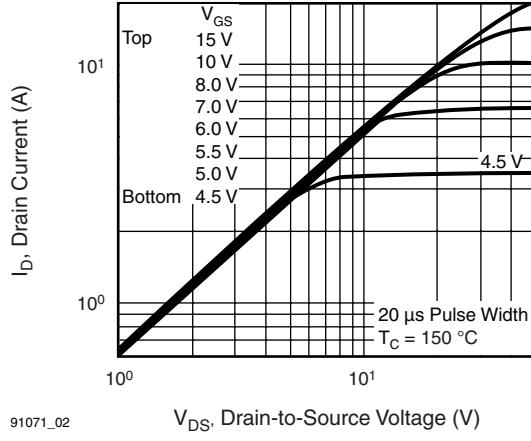
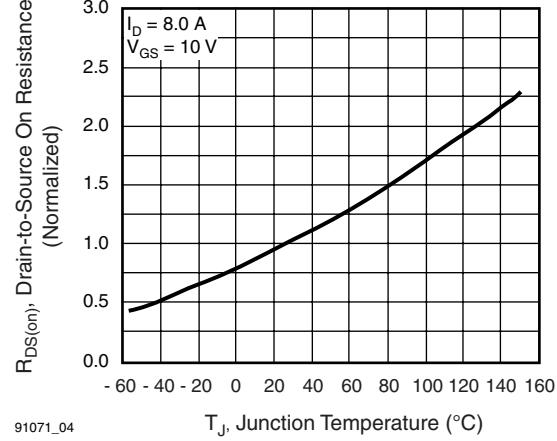
- a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25 \text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		500	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$, $I_D = 1 \text{ mA}$		-	0.78	-	$^{\circ}\text{C}/\text{V}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	25	μA	
		$V_{DS} = 400 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 4.8 \text{ A}^b$	-	-	0.85	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$, $I_D = 4.8 \text{ A}^b$		4.9	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	1300	-	pF	
Output Capacitance	C_{oss}			-	310	-		
Reverse Transfer Capacitance	C_{rss}			-	120	-		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 8.0 \text{ A}$, $V_{DS} = 400 \text{ V}$, see fig. 6 and 13 ^b	-	-	63	nC	
Gate-Source Charge	Q_{gs}			-	-	9.3		
Gate-Drain Charge	Q_{gd}			-	-	32		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250 \text{ V}$, $I_D = 8.0 \text{ A}$, $R_G = 9.1 \Omega$, $R_D = 31 \Omega$, see fig. 10 ^b		-	14	-	ns	
Rise Time	t_r			-	23	-		
Turn-Off Delay Time	$t_{d(off)}$			-	49	-		
Fall Time	t_f			-	20	-		
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	L_S			-	7.5	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	8.0	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	32		
Body Diode Voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = 8.0 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	2.0	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_F = 8.0 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	460	970	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	4.2	8.9	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

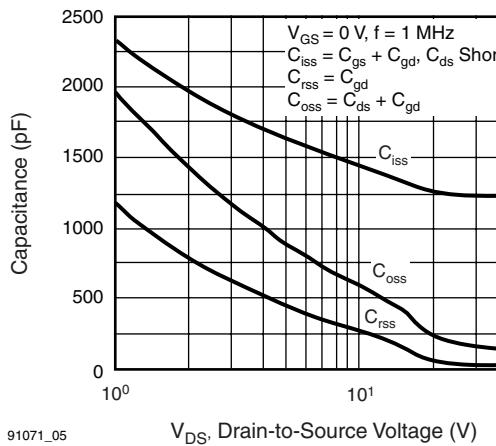
Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.

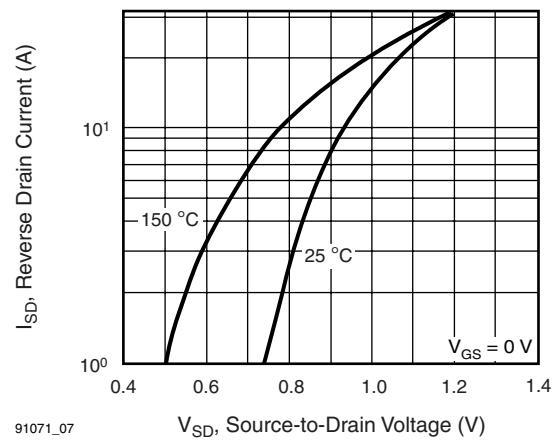
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 1 - Typical Output Characteristics, $T_C = 25 \text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150 \text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

IRF840S, SiHF840S

Vishay Siliconix



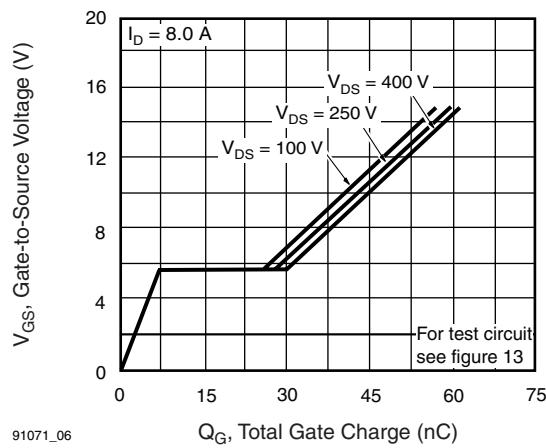
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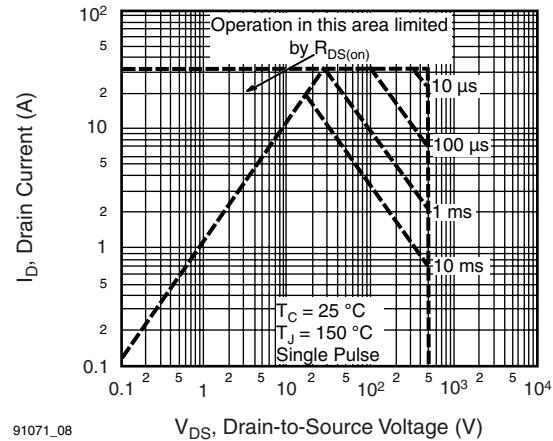
Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage



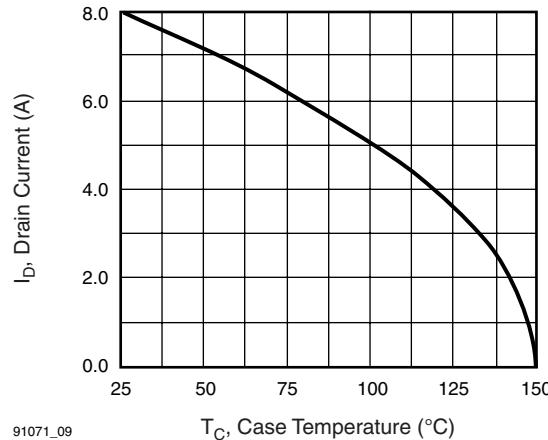
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

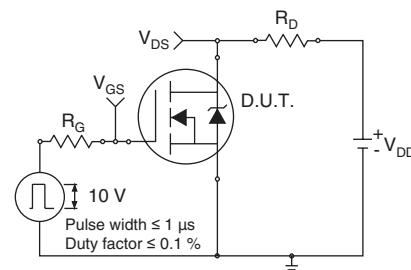
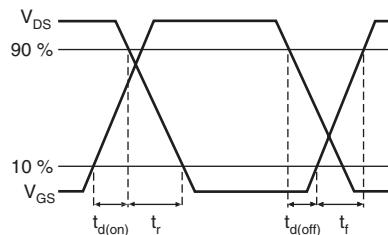
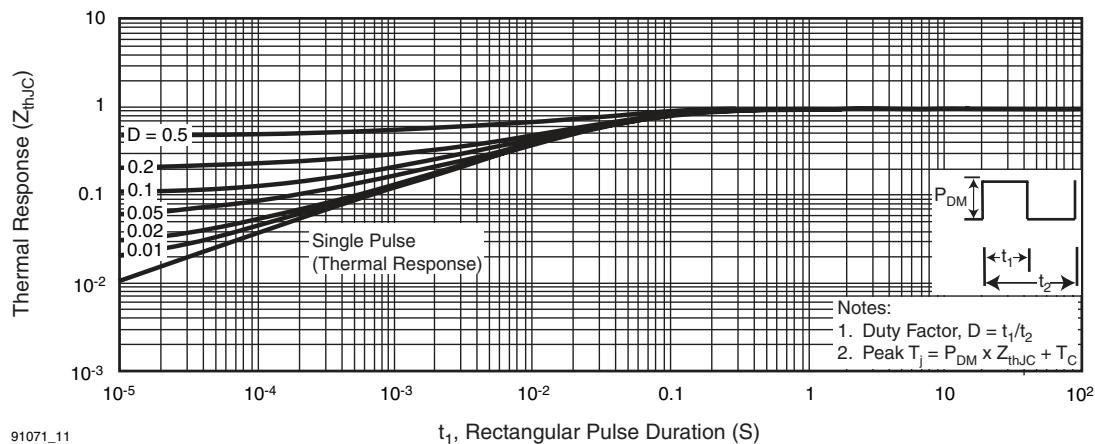


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Fig. 8 - Maximum Safe Operating Area



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Fig. 9 - Maximum Drain Current vs. Case Temperature**Fig. 10a - Switching Time Test Circuit****Fig. 10b - Switching Time Waveforms**

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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

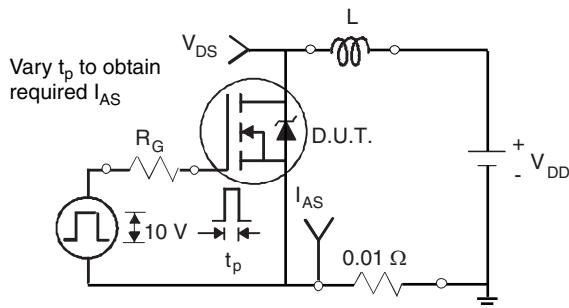


Fig. 12a - Unclamped Inductive Test Circuit

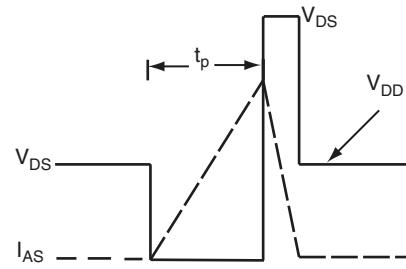


Fig. 12b - Unclamped Inductive Waveforms

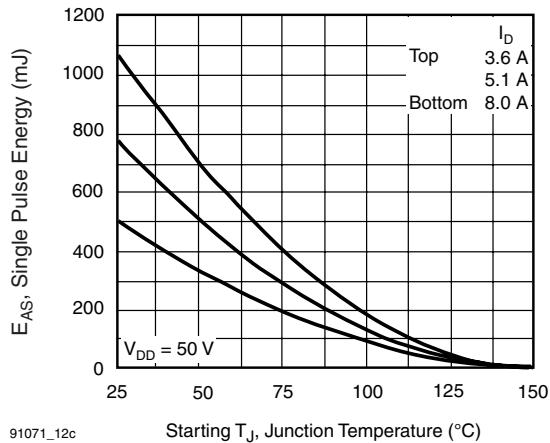


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

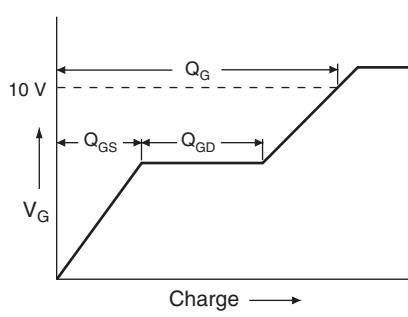


Fig. 13a - Basic Gate Charge Waveform

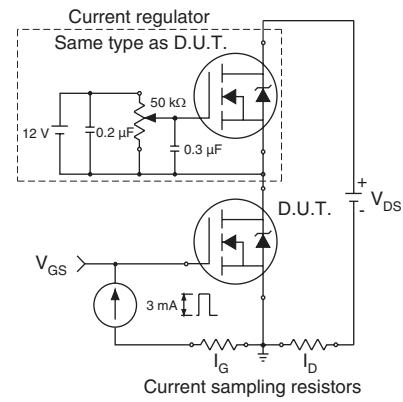


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

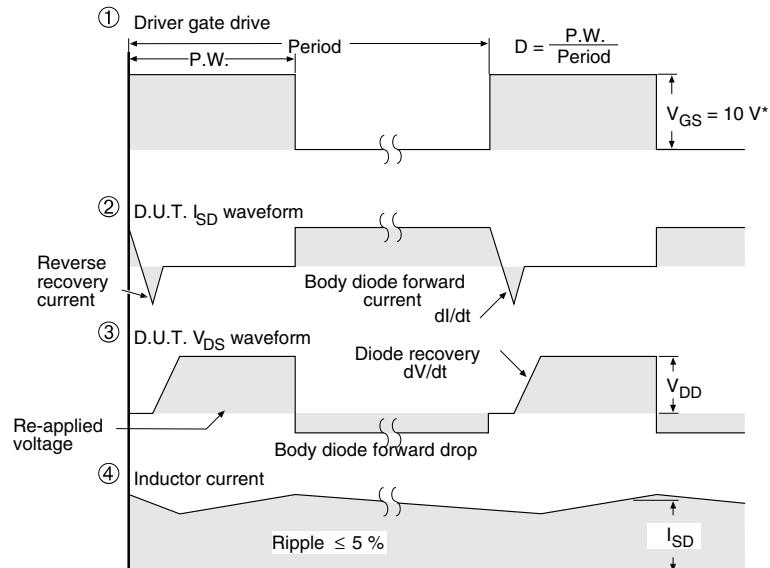
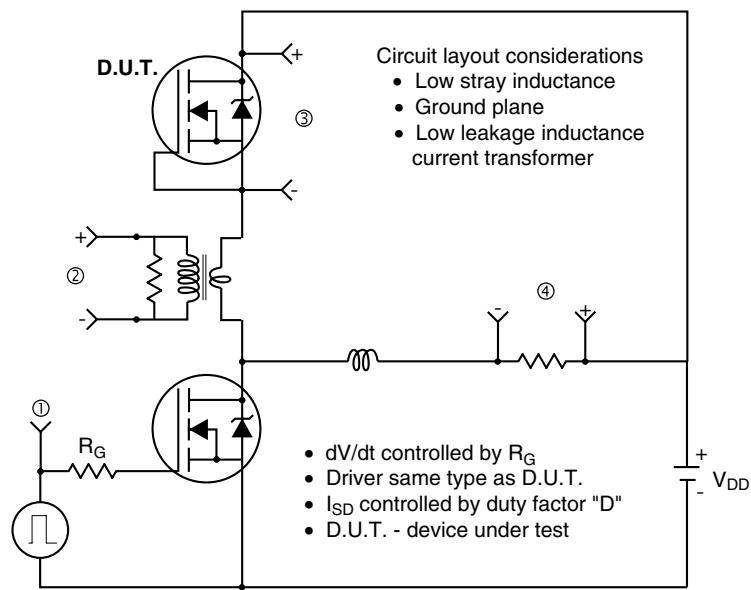


Fig. 14 - For N-Channel

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