

Power MOSFET

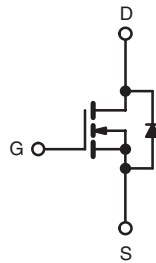
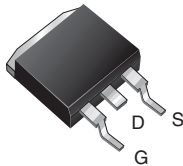
PRODUCT SUMMARY

V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.45
Q_g (Max.) (nC)	41	
Q_{gs} (nC)	6.5	
Q_{gd} (nC)	22	
Configuration	Single	

FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available


 Available
RoHS*
 COMPLIANT

SMD-220


N-Channel MOSFET

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

Package	SMD-220	SMD-220
Lead (Pb)-free	IRF634SPbF	IRF634STRRPbFa
	SiHF634S-E3	SiHF634STR-E3a
SnPb	IRF634S	-
	SiHF634S	-

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	32	W/ $^\circ\text{C}$
Linear Derating Factor		0.59	
Linear Derating Factor (PCB Mount) ^e		0.025	
Single Pulse Avalanche Energy ^b	E_{AS}	300	mJ
Avalanche Current ^a	I_{AR}	8.1	A
Repetitive Avalanche Energy ^a	E_{AR}	7.4	mJ
Maximum Power Dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	W
Maximum Power Dissipation (PCB Mount) ^e		$T_A = 25\text{ }^\circ\text{C}$	

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Peak Diode Recovery dV/dt^c	dV/dt	4.8	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

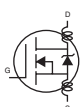
Notes


- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 7.3\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 8.1\text{ A}$ (see fig. 12).
- c. $I_{SD} \leq 8.1\text{ A}$, $dI/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

- a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	250	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.37	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 5.1\text{ A}^b$	-	-	0.45	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 5.1\text{ A}^b$	1.6	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	770	-	pF
Output Capacitance	C_{oss}		-	190	-	
Reverse Transfer Capacitance	C_{rss}		-	52	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$ $I_D = 5.6\text{ A}$, $V_{DS} = 200\text{ V}$, see fig. 6 and 13 ^b	-	-	41	nC
Gate-Source Charge	Q_{gs}		-	-	6.5	
Gate-Drain Charge	Q_{gd}		-	-	22	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}$, $I_D = 5.6\text{ A}$, $R_G = 12\text{ }\Omega$, $R_D = 22\text{ }\Omega$, see fig. 10 ^b	-	9.6	-	ns
Rise Time	t_r		-	21	-	
Turn-Off Delay Time	$t_{d(off)}$		-	42	-	
Fall Time	t_f		-	19	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8.1	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	32	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 8.1\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 5.6\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	220	440	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.2	2.4	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

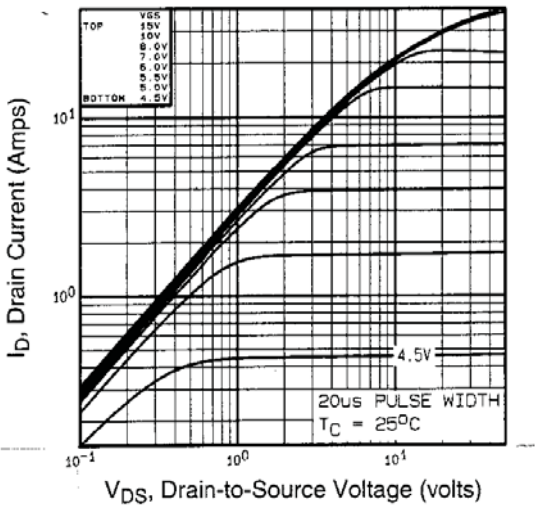


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

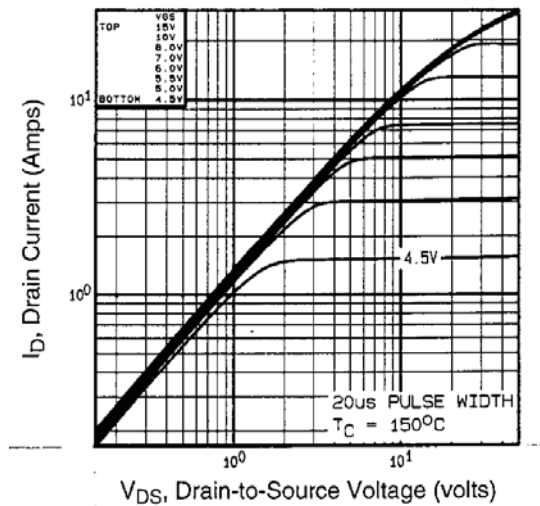


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

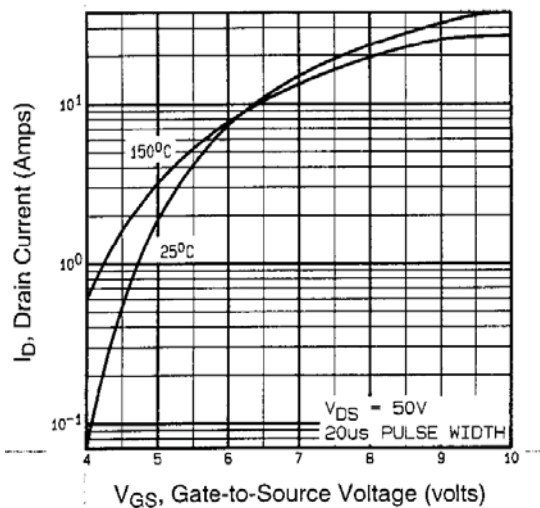


Fig. 3 - Typical Transfer Characteristics

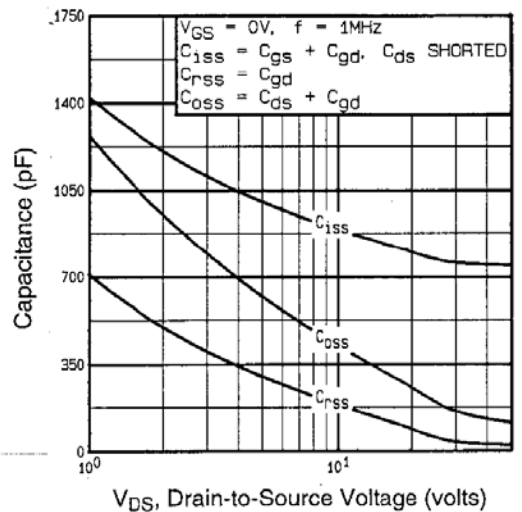


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

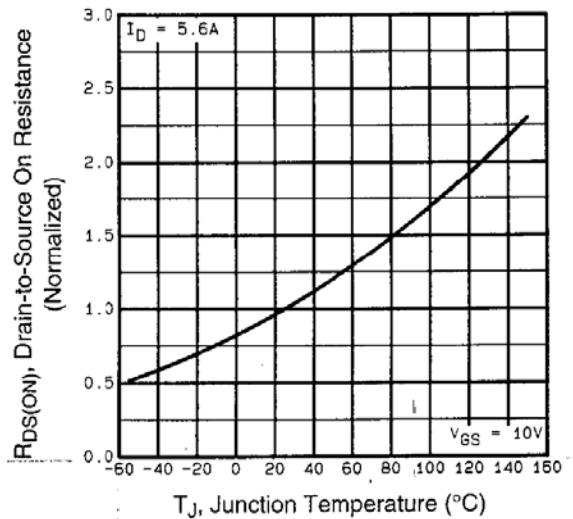


Fig. 4 - Normalized On-Resistance vs. Temperature

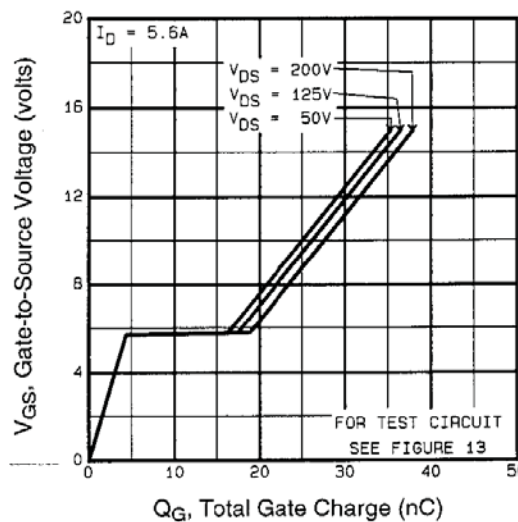


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

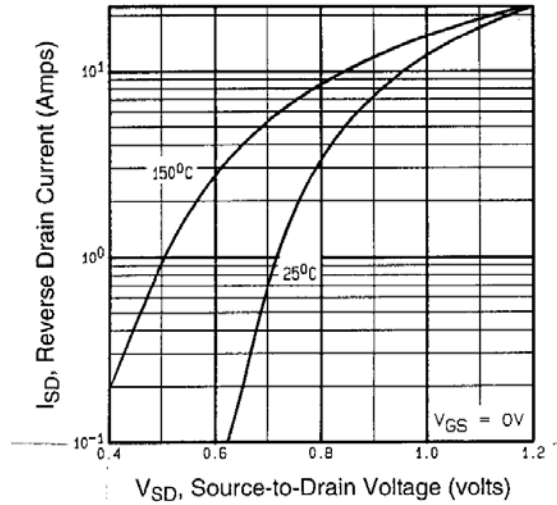


Fig. 7 - Typical Source-Drain Diode Forward Voltage

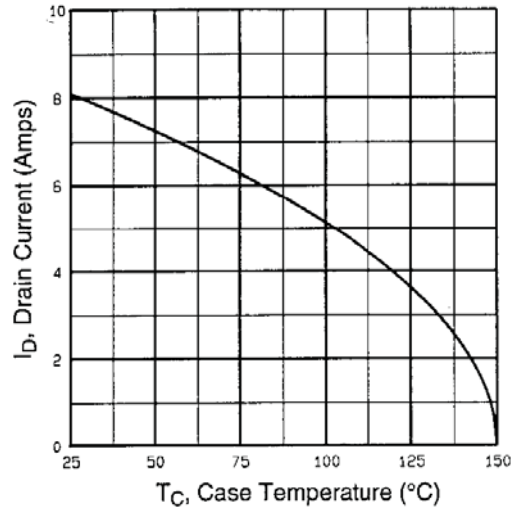


Fig. 9 - Maximum Drain Current vs. Case Temperature

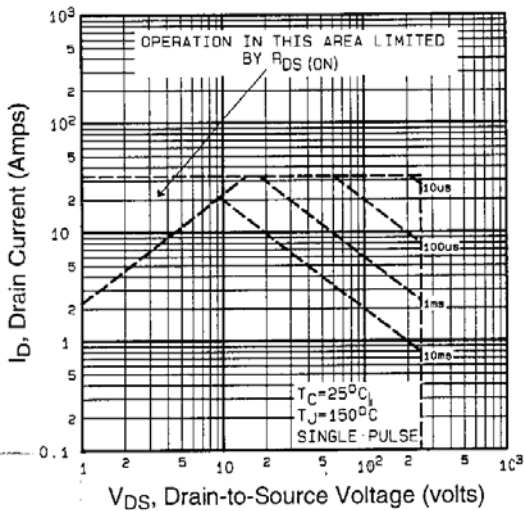


Fig. 8 - Maximum Safe Operating Area

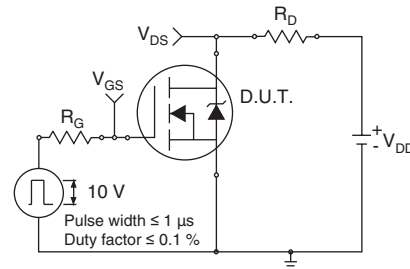


Fig. 10a - Switching Time Test Circuit

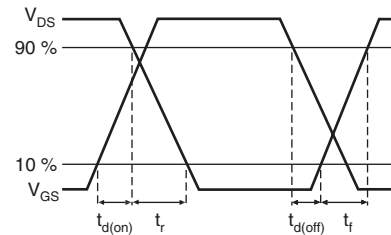


Fig. 10b - Switching Time Waveforms

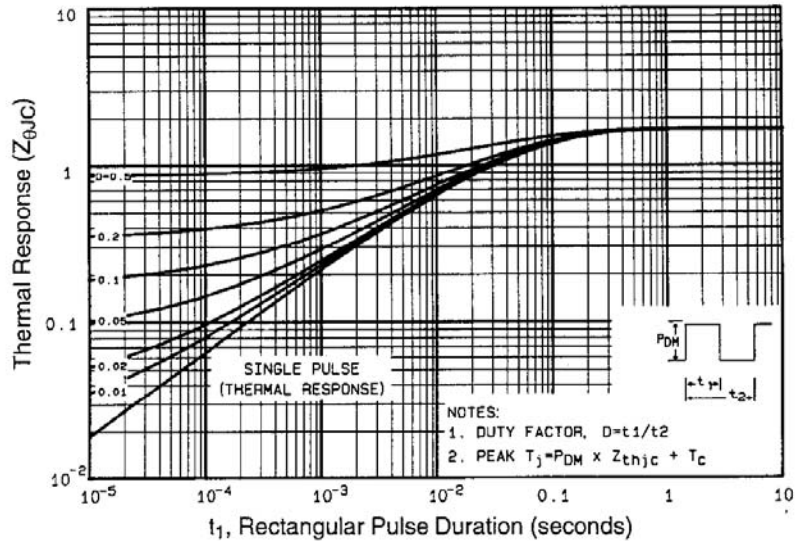


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

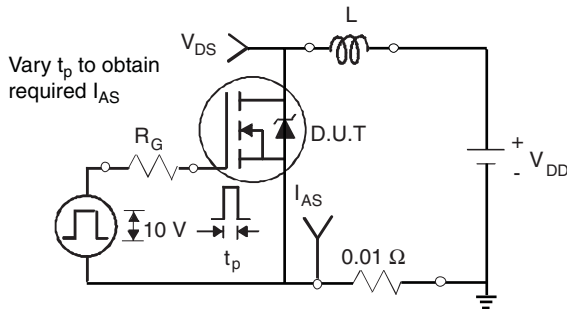


Fig. 12a - Unclamped Inductive Test Circuit

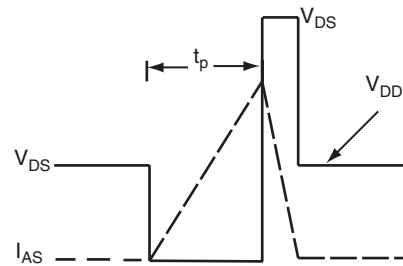


Fig. 12b - Unclamped Inductive Waveforms

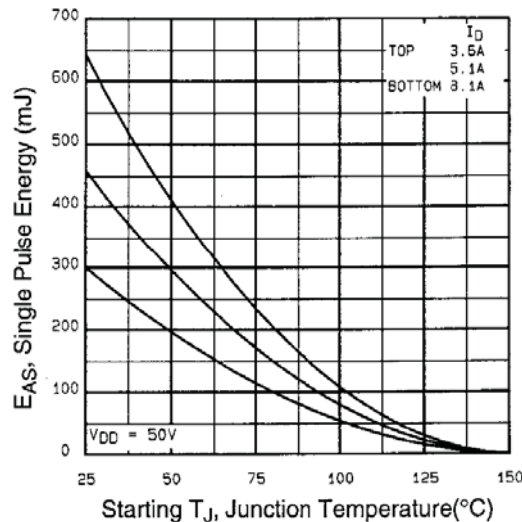


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

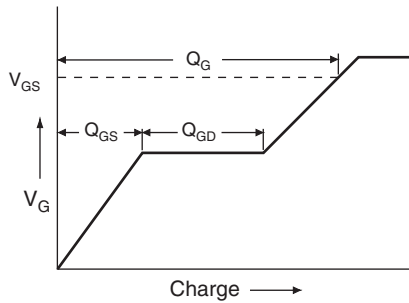


Fig. 13a - Basic Gate Charge Waveform

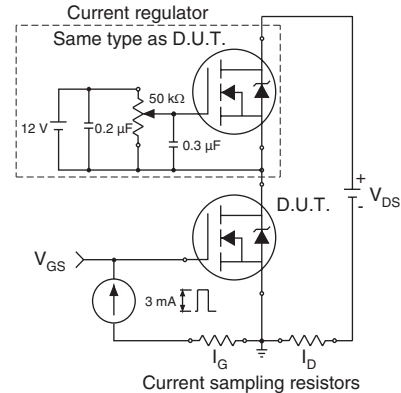
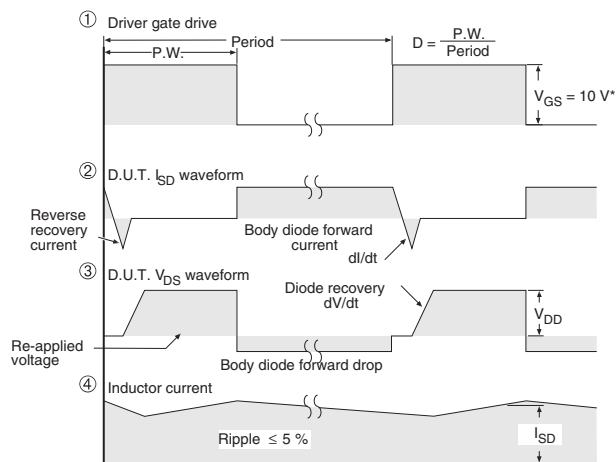
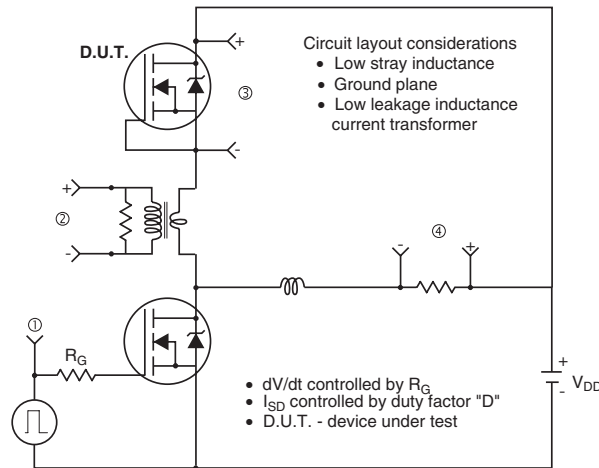


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5V$ for logic level and $3V$ drive devices

Fig. 14 - For N-Channel

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