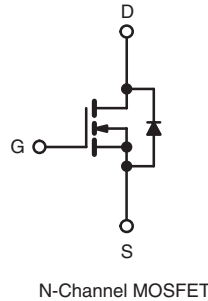
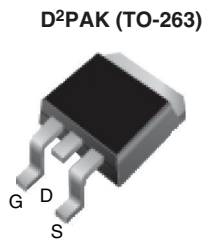


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	1.1
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	2.7	
Q_{gd} (nC)	7.8	
Configuration	Single	



FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION	
Package	D ² PAK (TO-263)
Lead (Pb)-free	IRF624SPbF SiHF624S-E3
SnPb	IRF624S SiHF624S

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V_{DS}		250	V
Gate-Source Voltage	V_{GS}		± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	4.4	A
		$T_C = 100$ °C	2.8	
Pulsed Drain Current ^a	I_{DM}		14	W/°C
Linear Derating Factor			0.40	
Linear Derating Factor (PCB Mount) ^e			0.025	
Single Pulse Avalanche Energy ^b	E_{AS}		100	mJ
Repetitive Avalanche Current ^a	I_{AR}		4.4	A
Repetitive Avalanche Energy ^a	E_{AR}		5.0	mJ
Maximum Power Dissipation	$T_C = 25$ °C		50	W
	$T_A = 25$ °C		3.1	
Peak Diode Recovery dV/dt^c	dV/dt		4.8	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)		for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 8.3$ mH, $R_G = 25$ Ω , $I_{AS} = 4.4$ A (see fig. 12).
- $I_{SD} \leq 4.4$ A, $dI/dt \leq 90$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	40	°C/W	
Maximum Junction-to-Ambient	R_{thJA}	-	-	62		
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	2.5		

Note

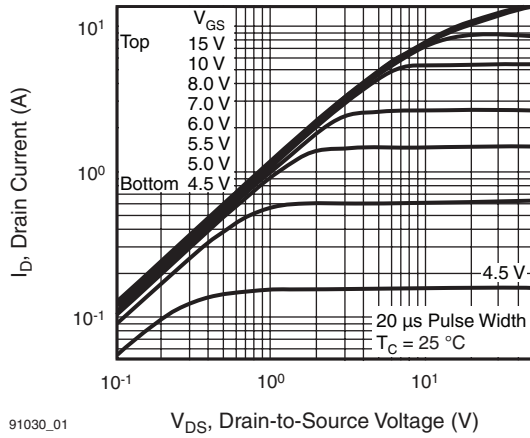
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX. UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		250	-	- V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.36	- V/ $^\circ\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0 V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100 nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$		-	-	25 μA	
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250 μA	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.6\text{ A}^b$	-	-	1.1 Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 2.6\text{ A}^b$		1.5	-	- S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	260	-	pF
Output Capacitance	C_{oss}			-	77	-	
Reverse Transfer Capacitance	C_{rss}			-	15	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 4.4\text{ A}, V_{DS} = 200\text{ V}$ see fig. 6 and 13 ^b	-	-	14	nC
Gate-Source Charge	Q_{gs}			-	-	2.7	
Gate-Drain Charge	Q_{gd}			-	-	7.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, I_D = 4.4\text{ A}$ $R_G = 18\text{ }\Omega, R_D = 28\text{ }\Omega$ see fig. 10 ^b		-	7.0	-	ns
Rise Time	t_r			-	13	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	t_f			-	12	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.4	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	14	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 4.4\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 4.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	200	400	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.93	1.9	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

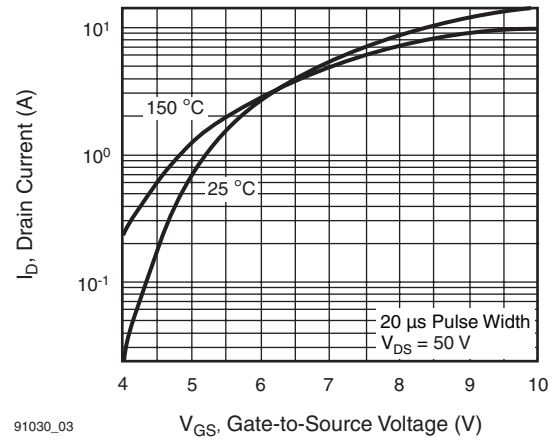
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



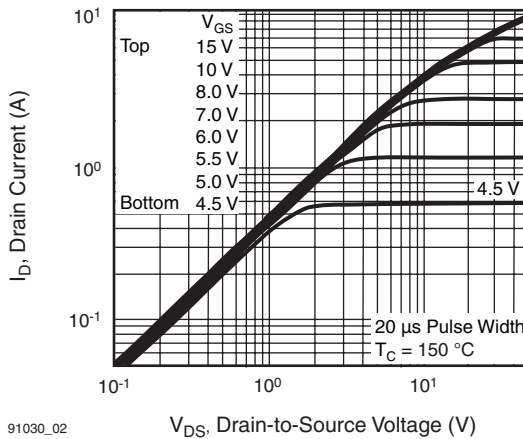
91030_01

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ °C}$



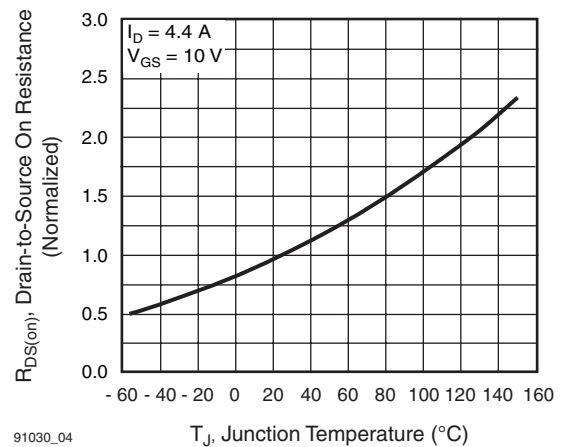
91030_03

Fig. 3 - Typical Transfer Characteristics



91030_02

Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ °C}$



91030_04

Fig. 4 - Normalized On-Resistance vs. Temperature

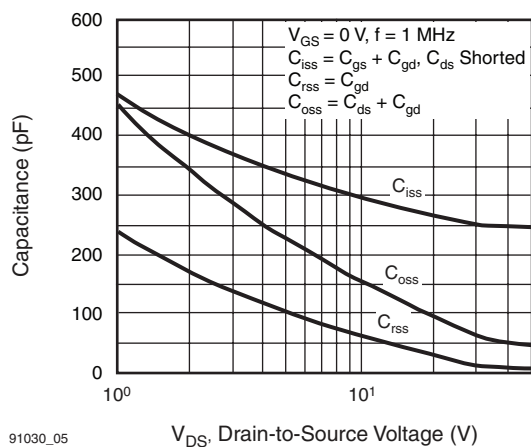


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

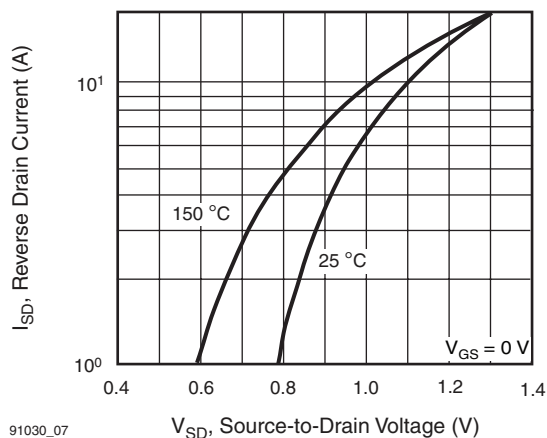


Fig. 7 - Typical Source-Drain Diode Forward Voltage

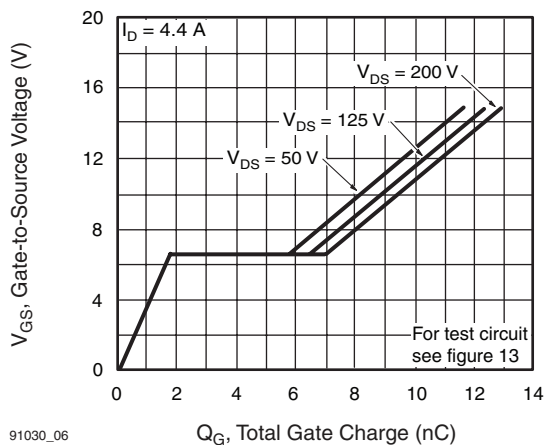


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

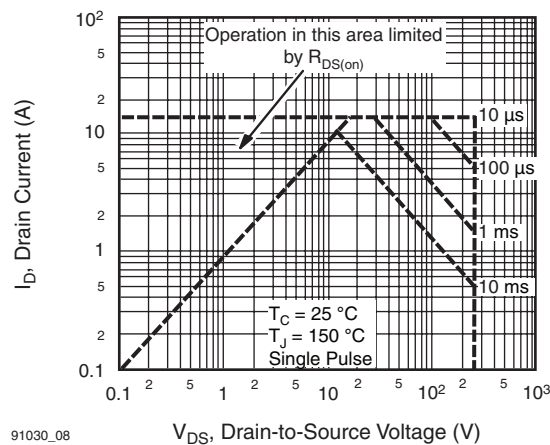
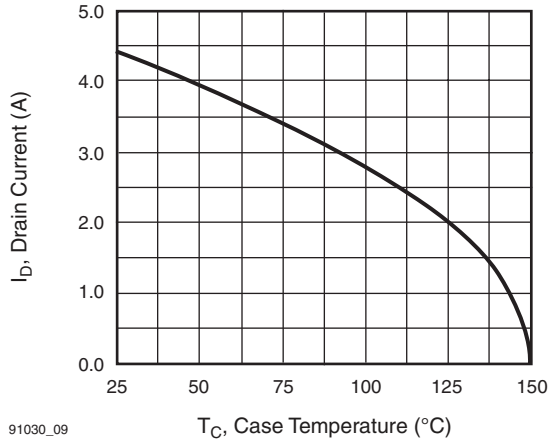


Fig. 8 - Maximum Safe Operating Area



91030_09

Fig. 9 - Maximum Drain Current vs. Case Temperature

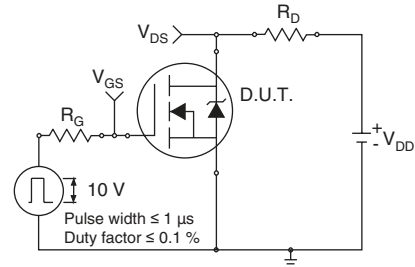


Fig. 10a - Switching Time Test Circuit

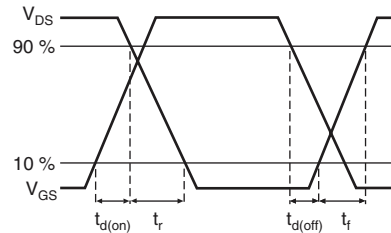
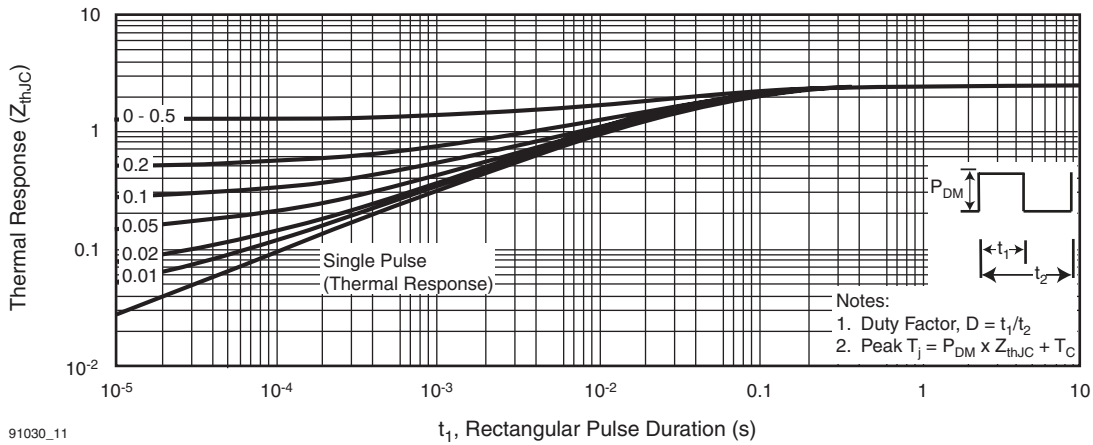


Fig. 10b - Switching Time Waveforms



91030_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

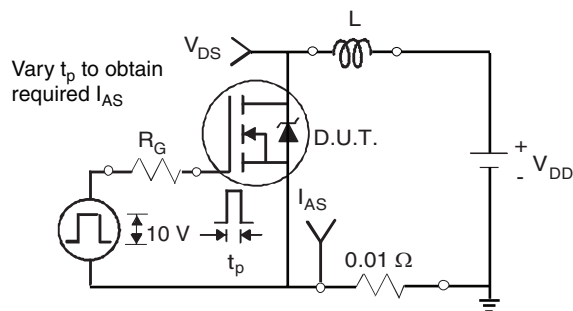


Fig. 12a - Unclamped Inductive Test Circuit

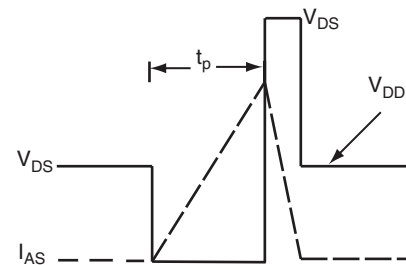
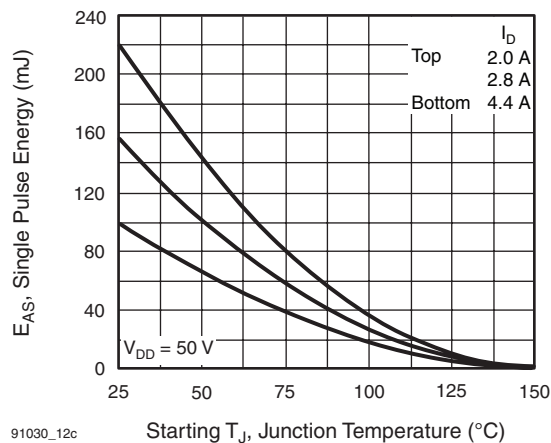


Fig. 12b - Unclamped Inductive Waveforms



91030_12c

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

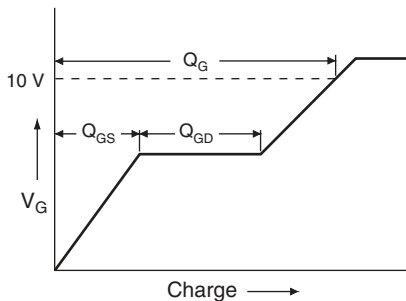


Fig. 13a - Basic Gate Charge Waveform

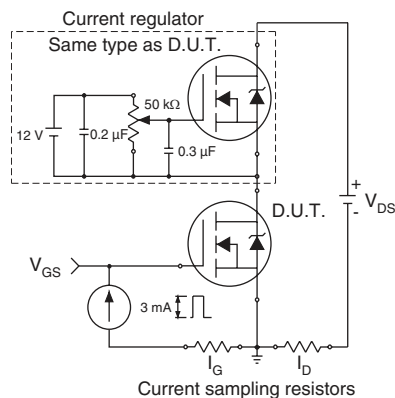
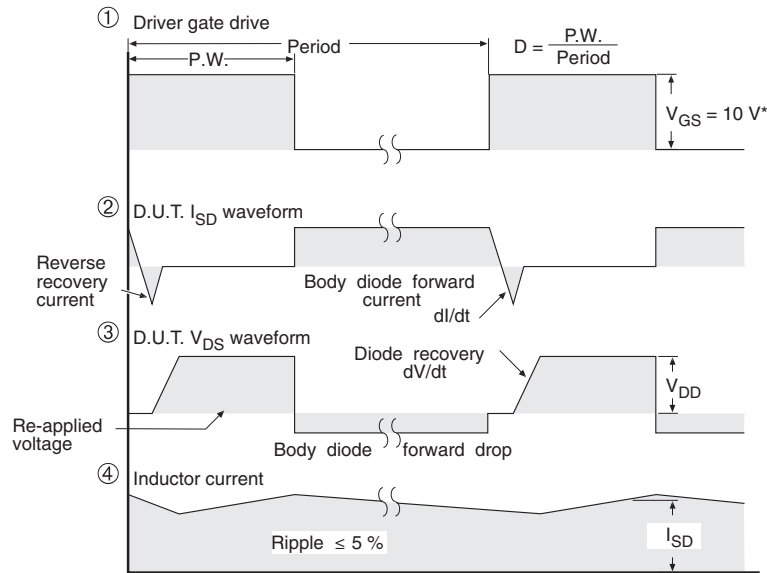
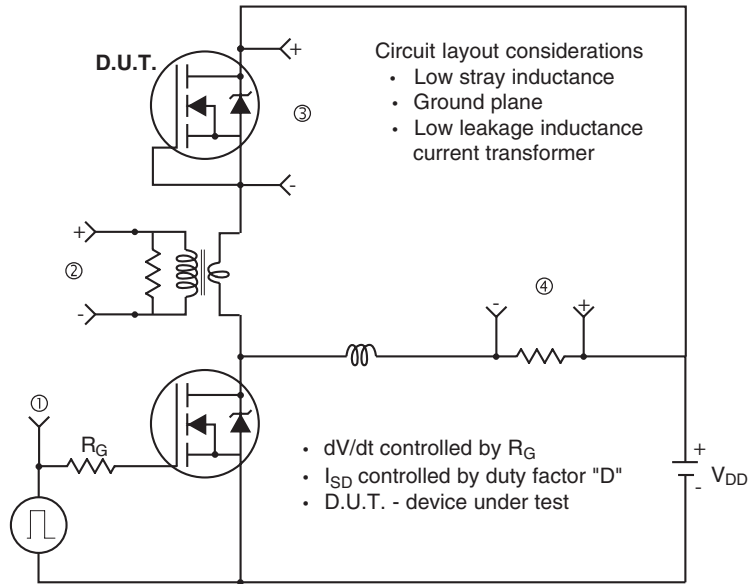


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level and $3 V$ drive devices

Fig. 14 - For N-Channel

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