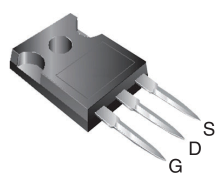
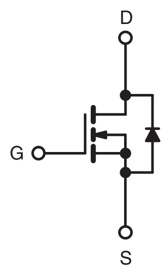
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.014
Q_g (Max.) (nC)	160	
Q_{gs} (nC)	48	
Q_{gd} (nC)	54	
Configuration	Single	

TO-247





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Isolated Central Mounting Hole
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mouting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP054PbF
	SiHFP054-E3
SnPb	IRFP054
	SiHFP054

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

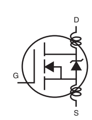
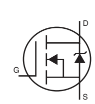
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current[e]	V_{GS} at 10 V	T_C = 25 °C	I_D	70	A
Continuous Drain Current		T_C = 100 °C		64	
Pulsed Drain Current[a]			I_{DM}	360	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	640	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	230	W
Peak Diode Recovery dV/dt[c]			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 92 µH, R_G = 25 Ω, I_{AS} = 90 A (see fig. 12).
c. $I_{SD} \leq 90$ A, dI/dt ≤ 200 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
d. 1.6 mm from case.
e. Current limited by the package, (die current = 90 A).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	40	
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.65	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.056	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 54 A[b]	-	-	0.014	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 54 A[b]	25	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	4500	-	pF
Output Capacitance	C_{oss}		-	2000	-	
Reverse Transfer Capacitance	C_{rss}		-	300	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 64 A, V_{DS} = 48 V, see fig. 6 and 13[b]	-	-	160	nC
Gate-Source Charge	Q_{gs}		-	-	48	
Gate-Drain Charge	Q_{gd}		-	-	54	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 64 A, R_G = 6.2 Ω, R_D = 0.45 Ω, see fig. 10[b]	-	20	-	ns
Rise Time	t_r		-	160	-	
Turn-Off Delay Time	$t_{d(off)}$		-	83	-	
Fall Time	t_f		-	150	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	5.0	-	nH
Internal Source Inductance	L_S		-	13	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	70	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	360	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 90 A, V_{GS} = 0 V[b]	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 6.4 A, dI/dt = 100 A/µs[b]	-	270	540	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.1	2.2	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

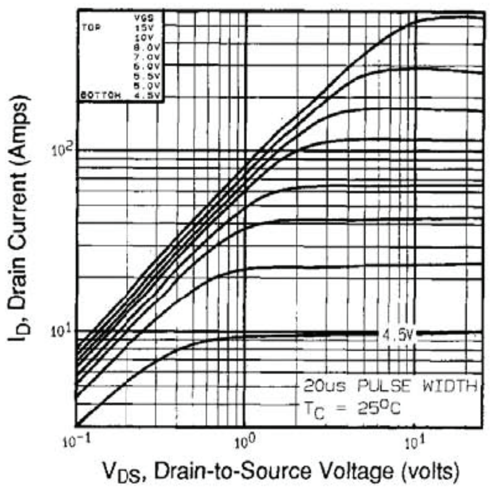


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

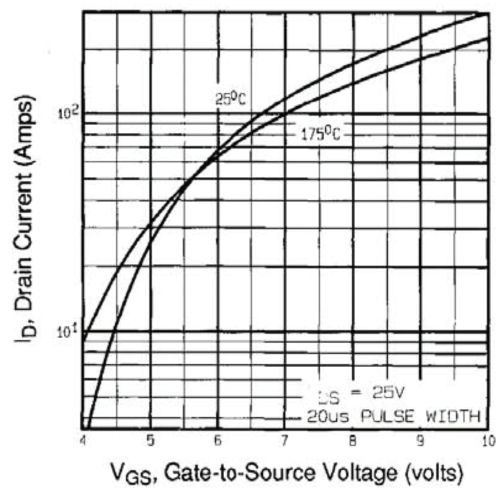


Fig. 3 - Typical Transfer Characteristics

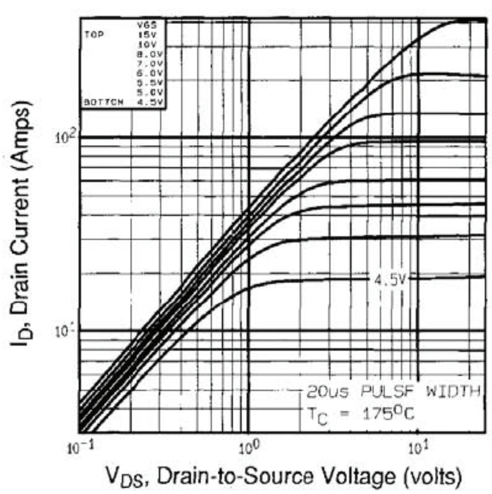


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

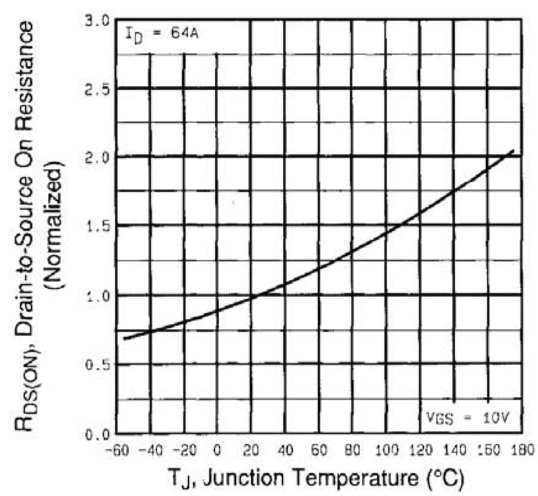


Fig. 4 - Normalized On-Resistance vs. Temperature

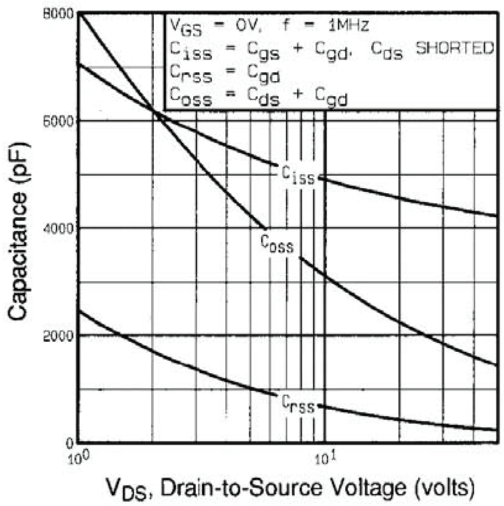


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

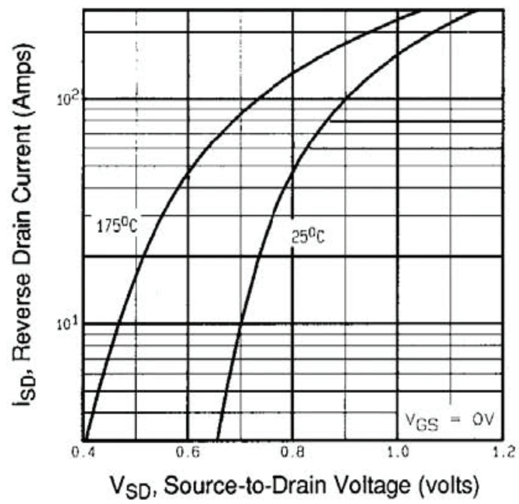


Fig. 7 - Typical Source-Drain Diode Forward Voltage

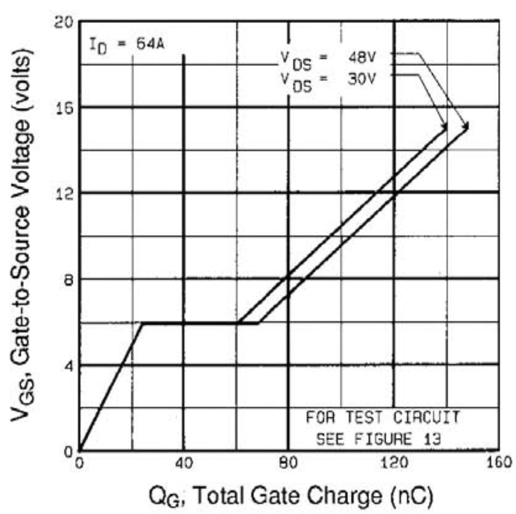


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

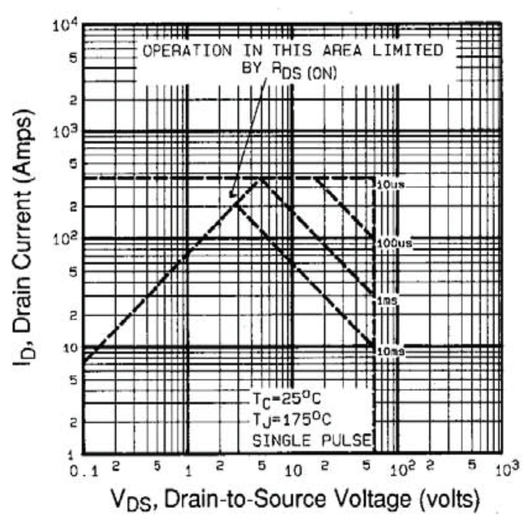


Fig. 8 - Maximum Safe Operating Area

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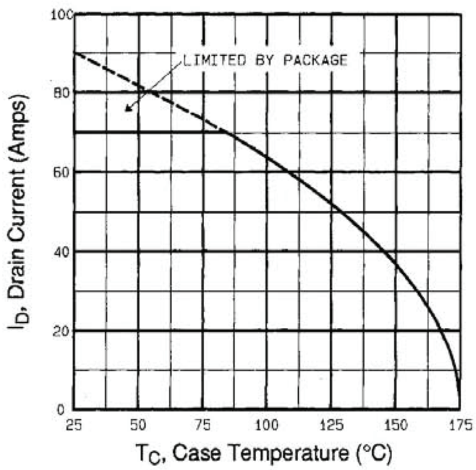

Fig. 9 - Maximum Drain Current vs. Case Temperature

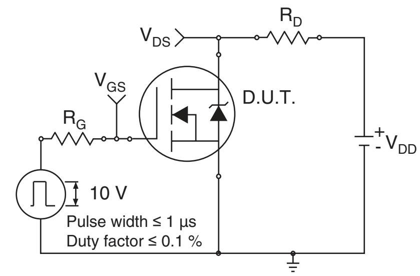

Fig. 10a - Switching Time Test Circuit

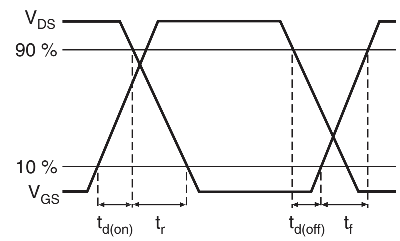

Fig. 10b - Switching Time Waveforms

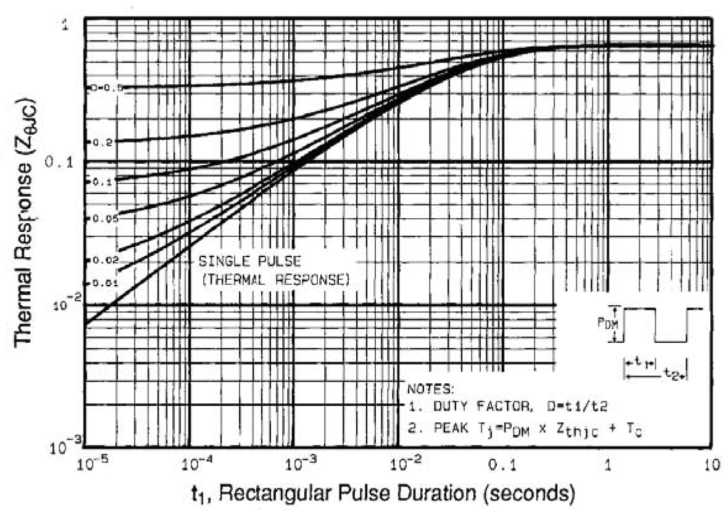

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

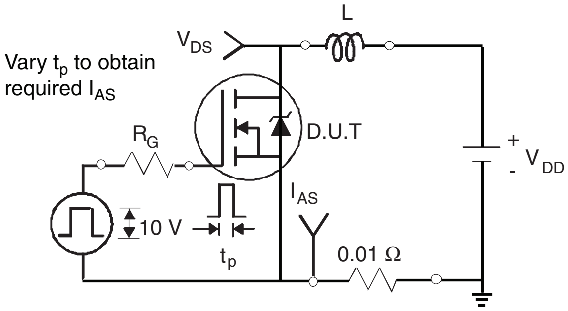

Fig. 12a - Unclamped Inductive Test Circuit

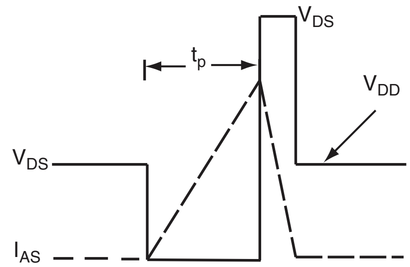

Fig. 12b - Unclamped Inductive Waveforms

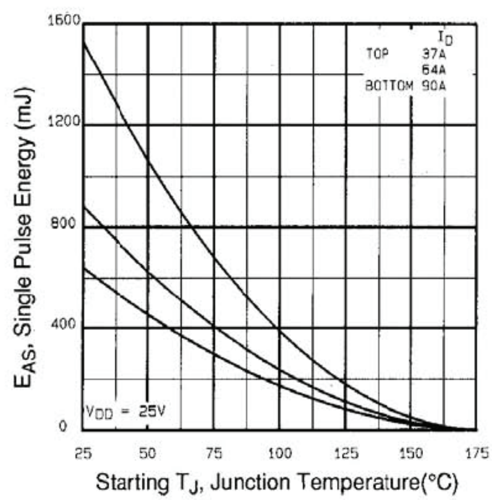

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

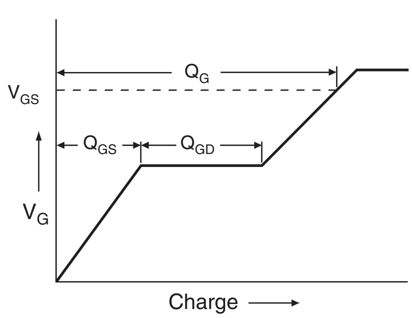

Fig. 13a - Basic Gate Charge Waveform

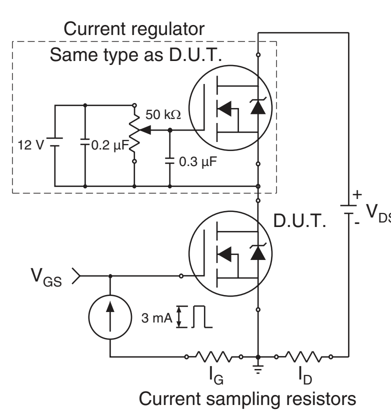

Fig. 13b - Gate Charge Test Circuit

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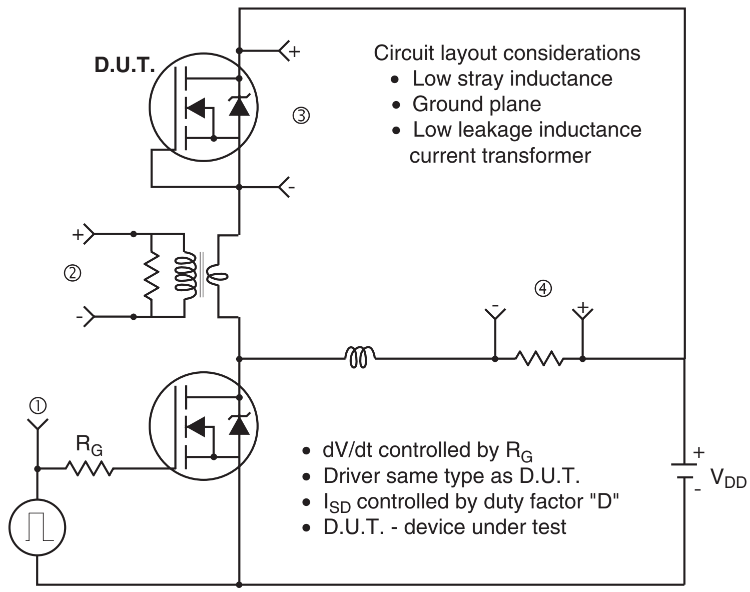
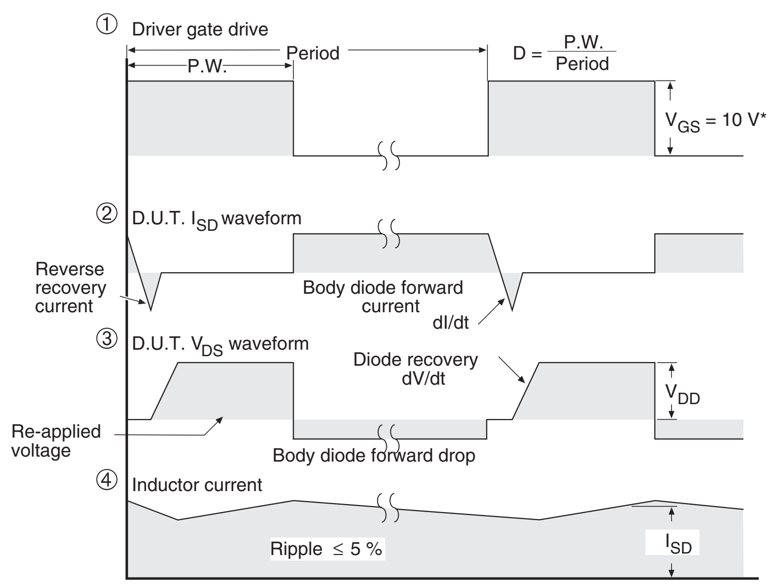
Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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