

**100V P-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$ $T_A = 25^\circ C$
-100V	350mΩ @ $V_{GS} = -10V$	-2.4
	450mΩ @ $V_{GS} = -6.0V$	-2.1

**Description and Applications**

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Motor control
- DC-DC Converters
- Power management functions
- Uninterrupted power supply

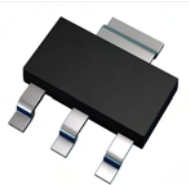
**Features and Benefits**

- Fast switching speed
- Low gate drive
- Low input capacitance
- **Qualified to AEC-Q101 Standards for High Reliability**

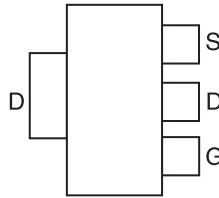
**Mechanical Data**

- Case: SOT223
- Case Material: Molded Plastic, UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.112 grams (approximate)

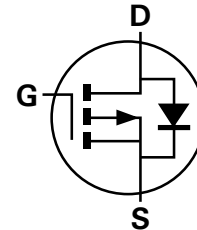
SOT223



Top View



Pin Out - Top View

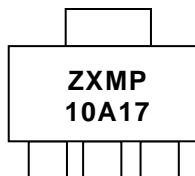


Equivalent Circuit

**Ordering Information**

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMP10A17GTA	See below	7	12	1,000

**Marking Information**



ZXMP = Product Type Marking Code, Line 1  
10A17 = Product Type Marking Code, Line 2

**Maximum Ratings** @T<sub>A</sub> = 25°C unless otherwise specified

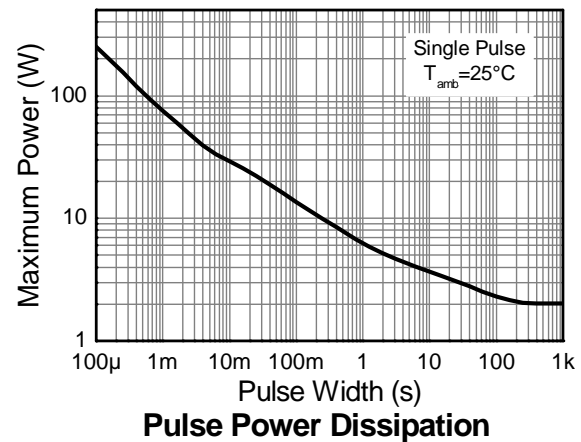
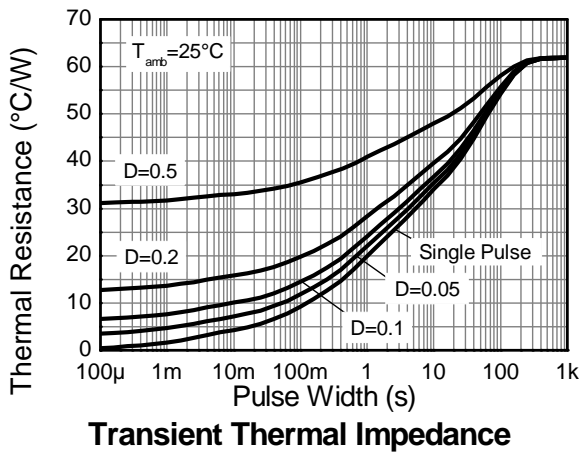
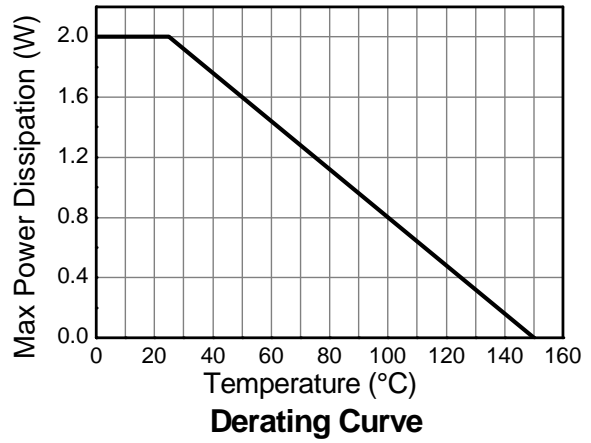
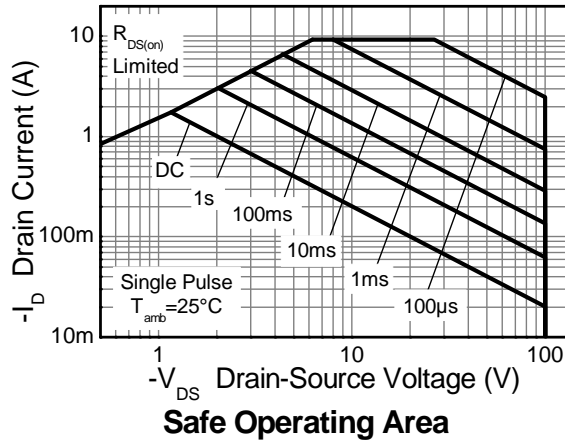
Characteristic			Symbol	Value	Unit
Drain-Source voltage			V <sub>DSS</sub>	-100	V
Gate-Source voltage			V <sub>GS</sub>	±20	V
Continuous Drain current	V <sub>GS</sub> = 10V	(Note 2)	I <sub>D</sub>	-2.4	A
		T <sub>A</sub> = 70°C (Note 2)		-1.9	
		(Note 1)		-1.7	
Pulsed Drain current	V <sub>GS</sub> = 10V	(Note 3)	I <sub>DM</sub>	-9.4	A
Continuous Source current (Body diode)			I <sub>S</sub>	-4.5	A
Pulsed Source current (Body diode)			I <sub>SM</sub>	-9.4	A

**Thermal Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Power dissipation Linear derating factor		(Note 1)	P <sub>D</sub>	2.0	W mW/°C
				16	
		(Note 2)		3.9	
Thermal Resistance, Junction to Ambient		(Note 1)	R <sub>θJA</sub>	62.5	°C/W
		(Note 2)		32.0	
Thermal Resistance, Junction to Lead		(Note 4)	R <sub>θJL</sub>	9.8	
Operating and storage temperature range			T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

- Notes:
1. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  2. Same as note (1), except the device is measured at t ≤ 10 sec.
  3. Same as note (1), except the device is pulsed with D= 0.02 and pulse width 300 μs. The pulse current is limited by the maximum junction temperature.
  4. Thermal resistance from junction to solder-point (at the end of the drain lead).

**Thermal Characteristics**

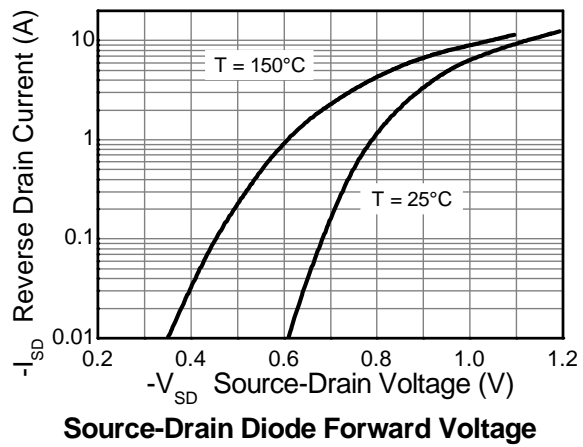
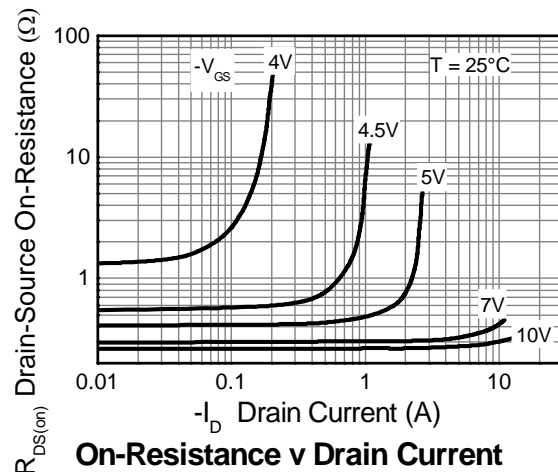
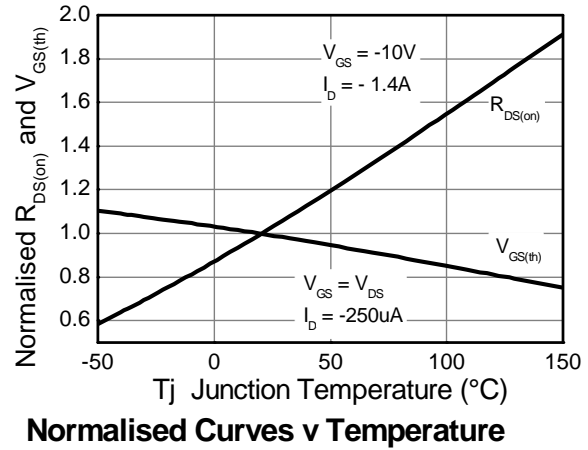
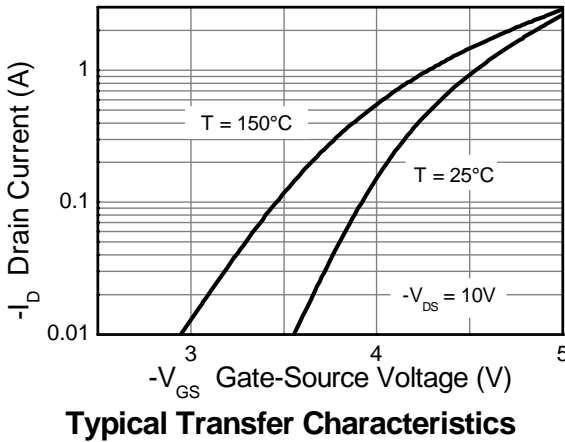
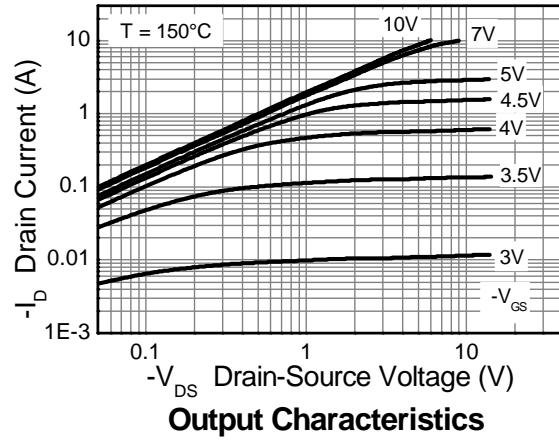
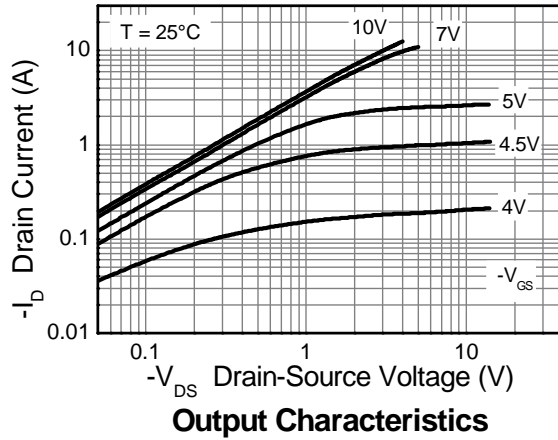


**Electrical Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

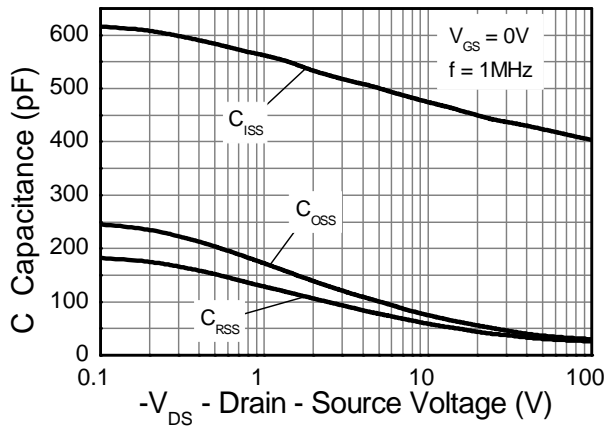
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-100	—	—	V	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-0.5	$\mu\text{A}$	$V_{DS} = -100\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	-2.0	—	-4.0	V	$I_D = -250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 5)	$R_{DS(on)}$	—	—	0.350	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -1.4\text{A}$
				0.450		$V_{GS} = -6\text{V}$ , $I_D = -1.2\text{A}$
Forward Transconductance (Notes 5 & 6)	$g_{fs}$	—	2.8	—	S	$V_{DS} = -15\text{V}$ , $I_D = -1.4\text{A}$
Diode Forward Voltage (Note 5)	$V_{SD}$	—	-0.85	-0.95	V	$I_S = -1.7\text{A}$ , $V_{GS} = 0\text{V}$
Reverse recovery time (Note 6)	$t_{rr}$	—	33	—	ns	$I_S = -1.5\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge (Note 6)	$Q_{rr}$	—	48	—	nC	
<b>DYNAMIC CHARACTERISTICS (Note 6)</b>						
Input Capacitance	$C_{iss}$	—	424	—	pF	$V_{DS} = -50\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	$C_{oss}$	—	36.6	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	29.8	—	pF	
Total Gate Charge (Note 7)	$Q_g$	—	7.1	—	nC	$V_{GS} = -6.0\text{V}$
Total Gate Charge (Note 7)	$Q_g$	—	10.7	—	nC	$V_{GS} = -10\text{V}$ $V_{DS} = -50\text{V}$ $I_D = -1.4\text{A}$
Gate-Source Charge (Note 7)	$Q_{gs}$	—	1.7	—	nC	
Gate-Drain Charge (Note 7)	$Q_{gd}$	—	3.8	—	nC	
Turn-On Delay Time (Note 7)	$t_{D(on)}$	—	3.0	—	ns	$V_{DD} = -50\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -1\text{A}$ , $R_G = 6.0\Omega$
Turn-On Rise Time (Note 7)	$t_r$	—	3.5	—	ns	
Turn-Off Delay Time (Note 7)	$t_{D(off)}$	—	13.4	—	ns	
Turn-Off Fall Time (Note 7)	$t_f$	—	7.2	—	ns	

- Notes:
5. Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
  6. For design aid only, not subject to production testing.
  7. Switching characteristics are independent of operating junction temperatures.

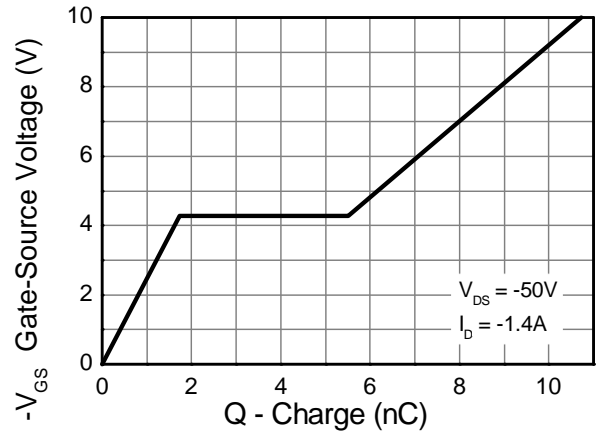
**Typical Characteristics**



**Typical Characteristics - continued**

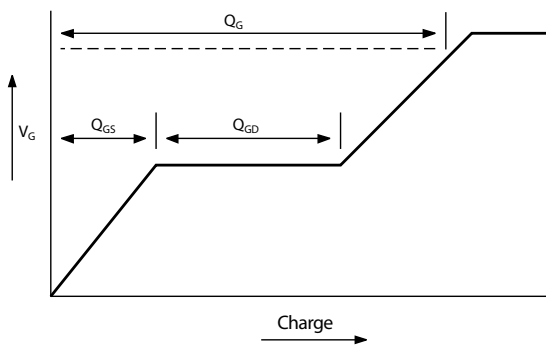


**Capacitance v Drain-Source Voltage**

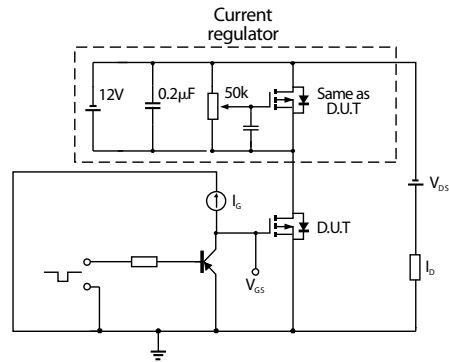


**Gate-Source Voltage v Gate Charge**

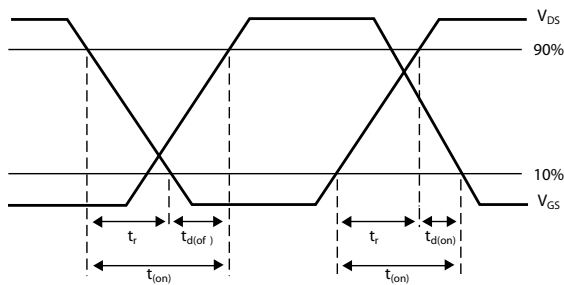
**Test Circuits**



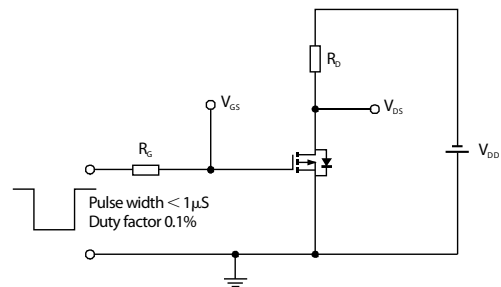
**Basic gate charge waveform**



**Gate charge test circuit**

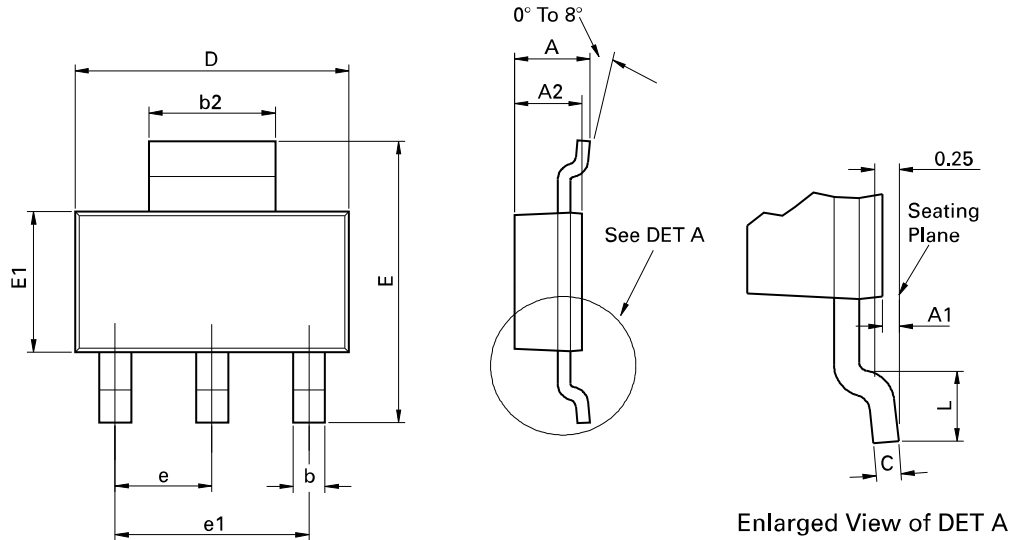


**Switching time waveforms**



**Switching time test circuit**

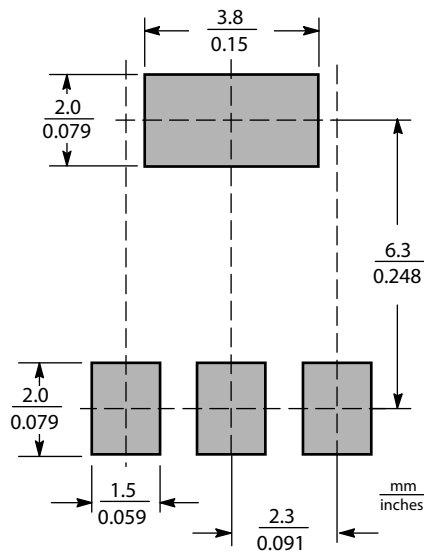
**Package Outline Dimensions**



Conforms to JEDEC TO-261 AA Issue B

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	-	1.80	-	0.071	D	6.30	6.70	0.248	0.264
A1	0.02	0.10	0.0008	0.004	e	2.30 BSC		0.0905 BSC	
A2	1.55	1.65	0.0610	0.0649	e1	4.60 BSC		0.181 BSC	
b	0.66	0.84	0.026	0.033	E	6.70	7.30	0.264	0.287
b2	2.90	3.10	0.114	0.122	E1	3.30	3.70	0.130	0.146
C	0.23	0.33	0.009	0.013	L	0.90	-	0.355	-

**Suggested Pad Layout**



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