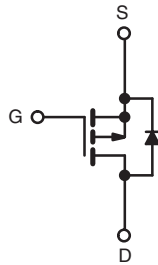
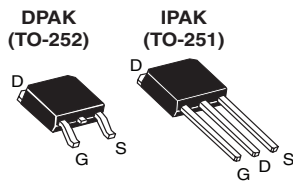


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 100	
$R_{DS(on)}$ (Ω)	$V_{GS} = - 10$ V	1.2
Q_g (Max.) (nC)	8.7	
Q_{gs} (nC)	2.2	
Q_{gd} (nC)	4.1	
Configuration	Single	



P-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR9110, SiHFR9110)
- Straight Lead (IRFU9110, SiHFU9110)
- Available in Tape and Reel
- P-Channel
- Fast Switching
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU Series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR9110PbF	IRFR9110TRLPbF ^a	IRFR9110TRPbF ^a	IRFU9110PbF
	SiHFR9110-E3	SiHFR9110TL-E3 ^a	SiHFR9110T-E3 ^a	SiHFU9110-E3
SnPb	IRFR9110	IRFR9110TRL ^a	IRFR9110TR ^a	IRFU9110
	SiHFR9110	SiHFR9110TL ^a	SiHFR9110T ^a	SiHFU9110

Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 100	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25^\circ\text{C}$	I_D	- 3.1	A
		$T_C = 100^\circ\text{C}$		- 2.0	
Pulsed Drain Current ^a			I_{DM}	- 12	W/ $^\circ\text{C}$
Linear Derating Factor				0.20	
Linear Derating Factor (PCB Mount) ^e				0.020	
Single Pulse Avalanche Energy ^b			E_{AS}	140	mJ
Repetitive Avalanche Current ^a			I_{AR}	- 3.1	A
Repetitive Avalanche Energy ^a			E_{AR}	2.5	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$		P_D	25	W
Maximum Power Dissipation (PCB Mount) ^e	$T_A = 25^\circ\text{C}$			2.5	
Peak Diode Recovery dV/dt ^c				- 5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			260 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = - 25$ V, starting $T_J = 25^\circ\text{C}$, $L = 21$ mH, $R_G = 25 \Omega$, $I_{AS} = - 3.1$ A (see fig. 12).
- $I_{SD} \leq - 4.0$ A, $dI/dt \leq 75$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W	
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50		
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	5.0		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		- 100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	- 0.093	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$		-	-	- 100	μA
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -1.9\text{ A}^b$	-	-	1.2	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -1.9\text{ A}$		0.97	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	200	-	pF
Output Capacitance	C_{oss}			-	94	-	
Reverse Transfer Capacitance	C_{rss}			-	18	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$	$I_D = -4.0\text{ A}, V_{DS} = -80\text{ V}$, see fig. 6 and 13 ^b	-	-	8.7	nC
Gate-Source Charge	Q_{gs}			-	-	2.2	
Gate-Drain Charge	Q_{gd}			-	-	4.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, I_D = -4.0\text{ A}, R_G = 24\text{ }\Omega, R_D = 11\text{ }\Omega$, see fig. 10 ^b		-	10	-	ns
Rise Time	t_r			-	27	-	
Turn-Off Delay Time	$t_{d(off)}$			-	15	-	
Fall Time	t_f			-	17	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode		-	-	- 3.1	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	- 12	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -3.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	- 5.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -4.0\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	80	160	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.17	0.30	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

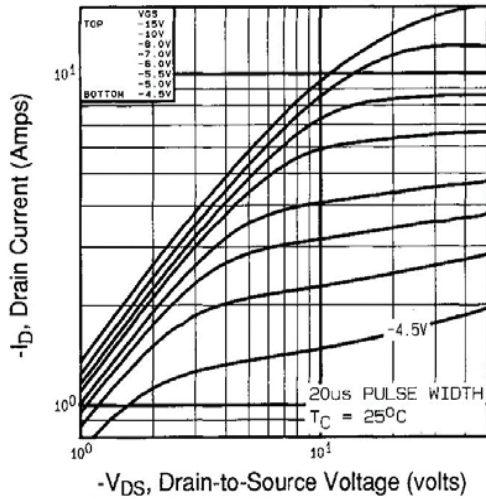


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

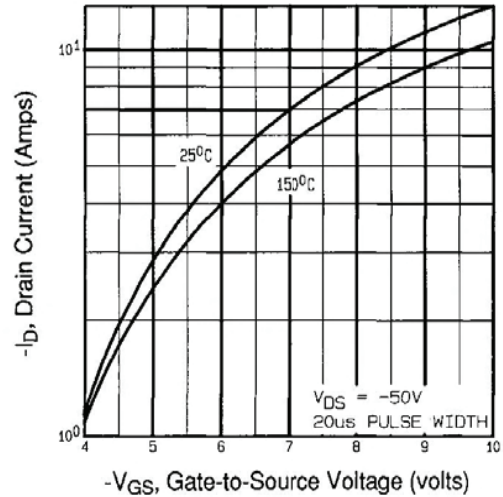


Fig. 3 - Typical Transfer Characteristics

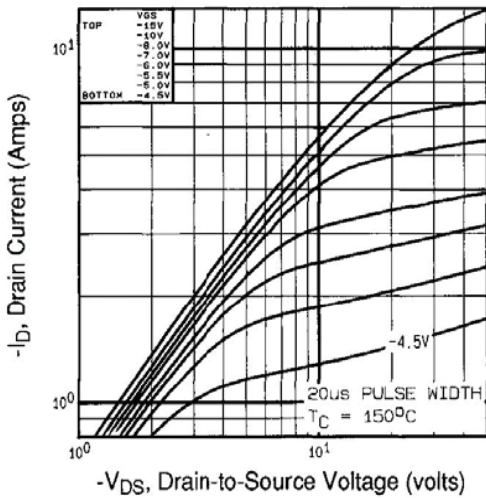


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

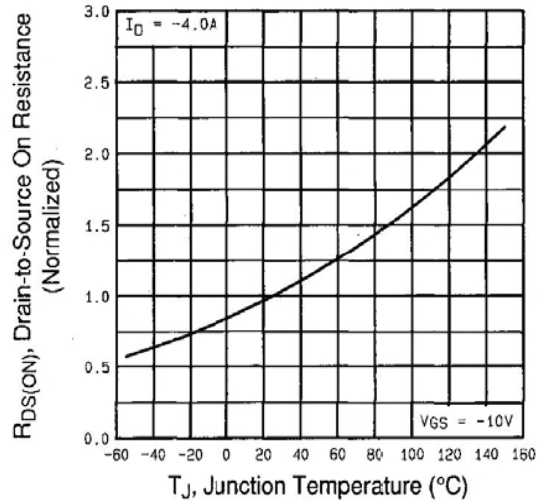


Fig. 4 - Normalized On-Resistance vs. Temperature

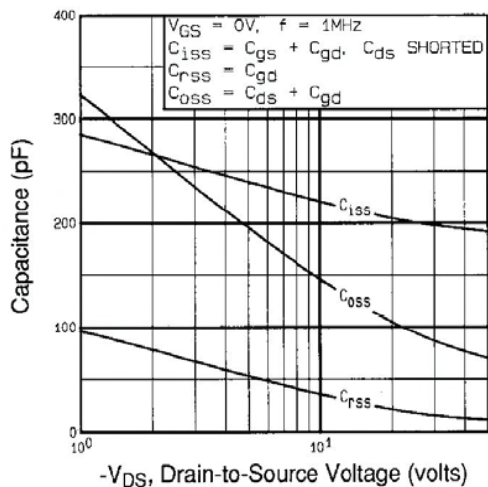


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

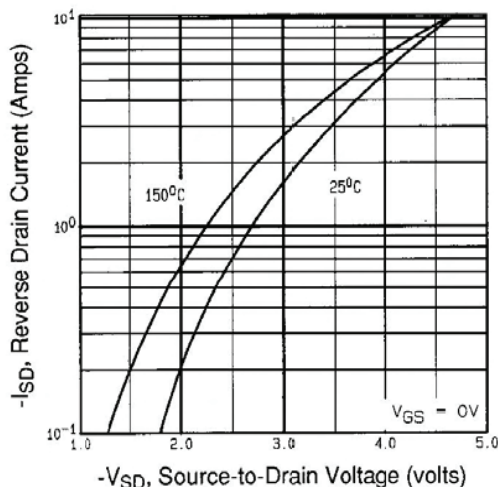


Fig. 7 - Typical Source-Drain Diode Forward Voltage

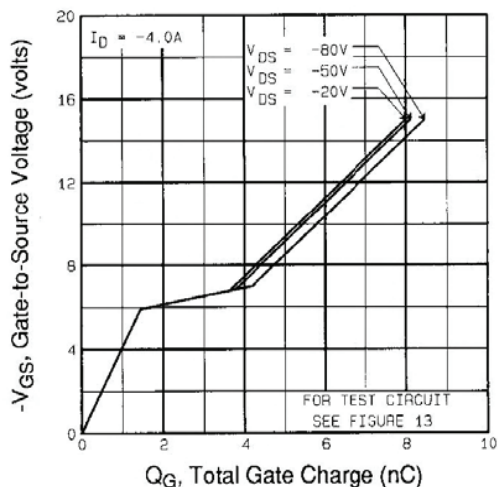


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

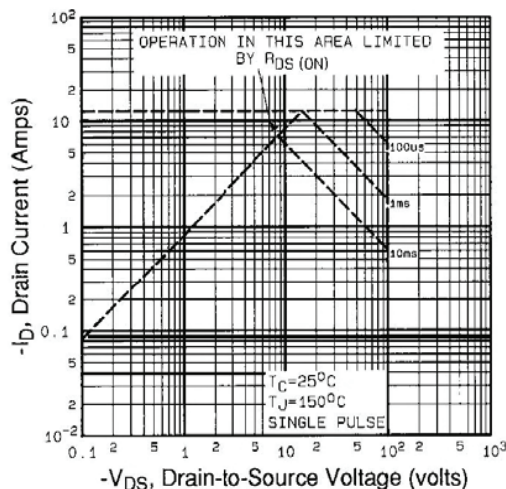


Fig. 8 - Maximum Safe Operating Area

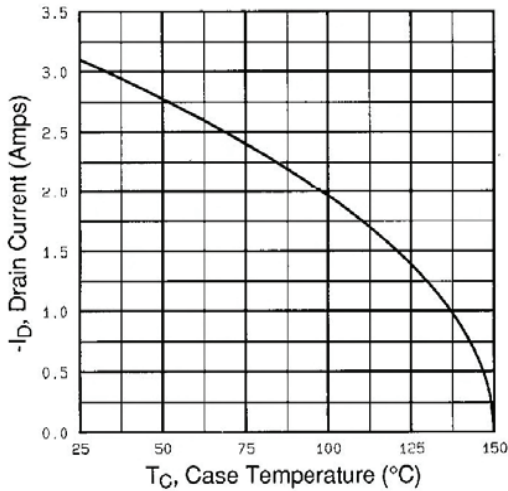


Fig. 9 - Maximum Drain Current vs. Case Temperature

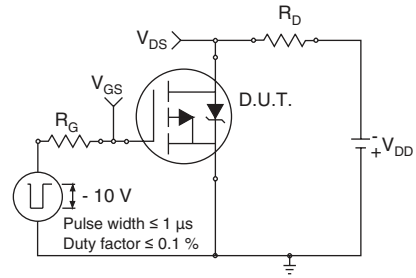


Fig. 10a - Switching Time Test Circuit

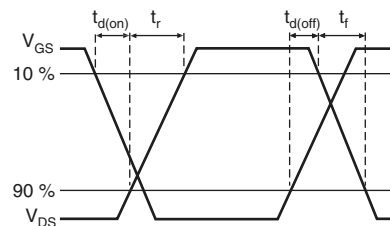


Fig. 10b - Switching Time Waveforms

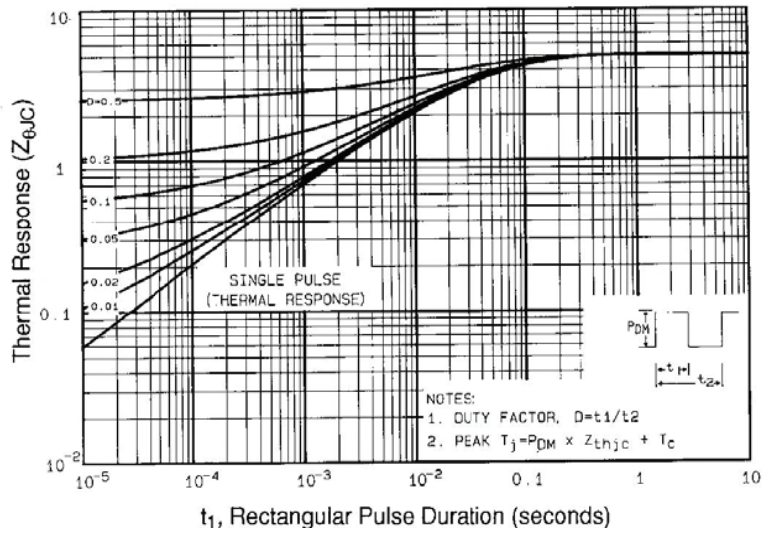


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

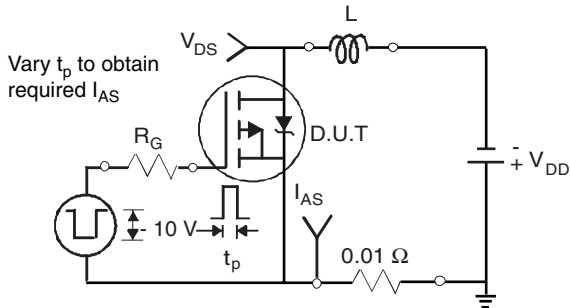


Fig. 12a - Unclamped Inductive Test Circuit

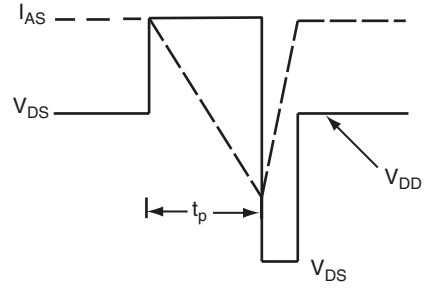


Fig. 12b - Unclamped Inductive Waveforms

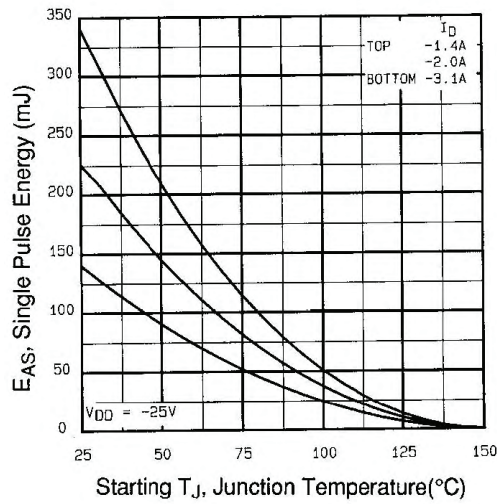


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

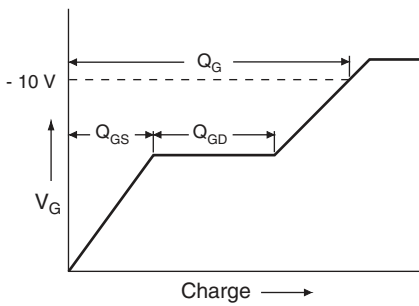


Fig. 13a - Basic Gate Charge Waveform

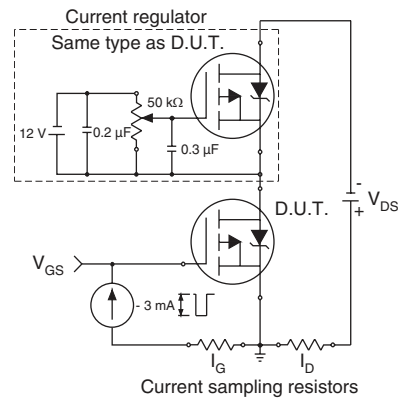
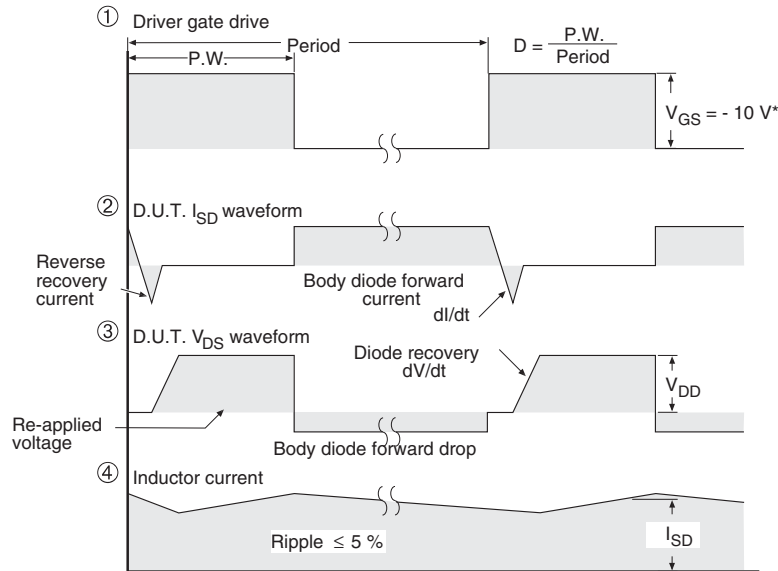
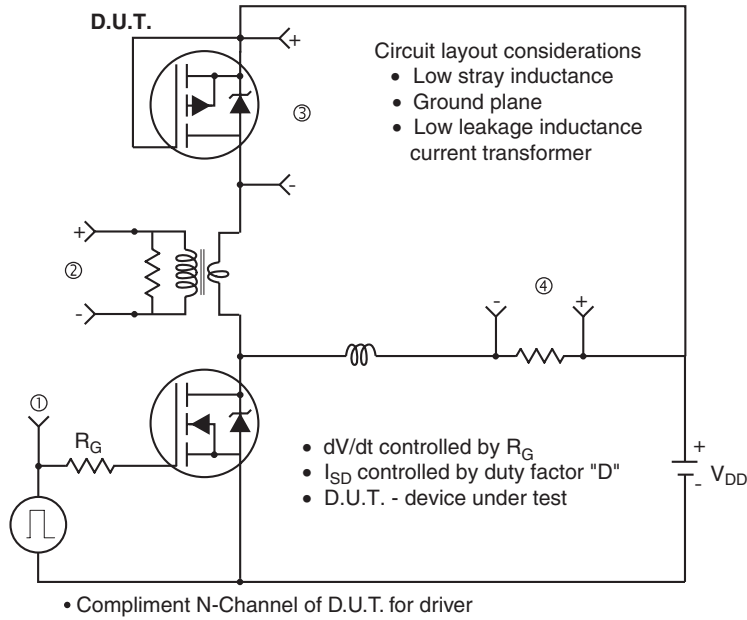


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel

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