2SK3044

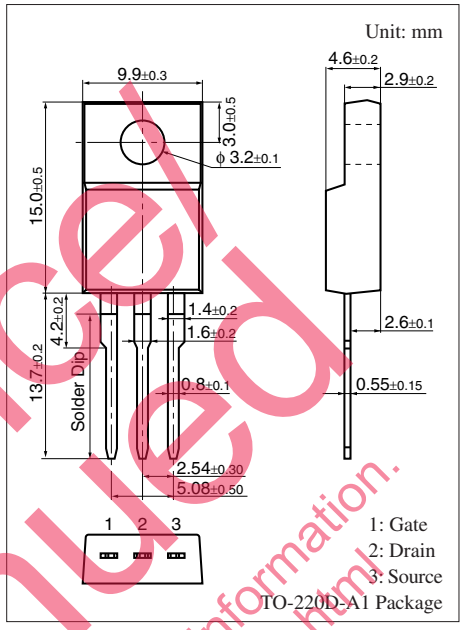
Silicon N-channel power MOSFET

■ Features

- Avalanche energy capability guaranteed: EAS > 130 mJ
- Gate-source surrender voltage V_{GSS} : ±30 V guaranteed
- High-speed switching
- No secondary breakdown

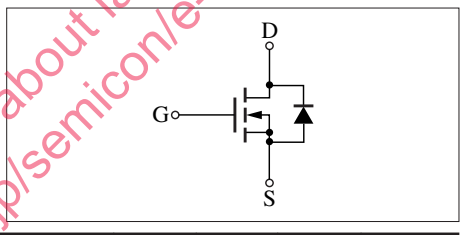
■ Applications

- Non-contact relay
- Solenoid drive
- Motor drive
- Control equipment
- Switching mode regulator



Marking Symbol: K3044

Internal Connection



■ Absolute Maximum Ratings $T_C = 25°C$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	450	V
Gate-source surrender voltage	V_{GSS}	±30	V
Drain current	I_D	±7	A
Peak drain current	I_{DP}	±14	A
Avalanche energy capability *	EAS	130	mJ
Power dissipation	P_D	40	W
$T_a = 25°C$		2	
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note) *: L = 5.4 mH, I_L = 7 A, 1 pulse

■ Electrical Characteristics $T_C = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 1 mA, V_{GS} = 0	450			V
Drain-source cutoff current	I_{DSS}	V_{DS} = 360 V, V_{GS} = 0			100	µA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0			±1	µA
Gate threshold voltage	V_{th}	V_{DS} = 25 V, I_D = 1 mA	2.0		5.0	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 25 V, I_D = 4 A	3.0	5.0		S
Drain-source ON resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4 A		0.56	0.75	Ω
Diode forward voltage	V_{DF}	I_{DR} = 7 A, V_{GS} = 0			−1.7	V
Short-circuit forward transfer capacitance (Common source)	C_{iss}	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz		1 300		pF
Short-circuit output capacitance (Common source)	C_{oss}			160		pF
Reverse transfer capacitance (Common source)	C_{rss}			70		pF
Turn-on delay time	$t_{d(on)}$	V_{DD} = 150 V, I_D = 4 A, R_L = 37.5 Ω		25		ns
Rise time	t_r	V_{GS} = 10 V		45		ns
Fall time	t_f			50		ns
Turn-off delay time	$t_{d(off)}$			150		ns
Thermal resistance (ch-c)	$R_{th(ch-c)}$				3.1	°C/W
Thermal resistance (ch-a)	$R_{th(ch-a)}$				62.5	°C/W

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

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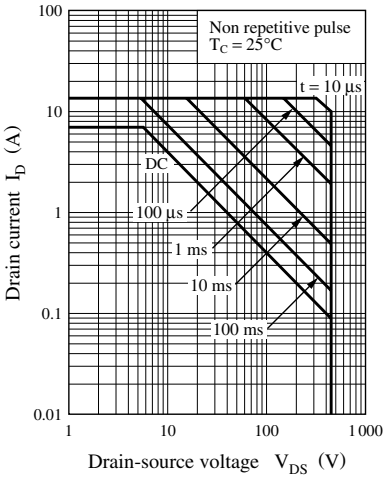
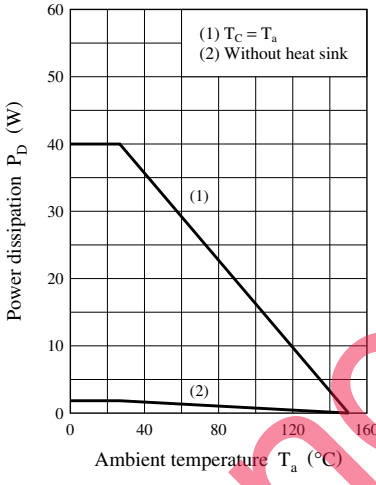
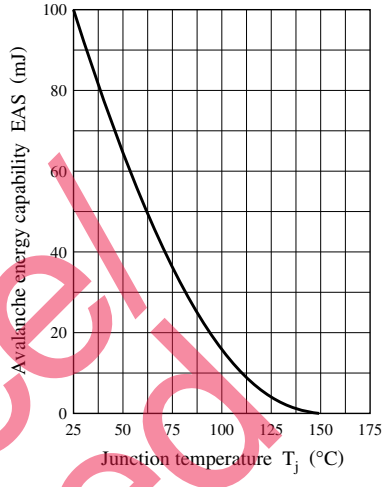
Safe operation area



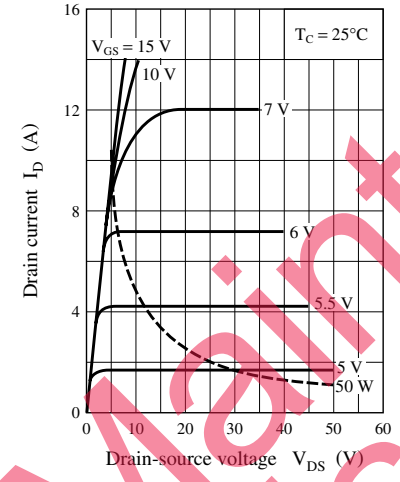
P_D — T_a



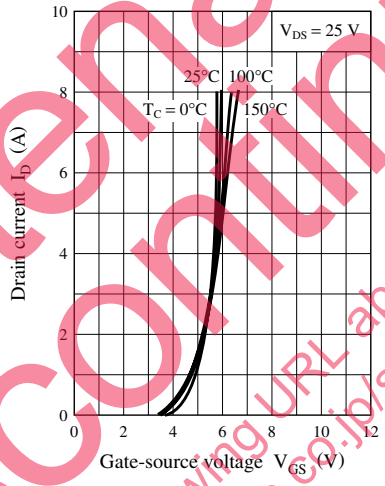
EAS — T_j



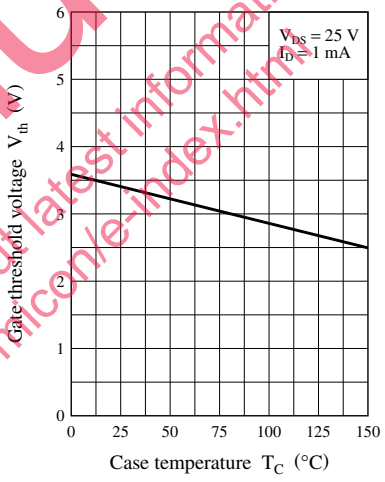
I_D — V_{DS}



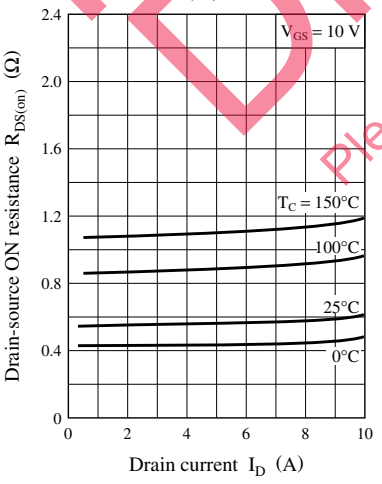
I_D — V_{GS}



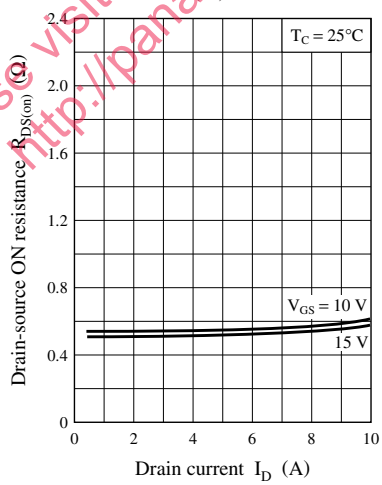
V_{th} — T_C



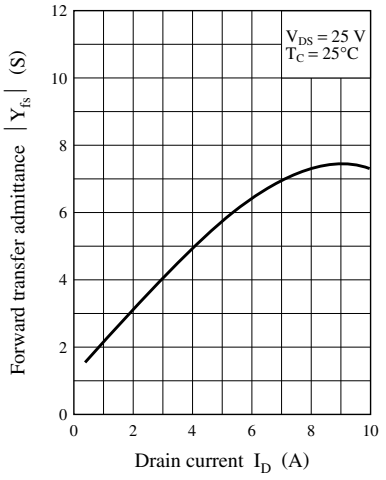
$R_{DS(on)}$ — I_D



$R_{DS(on)}$ — I_D



$|Y_{fs}|$ — I_D



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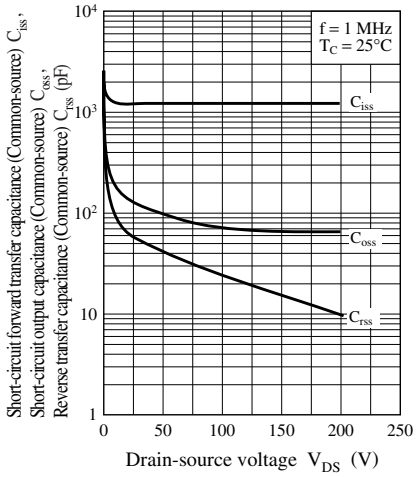
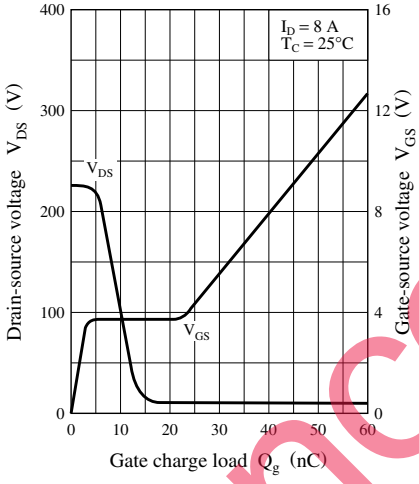
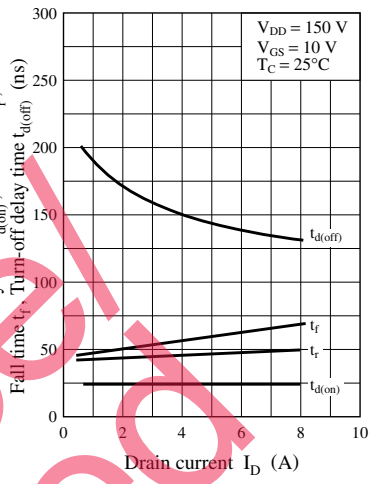
C_{iss} , C_{oss} , C_{rss} — V_{DS}



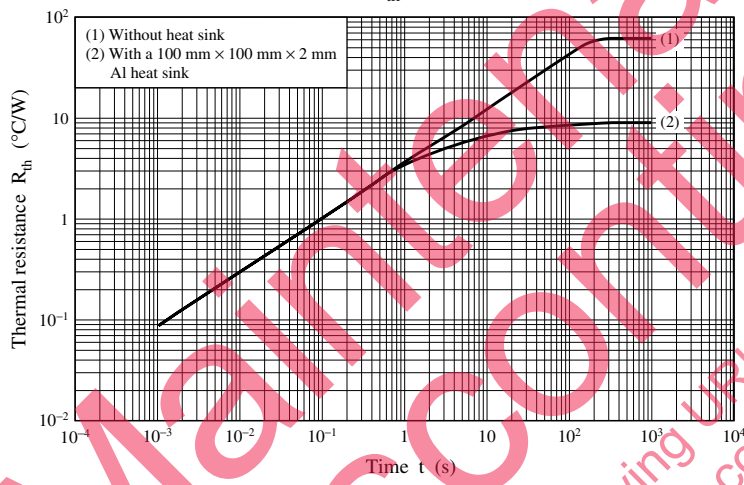
V_{DS} , V_{GS} — Q_g



$t_{d(on)}$, t_r , t_f , $t_{d(off)}$ — I_D



R_{th} — t



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