




Technical Data of Ceramic Resonator

MURATA Part No.: CSTLS10M0G53-B0

Applied to R5F212D8SNFP(High)(CM11=0)

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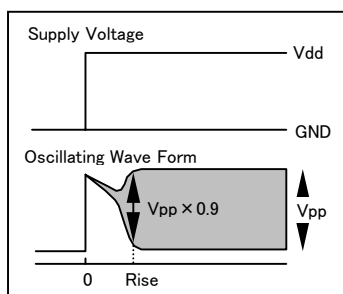
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### Note : Rise Time

We define "Rise time" is the time while the oscillation amplitude ( $V_{pp}$ ) reaches 90% of it at steady condition after  $V_{dd}(V_{set})$  is supplied.

「Rise time」は $V_{dd}(V_{set})$ が供給されてから発振電圧が最大電圧の90%に達するまでの時間と定義しています。

<General start up wave form> <標準的な発振立上り波形>



In general, Ceramic resonator is able to rise up during several microseconds to a hundred microseconds, and it is shorter than usual X'tal resonator that is able to rise up around several millisecond.

However, this rise up time depends on the rise up time of  $V_{dd}(V_{set})$ . Therefore, rise up time of ceramic resonator will be long if rise up time of  $V_{dd}(V_{set})$  is longer than rise up time of ceramic resonator own.

In other case, rise up time will be also long if supply voltage to the oscillation circuit takes a certain time by reset time etc. after  $V_{dd}(V_{set})$  is supplied.

Add to this, we can not measure rise time more than dozens of seconds due to measurement system. In this case, we will discribe "Unable to measure" in rise time data area.

一般にセラミック発振子そのものによる立ち上がり時間は水晶が数msecであるのに対して数 $\mu$ ~百 $\mu$ sec程度と非常に早いものとなっております。

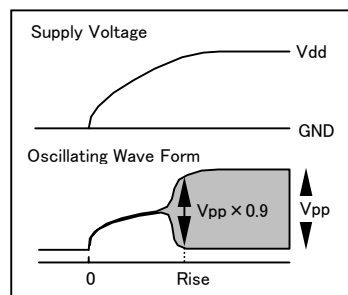
しかしながら、バイパスコンデンサの影響により、発振子の立ち上がり時間に比べて $V_{dd}(V_{set})$ の立ち上がり時間が遅くなる場合、発振子の立上り時間も $V_{dd}(V_{set})$ の立上り時間に依存しているため遅くなります。

$V_{dd}(V_{set})$ が供給されたあと、リセット時間等により、発振回路へ電圧が供給されるまでに一定時間かかる場合も同様に、発振子の立上り時間が遅くなります。

なお、測定器の都合により、数十秒以上の立ち上がり時間は測定不可となりますので、その場合は「Unable to measure」と記載しています。

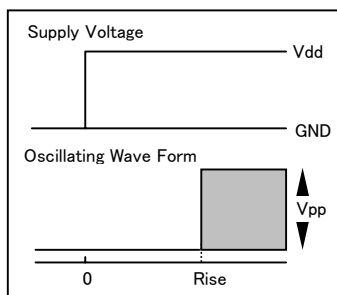
<Start up wave form with bypass capacitor>

<バイパスコンデンサによる影響>

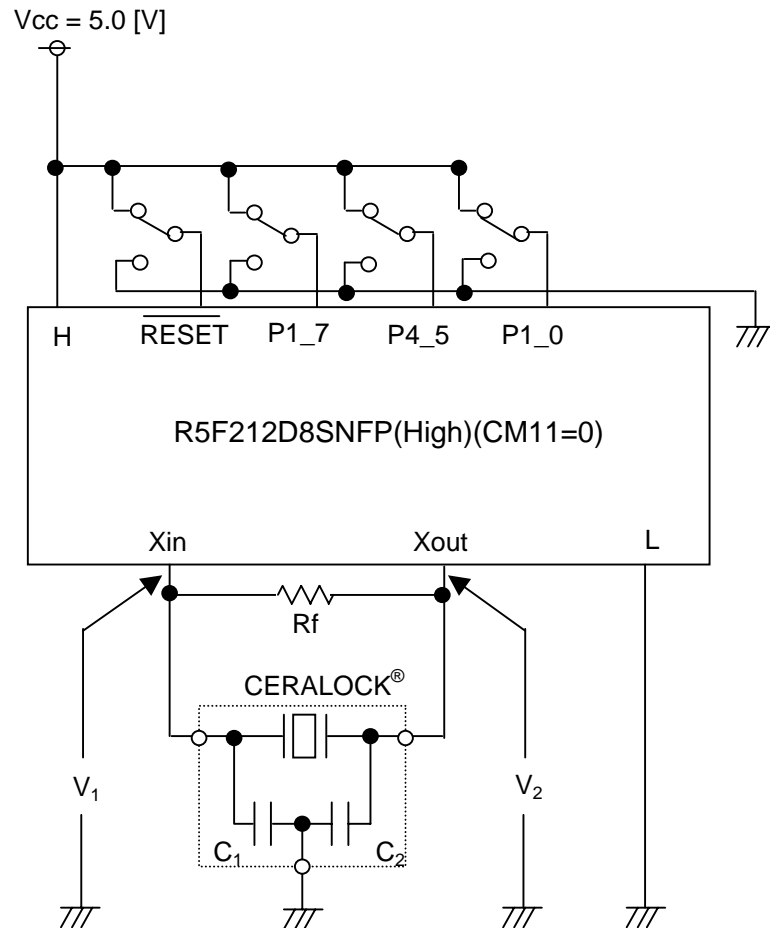


<Start up wave form with Reset function IC>

<リセット機能による影響>



## Test Circuit



Xin : 12       $\overline{\text{RESET}}$ : 9  
 Xout: 10      P1\_7: 31  
 H : 6,78      P4\_5: 44  
 L : 11      P1\_0: 57

$\overline{\text{RESET}}$	L→H
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## Recommended Value

CERALOCK<sup>®</sup> : CSTLS10M0G53-B0

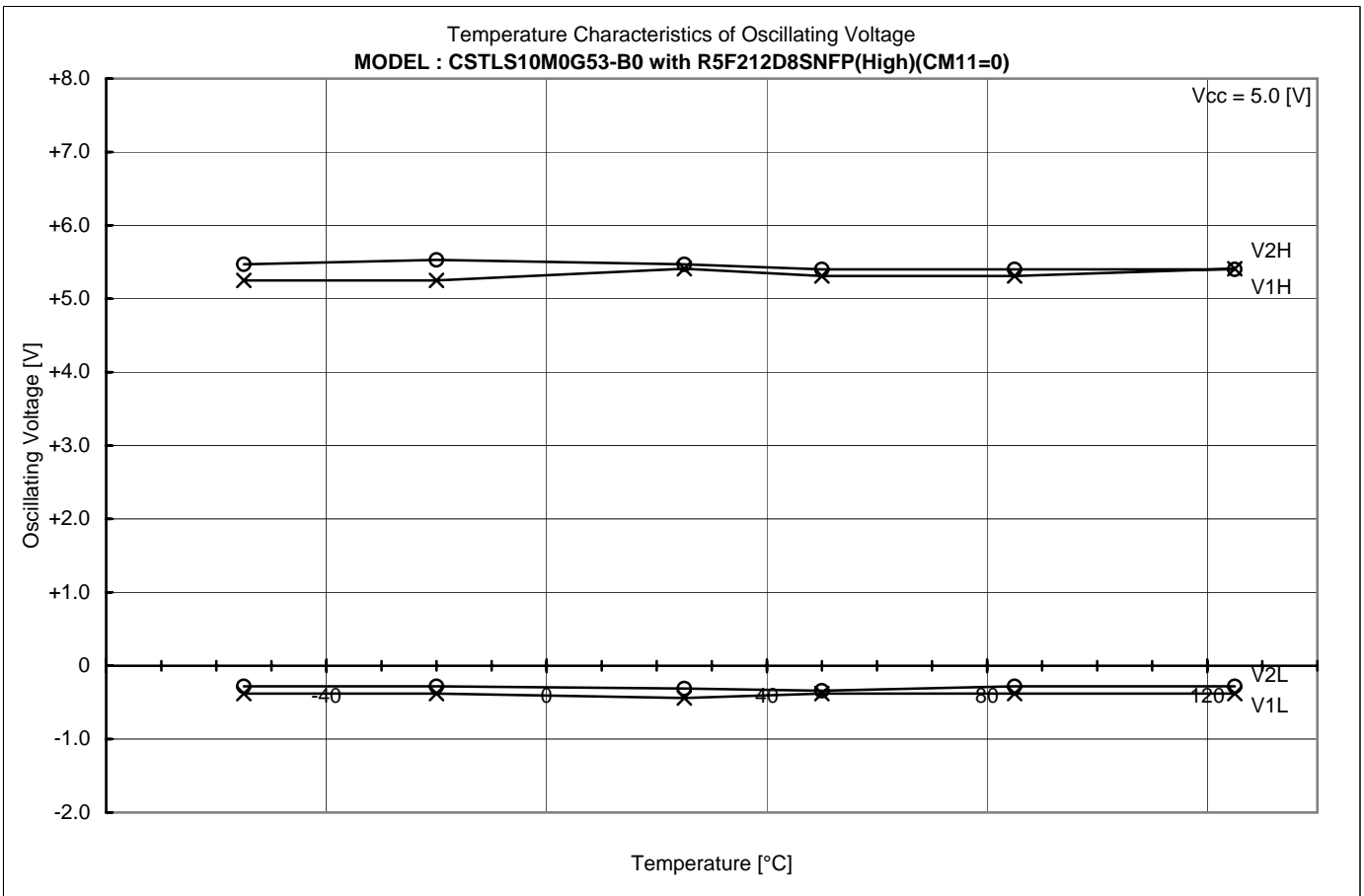
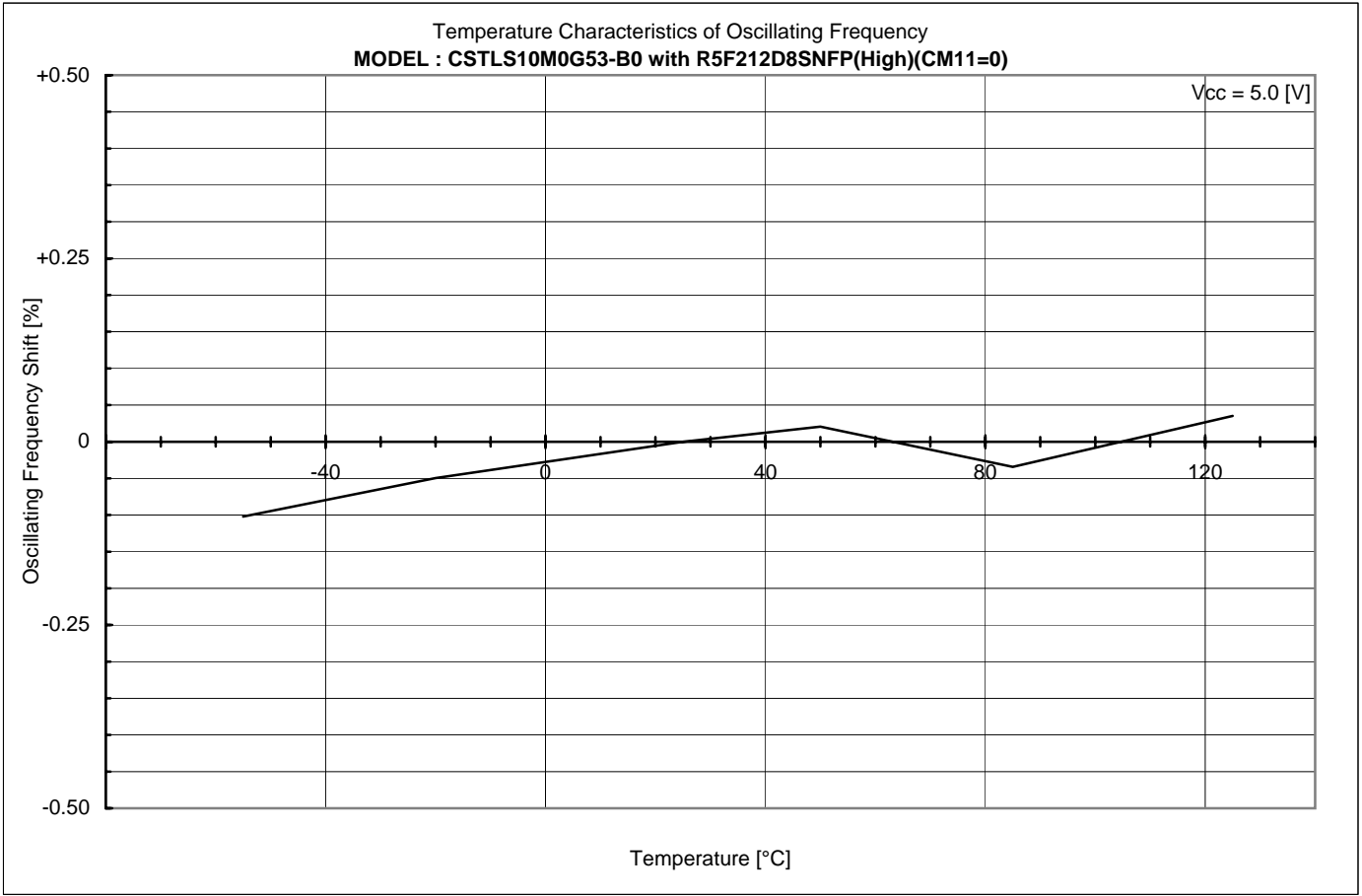
Vcc = 2.2 to 5.5 [V]

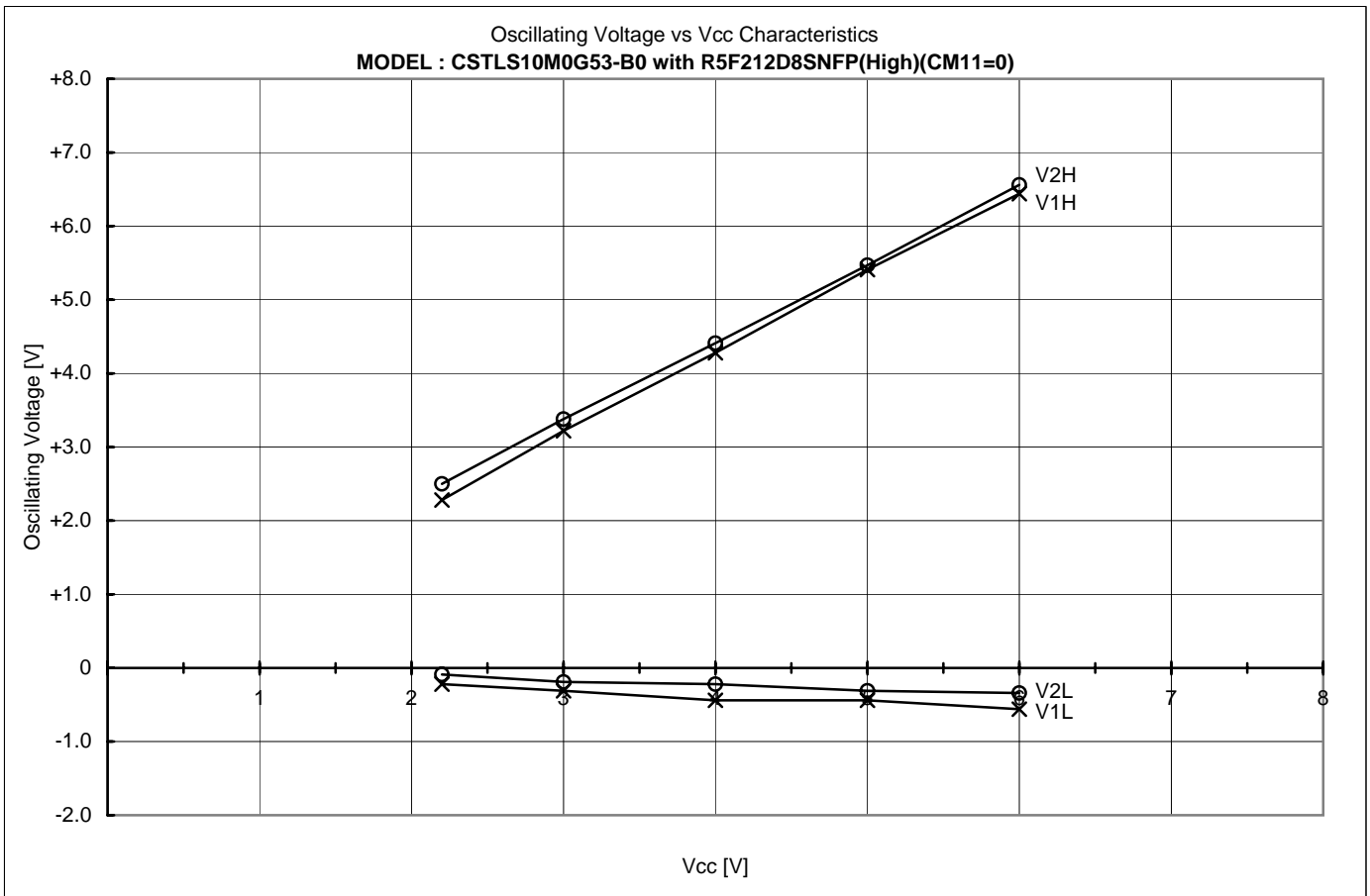
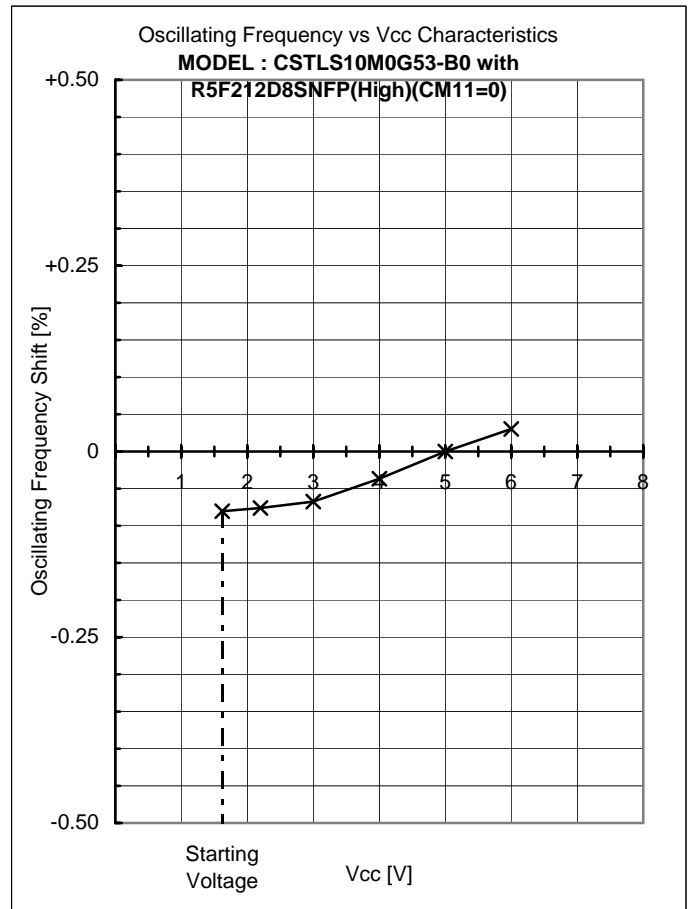
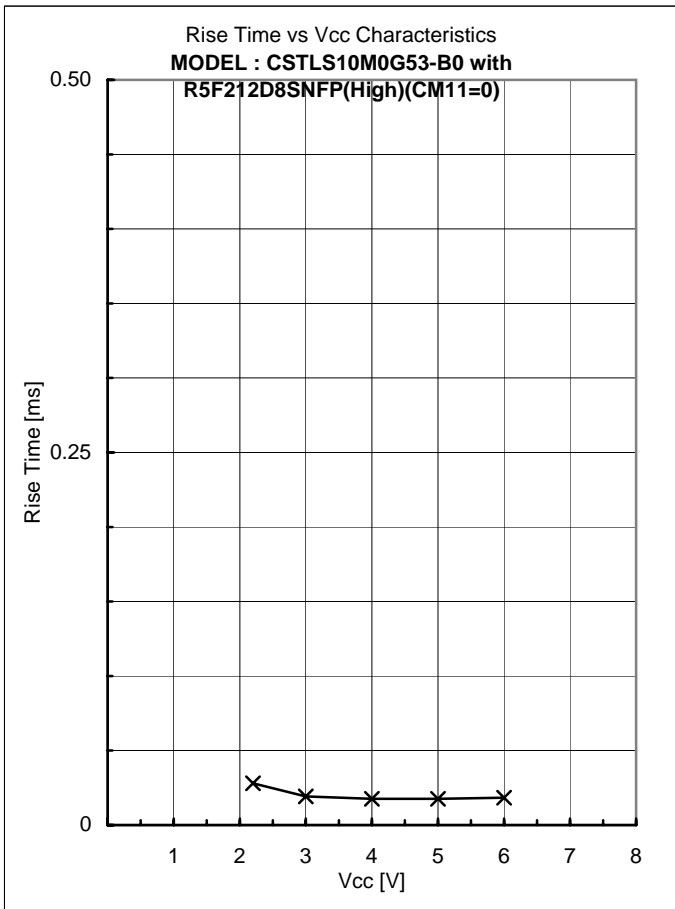
C1 = 15 [pF] (Typ.)

C2 = 15 [pF] (Typ.)

Rf = 1 [Mohm]

Ta = -40 to 85 [°C]







## Appendixes

### 4. Comparison Table

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**Comparison Table**

IC : No	V1H [V]	V1L [V]	V1p-p [V]	V2H [V]	V2L [V]	V2p-p [V]	Fosc [kHz]	Trise [ms]	Vstart [V]
HH	5.34	-0.41	5.75	5.59	-0.31	5.90	10040.498	0.018	1.70
HL	5.41	-0.41	5.82	5.41	-0.31	5.72	10039.657	0.018	1.60
ES	5.41	-0.44	5.85	5.47	-0.31	5.78	10040.894	0.018	1.62
LH	5.41	-0.47	5.88	5.53	-0.25	5.78	10040.546	0.020	1.57
LL	5.34	-0.41	5.75	5.47	-0.31	5.78	10041.541	0.018	1.46

Ref.

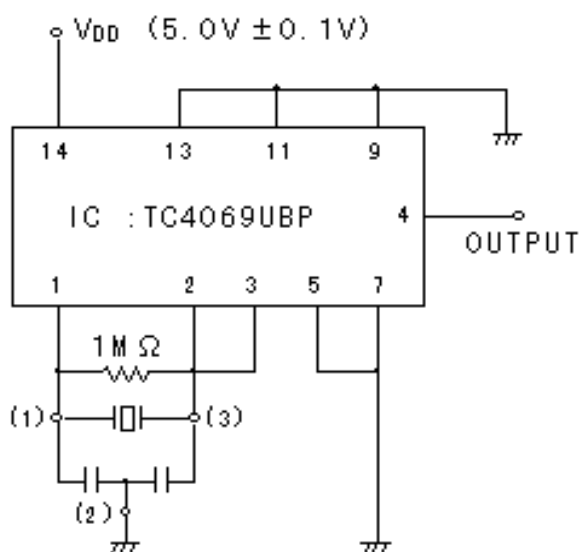
Performance described page 2 to 3 were measured with IC No. ES



### Frequency Correlation Data

Sample No.	R5F212D8SNFP(High)(CM11=0) Fosc [kHz]	TC4069UBP x 2 Fosc [kHz]	Shift [%]
1	10046.308	9999.870	0.4644
2	10050.659	10007.190	0.4344
3	10045.492	9997.160	0.4835
4	10048.180	10007.080	0.4107
5	10048.168	10002.920	0.4524
— X	10047.762	10002.844	0.4490

#### muRata Standard Circuit



CERALOCK® : CSTLS10M0G53-B0

Vdd = +5V

C1 = 15 [pF]

C2 = 15 [pF]

Rf = 1M [ohm]