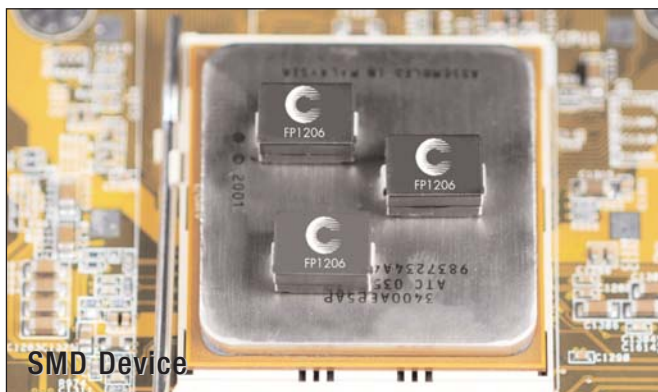


High Current, High Frequency, Power Inductors

FLAT-PAC™ FP1206 Series



Description

- Halogen free
- 125°C maximum total temperature operation
- 8.0 x 12.0 x 6.0mm surface mount package
- Ferrite core material
- High current carrying capacity, low core losses
- Designed for high speed, high current switch mode applications
- Controlled DCR tolerance for sensing circuits
- Inductance range from 120nH to 400nH
- Current range from 24 to 88 amps
- Frequency range up to 1MHz
- RoHS compliant

Applications

- Multi-phase regulators
- Voltage Regulator Module (VRM)
- Desktop and server VRMs and EVRDs
- Data networking and storage systems
- Notebook regulators
- Graphics cards and battery power systems
- Point of load modules
- DCR current sensing



Environmental Data

- Storage temperature range: -40°C to +125°C
- Operating temperature range: -40°C to +125°C (with derated current)
- Solder reflow temperature: J-STD-020D compliant

Packaging

- Supplied in tape-and-reel packaging, 620 parts per reel, 13" diameter reel

Product Specifications

Part Number ⁷	OCL ¹ ± 10% (nH)	FLL ² Min. (nH)	I _{rms} ³ (Amps)	I _{sat} ¹⁴ (Amps) @25°C	I _{sat} ²⁵ (Amps) @125°C	DCR (mΩ) @20°C	K-factor ⁶
FP1206R1-R12-R	120	86	50	88	65	0.43 ± 6.5%	358
FP1206R1-R15-R	150	108		70	51		358
FP1206R1-R25-R	250	180		43	32		358
FP1206R1-R30-R	300	216		34	26		358
FP1206R1-R40-R	400	288		24	19		358

1 Open Circuit Inductance (OCL) Test Parameters: 100kHz, 0.1V_{rms}, 0.0A_{dc}

2 Full Load Inductance (FLL) Test Parameters: 100kHz, 0.1V_{rms}, I_{sat}¹

3 I_{rms}: DC current for an approximate temperature rise of 40°C without core loss. Derating is necessary for AC currents. PCB layout, trace thickness and width, air-flow, and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature of the part not exceed 125°C under worst case operating conditions verified in the end application.

4 I_{sat}¹: Peak current for approximately 20% rolloff at +25°C.

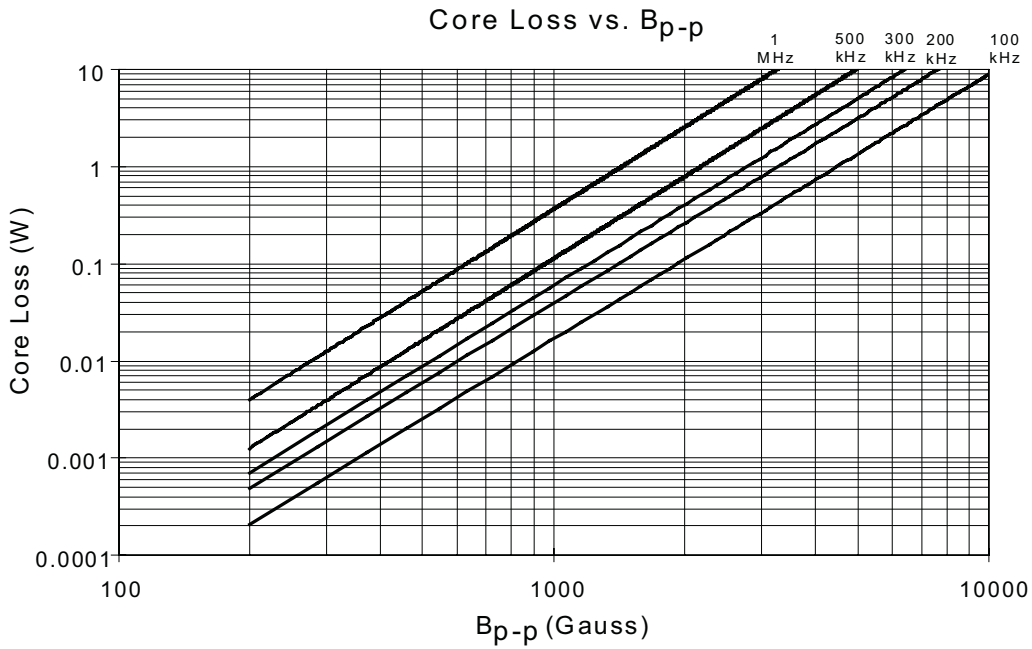
5 I_{sat}²: Peak current for approximately 20% rolloff at +125°C.

6 K-factor: Used to determine B_{p-p} for core loss (see graph). B_{p-p} = K * L * ΔI * 10⁻³. B_{p-p}:(Gauss), K: (K-factor from table), L: (Inductance in nH), ΔI (Peak-to-peak ripple current in amps).

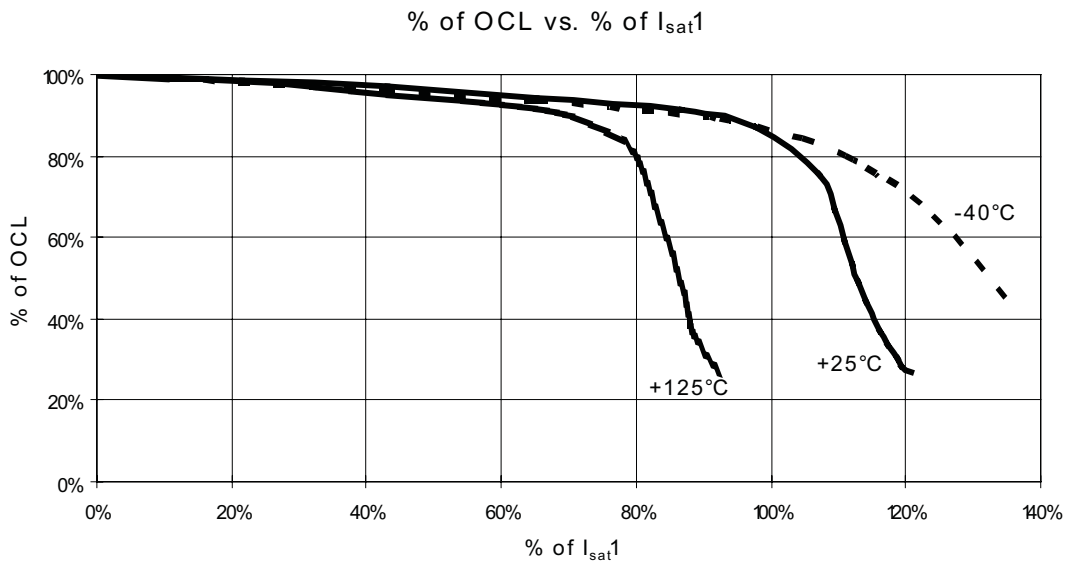
7 Part Number Definition: FP1206Rx-Rxx-R

- FP1206 = Product code and size
- Rx= DCR indicator
- Rxx= Inductance value in uH, R = decimal point
- -R suffix = RoHS compliant

Core Loss



Inductance Characteristics



Solder Reflow Profile

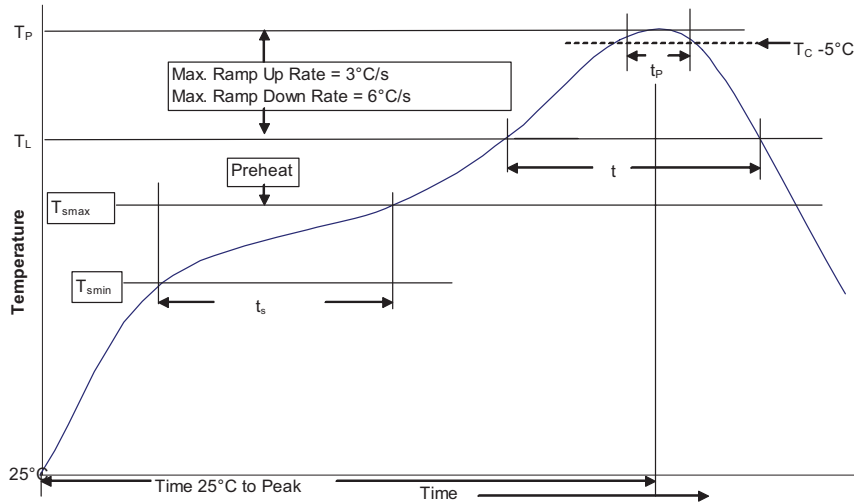


Table 1 - Standard SnPb Solder (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥ 350
<2.5mm	235°C	220°C
$\geq 2.5\text{mm}$	220°C	220°C

Table 2 - Lead (Pb) Free Solder (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6mm	260°C	260°C	260°C
1.6 - 2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

Reference JDEC J-STD-020D

Profile Feature	Standard SnPb Solder	Lead (Pb) Free Solder
Preheat and Soak		
• Temperature min. (T_{smin})	100°C	150°C
• Temperature max. (T_{smax})	150°C	200°C
• Time (T_{smin} to T_{smax}) (t_s)	60-120 Seconds	60-120 Seconds
Average ramp up rate T_{smax} to T_p	3°C/ Second Max.	3°C/ Second Max.
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60-150 Seconds	60-150 Seconds
Peak package body temperature (T_p)*	Table 1	Table 2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20 Seconds**	30 Seconds**
Average ramp-down rate (T_p to T_{smax})	6°C/ Second Max.	6°C/ Second Max.
Time 25°C to Peak Temperature	6 Minutes Max.	8 Minutes Max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

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